

# EEPROM Serial 8-Kb Microwire

## CAT93C76B



SOIC-8  
V SUFFIX  
CASE 751BD



TSSOP-8  
Y SUFFIX  
CASE 948AL



UDFN-8  
HU4 SUFFIX  
CASE 517AZ

### Description

The CAT93C76B is an 8-Kb Microwire Serial EEPROM memory device which is configured as either registers of 16 bits (ORG pin at V<sub>CC</sub> or Not Connected) or 8 bits (ORG pin at GND). Each register can be written (or read) serially by using the DI (or DO) pin. The CAT93C76B is manufactured using onsemi's advanced CMOS EEPROM floating gate technology. The device is designed to endure 1,000,000 program/erase cycles and has a data retention of 100 years. The device is available in 8-pin SOIC, TSSOP and 8-pad UDFN packages.

### Features

- High Speed Operation: 4 MHz (5 V), 2 MHz (1.8 V)
- 1.8 V (1.65 V\*) to 5.5 V Supply Voltage Range
- Selectable x8 or x16 Memory Organization
- Self-timed Write Cycle with Auto-clear
- Software Write Protection
- Power-up Inadvertant Write Protection
- Low Power CMOS Technology
- 1,000,000 Program/Erase Cycles
- 100 Year Data Retention
- Industrial and Extended Temperature Ranges
- Sequential Read
- 8-pin SOIC, TSSOP and 8-Pad UDFN Packages
- This Device is Pb-Free, Halogen Free/BFR Free and RoHS Compliant†

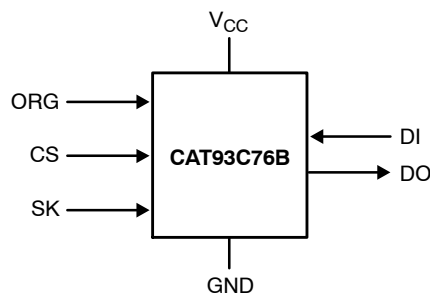
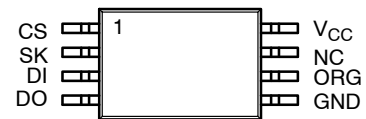


Figure 1. Functional Symbol

\*CAT93C76Bxx-xxL (T<sub>A</sub> = -20°C to +85°C)

†For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

### PIN CONFIGURATION



SOIC (V), TSSOP (Y), UDFN (HU4)  
(Top View)

### PIN FUNCTION

Pin Name	Function
CS	Chip Select
SK	Serial Clock Input
DI	Serial Data Input
DO	Serial Data Output
V <sub>CC</sub>	Power Supply
GND	Ground
ORG	Memory Organization
NC	No Connection

**NOTE:** When the ORG pin is connected to V<sub>CC</sub>, the x16 organization is selected. When it is connected to ground, the x8 organization is selected. If the ORG pin is left unconnected, then an internal pull-up device will select the x16 organization.

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.

# CAT93C76B

**Table 1. ABSOLUTE MAXIMUM RATINGS**

Parameters	Ratings	Units
Temperature Under Bias	-55 to +125	°C
Storage Temperature	-65 to +150	°C
Voltage on any Pin with Respect to Ground (Note 1)	-2.0 to +V <sub>CC</sub> +2.0	V
V <sub>CC</sub> with Respect to Ground	-2.0 to +7.0	V
Lead Soldering Temperature (10 seconds)	300	°C
Output Short Circuit Current (Note 2)	100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The minimum DC input voltage is -0.5 V. During transitions, inputs may undershoot to -2.0 V for periods of less than 20 ns. Maximum DC voltage on output pins is V<sub>CC</sub> +0.5 V, which may overshoot to V<sub>CC</sub> +2.0 V for periods of less than 20 ns.
2. Output shorted for no more than one second.

**Table 2. RELIABILITY CHARACTERISTICS (Note 2)**

Symbol	Parameter	Reference Test Method	Min	Units
N <sub>END</sub> (Note 3)	Endurance	MIL-STD-883, Test Method 1033	1,000,000	Cycles / Byte
T <sub>DR</sub> (Note 3)	Data Retention	MIL-STD-883, Test Method 1008	100	Years
V <sub>ZAP</sub> (Note 3)	ESD Susceptibility	MIL-STD-883, Test Method 3015	2,000	V
I <sub>LTH</sub> (Notes 3, 4)	Latch-Up	JEDEC Standard 17	100	mA

3. These parameters are tested initially and after a design or process change that affects the parameter.
4. Latch-up protection is provided for stresses up to 100 mA on I/O pins from -1 V to V<sub>CC</sub> + 1 V.

**Table 3. D.C. OPERATING CHARACTERISTICS**

(V<sub>CC</sub> = +1.8 V to +5.5 V, T<sub>A</sub> = -40°C to +125°C, V<sub>CC</sub> = +1.65 V to +5.5 V, T<sub>A</sub> = -20°C to +85°C unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min	Max	Units
I <sub>CC1</sub>	Supply Current (Write)	Write, V <sub>CC</sub> = 5.0 V		2	mA
I <sub>CC2</sub>	Supply Current (Read)	Read, DO open, f <sub>SK</sub> = 2 MHz, V <sub>CC</sub> = 5.0 V		500	μA
I <sub>SB1</sub>	Standby Current (x8 Mode)	V <sub>IN</sub> = GND or V <sub>CC</sub> CS = GND, ORG = GND	T <sub>A</sub> = -40°C to +85°C	2	μA
			T <sub>A</sub> = -40°C to +125°C	5	
I <sub>SB2</sub>	Standby Current (x16 Mode)	V <sub>IN</sub> = GND or V <sub>CC</sub> CS = GND, ORG = Float or V <sub>CC</sub>	T <sub>A</sub> = -40°C to +85°C	1	μA
			T <sub>A</sub> = -40°C to +125°C	3	
I <sub>LI</sub>	Input Leakage Current	V <sub>IN</sub> = GND to V <sub>CC</sub>	T <sub>A</sub> = -40°C to +85°C	1	μA
			T <sub>A</sub> = -40°C to +125°C	2	
I <sub>LO</sub>	Output Leakage Current	V <sub>OUT</sub> = GND to V <sub>CC</sub> CS = GND	T <sub>A</sub> = -40°C to +85°C	1	μA
			T <sub>A</sub> = -40°C to +125°C	2	
V <sub>IL1</sub>	Input Low Voltage	4.5 V ≤ V <sub>CC</sub> < 5.5 V	-0.1	0.8	V
V <sub>IH1</sub>	Input High Voltage	4.5 V ≤ V <sub>CC</sub> < 5.5 V	2	V <sub>CC</sub> + 1	V
V <sub>IL2</sub>	Input Low Voltage	1.65 V ≤ V <sub>CC</sub> < 4.5 V	0	V <sub>CC</sub> × 0.2	V
V <sub>IH2</sub>	Input High Voltage	1.65 V ≤ V <sub>CC</sub> < 4.5 V	V <sub>CC</sub> × 0.7	V <sub>CC</sub> + 1	V
V <sub>OL1</sub>	Output Low Voltage	4.5 V ≤ V <sub>CC</sub> < 5.5 V, I <sub>OL</sub> = 3 mA		0.4	V
V <sub>OH1</sub>	Output High Voltage	4.5 V ≤ V <sub>CC</sub> < 5.5 V, I <sub>OH</sub> = -400 μA	2.4		V
V <sub>OL2</sub>	Output Low Voltage	1.65 V ≤ V <sub>CC</sub> < 4.5 V, I <sub>OL</sub> = 1 mA		0.2	V
V <sub>OH2</sub>	Output High Voltage	1.65 V ≤ V <sub>CC</sub> < 4.5 V, I <sub>OH</sub> = -100 μA	V <sub>CC</sub> - 0.2		V

**Table 4. PIN CAPACITANCE (Note 3)**

Symbol	Test	Conditions	Min	Typ	Max	Units
C <sub>OUT</sub>	Output Capacitance (DO)	V <sub>OUT</sub> = 0 V			5	pF
C <sub>IN</sub>	Input Capacitance (CS, SK, DI, ORG)	V <sub>IN</sub> = 0 V			5	pF

# CAT93C76B

**Table 5. INSTRUCTION SET** (Note 5)

Instruction	Start Bit	Opcode	Address		Data		Comments
			x8	x16	x8	x16	
READ	1	10	A10–A0	A9–A0			Read Address AN– A0
ERASE	1	11	A10–A0	A9–A0			Clear Address AN– A0
WRITE	1	01	A10–A0	A9–A0	D7–D0	D15–D0	Write Address AN– A0
EWEN	1	00	11XXXXXXXXXX	11XXXXXXXXXX			Write Enable
EWDS	1	00	00XXXXXXXXXX	00XXXXXXXXXX			Write Disable
ERAL*	1	00	10XXXXXXXXXX	10XXXXXXXXXX			Clear All Addresses
WRAL*	1	00	01XXXXXXXXXX	01XXXXXXXXXX	D7–D0	D15–D0	Write All Addresses

\* Not available at  $V_{CC} < 1.8\text{ V}$

5. Address bit A10 for the 1,024x8 org. and A9 for the 512x16 org. are “don’t care” bits, but must be kept at either a “1” or “0” for READ, WRITE and ERASE commands.

**Table 6. A.C. CHARACTERISTICS**

( $V_{CC} = +1.8\text{ V}$  to  $+5.5\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ ,  $V_{CC} = +1.65\text{ V}$  to  $+5.5\text{ V}$ ,  $T_A = -20^\circ\text{C}$  to  $+85^\circ\text{C}$  unless otherwise specified.)

Symbol	Parameter	$V_{CC} < 4.5\text{ V}$		$V_{CC} > 4.5\text{ V}$		Units
		Min	Max	Min	Max	
$t_{CSS}$	CS Setup Time	50		50		ns
$t_{CSH}$	CS Hold Time	0		0		ns
$t_{DIS}$	DI Setup Time	100		50		ns
$t_{DIH}$	DI Hold Time	100		50		ns
$t_{PD1}$	Output Delay to 1		0.25		0.1	$\mu\text{s}$
$t_{PD0}$	Output Delay to 0		0.25		0.1	$\mu\text{s}$
$t_{HZ}$ (Note 6)	Output Delay to High–Z		100		100	ns
$t_{EW}$	Program/Erase Pulse Width		5		5	ms
$t_{CSMIN}$	Minimum CS Low Time	0.25		0.1		$\mu\text{s}$
$t_{SKHI}$	Minimum SK High Time	0.25		0.1		$\mu\text{s}$
$t_{SKLOW}$	Minimum SK Low Time	0.25		0.1		$\mu\text{s}$
$t_{SV}$	Output Delay to Status Valid		0.25		0.1	$\mu\text{s}$
$SK_{MAX}$	Maximum Clock Frequency	DC	2000	DC	4000	kHz

6. This parameter is tested initially and after a design or process change that affects the parameter.

**Table 7. POWER–UP TIMING** (Notes 6, 7)

Symbol	Parameter	Max	Units
$t_{PUR}$	Power–up to Read Operation	1	ms
$t_{PUW}$	Power–up to Write Operation	1	ms

7.  $t_{PUR}$  and  $t_{PUW}$  are the delays required from the time  $V_{CC}$  is stable until the specified operation can be initiated.

**Table 8. A.C. TEST CONDITIONS**

Input Rise and Fall Times	$\leq 50\text{ ns}$	
Input Pulse Voltages	0.4 V to 2.4 V	$4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$
Timing Reference Voltages	0.8 V, 2.0 V	$4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$
Input Pulse Voltages	$0.2 V_{CC}$ to $0.7 V_{CC}$	$1.65\text{ V} \leq V_{CC} \leq 4.5\text{ V}$
Timing Reference Voltages	$0.5 V_{CC}$	$1.65\text{ V} \leq V_{CC} \leq 4.5\text{ V}$
Output Load	Current Source $I_{OLmax}/I_{OHmax}$ ; $CL = 100\text{ pF}$	

**DEVICE OPERATION**

The CAT93C76B is a 8192-bit nonvolatile memory intended for use with industry standard microprocessors. The CAT93C76B can be organized as either registers of 16 bits or 8 bits. When organized as X16, seven 13-bit instructions control the read, write and erase operations of the device. When organized as X8, seven 14-bit instructions control the read, write and erase operations of the device. The CAT93C76B operates on a single power supply and will generate on chip, the high voltage required during any write operation.

Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (SK). The DO pin is normally in a high impedance state except when reading data from the device, or when checking the ready/busy status after a write operation.

The ready/busy status can be determined after the start of a write operation by selecting the device (CS high) and polling the DO pin; DO low indicates that the write operation is not completed, while DO high indicates that the device is ready for the next instruction. If necessary, the DO pin may be placed back into a high impedance state during chip select by shifting a dummy "1" into the DI pin. The DO pin will enter the high impedance state on the falling edge of the clock (SK). Placing the DO pin into the high impedance state is recommended in applications where the DI pin and the DO pin are to be tied together to form a common DI/O pin.

The format for all instructions sent to the device is a logical "1" start bit, a 2-bit (or 4-bit) opcode, 10-bit address (an additional bit when organized X8) and for write operations a 16-bit data field (8-bit for X8 organizations). The most significant bit of the address is "don't care" but it must be present.

**Read**

Upon receiving a READ command and an address (clocked into the DI pin), the DO pin of the CAT93C76B will come out of the high impedance state and, after sending an initial dummy zero bit, will begin shifting out the data addressed (MSB first). The output data bits will toggle on the rising edge of the SK clock and are stable after the specified time delay ( $t_{PD0}$  or  $t_{PD1}$ ).

For the CAT93C76B, after the initial data word has been shifted out and CS remains asserted with the SK clock continuing to toggle, the device will automatically increment to the next address and shift out the next data word in a sequential READ mode. As long as CS is continuously asserted and SK continues to toggle, the device will keep incrementing to the next address automatically until it reaches the end of the address space, then loops back to address 0. In the sequential READ mode, only the initial data word is preceded by a dummy zero bit. All subsequent data words will follow without a dummy zero bit.

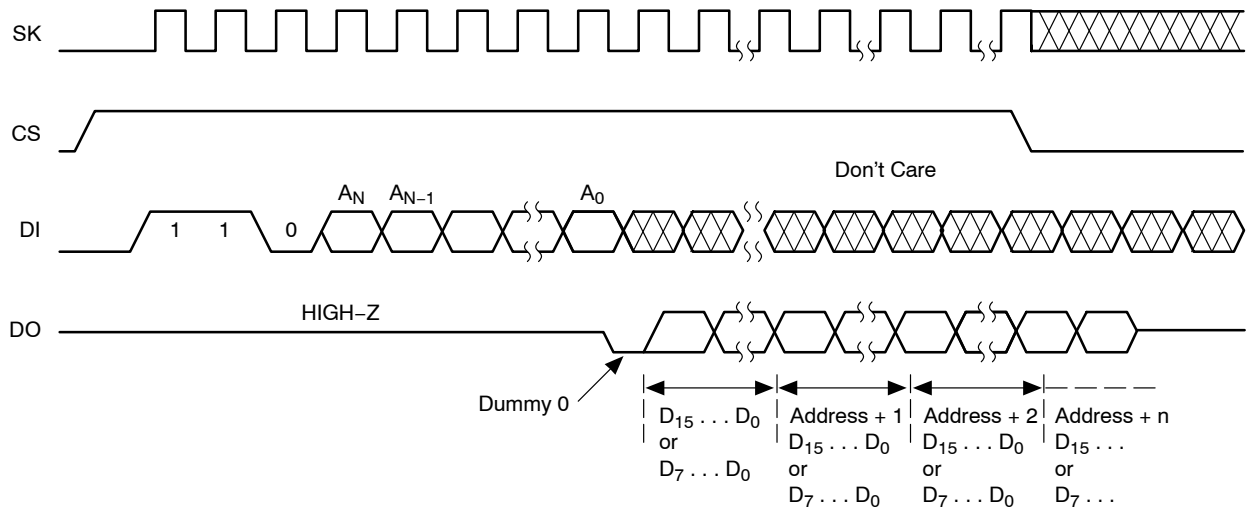
**Write**

After receiving a WRITE command, address and the data, the CS (Chip Select) pin must be deselected for a minimum of  $t_{CSMIN}$ . The falling edge of CS will start the self clocking clear and data store cycle of the memory location specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C76B can be determined by selecting the device and polling the DO pin. Since this device features Auto-Clear before write, it is NOT necessary to erase a memory location before it is written into.

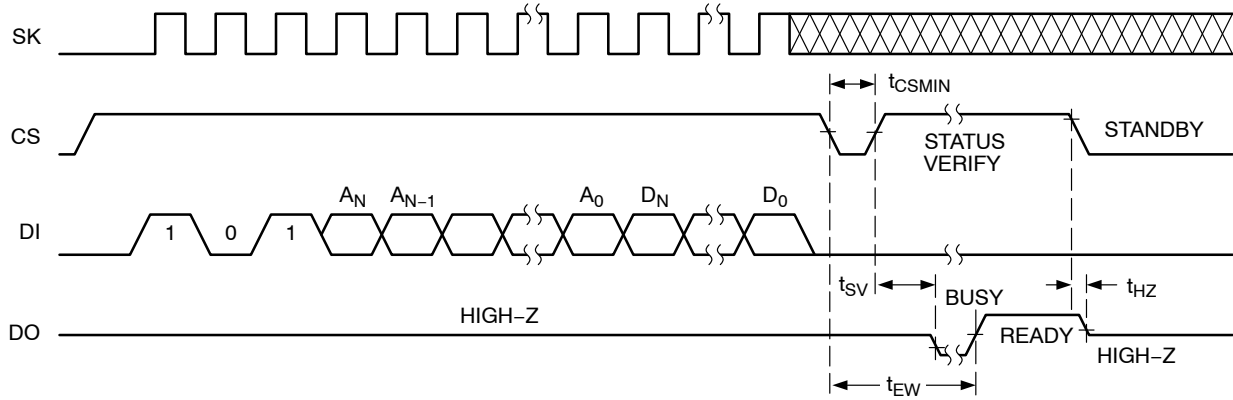


Figure 2. Synchronous Data Timing

# CAT93C76B



**Figure 3. READ Instruction Timing**



**Figure 4. WRITE Instruction Timing**

# CAT93C76B

## Erase

Upon receiving an ERASE command and address, the CS (Chip Select) pin must be deasserted for a minimum of  $t_{CSMIN}$ . The falling edge of CS will start the self clocking clear cycle of the selected memory location. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C76B can be determined by selecting the device and polling the DO pin. Once cleared, the content of a cleared location returns to a logical “1” state.

## Erase/Write Enable and Disable

The CAT93C76B powers up in the write disable state. Any writing after power-up or after an EWDS (write disable) instruction must first be preceded by the EWEN (write enable) instruction. Once the write instruction is enabled, it will remain enabled until power to the device is removed, or the EWDS instruction is sent. The EWDS instruction can be used to disable all CAT93C76B write and clear instructions, and will prevent any accidental writing or clearing of the device. Data can be read normally from the device regardless of the write enable/disable status.

## Erase All

Upon receiving an ERAL command, the CS (Chip Select) pin must be deselected for a minimum of  $t_{CSMIN}$ . The falling edge of CS will start the self clocking clear cycle of all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C76B can be

determined by selecting the device and polling the DO pin. Once cleared, the contents of all memory bits return to a logical “1” state.

## Write All

Upon receiving a WRAL command and data, the CS (Chip Select) pin must be deselected for a minimum of  $t_{CSMIN}$ . The falling edge of CS will start the self clocking data write to all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C76B can be determined by selecting the device and polling the DO pin. It is not necessary for all memory locations to be cleared before the WRAL command is executed.

**Note 1:** After the last data bit has been sampled, Chip Select (CS) must be brought Low before the next rising edge of the clock (SK) in order to start the self-timed high voltage cycle. This is important because if CS is brought low before or after this specific frame window, the addressed location will not be programmed or erased.

## Power-On Reset (POR)

The CAT93C76B incorporates Power-On Reset (POR) circuitry which protects the device against malfunctioning while  $V_{CC}$  is lower than the recommended operating voltage.

The device will power up into a read-only state and will power-down into a reset state when  $V_{CC}$  crosses the POR level of ~1.3 V.

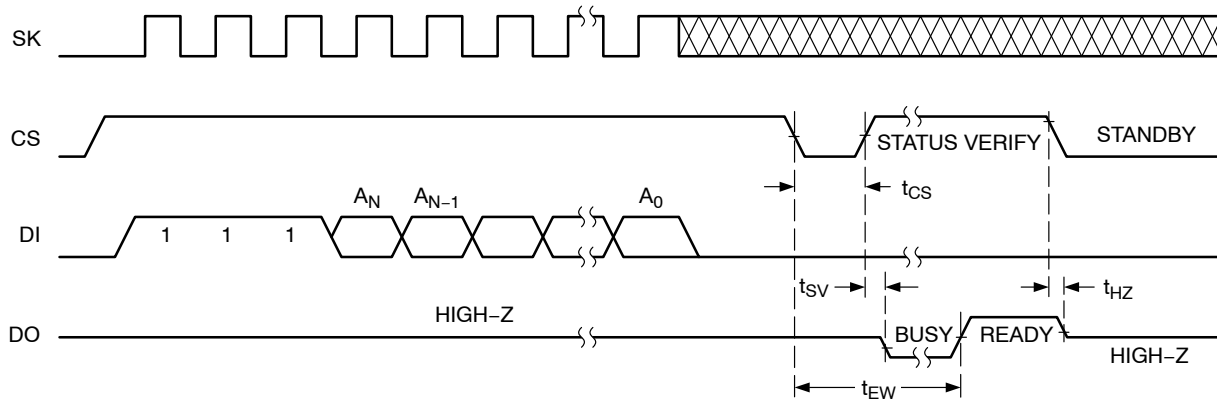


Figure 5. ERASE Instruction Timing

# CAT93C76B

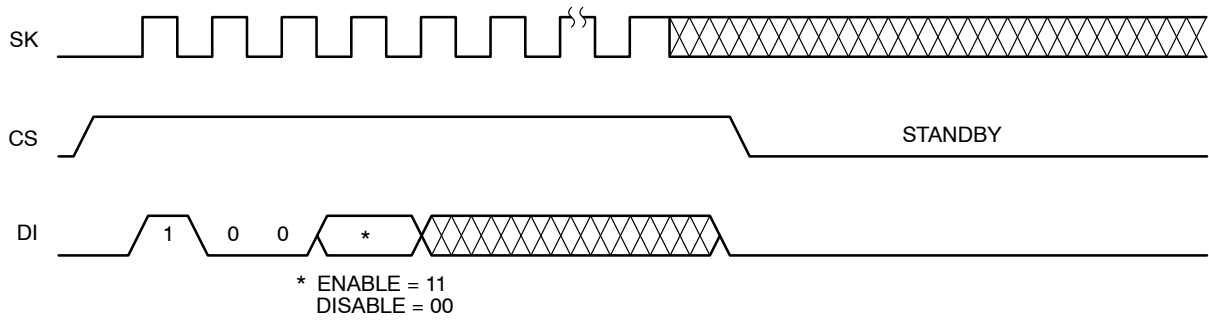


Figure 6. EWEN/EWDS Instruction Timing

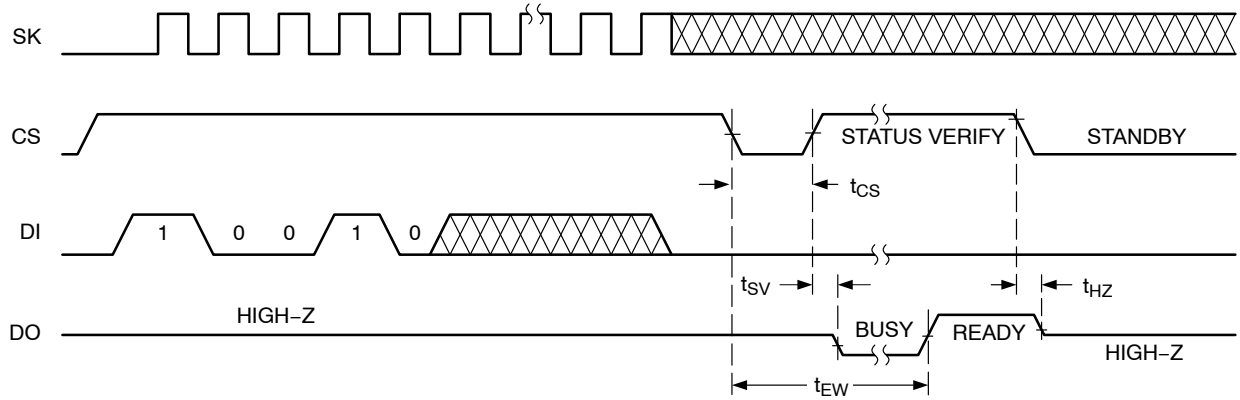


Figure 7. ERAL Instruction Timing

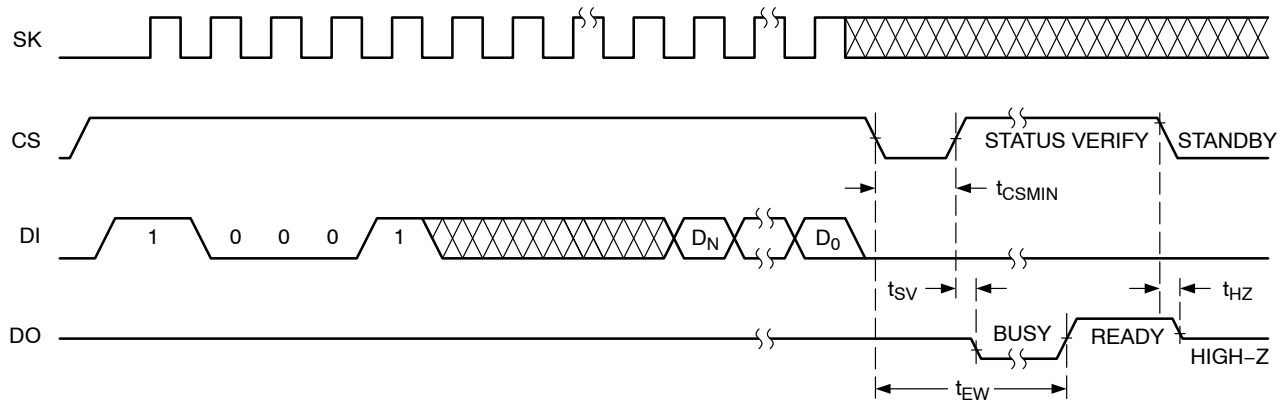


Figure 8. WRAL Instruction Timing

## CAT93C76B

### ORDERING INFORMATION

Device Order Number	Specific Device Marking	Package Type	Temperature Range	Shipping
CAT93C76BVI-GT3	93C76D	SOIC-8, JEDEC	I = Industrial (-40°C to +85°C)	Tape & Reel, 3,000 Units / Reel
CAT93C76BVI-GT3L	93C76D	SOIC-8, JEDEC	I = Industrial (-20°C to +85°C)	Tape & Reel, 3,000 Units / Reel
CAT93C76BVE-GT3	93C76D	SOIC-8, JEDEC	E = Extended (-40°C to +125°C)	Tape & Reel, 3,000 Units / Reel
CAT93C76BYI-GT3	M76D	TSSOP-8	I = Industrial (-40°C to +85°C)	Tape & Reel, 3,000 Units / Reel
CAT93C76BYE-GT3	M76D	TSSOP-8	E = Extended (-40°C to +125°C)	Tape & Reel, 3,000 Units / Reel
CAT93C76BHU4I-GT3	M3U	UDFN-8	I = Industrial (-40°C to +85°C)	Tape & Reel, 3,000 Units / Reel

8. All packages are RoHS-compliant (Lead-free, Halogen-free).

9. The standard lead finish is NiPdAu.

10. For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

11. For additional package and temperature options, please contact your nearest **onsemi** sales office.

12. For detailed information and a breakdown of device nomenclature and numbering systems, please see the **onsemi** Device Nomenclature document, TND310/D, available at [www.onsemi.com](http://www.onsemi.com)



# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

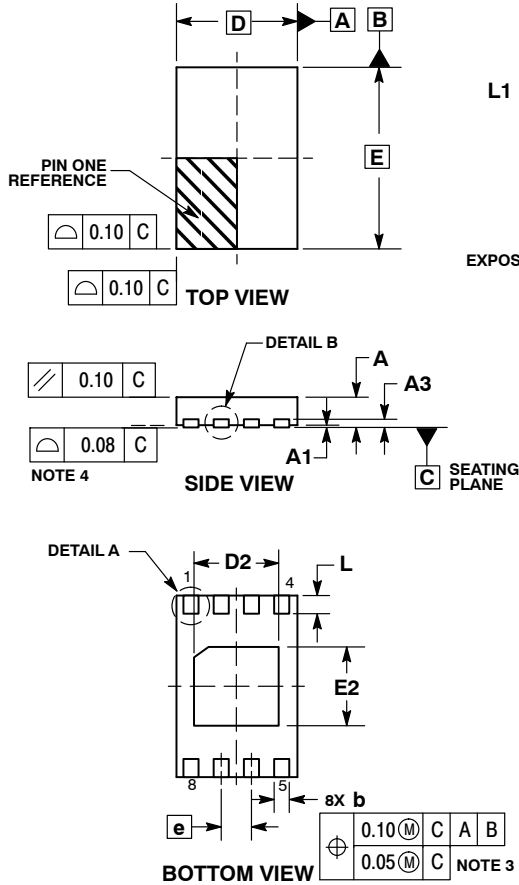
ON Semiconductor®



SCALE 2:1

### UDFN8, 2x3 EXTENDED PAD CASE 517AZ ISSUE A

DATE 23 MAR 2015

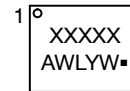


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.25MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS	
	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13 REF	
b	0.20	0.30
D	2.00 BSC	
D2	1.35	1.45
E	3.00 BSC	
E2	1.25	1.35
e	0.50 BSC	
L	0.25	0.35
L1	---	0.15

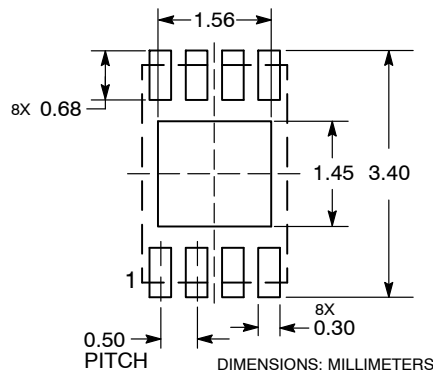
### GENERIC MARKING DIAGRAM\*



- XXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

### RECOMMENDED SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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<b>DESCRIPTION:</b>	<b>UDFN8, 2X3 EXTENDED PAD</b>	<b>PAGE 1 OF 1</b>

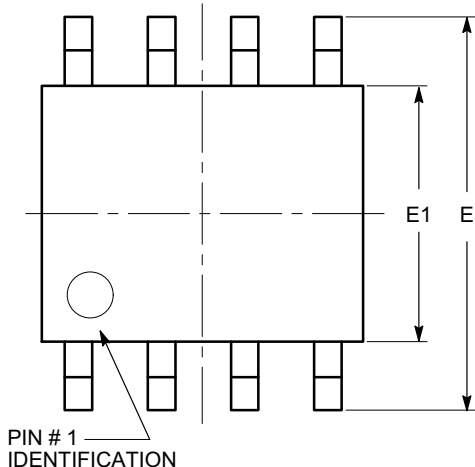
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**MECHANICAL CASE OUTLINE**  
**PACKAGE DIMENSIONS**



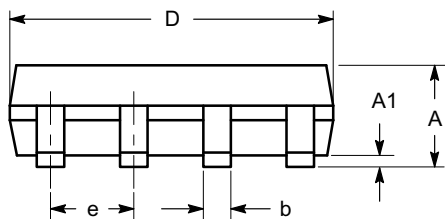
**SOIC-8, 150 mils**  
**CASE 751BD**  
**ISSUE O**

DATE 19 DEC 2008

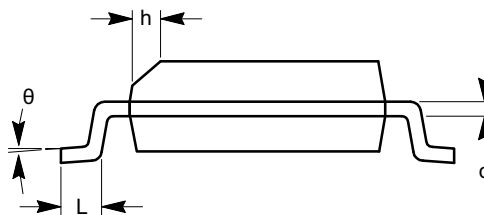


**TOP VIEW**

SYMBOL	MIN	NOM	MAX
A	1.35		1.75
A1	0.10		0.25
b	0.33		0.51
c	0.19		0.25
D	4.80		5.00
E	5.80		6.20
E1	3.80		4.00
e	1.27 BSC		
h	0.25		0.50
L	0.40		1.27
$\theta$	0°		8°



**SIDE VIEW**



**END VIEW**

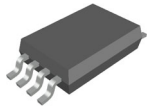
**Notes:**

- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC MS-012.

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<b>DESCRIPTION:</b>	<b>SOIC 8, 150 MILS</b>	<b>PAGE 1 OF 1</b>

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# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



TSSOP8, 4.4x3.0, 0.65P  
CASE 948AL  
ISSUE A

DATE 20 MAY 2022



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5, 2009..
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL NOT BE 0.15 IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.
5. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONS D AND E1 ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AT DATUM PLANE H.
7. DATUMS A AND B ARE TO BE DETERMINED AT DATUM H.
8. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 AND 0.25 FROM THE LEAD TIP..
9. A1 IS DEFINED AS THE LOWEST VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY..



DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	---	---	1.20
A1	0.05	---	0.15
A2	0.80	0.90	1.05
b	0.19	---	0.30
c	0.09	---	0.20
D	2.90	3.00	3.10
E	6.30	6.40	6.50
E1	4.30	4.40	4.50
e	0.65 BSC		
L	1.00 REF		
L1	0.50	0.60	0.70
θ	0°	---	8°

GENERIC  
MARKING DIAGRAM\*



- XXX = Specific Device Code
- Y = Year
- WW = Work Week
- A = Assembly Location
- = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



\* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	TSSOP8, 4.4X3.0, 0.65P	PAGE 1 OF 1

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