

High Current Bias Resistor Transistor

PNP Silicon

**NSB9435T1G,
NSV9435T1G**

Features

- Collector–Emitter Sustaining Voltage –
 $V_{CEO(sus)} = 30 \text{ Vdc (Min) @ } I_C = 10 \text{ mAdc}$
- High DC Current Gain –
 $h_{FE} = 125 \text{ (Min) @ } I_C = 0.8 \text{ Adc}$
 $= 90 \text{ (Min) @ } I_C = 3.0 \text{ Adc}$
- Low Collector–Emitter Saturation Voltage –
 $V_{CE(sat)} = 0.275 \text{ Vdc (Max) @ } I_C = 1.2 \text{ Adc}$
 $= 0.55 \text{ Vdc (Max) @ } I_C = 3.0 \text{ Adc}$
- SOT–223 Surface Mount Packaging
- ESD Rating – Human Body Model: Class 1B
– Machine Model: Class B
- AEC–Q101 Qualified and PPAP Capable
- NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant*

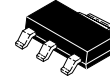
MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	30	Vdc
Collector–Base Voltage	V_{CB}	45	Vdc
Emitter–Base Voltage	V_{EB}	± 6.0	Vdc
Base Current – Continuous	I_B	1.0	Adc
Collector Current Continuous Peak	I_C	3.0 5.0	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C Total P_D @ $T_A = 25^\circ\text{C}$ mounted on 1" sq. (645 sq. mm) Collector pad on FR–4 bd material Total P_D @ $T_A = 25^\circ\text{C}$ mounted on 0.012" sq. (7.6 sq. mm) Collector pad on FR–4 bd material	P_D	3.0 24 1.56 0.72	W mW/ $^\circ\text{C}$ W W
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to +150	$^\circ\text{C}$

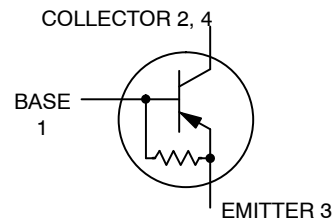
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

*For additional information on our Pb–Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

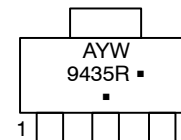
POWER BJT
 $I_C = 3.0 \text{ AMPERES}$
 $BV_{CEO} = 30 \text{ VOLTS}$
 $V_{CE(sat)} = 0.275 \text{ VOLTS}$



**SOT–223
CASE 318E
STYLE 1**



MARKING DIAGRAM



A = Assembly Location
Y = Year
W = Work Week
9435R = Device Code
▪ = Pb–Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NSB9435T1G	SOT–223 (Pb–Free)	1,000/Tape & Reel
NSV9435T1G	SOT–223 (Pb–Free)	1,000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NSB9435T1G, NSV9435T1G

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance Junction-to-Case Junction-to-Ambient on 1" sq. (645 sq. mm) Collector pad on FR-4 board material Junction-to-Ambient on 0.012" sq. (7.6 sq. mm) Collector pad on FR-4 board material	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	42 80 174	$^{\circ}\text{C/W}$
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 s	T_L	260	$^{\circ}\text{C}$

ELECTRICAL CHARACTERISTICS ($T_A = 25^{\circ}\text{C}$ unless otherwise noted)

Characteristics	Symbol	Min	Typ	Max	Unit
-----------------	--------	-----	-----	-----	------

OFF CHARACTERISTICS

Collector-Emitter Sustaining Voltage ($I_C = 10\text{ mAdc}$, $I_B = 0\text{ Adc}$)	$V_{CE(sus)}$	30	–	–	Vdc
Emitter-Base Voltage ($I_E = 50\text{ }\mu\text{Adc}$, $I_C = 0\text{ Adc}$)	V_{EBO}	6.0	–	–	Vdc
Collector Cutoff Current ($V_{CE} = 25\text{ Vdc}$) ($V_{CE} = 25\text{ Vdc}$, $T_J = 125^{\circ}\text{C}$)	I_{CER}	– –	– –	20 200	μAdc
Emitter Cutoff Current ($V_{BE} = 5.0\text{ Vdc}$)	I_{EBO}	–	–	700	μAdc

ON CHARACTERISTICS (Note 1)

Collector-Emitter Saturation Voltage ($I_C = 0.8\text{ Adc}$, $I_B = 20\text{ mAdc}$) ($I_C = 1.2\text{ Adc}$, $I_B = 20\text{ mAdc}$) ($I_C = 3.0\text{ Adc}$, $I_B = 0.3\text{ Adc}$)	$V_{CE(sat)}$	– – –	0.155 – –	0.210 0.275 0.550	Vdc
Base-Emitter Saturation Voltage ($I_C = 3.0\text{ Adc}$, $I_B = 0.3\text{ Adc}$)	$V_{BE(sat)}$	–	–	1.25	Vdc
Base-Emitter On Voltage ($I_C = 1.2\text{ Adc}$, $V_{CE} = 4.0\text{ Vdc}$)	$V_{BE(on)}$	–	–	1.10	Vdc
DC Current Gain ($I_C = 0.8\text{ Adc}$, $V_{CE} = 1.0\text{ Vdc}$) ($I_C = 1.2\text{ Adc}$, $V_{CE} = 1.0\text{ Vdc}$) ($I_C = 3.0\text{ Adc}$, $V_{CE} = 1.0\text{ Vdc}$)	h_{FE}	125 110 90	220 – –	– – –	–
Resistor	R1	7.5	10	12.5	k Ω

DYNAMIC CHARACTERISTICS

Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0\text{ Adc}$, $f = 1.0\text{ MHz}$)	C_{ob}	–	100	150	pF
Input Capacitance ($V_{EB} = 8.0\text{ Vdc}$)	C_{ib}	–	135	–	pF
Current-Gain – Bandwidth Product (Note 2) ($I_C = 500\text{ mA}$, $V_{CE} = 10\text{ V}$, $F_{test} = 1.0\text{ MHz}$)	f_T	–	110	–	MHz

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. Pulse Test: Pulse Width $\leq 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2\%$.
2. $f_T = |h_{FE}| \cdot f_{test}$

NSB9435T1G, NSV9435T1G

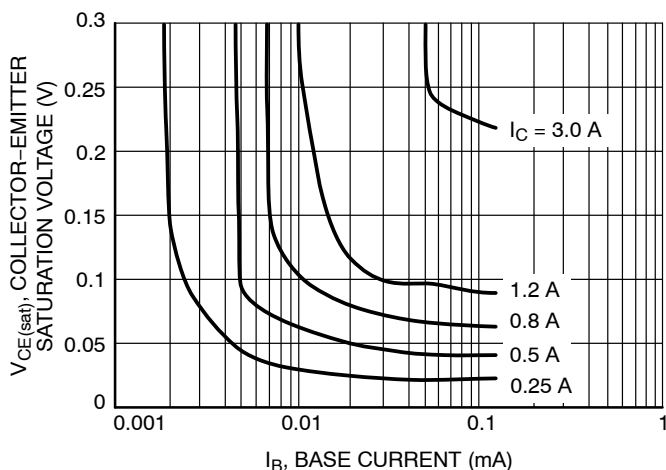


Figure 1. Collector Saturation Region

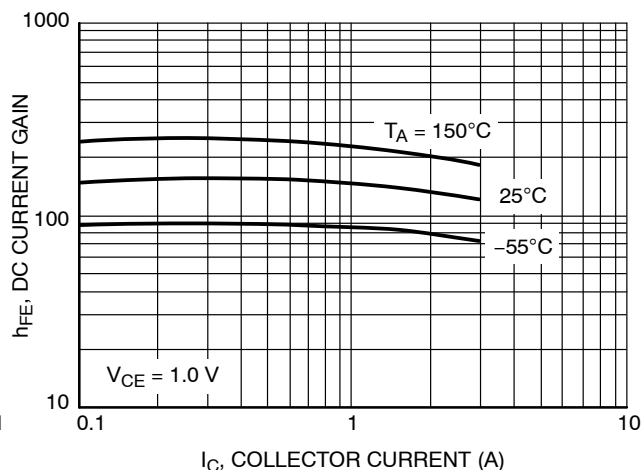


Figure 2. DC Current Gain

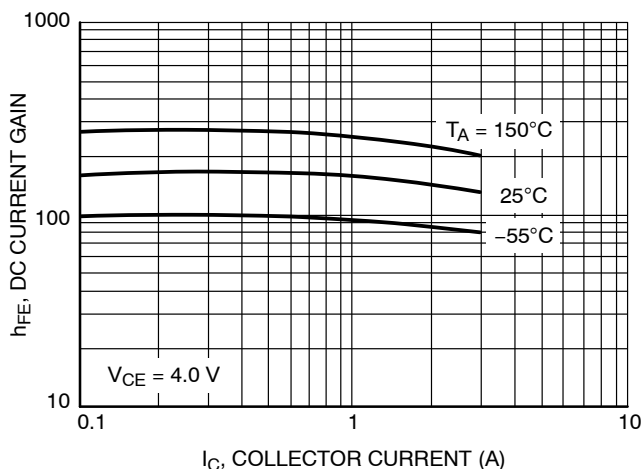


Figure 3. DC Current Gain

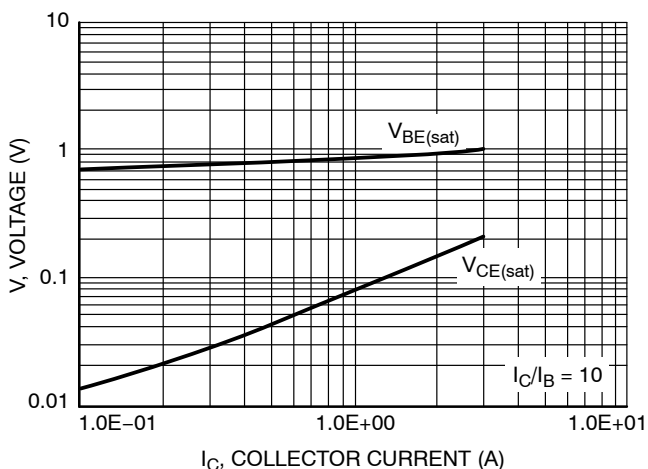


Figure 4. "ON" Voltages

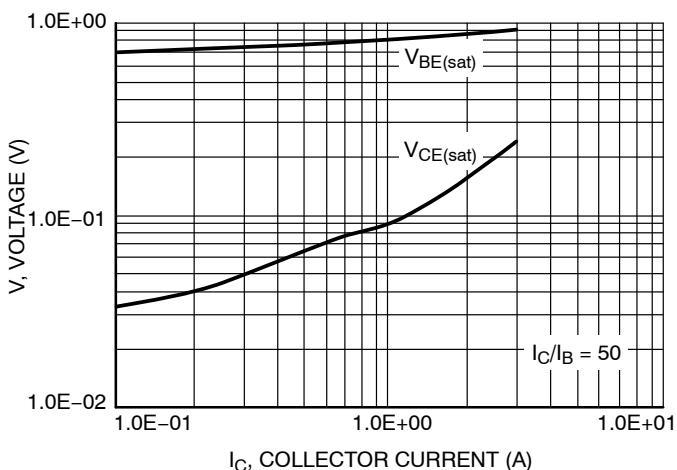


Figure 5. "ON" Voltages

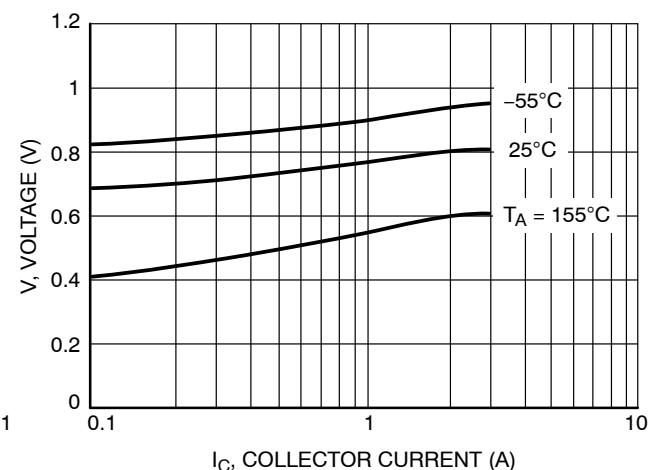


Figure 6. $V_{BE(on)}$ Voltage

NSB9435T1G, NSV9435T1G

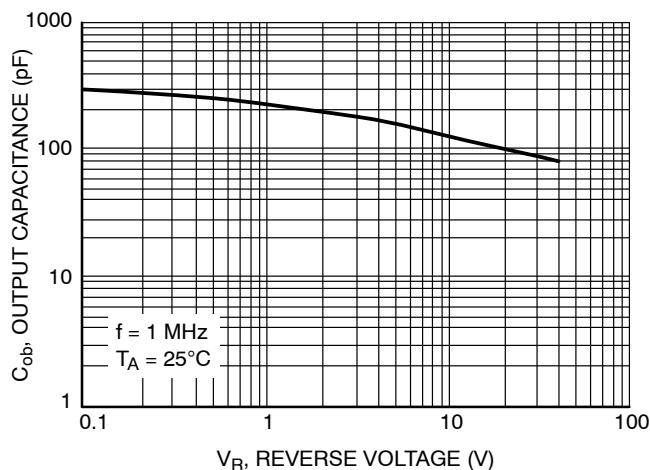


Figure 7. Output Capacitance

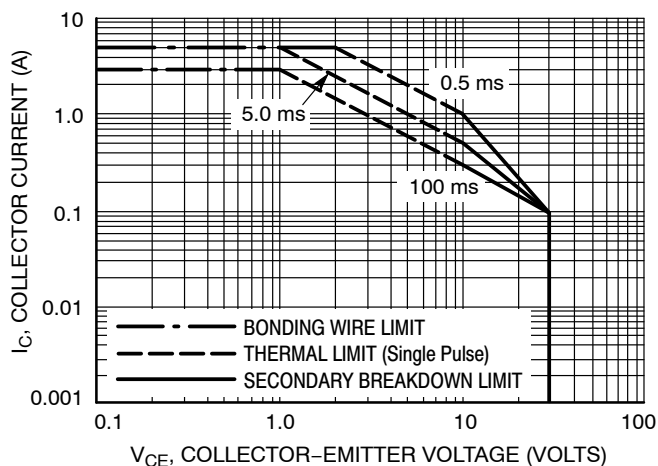


Figure 8. Active Region Safe Operating Area

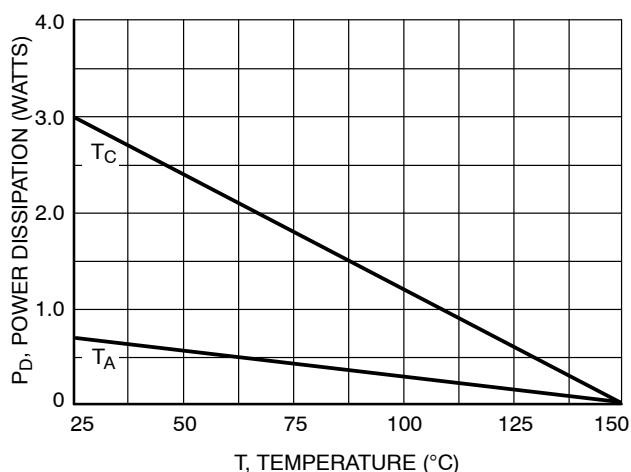


Figure 9. Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 8 is based on $T_{J(pk)} = 150^\circ\text{C}$; T_C is variable depending on conditions. Secondary breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^\circ\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 10. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

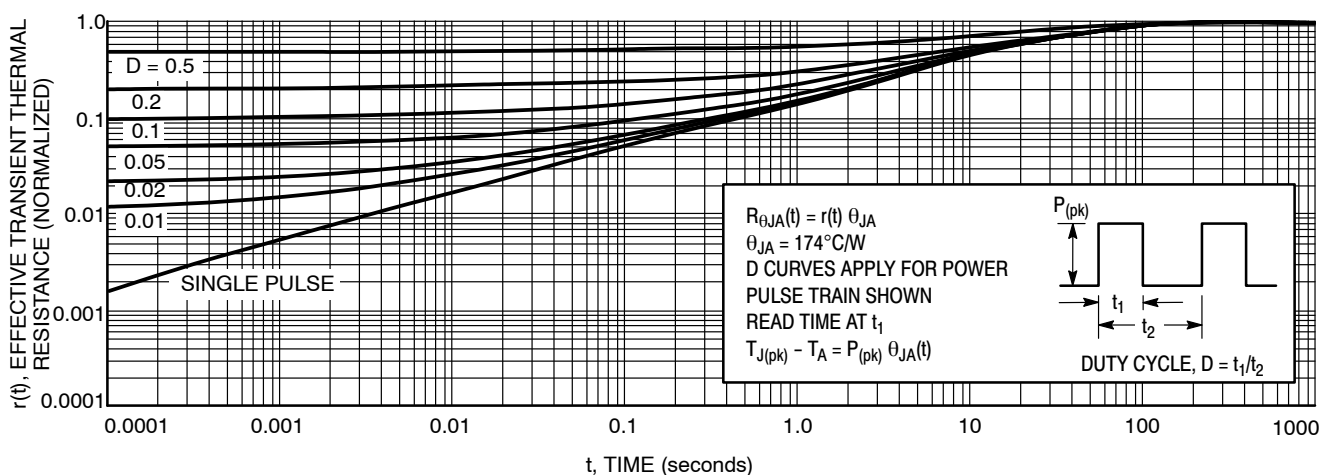


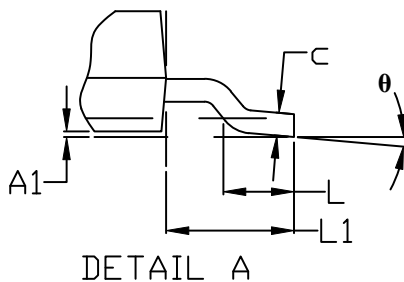
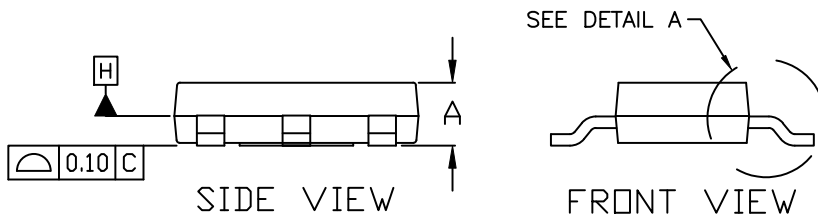
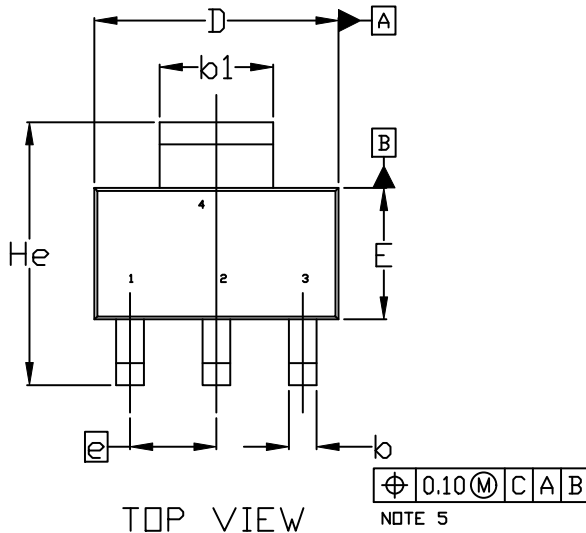
Figure 10. Thermal Response



SCALE 1:1

SOT-223 (TO-261)
CASE 318E-04
ISSUE R

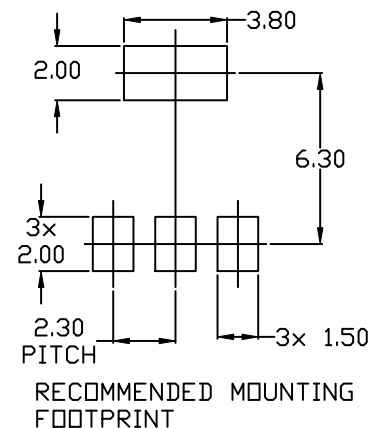
DATE 02 OCT 2018



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D & E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.200MM PER SIDE.
4. DATUMS A AND B ARE DETERMINED AT DATUM H.
5. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
6. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS b AND b1.

MILLIMETERS			
DIM	MIN.	NOM.	MAX.
A	1.50	1.63	1.75
A1	0.02	0.06	0.10
b	0.60	0.75	0.89
b1	2.90	3.06	3.20
c	0.24	0.29	0.35
D	6.30	6.50	6.70
E	3.30	3.50	3.70
e	2.30 BSC		
L	0.20	---	---
L1	1.50	1.75	2.00
He	6.70	7.00	7.30
θ	0°	---	10°



DOCUMENT NUMBER:	98ASB42680B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOT-223 (TO-261)	PAGE 1 OF 2

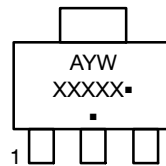
ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

SOT-223 (TO-261)
CASE 318E-04
ISSUE R

DATE 02 OCT 2018

STYLE 1: PIN 1. BASE 2. COLLECTOR 3. EMITTER 4. COLLECTOR	STYLE 2: PIN 1. ANODE 2. CATHODE 3. NC 4. CATHODE	STYLE 3: PIN 1. GATE 2. DRAIN 3. SOURCE 4. DRAIN	STYLE 4: PIN 1. SOURCE 2. DRAIN 3. GATE 4. DRAIN	STYLE 5: PIN 1. DRAIN 2. GATE 3. SOURCE 4. GATE
STYLE 6: PIN 1. RETURN 2. INPUT 3. OUTPUT 4. INPUT	STYLE 7: PIN 1. ANODE 1 2. CATHODE 3. ANODE 2 4. CATHODE	STYLE 8: CANCELLED	STYLE 9: PIN 1. INPUT 2. GROUND 3. LOGIC 4. GROUND	STYLE 10: PIN 1. CATHODE 2. ANODE 3. GATE 4. ANODE
STYLE 11: PIN 1. MT 1 2. MT 2 3. GATE 4. MT 2	STYLE 12: PIN 1. INPUT 2. OUTPUT 3. NC 4. OUTPUT	STYLE 13: PIN 1. GATE 2. COLLECTOR 3. EMITTER 4. COLLECTOR		

**GENERIC
MARKING DIAGRAM***



- A = Assembly Location
- Y = Year
- W = Work Week
- XXXXX = Specific Device Code
- = Pb-Free Package

(Note: Microdot may be in either location)
 *This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	98ASB42680B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOT-223 (TO-261)	PAGE 2 OF 2

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at
www.onsemi.com/support/sales