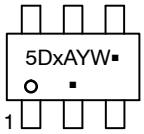
# Current-Mode PWM Controller for Off-line Power Supplies

# NCP12510




**TSOP−6**
**(SOT23−6)**
**SN SUFFIX**
**CASE 318G**
**STYLE 13**

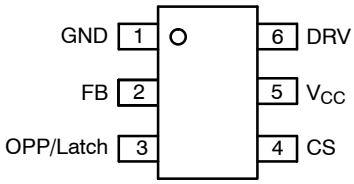
**MARKING DIAGRAM**




| | |
|---|---|
| 5Dx | = Specific Device Code |
| x | = A, 2, C, D, J, or K |
| A | = Assembly Location |
| Y | = Year |
| W | = Work Week |
| ▪ | = Pb−Free Package |

(Note: Microdot may be in either location)

**PIN CONNECTIONS**




(Top View)

**ORDERING INFORMATION**

See detailed ordering, marking and shipping information on page 2 of this data sheet.

The NCP12510 is a highly integrated PWM controller capable of delivering a rugged and high performance offline power supply in a tiny TSOP−6 package. With a voltage supply range up to 35 V, the controller hosts a jittered 65 kHz or 100 kHz switching circuitry operated in peak current mode control. When the power on the secondary side starts decreasing, the controller automatically folds back its switching frequency down to a minimum level of 26 kHz. As the power further goes down, the part enters skip cycle while limiting the peak current.

Over Power Protection (OPP) is a difficult exercise especially when no−load standby requirements drive the converter specifications. The **onsemi** proprietary integrated OPP allows harness the maximum delivered power without affecting the standby performance simply via two external resistors. An Over Voltage Protection (OVP) input is also combined on the same pin and protects the whole circuitry in case of optocoupler destruction or adverse open loop operation.

Finally, a timer−based short−circuit protection offers the best protection scheme, allowing precisely select the protection trip point without caring of a loose coupling between the auxiliary and the power windings.

NCP12510 is improved and pin compatible controller based on very popular flyback controller NCP1250.

### Features

- Fixed−Frequency 65 kHz or 100 kHz Current−Mode Control Operation
- Frequency Foldback Down to 26 kHz and Skip−Cycle in Light Load Conditions
- Frequency Jittering in Normal and Frequency Foldback Modes
- Internal and Adjustable Over Power Protection (OPP) Circuit
- Auto−Recovery Over Voltage Protection (OVP) on the VCC Pin
- Internal and Adjustable Slope Compensation
- Internal Fixed 4 ms Soft−Start
- Auto−Recovery or Latched Short−Circuit Protection
- Pre−Short Ready for Latched OCP Version
- OVP/OTP Latch Input for Improved Robustness
- +300 mA/ −500 mA Source/Sink Drive Capability
- Improved Consumption
- Improved Reset Time in Latch State
- High Robustness and High ESD Capabilities
- EPS 2.0 Compliant
- This is a Pb−Free Device

### Typical Applications

- Ac−dc Converters for TVs, Set−top Boxes and DVD Players
- Offline Adapters for Notebooks and Netbooks

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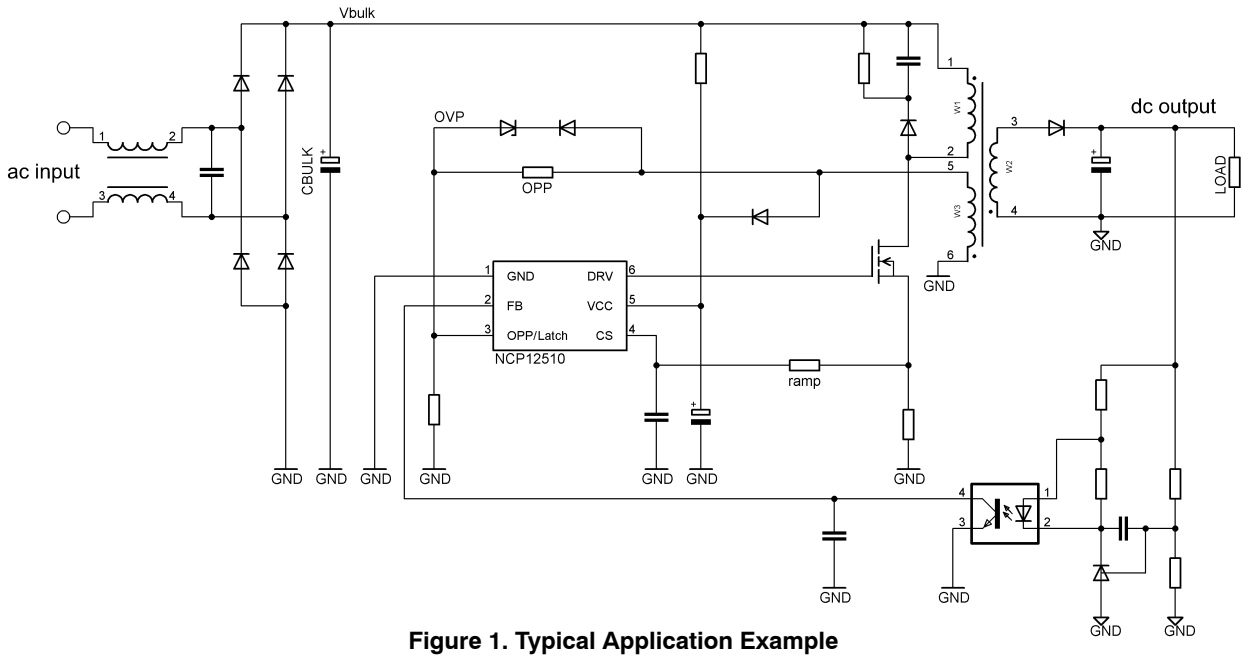



**Figure 1. Typical Application Example**

**Table 1. PIN DESCRIPTION**

| Pin No | Pin Name | Function | Pin Description |
|---|---|---|---|
| 1 | GND | – | The controller ground. |
| 2 | FB | Feedback pin | Hooking an optocoupler collector to this pin will allow regulation. |
| 3 | OPP/Latch | Adjust the Over Power Protection Latches off the part | A resistive divider from the auxiliary winding to this pin sets the OPP compensation level during the on−time. When the voltage exceeds a certain level at turn off, the part is fully latched off. |
| 4 | CS | Current sense + slope compensation | This pin monitors the primary peak current but also offers a means to introduce slope compensation. |
| 5 | $V_{CC}$ | Supplies the controller − protects the IC | This pin is connected to an external auxiliary voltage. When the $V_{CC}$ exceeds a certain level, the part enters an auto−recovery hiccup. |
| 6 | DRV | Driver output | The driver output to an external MOSFET gate. |

**Table 2. DEVICE OPTIONS AND ORDERING INFORMATION**

| **Controller** (Note 1) | **Package Marking** | **OCP protection** | **OVP/OTP protection** | **Switching Frequency** | **$V_{OVP}$** | **Package** | **Shipping†** |
|---|---|---|---|---|---|---|---|
| NCP12510ASN65T1G | 5DA | Latched w/o Pre−short | Latched | 65 kHz | 25.5 V | TSOP−6 (Pb−Free) | 3000 / Tape & Reel |
| NCP12510BSN65T1G | 5D2 | Auto−recovery | Latched | 65 kHz | 25.5 V | | |
| NCP12510CSN65T1G | 5DC | Auto−recovery | Auto−recovery | 65 kHz | 25.5 V | | |
| NCP12510DSN65T1G | 5DD | Auto−recovery | Latched | 65 kHz | 32 V | | |
| NCP12510ASN100T1G | 5DJ | Latched w/o Pre−short | Latched | 100 kHz | 25.5 V | | |
| NCP12510BSN100T1G | 5DK | Auto−recovery | Latched | 100 kHz | 25.5 V | | |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

1. Other options available upon customer request.

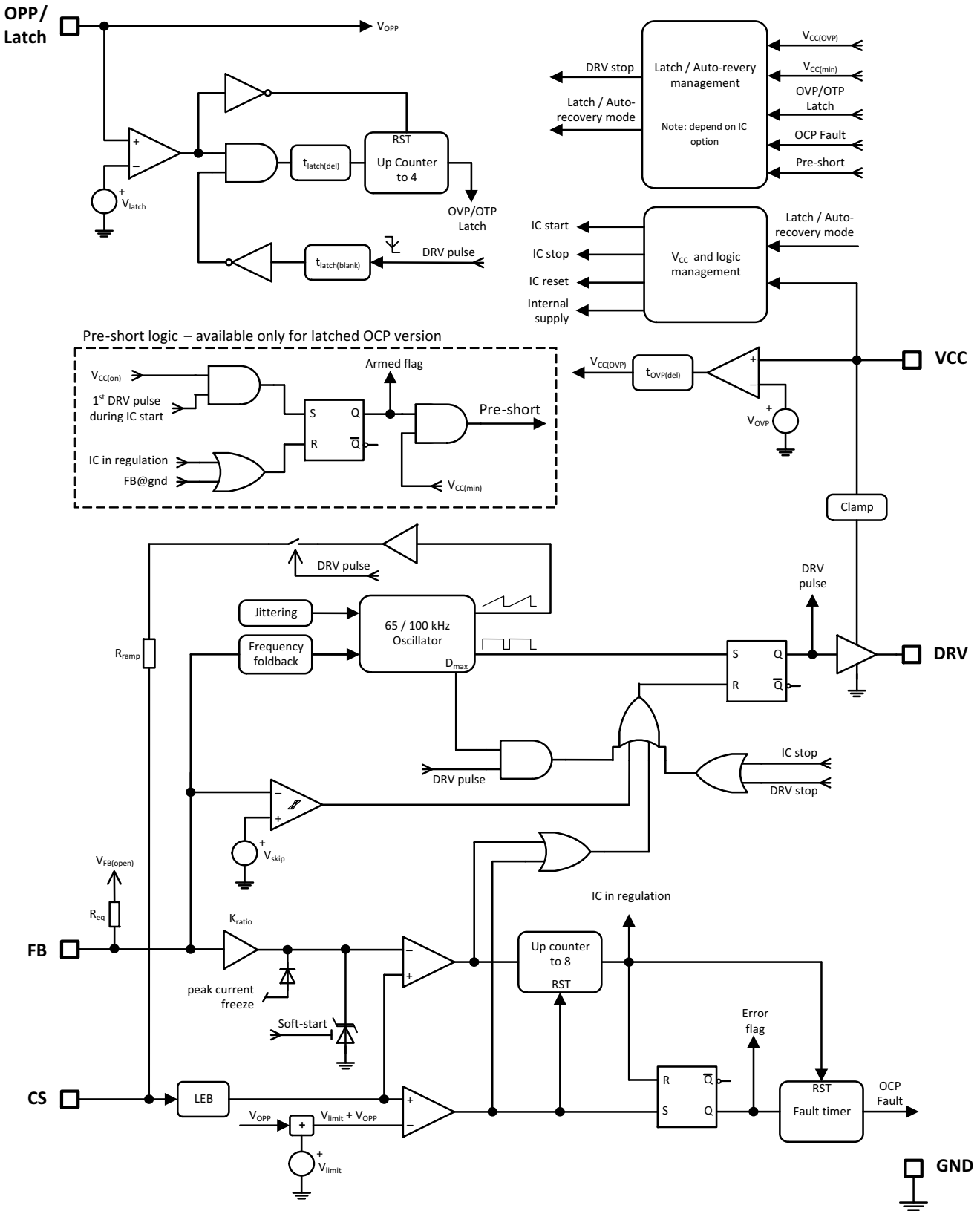



**Figure 2. Internal Circuit Architecture**

**Table 3. MAXIMUM RATINGS TABLE**

| Symbol | Rating | Value | Unit |
|---|---|---|---|
| $V_{CC}$ | Power Supply voltage, VCC pin, continuous voltage | −0.3 to 35 | V |
| $V_{DRV(tran)}$ | Maximum DRV pin voltage when DRV in H state, transient voltage (Note 1) | −0.3 to $V_{CC}$ + 0.3 | V |
| $V_{CS}$, $V_{FB}$, $V_{OPP}$ | Maximum voltage on low power pins CS, FB and OPP (Note 2) | −0.3 to 5.5 | V |
| $V_{OPP(tran)}$ | Maximum negative transient voltage on OPP pin (Note 2) | −1 | V |
| $I_{source,max}$ | Maximum sourced current, pulsed width < 800 ns | 0.6 | A |
| $I_{sink,max}$ | Maximum sinked current, pulse width < 800 ns | 1.0 | A |
| $I_{OPP}$ | Maximum injected negative current into the OPP pin (pin 3) | −2 | mA |
| $R_{\theta J-A}$ | Thermal Resistance Junction−to−Air | 360 | °C/W |
| $T_{J,max}$ | Maximum Junction Temperature | 150 | °C |
| | Storage Temperature Range | −60 to +150 | °C |
| HBM | Human Body Model ESD Capability per JEDEC JESD22−A114F (All pins) | 4 | kV |
| CDM | Charged−Device Model ESD Capability per JEDEC JESD22−C101E | 750 | V |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The transient voltage is a voltage spike injected to DRV pin being in high state. Maximum transient duration is 100 ns.
2. See the Figure 3 for detailed specification of transient voltage.
3. This device contains latch−up protection and exceeds 100 mA per JEDEC Standard JESD78.

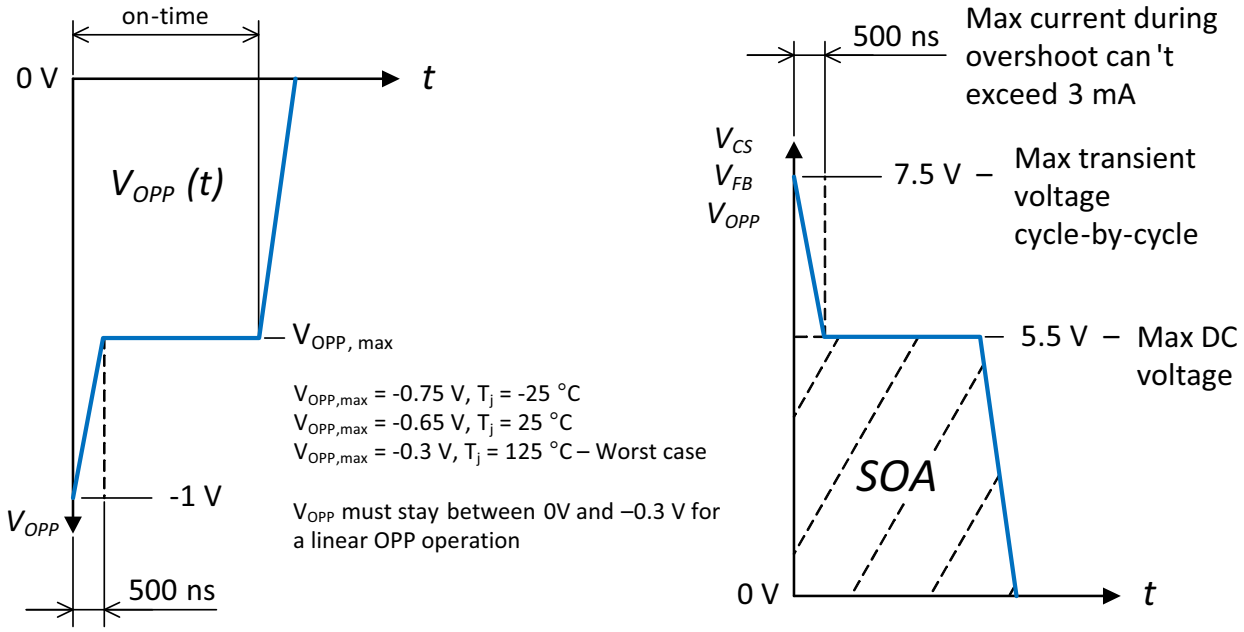



**Figure 3. Negative Pulse for OPP Pin during On−time and Positive Pulse for All Low Power Pins**

**Table 4. ELECTRICAL CHARACTERISTICS**
(For typical values $T_J$ = 25°C, for min/max values $T_J$ = −40°C to +125°C, $V_{CC}$ = 12 V unless otherwise noted)

| Symbol | Rating | Pin | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **SUPPLY SECTION** | | | | | | |
| $V_{CC(on)}$ | $V_{CC}$ increasing level at which driving pulses are authorized | 5 | 16 | 18 | 20 | V |
| $V_{CC(min)}$ | $V_{CC}$ decreasing level at which driving pulses are stopped | 5 | 8.3 | 8.9 | 9.5 | V |
| $V_{CC(hyst)}$ | Hysteresis $V_{CC(on)} - V_{CC(min)}$ | 5 | 7.7 | – | – | V |
| $V_{CC(reset)}$ | Latched state reset voltage | 5 | – | 8.6 | – | V |
| $V_{CC(reset_hyst)}$ | Defined hysteresis between minimum and reset voltage $V_{CC(min)} - V_{CC(reset)}$ | 5 | 0.15 | 0.30 | 0.45 | V |
| $V_{CC(latch_hyst)}$ | Defined hysteresis for hiccupping between two voltage levels in latch mode | 5 | – | 0.55 | – | V |
| $I_{CC1}$ | Start−up current ($V_{CC(on)}$ − 100 mV) | 5 | – | 6 | 10 | μA |
| $I_{CC2}$ | Internal IC consumption with $V_{FB}$ = 3.2 V, $f_{SW}$ = 65 kHz and $C_L$ = 0 nF<br>Internal IC consumption with $V_{FB}$ = 3.2 V, $f_{SW}$ = 100 kHz and $C_L$ = 0 nF | 5 | – | 1.0<br>1.1 | 1.4<br>1.5 | mA |
| $I_{CC3}$ | Internal IC consumption with $V_{FB}$ = 3.2 V, $f_{SW}$ = 65 kHz and $C_L$ = 1 nF<br>Internal IC consumption with $V_{FB}$ = 3.2 V, $f_{SW}$ = 100 kHz and $C_L$ = 1 nF | 5 | – | 1.7<br>2.3 | 2.7<br>3.0 | mA |
| $I_{CC(no-load)}$ | Internal consumption in skip mode − non switching, $V_{FB}$ = 0 V | 5 | – | 300 | – | μA |
| $I_{CC(fault)}$ | Internal consumption in fault during going−down $V_{CC}$, $V_{FB}$ = 4 V | 5 | 300 | 370 | – | μA |
| $I_{CC(standby)}$ | Internal IC consumption in skip mode for 65 kHz version ($V_{CC}$ = 14 V, driving a typical 7−A/600−V MOSFET, includes opto current) − (Note 4) | 5 | – | 420 | – | μA |
| **DRIVE OUTPUT** | | | | | | |
| $t_r$ | Output voltage rise−time @ $C_L$ = 1 nF, 10−90% of output signal | 6 | – | 40 | – | ns |
| $t_f$ | Output voltage fall−time @ $C_L$ = 1 nF, 10−90% of output signal | 6 | – | 30 | – | ns |
| $R_{OH}$ | Source resistance, $V_{CC}$ = 12 V, $I_{DRV}$ = 100 mA | 6 | – | 28 | – | Ω |
| $R_{OL}$ | Sink resistance, $V_{CC}$ = 12 V, $I_{DRV}$ = 100 mA | 6 | – | 7 | – | Ω |
| $I_{source}$ | Peak source current, $V_{GS}$ = 0 V | 6 | – | 300 | – | mA |
| $I_{sink}$ | Peak sink current, $V_{GS}$ = 12 V | 6 | – | 500 | – | mA |
| $V_{DRV(low)}$ | DRV pin level at $V_{CC}$ = $V_{CC(min)}$ + 100 mV with a 33 kΩ resistor to GND | 6 | 8 | – | – | V |
| $V_{DRV(high)}$ | DRV pin level at $V_{CC}$ = $V_{OVP}$ − 100 mV (DRV unloaded) | 6 | 10 | 12 | 14 | V |
| **CURRENT COMPARATOR** | | | | | | |
| $V_{limit}$ | Maximum internal current set point − $T_J$ = 25°C − pin 3 grounded<br>Maximum internal current set point − $T_J$ = −40°C to 125°C − pin 3 grounded | 4 | 0.744<br>0.720 | 0.8<br>0.8 | 0.856<br>0.880 | V |
| $V_{CS(fold)}$ | Internal voltage setpoint for frequency foldback trip point − 59% of $V_{limit}$ | 4 | – | 475 | – | mV |
| $V_{CS(freeze)}$ | Internal peak current setpoint freeze (≈31% of $V_{limit}$) | 4 | – | 250 | – | mV |
| $t_{DEL}$ | Propagation delay from CS pin to DRV output | 4 | – | 50 | 80 | ns |
| $t_{LEB}$ | Leading Edge Blanking Duration | 4 | – | 300 | – | ns |
| $t_{SS}$ | Internal soft−start duration activated upon startup or auto−recovery | 4 | – | 4 | – | ms |
| $I_{OPPs}$ | Set point decrease for pin 3 grounded | 3 | – | 0 | – | % |
| $I_{OPPo}$ | Set point decrease for pin 3 biased to −250 mV | 3 | – | 31.3 | – | % |
| $I_{OOPv}$ | Voltage set point for pin 3 biased to −250 mV, $T_J$ = 25°C<br>Voltage set point for pin 3 biased to −250 mV, $T_J$ = −40° to 125°C | 3 | 0.51<br>0.50 | 0.55<br>0.55 | 0.60<br>0.62 | V |
| **INTERNAL OSCILLATOR** | | | | | | |
| $f_{OSC(nom)}$ | Oscillation frequency (65 kHz version)<br>Oscillation frequency (100 kHz version) | – | 61<br>92 | 65<br>100 | 71<br>108 | kHz |
| $D_{max}$ | Maximum duty−ratio | – | 76 | 80 | 84 | % |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Application parameter for information only.
5. 1−MΩ resistor is connected from pin 4 to the ground for the measurement.

**Table 4. ELECTRICAL CHARACTERISTICS**
(For typical values $T_J$ = 25°C, for min/max values $T_J$ = −40°C to +125°C, $V_{CC}$ = 12 V unless otherwise noted)

| Symbol | Rating | Pin | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **INTERNAL OSCILLATOR** | | | | | | |
| $f_{jitter}$ | Frequency jittering in percentage of $f_{OSC}$ − jitter is kept even in foldback mode | − | − | ±5 | − | % |
| $f_{swing}$ | Swing frequency | − | − | 240 | − | Hz |
| **FEEDBACK SECTION** | | | | | | |
| $R_{eq}$ | Internal equivalent feedback resistance | 2 | − | 29 | − | kΩ |
| $K_{ratio}$ | FB pin to current set point division ratio | − | − | 4 | − | − |
| $V_{FB(freeze)}$ | Feedback voltage below which the peak current is frozen | 2 | − | 1.0 | − | V |
| $V_{FB(limit)}$ | Feedback voltage corresponding with maximum internal current set point | 2 | − | 3.2 | − | V |
| $V_{FB(open)}$ | Internal pull−up voltage on FB pin | 2 | − | 4 | − | V |
| **FREQUENCY FOLDBACK** | | | | | | |
| $V_{fold(start)}$ | Frequency foldback level on the FB pin − ≈59% of maximum peak current | − | − | 1.9 | − | V |
| $f_{trans}$ | Minimum operating frequency | − | 22 | 26 | 30 | kHz |
| $V_{fold(end)}$ | End of frequency foldback feedback level, $f_{sw} = f_{trans}$ | − | − | 1.5 | − | V |
| $V_{skip}$ | Skip−cycle level voltage on the feedback pin | − | − | 0.8 | − | V |
| $V_{skip(hyst)}$ | Hysteresis on the skip comparator | − | − | 50 | − | mV |
| **INTERNAL SLOPE COMPENSATION** | | | | | | |
| $V_{ramp}$ | Internal ramp level @ 25°C (Note 5) | 4 | − | 2.5 | − | V |
| $R_{ramp}$ | Internal ramp resistance to CS pin | 4 | − | 20 | − | kΩ |
| **PROTECTIONS** | | | | | | |
| $V_{latch}$ | Latching level input on OPP/Latch pin | 3 | 2.85 | 3.0 | 3.15 | V |
| $t_{latch(blank)}$ | Blanking time after Drive output turn off | 3 | − | 1 | − | μs |
| $t_{latch(count)}$ | Number of clock cycles before latch is confirmed | 3 | − | 4 | − | |
| $t_{latch(del)}$ | OVP/OTP delay time constant before latch is confirmed | 3 | − | 600 | − | ns |
| $V_{OVP}$ | Over voltage protection on the VCC pin (except D version) | 5 | 24.0 | 25.5 | 27.0 | V |
| $V_{OVP}$ | Over voltage protection on the VCC pin (D version only) | 5 | 30 | 32 | 34 | V |
| $t_{OVP(del)}$ | Delay time constant before OVP on VCC is confirmed | 5 | − | 20 | − | μs |
| $t_{fault}$ | Internal fault timer duration | − | 100 | 115 | 130 | ms |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Application parameter for information only.
5. 1−MΩ resistor is connected from pin 4 to the ground for the measurement.

## TYPICAL CHARACTERISTICS

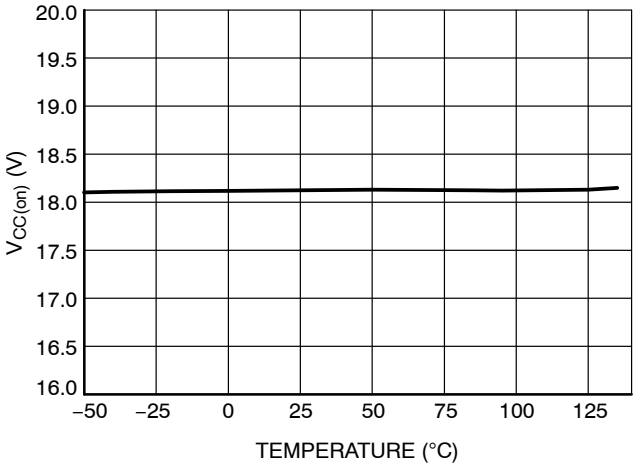



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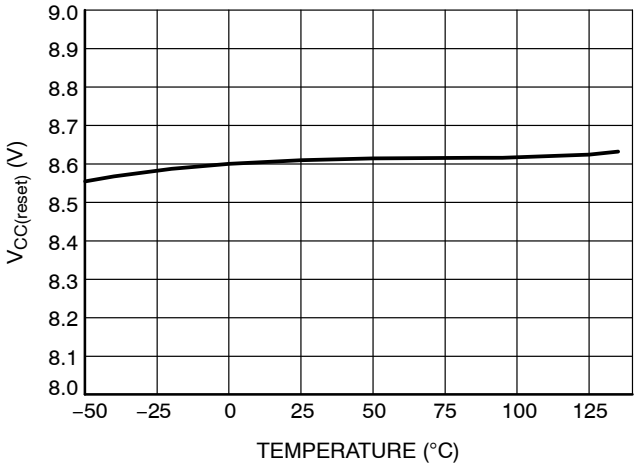



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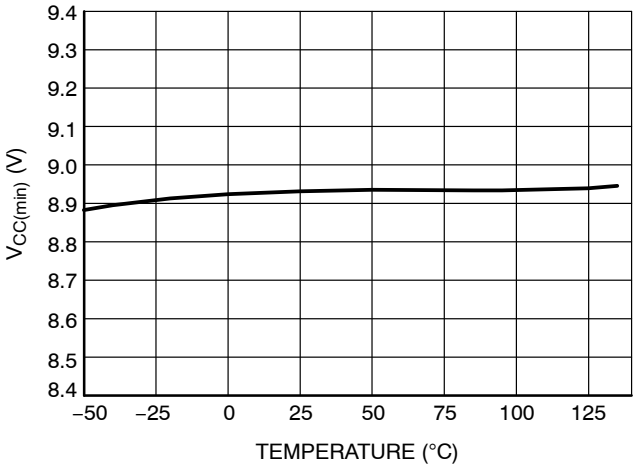



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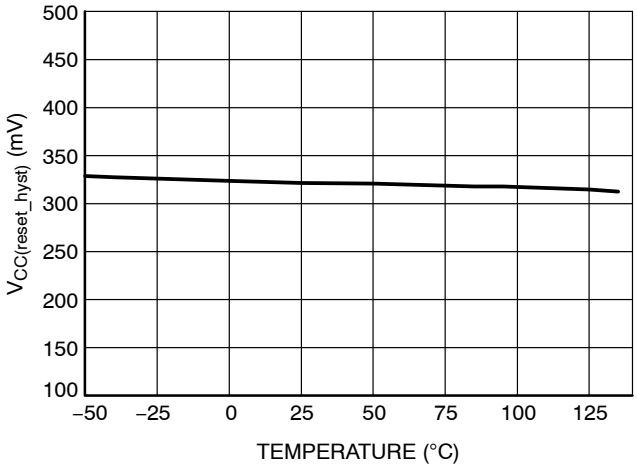



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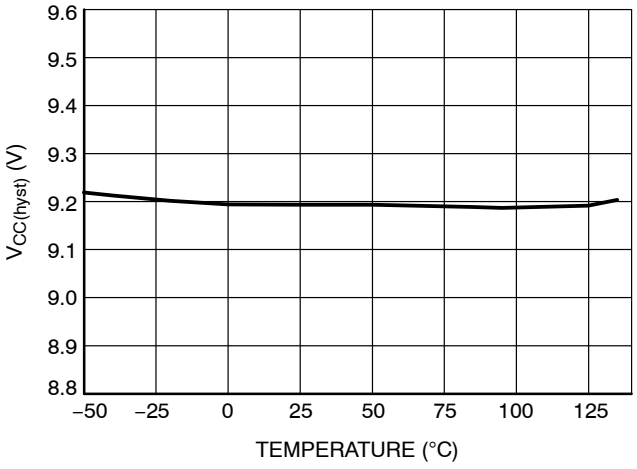



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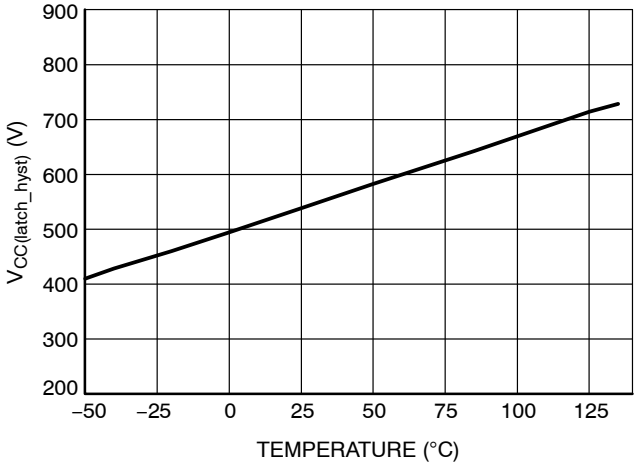



**Figure 9.**

## TYPICAL CHARACTERISTICS

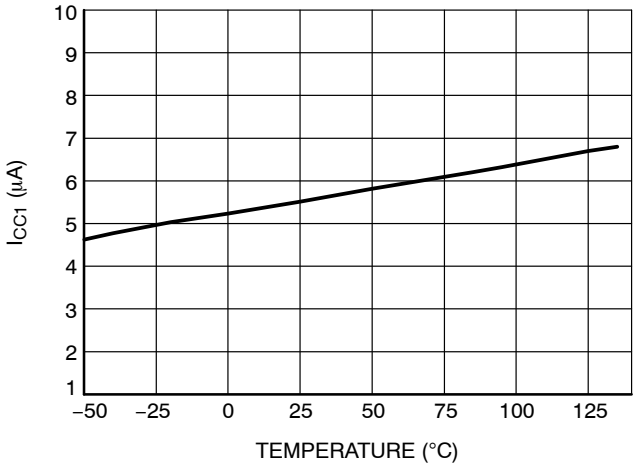



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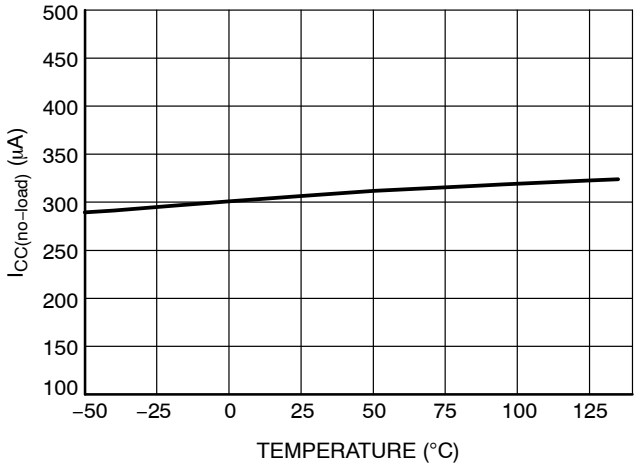



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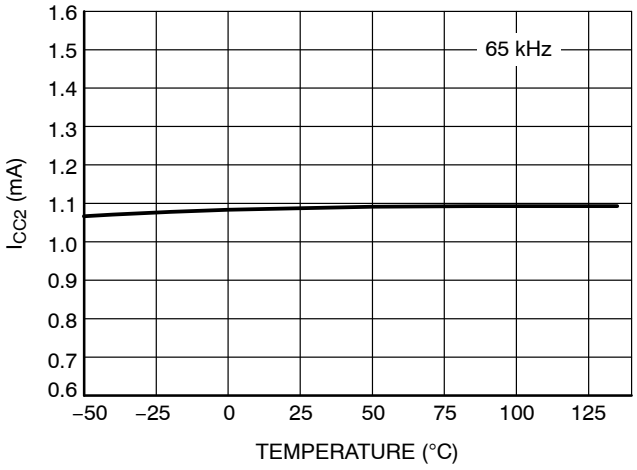



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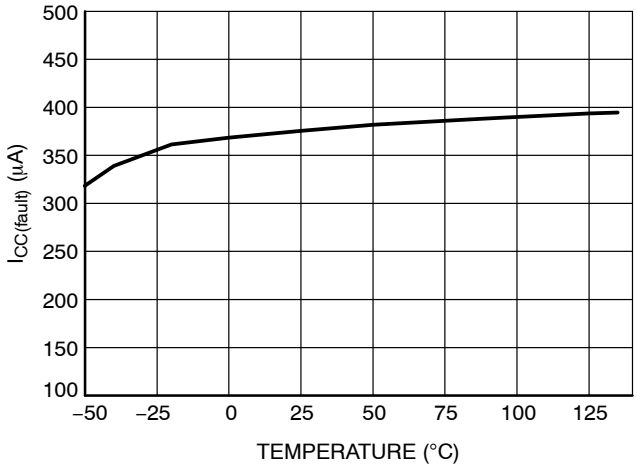



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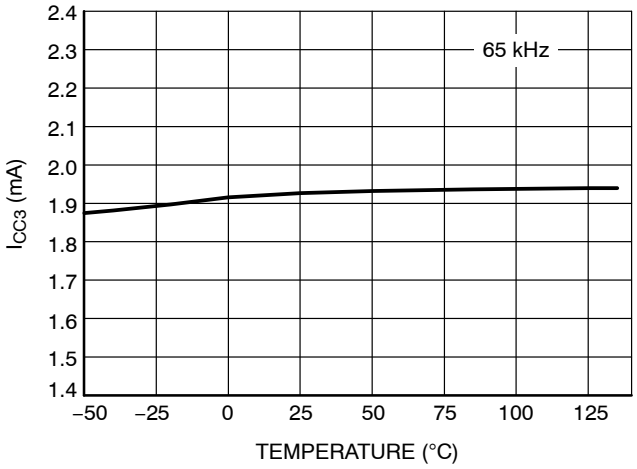



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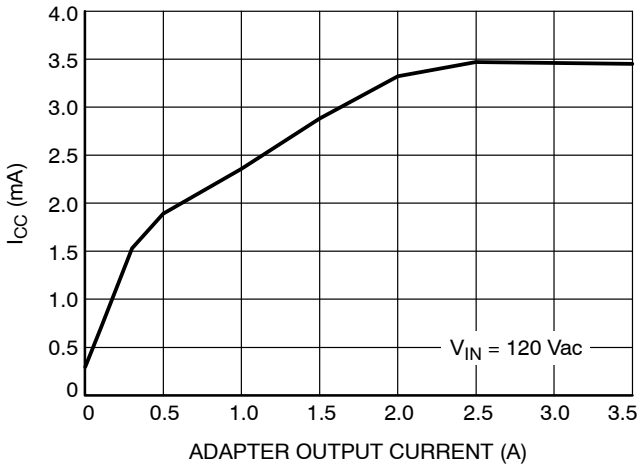



**Figure 15.**

## TYPICAL CHARACTERISTICS

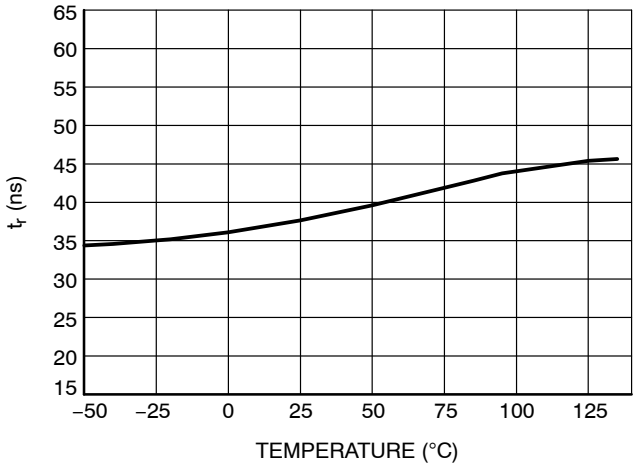



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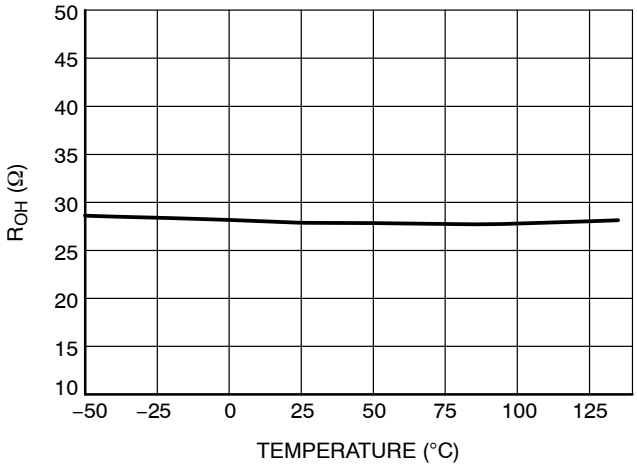



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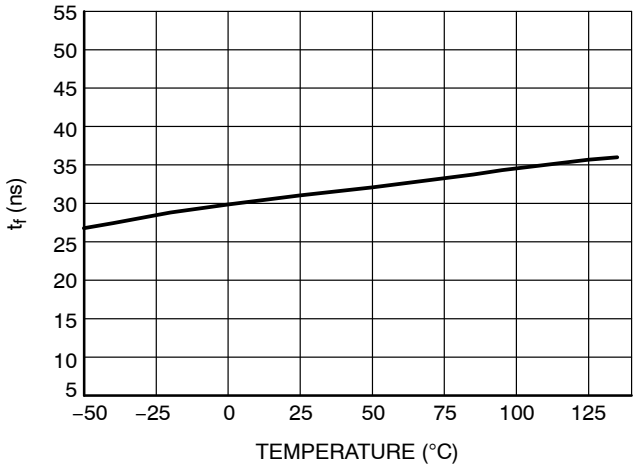



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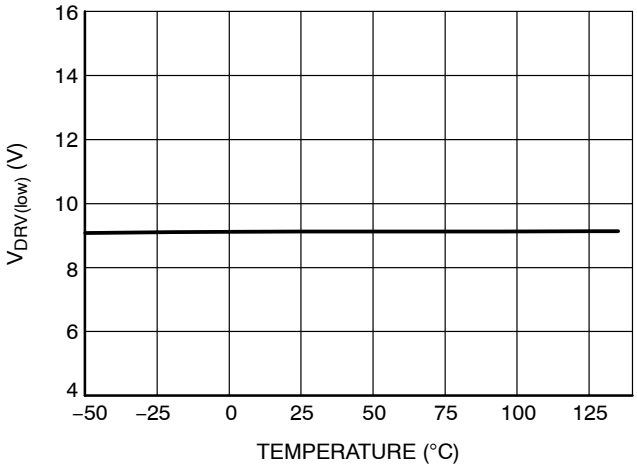



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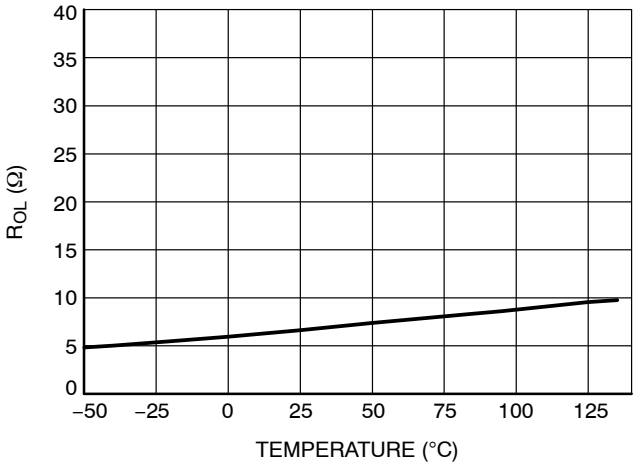



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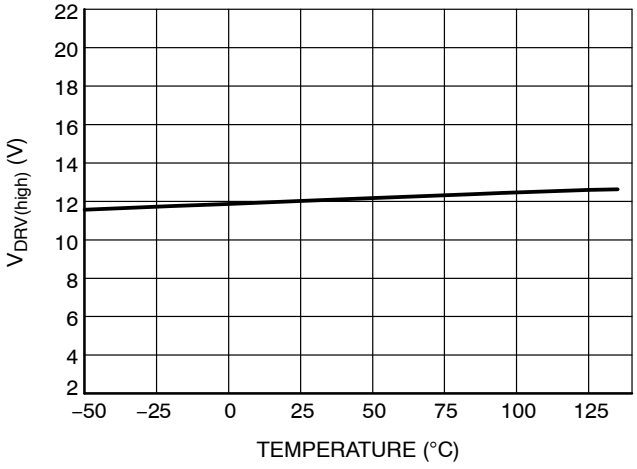



**Figure 21.**

## TYPICAL CHARACTERISTICS

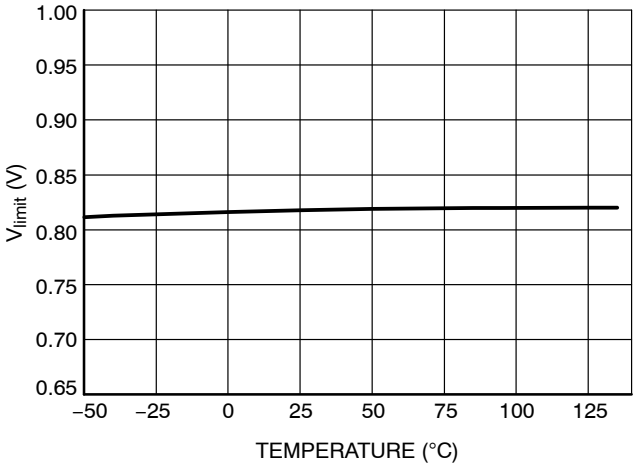



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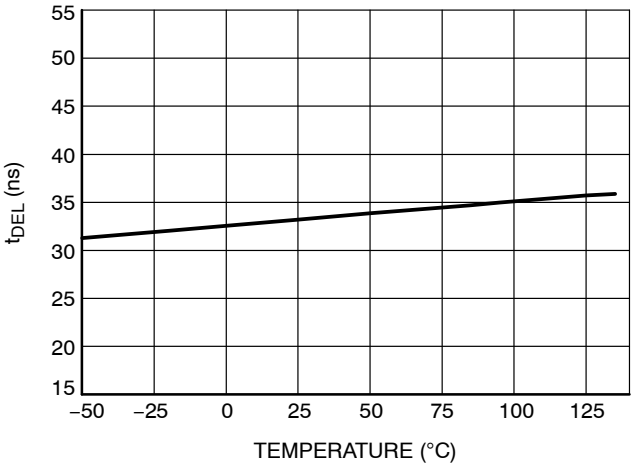



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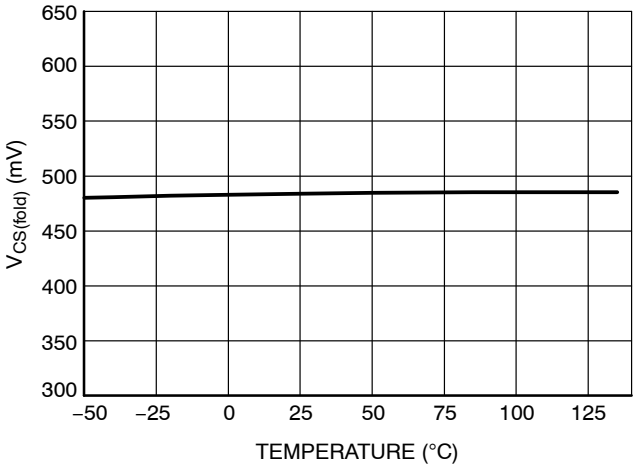



**Figure 24.**

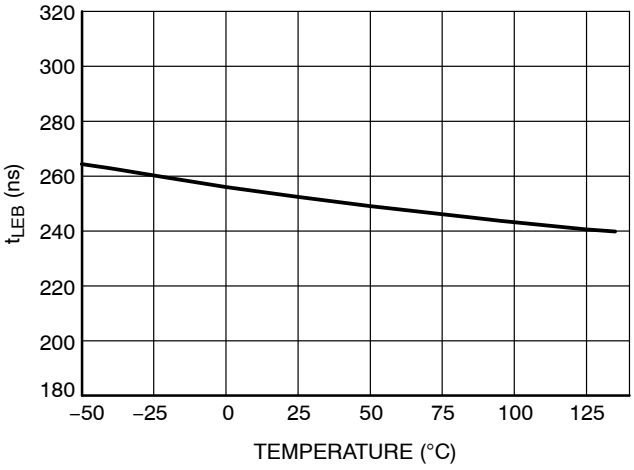



**Figure 25.**

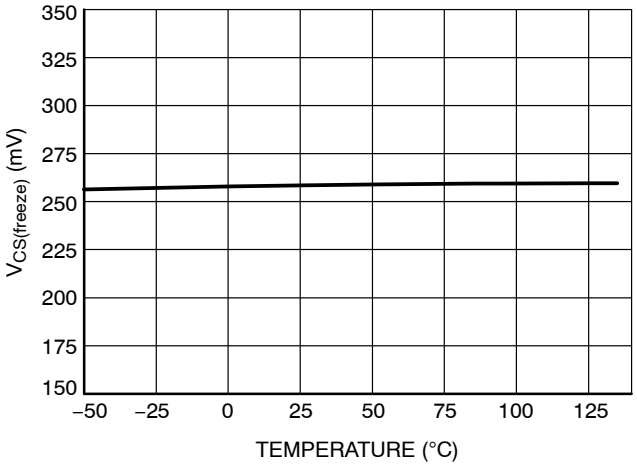



**Figure 26.**

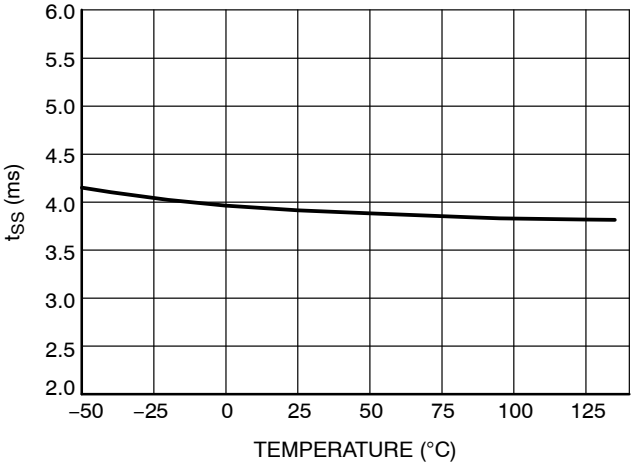



**Figure 27.**

## TYPICAL CHARACTERISTICS

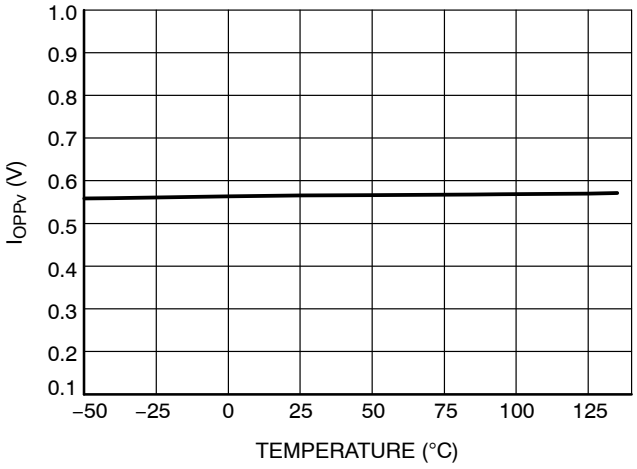



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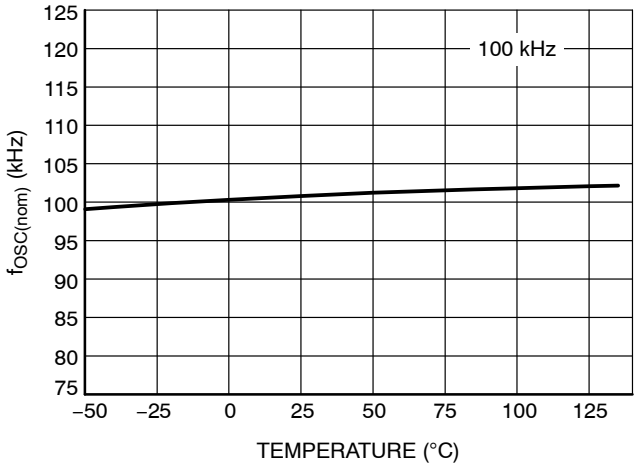



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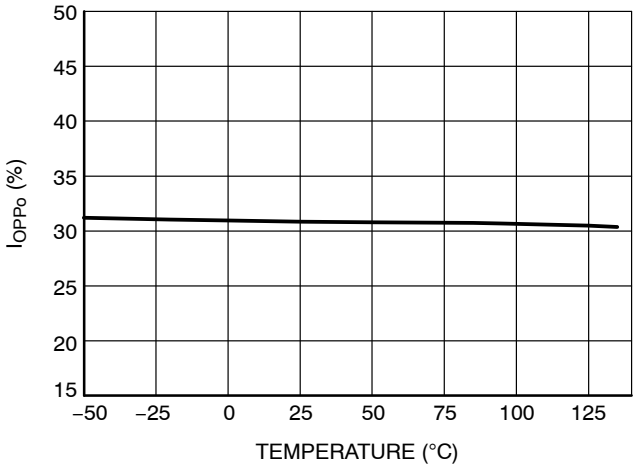



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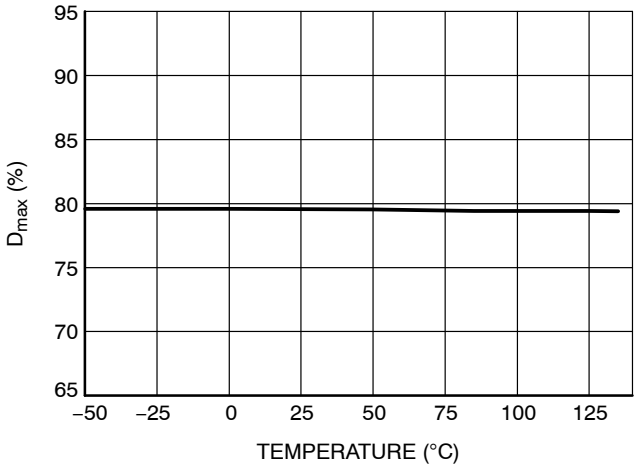



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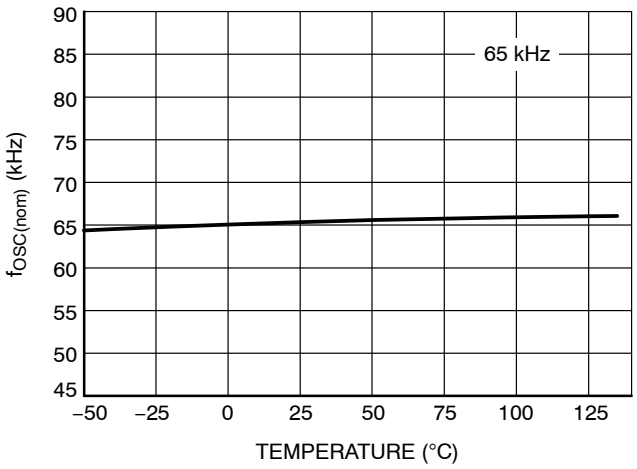



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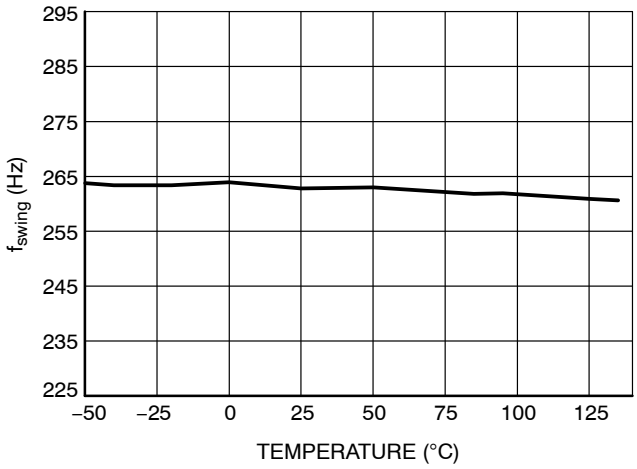



**Figure 33.**

## TYPICAL CHARACTERISTICS

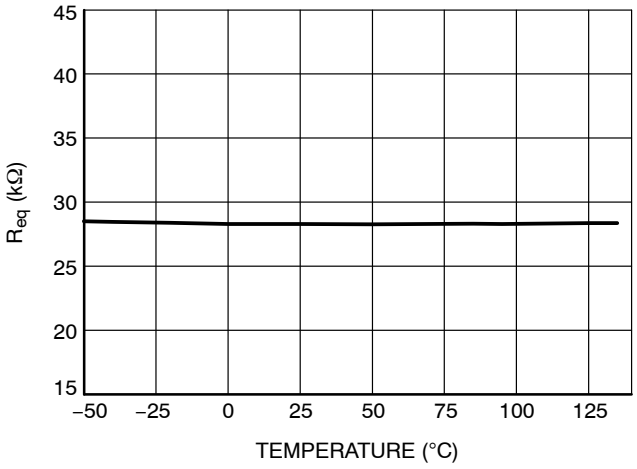



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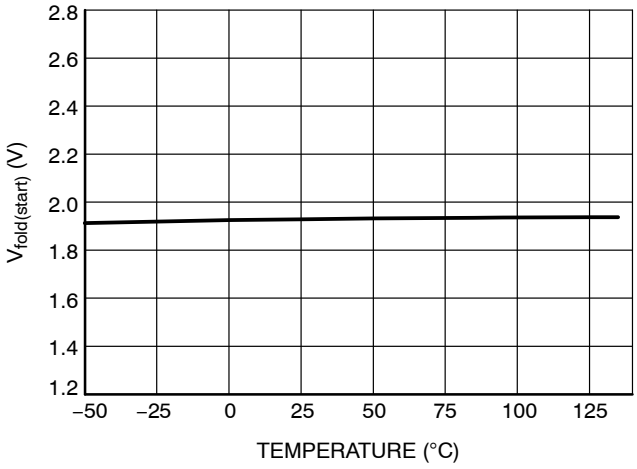



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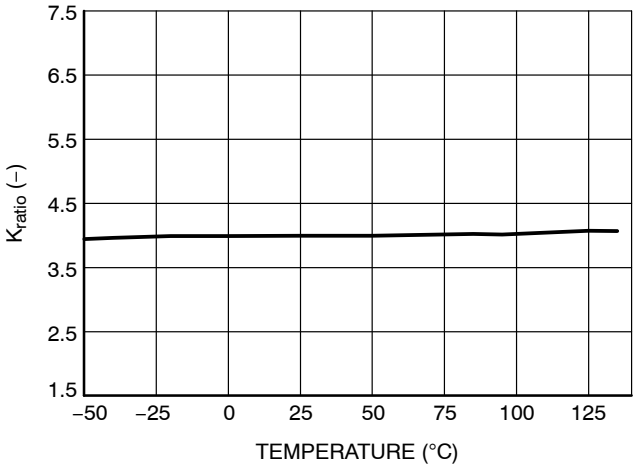



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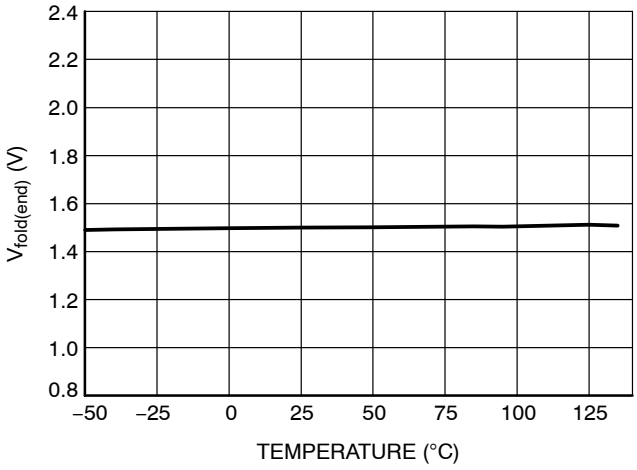



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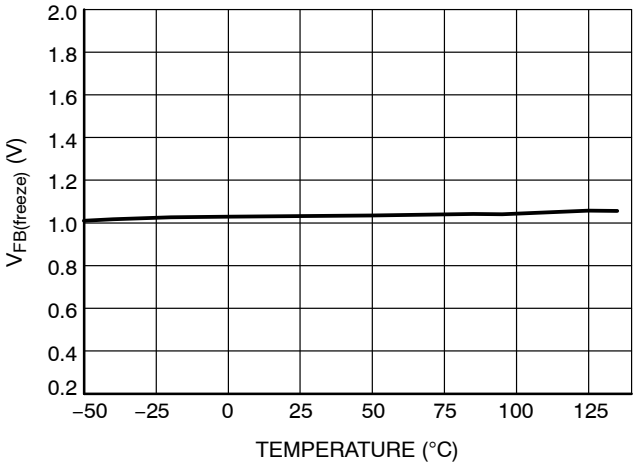



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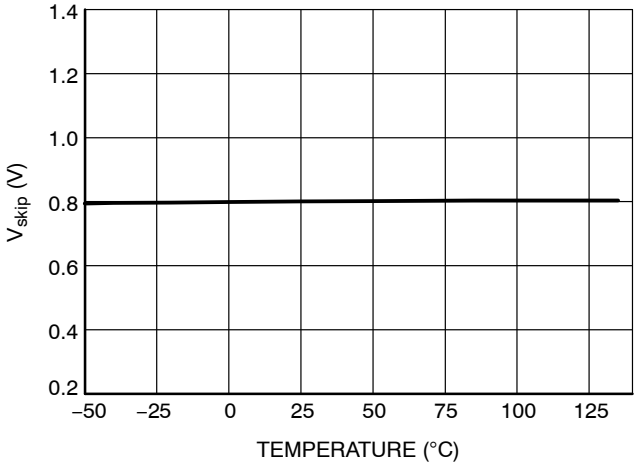



**Figure 39.**

## TYPICAL CHARACTERISTICS

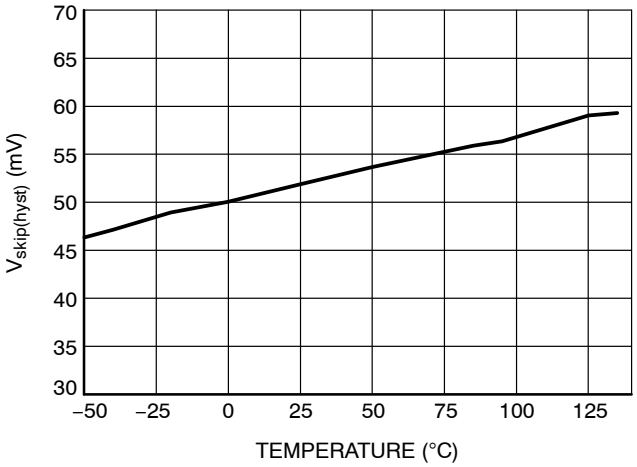



**Figure 40.**

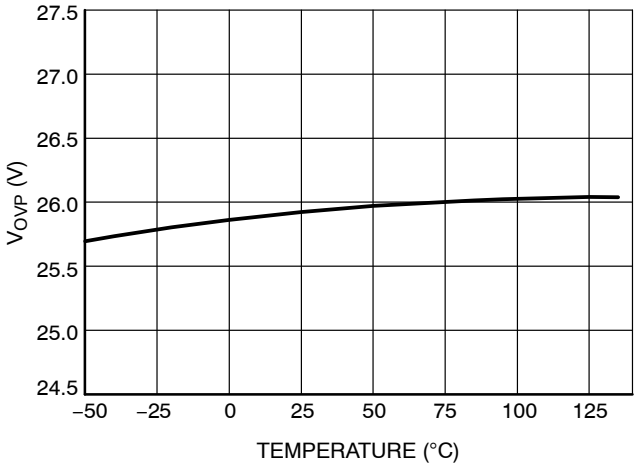



**Figure 41.**

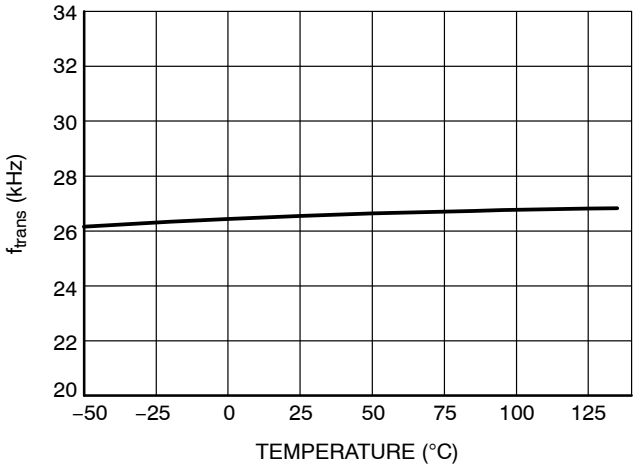



**Figure 42.**

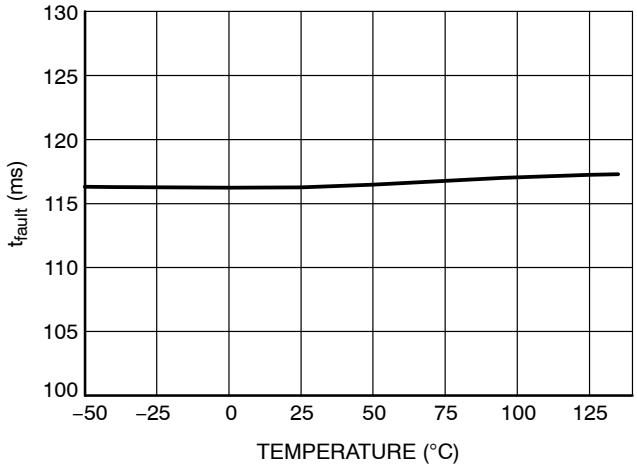



**Figure 43.**

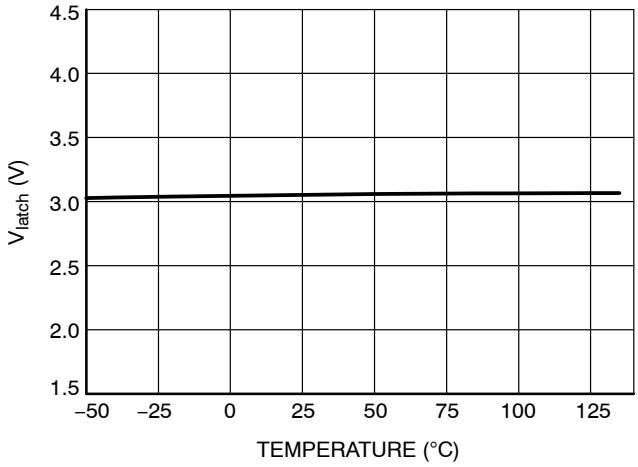



**Figure 44.**

## APPLICATION INFORMATION

### Introduction

NCP12510 implements a standard current mode architecture where the switch−off event is dictated by the peak current set point. This component represents the ideal candidate where low part−count and cost effectiveness are the key parameters, particularly in low−cost ac−dc adapters, open−frame power supplies etc. Updated controller, the NCP12510 packs all the necessary components normally needed in today modern power supply designs, bringing several enhancements such as a non−dissipative OPP, OVP/OTP implementation, short−circuit protection with pre−short ready for latched version and improved consumption, robustness and ESD capabilities.

- **Current−mode operation with internal slope compensation:** implementing peak current mode control at a 65 or 100 kHz switching frequency, the NCP12510 offers an internal slope compensation signal that can easily by summed up to the sensed current. Sub harmonic oscillations can thus be fought via the inclusion of a simple resistor in series with the current−sense information.
- **Internal OPP:** by routing a portion of the negative voltage present during the on−time on the auxiliary winding to the dedicated OPP pin (pin 3), the user has a simple and non−dissipative means to alter the maximum peak current set point as the bulk voltage increases. If the pin is grounded, no OPP compensation occurs. If the pin receives a negative voltage, then a peak current is reduced down.
- **Low startup and standby current:** reaching a low no−load standby power always represents a difficult exercise when the controller draws a significant amount of current during startup. The NCP12510 brings improved consumption to easing the design of low standby power adapters.
- **EMI jittering:** an internal low−frequency modulation signal varies the pace at which the oscillator frequency is modulated. This helps spreading out energy in conducted noise analysis. To improve the EMI signature at low power levels, the jittering is kept in frequency foldback mode (light load conditions).
- **Frequency foldback capability:** a continuous flow of pulses is not compatible with no−load/light−load standby power requirements. To excel in this domain, the controller observes the feedback pin and when it reaches a level of $V_{fold(start)}$, it starts reduce switching frequency. When the feedback level reaches $V_{fold(end)}$, the frequency hits its lower stop at $f_{trans}$. When the feedback pin goes further down and reaches $V_{FB(freeze)}$, the peak current setpoint is internally frozen. Below this point, if power continues to drop, the controller enters classical skip−cycle mode, as both frequency and peak current are frozen.
- **Internal soft−start:** a soft−start precludes the main power switch from being stressed upon start−up. The soft−start duration is internally fixed for time $t_{SS}$ and it is activated during new startup sequence or during recovering after auto−recovery double hiccup.
- **Latch input:** the controller includes a latch input (pin 3) that can be used to sense an over voltage or an over temperature event on the adapter. If this pin is brought higher than the internal reference voltage $V_{latch}$ for four consecutive cycles, then the circuit is latched off – $V_{CC}$ hiccups from $V_{CC(min)}$ voltage level with hysteresis $V_{CC(latch_hyst)}$ = 550 mV typically, until a reset occurs. The latch reset occurs when the user disconnects the adapter from the mains and lets the $V_{CC}$ falls below the $V_{CC(reset)}$ level. For the C version, despite an OVP/OTP detection, the circuit autorecovers and never latches.
- **Auto−recovery OVP on $V_{CC}$:** an OVP protects the circuit against $V_{CC}$ runaways. If the fault is present at least for time $t_{OVP(del)}$ then the OVP is validated and the controller enters double hiccup mode. When the $V_{CC}$ returns to a nominal level, the controller resumes operation.
- **Short−circuit protection:** short−circuit and especially overload protections are difficult to implement when a strong leakage inductance between auxiliary and power windings affects the transformer (the aux winding level does not properly collapse in presence of an output short). In this controller, every time the internal maximum peak current limit $V_{limit}$ is activated (or less when OPP is used), an error flag is asserted and a time period starts thanks to an internal timer. When the timer has elapsed while a fault is still present, the controller is latched or enters an auto−recovery mode, depending on the selected OCP option.
  Please note that with active Pre−short option (could be active only for latched OCP version), the part becomes sensitive to the first UVLO event during the start−up sequence (without Pre−short, first and any other UVLO is auto−recovery). Any other UVLO events are ignored afterwards – auto−recovery operation. With the first drive pulse is generated armed flag. Armed flag is reset after the first successful start−up sequence (the controller gets into regulation). This is to pass the pre−short test at power up:.
  1. if the internal armed flag is active and an UVLO event is sensed, the part is immediately latched.
  2. if an UVLO signal is detected but the armed flag is not asserted, double−hiccup auto−recovery occurs.
  3. if the controller gets into regulation, the armed flag is reset. Then UVLO event is sensed, the part is in auto−recovery operation.

### Start−up Sequence

The ***NCP12510*** start−up voltage is made purposely high to permit large energy storage in a small $V_{CC}$ capacitor value. This helps operate with a small start−up current which, together with a small $V_{CC}$ capacitor, will not hamper the start−up time. To further reduce the standby power, the start−up current of the controller is extremely low, below 10 μA. The start−up resistor can therefore be connected to the bulk capacitor or directly to the mains input voltage to further reduce the power dissipation.

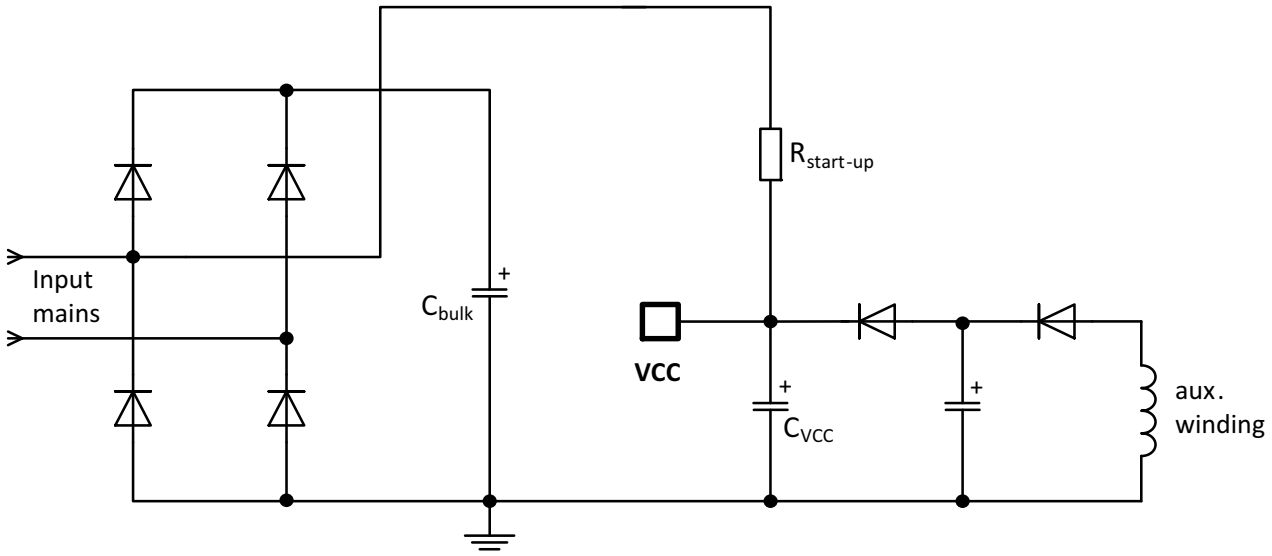



**Figure 45. The startup resistor can be connected to the input mains for further power dissipation reduction.**

The first step starts with the calculation of the needed VCC capacitor which will supply the controller which it operates until the auxiliary winding takes it over. Experience shows that this time $t_1$ can be between 5 and 20 ms. If we consider we need at least an energy reservoir for a $t_1$ time of 10 ms, the VCC capacitor must be larger than:

$$C_{VCC} \geq \frac{I_{CC} \cdot t_1}{V_{CC(on)} - V_{CC(min)}} \geq \frac{1.7\ m \cdot 10\ m}{18 - 8.9} \geq 1.9\ \mu F \quad \text{(eq. 1)}$$

Let us select a 2.2 μF capacitor at first and experiments in the laboratory will let us know if we were too optimistic for the time $t_1$. The VCC capacitor being known, we can now evaluate the charging current we need to bring the $V_{CC}$ voltage from 0 V to the $V_{CC(on)}$ of the IC. This current has to be selected to ensure a start−up at the lowest mains (85 $V_{rms}$) to be less than 3 s (2.5 s for design margin):

$$I_{charge} \geq \frac{V_{CC(on)} \cdot C_{VCC}}{t_{start-up}} \geq \frac{18 \cdot 2.2\ \mu}{2.5} \geq 16\ \mu A \quad \text{(eq. 2)}$$

If we account for the 10 μA (maximum) that will flow to the controller, then the total charging current delivered by the start−up resistor must be 26 μA. If we connect the start−up network to the mains (half−wave connection then), we know that the average current flowing into this start−up resistor will be the smallest when $V_{CC}$ reaches the $V_{CC(on)}$ of the controller:

$$I_{CVCC,min} = \frac{\frac{V_{ac,rms}\sqrt{2}}{\pi} - V_{CC(on)}}{R_{start-up}} \quad \text{(eq. 3)}$$

To make sure this current is always greater than 26 μA, then, the minimum value for $R_{start-up}$ can be extracted:

$$R_{start-up} \leq \frac{\frac{V_{ac,rms}\sqrt{2}}{\pi} - V_{CC(on)}}{I_{CVCC(min)}} \leq \frac{\frac{85\sqrt{2}}{\pi} - 18}{26\ \mu} \leq 779\ k\Omega \quad \text{(eq. 4)}$$

For auto−recovery version, the calculation of the minimum value of the startup resistor has to be done, especially when the fast startup is required. The current flowing into the VCC capacitor cannot be higher than $I_{CC(fault)}$ current, otherwise the auto−recovery function is lost. Therefore, the same calculation as for maximum value can be used, but the minimum resistor value should be determined at maximum input voltage.

This calculation is purely theoretical, considering a constant charging current. In reality, the take over time can be shorter (or longer!) and it can lead to a reduction of the VCC capacitor. Thus, a decrease in charging current and an increase of the start−up resistor can be experimentally tested, for the benefit of standby power. Laboratory experiments on the prototype are thus mandatory to fine tune the converter. If we chose the 750 kΩ resistor as suggested by Equation 4, the dissipated power at high line amounts to:

$$P_{R_{start-up,max}} \approx \frac{V_{ac,peak}^{\ 2}}{4 \cdot R_{start-up}} \approx \frac{\left(230 \cdot \sqrt{2}\right)^2}{4 \cdot 750\ k} \approx 35\ mW \quad \text{(eq. 5)}$$

Now that the first VCC capacitor has been selected, we must ensure that the self−supply does not disappear when in no−load conditions. In this mode, the skip−cycle can be so

deep that refreshing pulses are likely to be widely spaced, inducing a large ripple on the VCC capacitor. If this ripple is too large, chances exist to touch the $V_{CC(min)}$ and reset the controller into a new start−up sequence. A solution is to grow this capacitor but it will obviously be detrimental to the start−up time. The option offered in Figure 45 elegantly solves this potential issue by adding an extra capacitor on the auxiliary winding. However, this component is separated from the VCC pin via a simple diode. You therefore have the ability to grow this capacitor as you need to ensure the self−supply of the controller without affecting the start−up time and standby power.

### Internal Over Power Protection

There are several known ways to implement Over Power Protection (OPP), all suffering from particular problems. These problems range from the added consumption burden on the converter or the skip−cycle disturbance brought by the current−sense offset. A way to reduce the power capability at high line is to capitalize on the negative voltage swing present on the auxiliary diode anode. During the turn−on time, this point dips to $-N_2 V_{bulk}$, where $N_2$ being the turns ratio between the primary winding and the auxiliary winding. The negative plateau observed on Figure 46 will have amplitude depending on the input voltage. The idea implemented in this chip is to sum a portion of this negative swing with the internal voltage reference $V_{limit}$ = 0.8 V. For instance, if the voltage swings down to −150 mV during the on−time, then the internal peak current set point will be fixed to the value 0.8 V – 0.150 V = 650 mV. The adopted principle appears in Figure 47 and shows how the final peak current set point is constructed.

Let's assume we need to reduce the peak current from 2.5 A at low line, to 2 A at high line. This corresponds to a 20% reduction or a set point voltage of 640 mV. To reach this level, then the negative voltage developed on the OPP pin must reach:

$$V_{OPP} = 0.8 \cdot V_{limit} - V_{limit} = 0.64 - 0.8 = -160\ mV \quad \text{(eq. 6)}$$

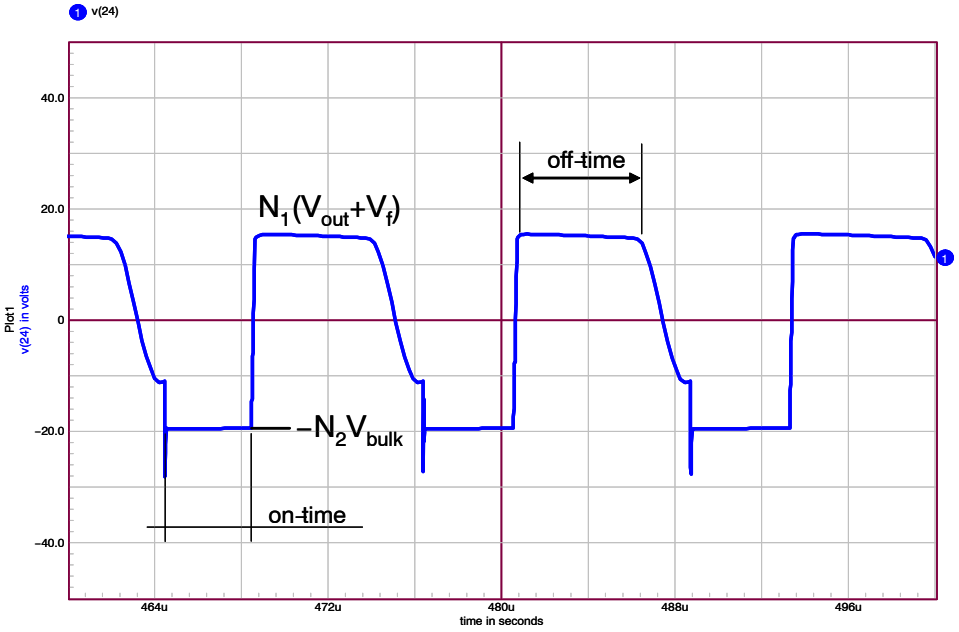



**Figure 46. The signal obtained on the auxiliary winding swings negative during the on−time.**

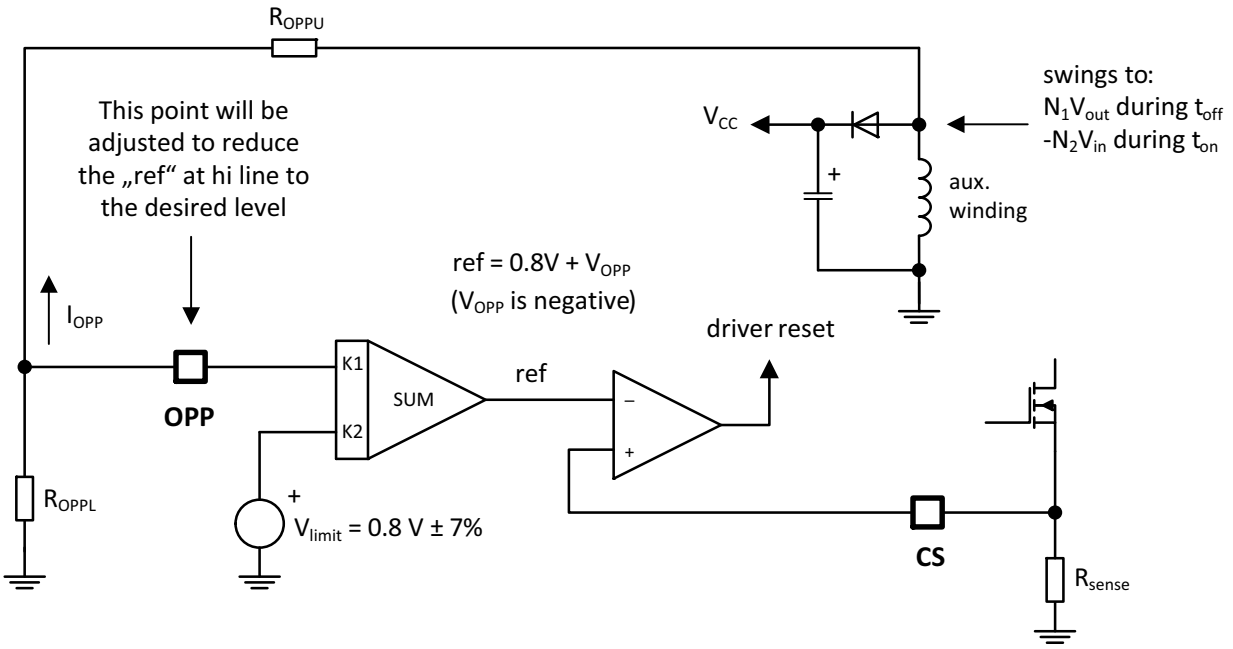



**Figure 47. The OPP circuitry affects the maximum peak current set point by summing a negative voltage to the internal voltage reference.**

Let us assume that we have the following converter characteristics:

$V_{out}$ = 19 V
$V_{in}$ = 85 to 265 $V_{rms}$
$N_1 = N_p:N_s$ = 1:0.25
$N_2 = N_p:N_{aux}$ = 1:0.18

Given the turns ratio between the primary and the auxiliary windings, the on−time voltage at high line (265 $V_{rms}$) on the auxiliary winding swings down to:

$$V_{aux} = -N_2 \cdot V_{in,max} = -0.18 \cdot 375 = -67.5\ V \quad \text{(eq. 7)}$$

To obtain a level as imposed by Equation 7, we need to install a divider featuring the following ratio:

$$Div = \frac{V_{OPP}}{V_{aux}} = \frac{-0.16}{-67.5} \approx 2.4\ m \quad \text{(eq. 8)}$$

If we arbitrarily fix the pull−down resistor $R_{OPPL}$ to 1 kΩ, then the upper resistor can be obtained by:

$$R_{OPPU} = \frac{V_{aux} - V_{OPP}}{\frac{V_{OPP}}{R_{OPPL}}} = \frac{-67.5 + 0.16}{\frac{-0.16}{1\ k}} \approx 422\ k\Omega \quad \text{(eq. 9)}$$

If we now plot the peak current set point obtained by implementing the recommended resistor values, we obtain the following curve, as shown in Figure 48.

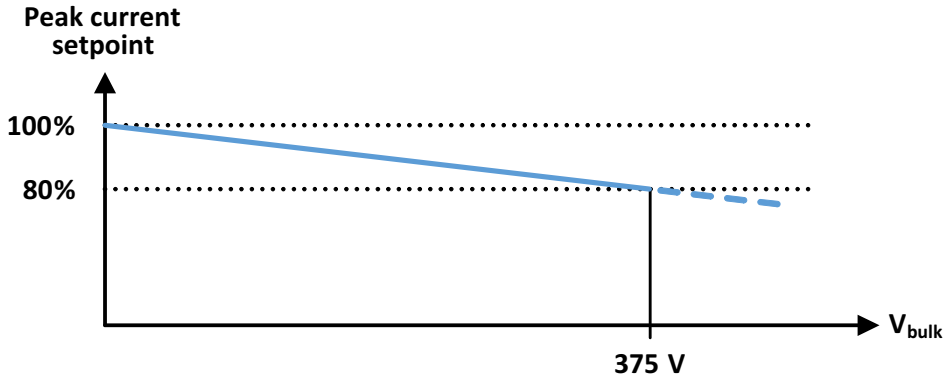



**Figure 48. The peak current regularly reduces down to 80% at 375 Vdc.**

The OPP pin is surrounded by Zener diodes stacked to protect the pin against ESD pulses. These diodes accept some peak current in the avalanche mode and are designed to sustain a certain amount of energy. On the other side, negative injection into these diodes (or forward bias) can cause substrate injection which can lead to an erratic circuit behavior. To avoid this problem, the pin is internal clamped slightly below –300 mV which means that if more current is injected before reaching the ESD forward drop, then the maximum peak reduction is kept to 40%. If the voltage finally forward biases the internal zener diode, then care must be taken to avoid injecting a current beyond –2 mA. Given the value of $R_{OPPU}$, there is no risk in the present example.

Finally, please note that another comparator internally fixes the maximum peak current set point to value $V_{limit}$ even if the OPP pin is adversely biased above 0 V.

### Frequency Foldback

The reduction of no−load standby power associated with the need for improving the efficiency, requires a change in the traditional fixed−frequency type of operation. This controller implements a switching frequency foldback when the feedback voltage passes below a certain level, $V_{fold(start)}$. At this point, the oscillator turns into a Voltage−Controlled Oscillator (VCO) and reduces switching frequency down to $f_{trans}$ value, till to feedback voltage reaches the level $V_{fold(end)}$. Below this level $V_{fold(end)}$, the frequency is fixed and cannot go further down. The peak current setpoint is following the feedback pin until its level reaches $V_{FB(freeze)}$. Below this value, the peak current setpoint is frozen to $V_{CS(freeze)}$ value or ≈31% of the maximum $V_{limit}$ setpoint. The only way to further reduce the transmitted power is to enter skip cycle, which is set when the feedback voltage reaches the level $V_{skip}$. Skip cycle offers the best noise−free performance in no−load conditions. Figure 49 and depicts the adopted scheme for the part.

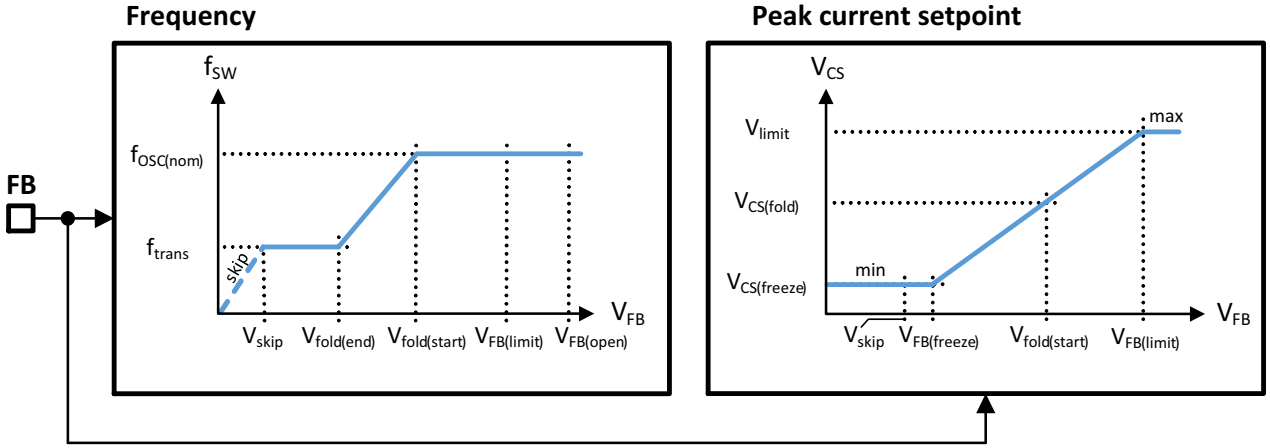



**Figure 49. By observing the voltage on the feedback pin, the controller reduces its switching frequency for an improved performance at light load.**

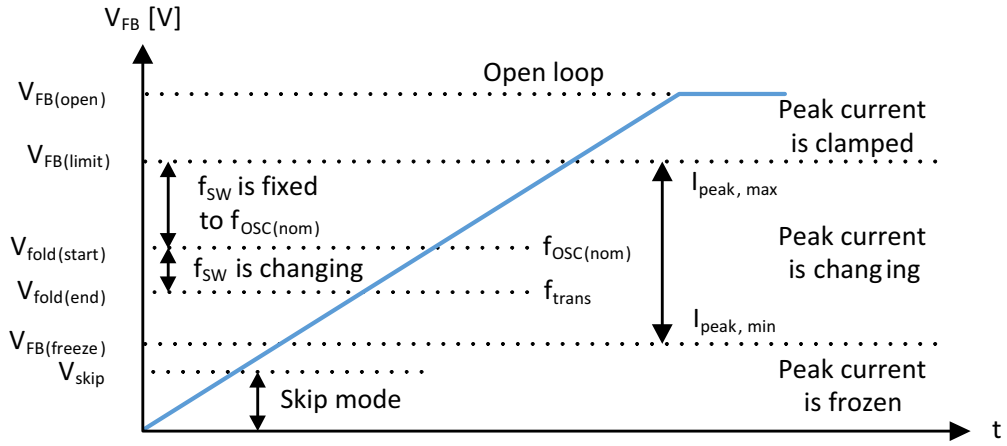



**Figure 50. Another look at the relationship between feedback and current setpoint while in frequency reduction mode.**

### Designing the primary FB loop

The primary Feedback loop is the loop from FB pin to optocoupler and back to ground pin of the IC with parallel decoupling feedback capacitor $C_{FB}$ as it shown in Figure 51. For best performance of the IC, the area of the FB loop has to be as smaller as possible and the ground has to be quiet. It means that ground between optocoupler and the IC should be standalone wire and not common wire with the other grounds, like power ground, auxiliary ground, etc.

The FB capacitor must be placed close to the FB pin and it is recommended to use 1 nF capacitor as minimum, because the capacitor eliminates the ringing on the FB voltage. Mainly the ringing during off−time should be kept below 40 mV.

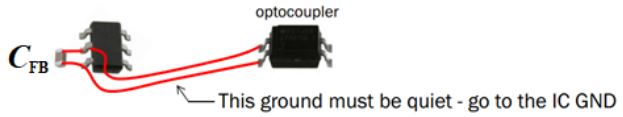



**Figure 51. The primary FB loop**

### Auto−Recovery Short−Circuit Protection

In case of output short−circuit or if the power supply experiences a severe overloading situation, an internal error flag is raised and the fault timer starts countdown. If the UVLO has come (see Figure 52 – Short−circuit case I.) or the error flag is asserted throughout the $t_{fault}$ time (see Figure 52 – Short−circuit case II.) – i.e. the fault timer has elapsed, the driving pulses are stopped and the $V_{CC}$ falls down as the auxiliary voltage are missing. When the supply voltage $V_{CC}$ touches the $V_{CC(min)}$ level, the controller consumption is down to a few μA and the $V_{CC}$ slowly builds up again thanks to the resistive startup network. When $V_{CC}$ reaches $V_{CC(on)}$, the controller purposely ignores the re−start and waits for another $V_{CC}$ cycle: this is the so−called double hiccup auto−recovery mode. Illustration of such principle appears in Figure 52. Please note that soft−start is activated upon every re−start attempt.

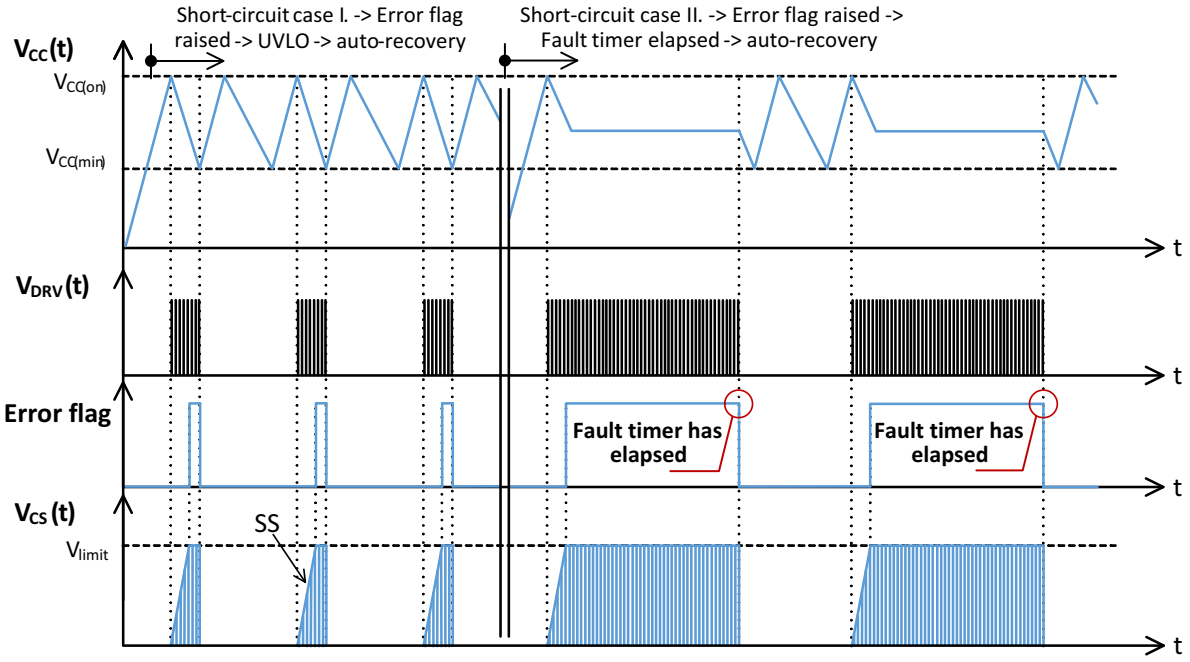



**Figure 52. An auto−recovery double hiccup mode is entered in case a faulty event longer than programmable fault timer value is acknowledged by the controller.**

### Latched Short−Circuit Protection with Pre−Short

In some applications, the controller must be fully latched in case of an output short circuit presence. In that case, you would select a controller with an OCP latched option in the Options table. When the error flag is asserted, meaning the controller is asked to deliver its full peak current, the controller latches off after the elapse of fault timer – i.e. the pulses are immediately stopped and $V_{CC}$ hiccups between two voltage levels, given by a $V_{CC(min)}$ level and added hysteresis $V_{CC(latch_hyst)}$, until a reset occurs ($V_{CC}$ falls down below $V_{CC(reset)}$). However, in presence of damaged or old VCC capacitor, it can very well be the case where the stored energy does not give enough time to let the timer elapse before $V_{CC}$ touches the UVLO level. When this happens, the latch is not acknowledged since the timer countdown has been prematurely aborted. To avoid this situation, the NCP12510 is equipped with Pre−short logic for OCP latched option, i.e. the Pre−short cannot be used for auto−recovery OCP option. The Pre−short logic combines the armed flag assertion together with the UVLO event to confirm a pre−short situation: upon start−up with first drive pulse, the armed flag is raised until regulation is met. If during the time the flag is raised an UVLO event is detected, the part latches off immediately. When IC is latched, $V_{CC}$ enters hiccup mode. In normal operation, if an UVLO event is detected for any reason, the controller will naturally resume operations. Details of this behavior are given in Figure 53.

Pre−short logic is active during the start−up sequence, i.e. the first startup of power supply or after recovering from double hiccup mode. The armed flag is asserted with the first drive pulse. If an UVLO event occurs when the armed flag is asserted, the part immediately latches off. If no UVLO occurs, once the output voltage has reached regulation in 8 consecutive cycles, the internal armed flag is reset (pre−short logic is no active anymore until new startup of power supply) and any new UVLO events will auto−recovery. Pre−short logic is available only on customer request. It is not active in standard devices.

Standard OCP latched option without Pre−short logic doesn't latch the controller during first UVLO, i.e. armed flag is not active so every UVLO event is auto−recovery.

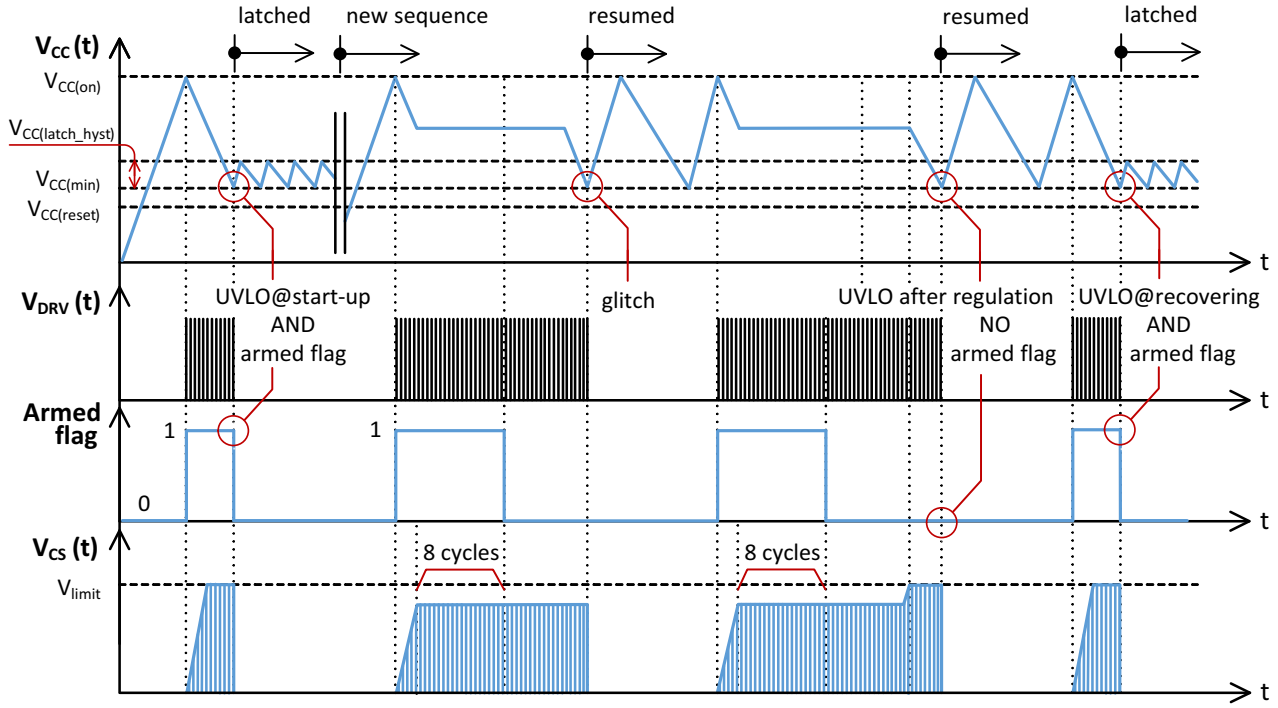



**Figure 53. Full latch occurs in case the UVLO@start−up or @recovering is detected while the armed flag is asserted**

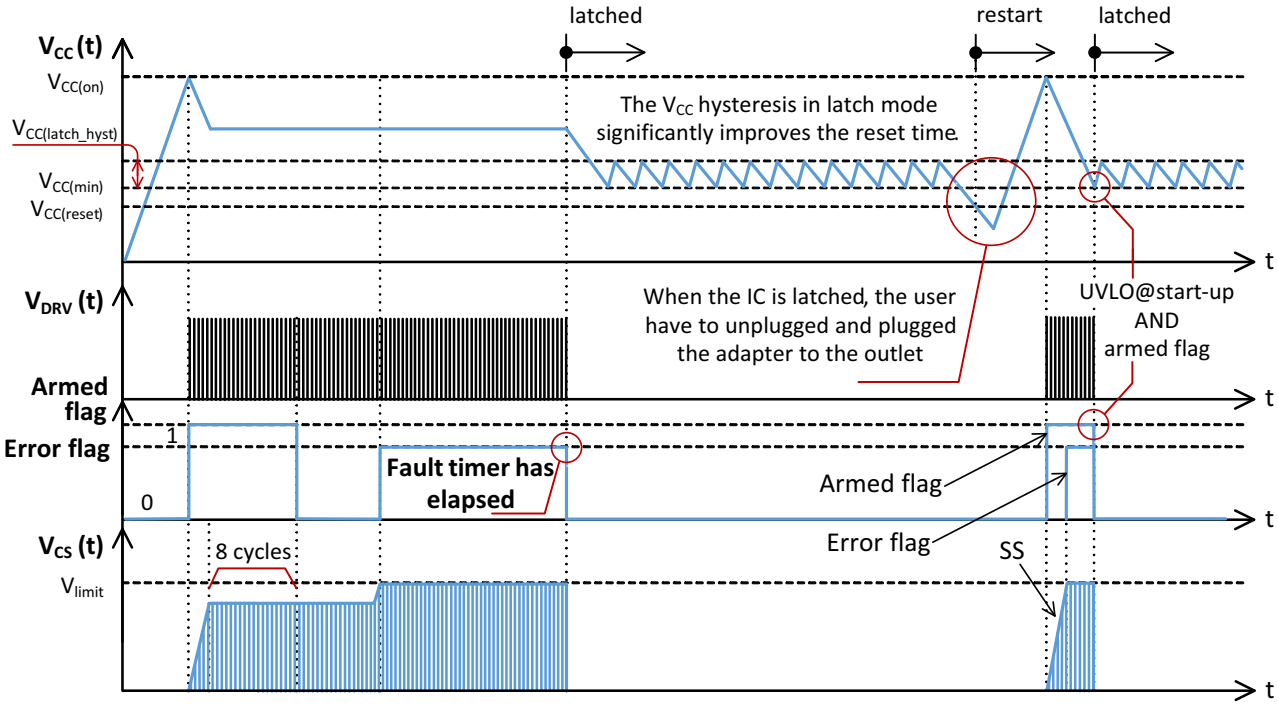



**Figure 54. Full latch occurs in case the fault timer has elapsed or UVLO@start−up is detected with asserted armed flag.**

### Operation with Grounded Feedback Pin

The NCP12510 offers the operation mode when the NCP12510 could be controlled by Master system via Feedback pin (pin 2). When FB pin is grounded, the controller driver pulses are stopped. This is the same situation, when the controller is in skip mode, but with the difference that FB pin could be forced to ground by Master system anytime during operation, even at start−up sequence.

When the $V_{CC}$ touches $V_{CC(on)}$ level, the controller internal logic starts and thus, first DRV pulse is authorized after the safety period of 200 μs passes. But the last DRV pulse can comes just before $V_{CC(min)}$ level. Therefore, there are extended rules to generation and cancellation the armed flag to avoid the false pre−short condition if the controller can't start properly because of the grounded FB pin.

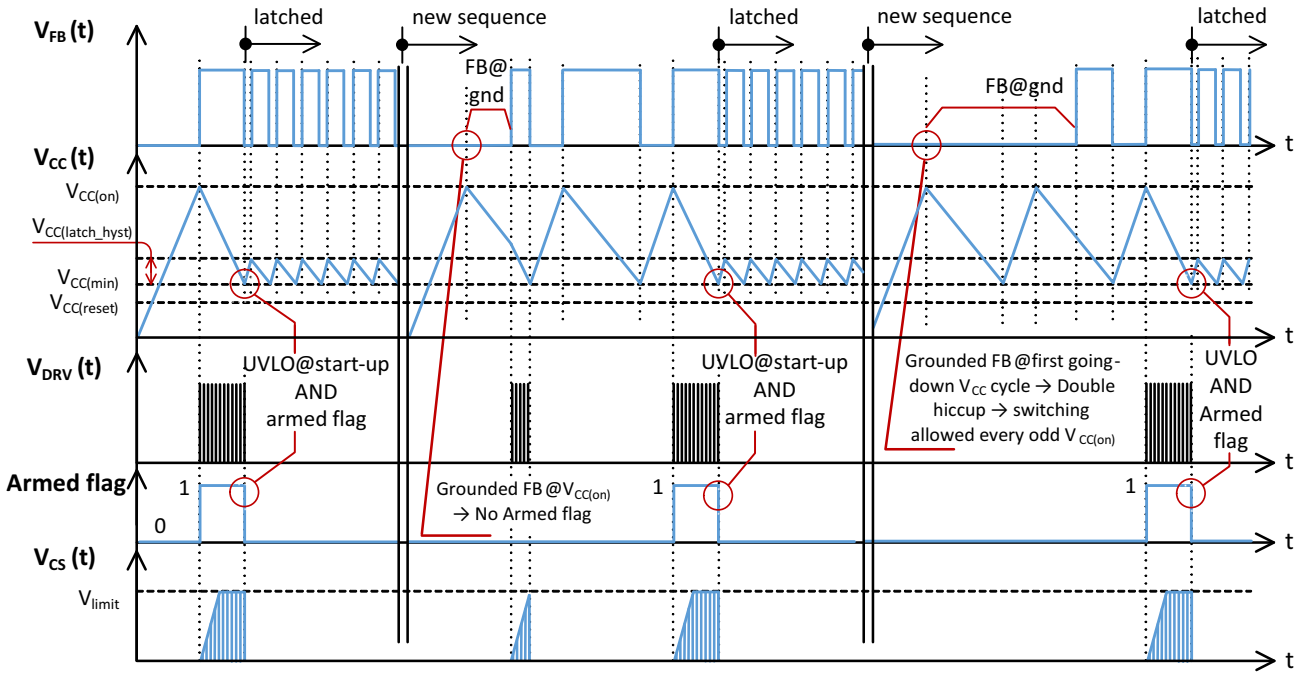



**Figure 55. The controller start−up sequence with grounded FB pin and Pre−short condition.**

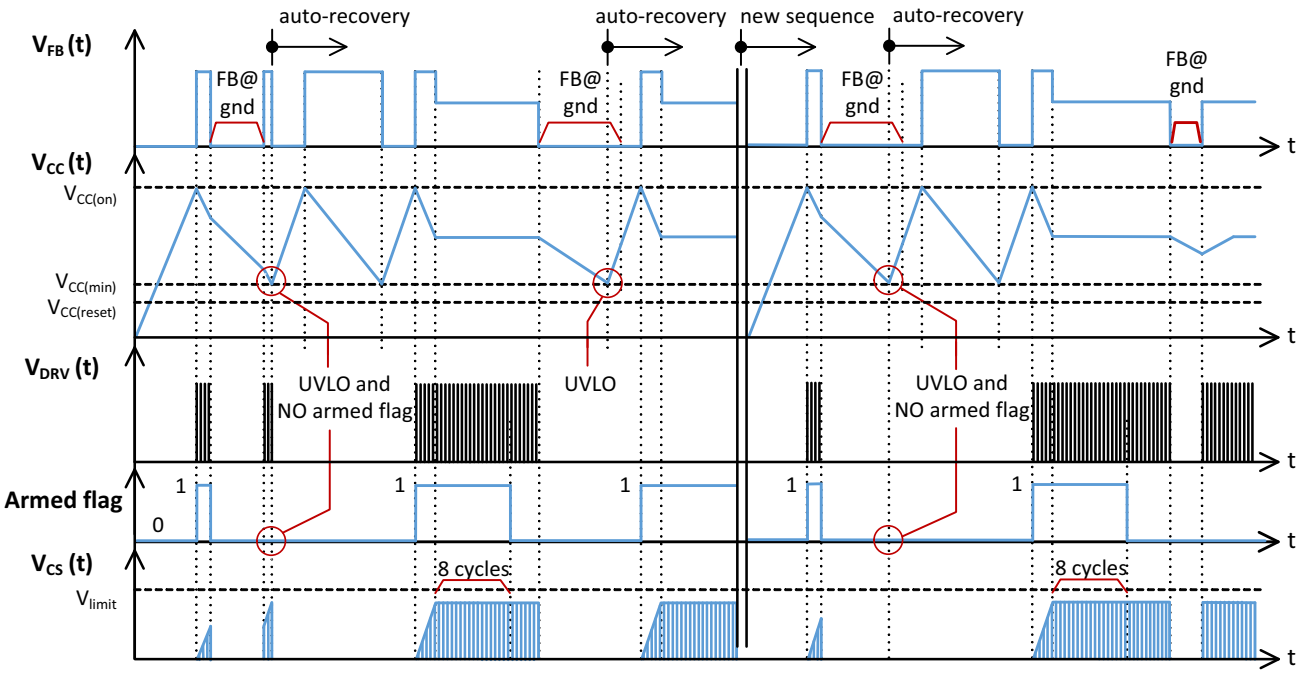



**Figure 56. The controller behaviour during start−up sequence interupted by grounded FB pin.**

The armed flag is generated with first DRV pulse, but only if the first DRV pulse is synchronized with $V_{CC(on)}$ event. If the FB pin is forced to ground during the $V_{CC(on)}$ event and it is released afterwards, the armed flag is not generated. The Figure 55 shows the cases of grounded FB pin at the beginning of start−up sequence.

If the armed flag isn't active and UVLO comes, the controller newly starts after double−hiccup auto−recovery sequence. Then, if UVLO comes again, the controller is latched off. DRV pulses are authorized during the whole first $V_{CC}$ going−down cycle. If any DRV pulse doesn't come during this time, the double−hiccup auto−recovery sequence is coming.

The armed flag could be canceled by two conditions. When the controller gets into regulation after start−up sequence, i.e. during the eight consecutive switching cycles is current setpoint voltage under $V_{limit}$, the armed flag is called off – this is the first armed flag cancelation condition. When the start−up sequence isn't complete and is interrupted by grounded FB pin, the armed flag is called off – this is the second armed flag cancelation condition. The Figure 56 shows the cases of interrupted start−up sequence by grounded FB pin.

If the start−up sequence is interrupted by grounded FB pin, the armed flag is canceled. Then, if UVLO comes, the controller newly starts after double−hiccup auto−recovery sequence. Then, if UVLO comes again, the controller is latched off.

The Figure 57 shows the case of operation, when the controller can operate under some master system with superordinate function. Then, the FB pin is used for authorization or denial DRV pulses. If the normal operation state is interrupted for a long time and afterwards the soft−start is demanded for proper start−up of power supply, the $V_{CC}$ have to be pulled−down below $V_{CC(reset)}$ level. Then, if the FB isn't grounded, the new start−up sequence are initialized when $V_{CC}$ touches $V_{CC(on)}$ level + 200 μs safety period. During this new start−up sequence is generated the armed flag.

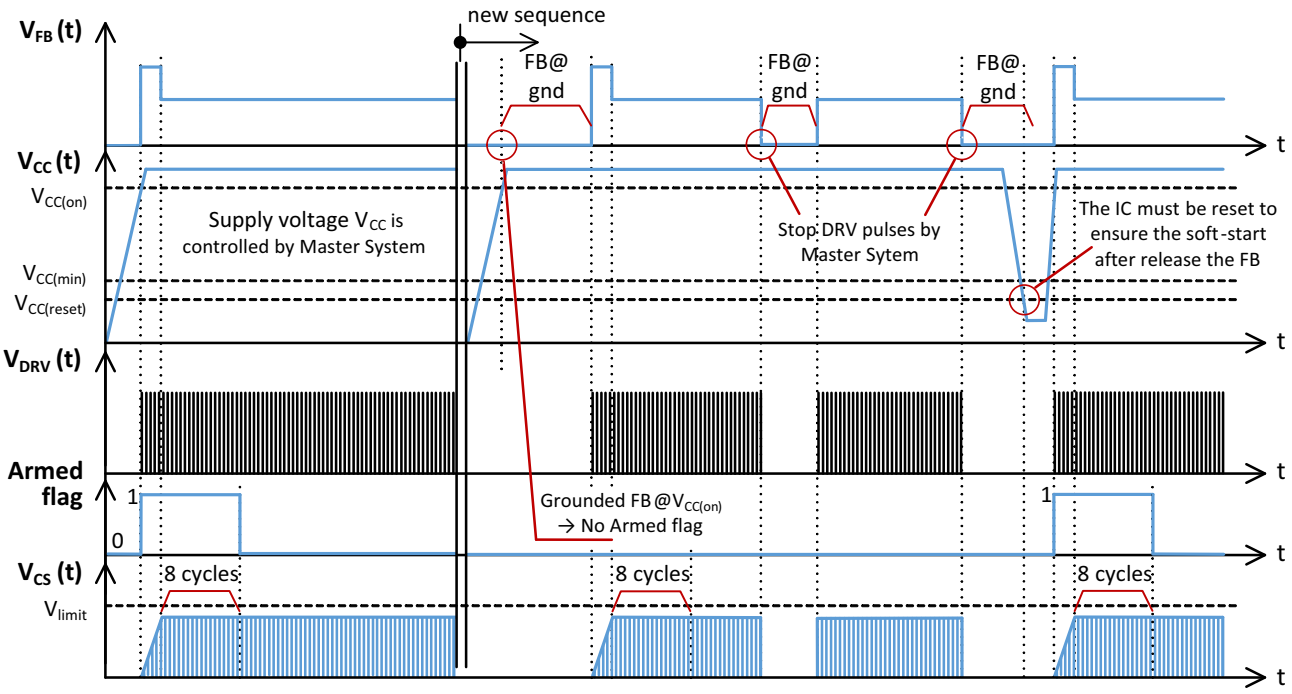



**Figure 57. The Master system driving the controller by forcing the FB pin to ground.**

### Slope Compensation

The NCP12510 includes an internal slope compensation signal. This is the buffered oscillator clock delivered during the on−time only. Its amplitude is around 2.5 V at the maximum duty ratio. Slope compensation is a known means used to cure sub harmonic oscillations in CCM−operated current−mode converters. These oscillations take place at half the switching frequency and occur only during Continuous Conduction Mode (CCM) with a duty ratio greater than 50%. To lower the current loop gain, one usually injects between 50 and 100% of the primary inductance downslope. Figure 58 depicts how the ramp is generated internally. Please note that the ramp signal will be disconnected from the CS pin during the off−time.

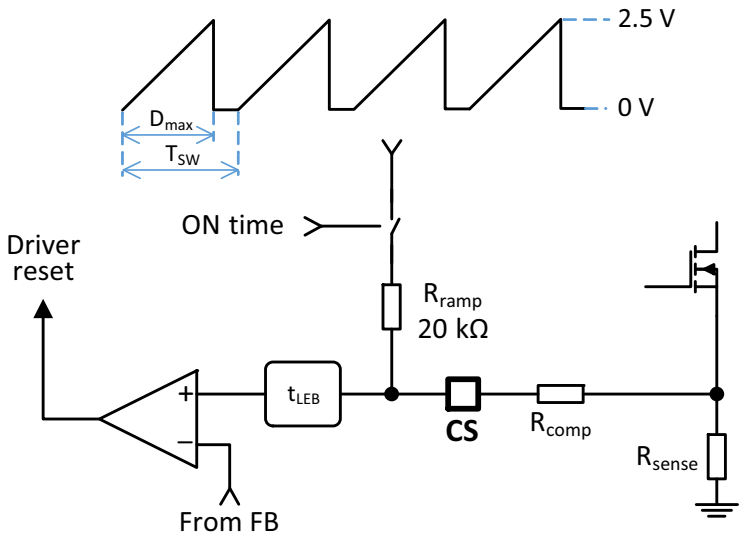



**Figure 58. Inserting a resistor in series with the current sense information brings slope compensation and stabilizes the converter in CCM operation.**

In the NCP12510 controller, the oscillator ramp features a 2.5 V swing. If the clock operates at a 65 kHz frequency, then the available oscillator slope corresponds to:

$$S_{ramp} = \frac{V_{ramp,peak}}{D_{max} \cdot T_{SW}} = \frac{2.5}{0.8 \cdot 15\ \mu} = 208\ mV/\mu s \quad \text{(eq. 10)}$$

In our flyback design, let's assume that our primary inductance $L_p$ is 770 µH, and the SMPS delivers 19 V with a $N_p$:$N_s$ ratio of 1:0.25. The off−time primary current slope $S_p$ is thus given by:

$$S_p = \frac{\left(V_{out} + V_f\right) \cdot \frac{N_s}{N_p}}{L_p} = \frac{(19 + 0.7) \cdot 4}{770\ \mu} = 102\ mA/\mu s \quad \text{(eq. 11)}$$

Given a sense resistor of 330 mΩ, the above current ramp turns into a voltage ramp of the following amplitude:

$$S_{sense} = S_p \cdot R_{sense} = 102\ m \cdot 0.33 = 34\ mV/\mu s \quad \text{(eq. 12)}$$

If we select 50% of the downslope as the required amount of slope compensation, then we shall inject a ramp whose slope is 17 mV/µs. Our internal compensation being of 208 mV/µs, the divider ratio (*divratio*) between $R_{comp}$ and the internal $R_{ramp}$ = 20 kΩ resistor is:

$$divratio = \frac{0.5 \cdot S_{sense}}{S_{ramp}} = 0.082 \quad \text{(eq. 13)}$$

The series compensation resistor value is thus:

$$R_{comp} = R_{ramp} \cdot divratio = 20\ k \cdot 0.082 = 1.64\ k\Omega \quad \text{(eq. 14)}$$

A resistor of the calculated value will then be inserted from the sense resistor to the current sense pin. We recommend adding a small capacitor of 100 pF, from the current sense pin to the controller ground for an improved immunity to the noise. Please make sure both components are located very close to the controller.

### Latching Off the Controller

The OPP pin not only allows a reduction of the peak current set point in relationship to the line voltage, it also offers a means to permanently latch−off the part. When the part is latched−off, all pulses are immediately stopped and $V_{CC}$ hiccups from $V_{CC(min)}$ voltage level with hysteresis $V_{CC(latch_hyst)}$ until a reset occurs ($V_{CC}$ falls down below level $V_{CCreset}$), e.g. by un−plugging the converter from the mains outlet. The $V_{CC}$ latch hysteresis helps significantly reduce the reset time, because when the user unplugged the adapter from the outlet in the less favorable time ($V_{CC}$ is in its maximum), the $V_{CC}$ has to fall down from voltage level given by 550 mV + 300 mV typically to reset level.

The latch detection is made by observing the OPP pin by a comparator featuring a $V_{latch}$ reference voltage. However, for noise reasons and in particular to avoid the leakage inductance contribution at turn off, a blanking delay $t_{latch-blank}$ is introduced before the output of the OVP comparator is checked. Then, the OVP comparator output is validated only if its high−state duration lasts for a minimum time $t_{latch-del}$. Below this value, the event is ignored. Then, a counter ensures that only 4 successive OVP events have occurred before actually latching the part. There are several possible implementations, depending on the needed precision and the parameters you want to control.

The first and easiest solution is the additional resistive divider on top of the OPP one. This solution is simple and inexpensive but requires the insertion of a diode to prevent disturbing the OPP divider during the on−time.

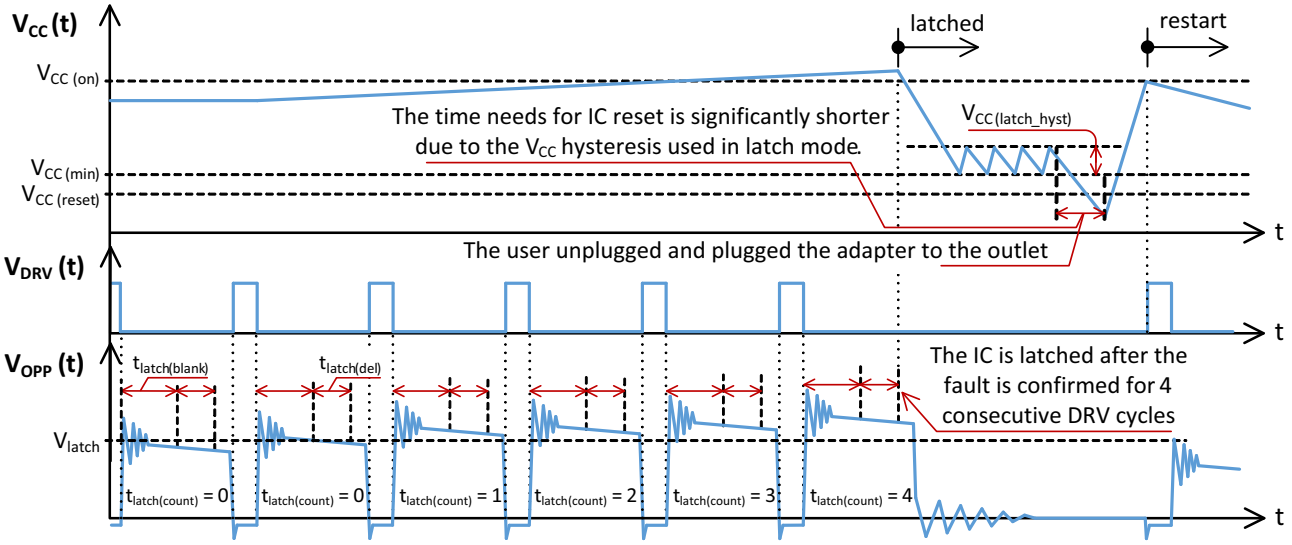



**Figure 59. Latching off the controller and resuming operation.**

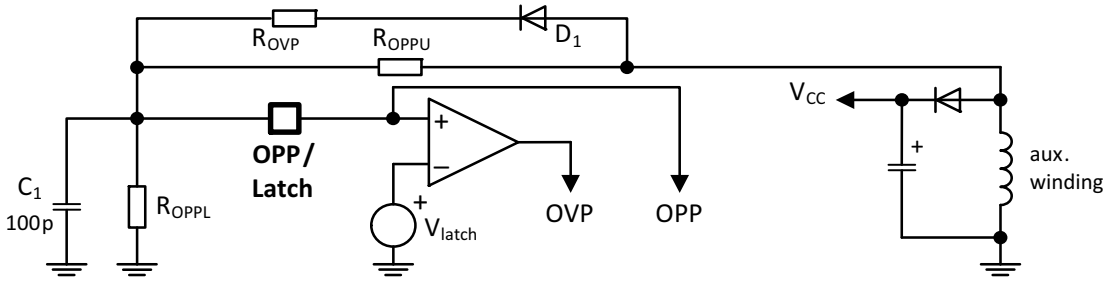



**Figure 60. A simple resistive divider brings the OPP pin above 3 V in case of a $V_{CC}$ voltage runaway above 18 V.**

First, calculate the OPP network with the above equations. Then, suppose we want to latch off our controller when $V_{out}$ exceeds 25 V. On the auxiliary winding, the plateau reflects the output voltage by the turns ratio between the power and the auxiliary winding. In case of voltage runaway for our 19 V adapter, the plateau will go up to:

$$V_{aux,OVP} = V_{out} \cdot \frac{N_s}{N_{aux}} = 25 \cdot \frac{0.18}{0.25} = 18\ V \quad \text{(eq. 15)}$$

Since our OVP comparator trips at level $V_{latch}$ = 3 V, across the 1 kΩ selected OPP pull−down resistor, it implies a 3 mA current. From 3 V to go up to 18 V, we need an additional 15 V. Under 3 mA and neglecting the series diode forward drop, it requires a series resistor of:

$$R_{OVP} = V_{out} \cdot \frac{V_{aux,OVP} - V_{latch}}{\frac{V_{OVP}}{R_{OPPL}}} = \frac{18 - 3}{\frac{3}{1\ k}} = 5\ k\Omega \quad \text{(eq. 16)}$$

In nominal conditions, the plateau establishes to around 14 V. Given the divide by 6 ratio, the OPP pin will swing to 14/6 = 2.3 V during normal conditions, leaving 700 mV for the noise immunity. A 100 pF capacitor can be added to improve it and avoid erratic trips in presence of external surges. Do not increase this capacitor too much otherwise the OPP signal will be affected by the integrating time constant.

A second solution for the OVP detection alone is to use a Zener diode wired as recommended by Figure 61.

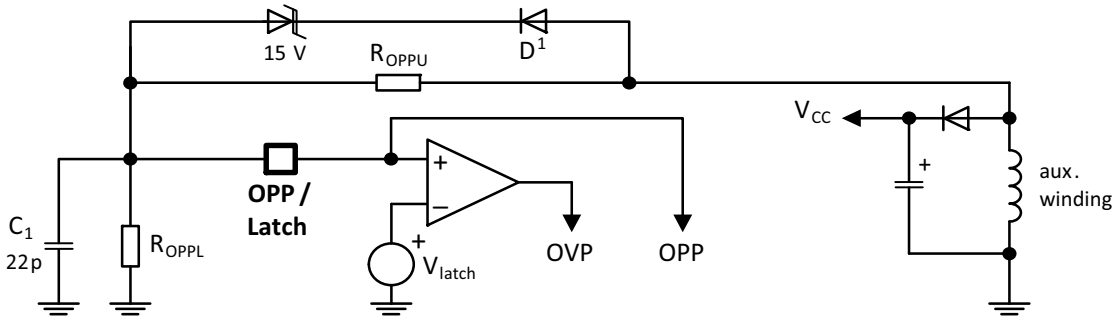



**Figure 61. A Zener diode in series with a diode helps to improve the noise immunity of the system.**

In this case, to still trip at 18 V level, we have selected a 15 V Zener diode. In nominal conditions, the voltage on the OPP pin is almost 0 V during the off−time as the Zener is fully blocked. This technique clearly improves the noise immunity of the system compared to that obtained from a resistive string as in Figure 60. Please note the reduction of the capacitor on the OPP pin to 10−22 pF. This is because of the potential spike going through the Zener parasitic capacitor and the possible auxiliary level shortly exceeding its breakdown voltage during the leakage inductance reset period (hence the internal blanking delay $t_{latch-blank}$ at turn off). This spike despite its very short time is energetic enough to charge the added capacitor $C_1$ and given the time constant, could make it discharge slower, potentially disturbing the blanking circuit. When implementing the Zener option, it is important to carefully observe the OPP pin voltage (short probe connections!) and check that enough margin exists to that respect.

### Over Temperature Protection

In a lot of designs, the adapter must be protected against thermal runaways, e.g. when the temperature inside the adapter box increases a certain value. Figure 62 shows how to implement a simple OTP using an external NTC and a series diode. The principle remains the same: make sure the OPP network is not bothered by the additional NTC hence the presence of this diode.

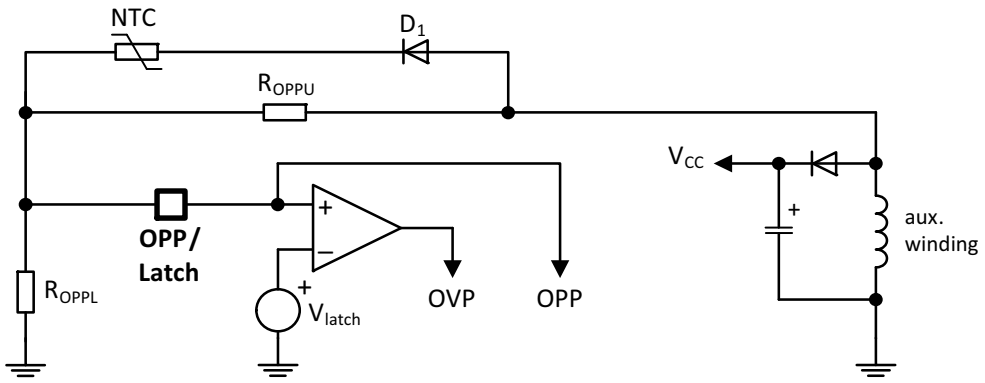



**Figure 62. The internal circuitry hooked to OPP/Latch pin can be used to implement over temperature protection (OTP).**

When the NTC resistor will diminish as the temperature increases, the voltage on the OPP pin during the off−time will slowly increase and, once it passes $V_{latch}$ level for 4 consecutive clock cycles, the controller will permanently latch off.

Back to our 19 V adapter, we have found that the plateau voltage on the auxiliary diode was 14 V in nominal conditions. We have selected an NTC which offers a 470 kΩ resistance at 25°C and drops to 8.8 kΩ at 110°C. If our auxiliary winding plateau is 14 V and we consider a 0.7 V forward drop for the diode, then the voltage across the NTC in fault mode must be:

$$V_{NTC} = V_{aux} - V_{latch} - V_F = 14 - 3 - 0.7 = 10.3\ V \quad \text{(eq. 17)}$$

Based on the 8.8 kΩ NTC resistor at 110°C, the current inside the device must be:

$$I_{NTC} = \frac{V_{NTC}}{R_{NTC(110)}} = \frac{10.3}{8.8\ k} = 1.2\ mA \quad \text{(eq. 18)}$$

As such, the bottom resistor $R_{OPPL}$, can easily be calculated:

$$R_{OPPL} = \frac{V_{latch}}{I_{NTC}} = 2.5\ k\Omega \quad \text{(eq. 19)}$$

Now the pull down OPP resistor is known, we can calculate the upper resistor value $R_{OPPU}$ to adjust the power limit at the chosen output power level. Suppose we need a 200 mV decrease from the $V_{limit}$ setpoint and the on−time swing on the auxiliary anode is −67.5 V, then we need to drop over $R_{OPPU}$ a voltage of:

$$V_{R_{OPPU}} = V_{aux} - V_{OPP} = -67.5 + 0.2 = -67.3\ V \quad \text{(eq. 20)}$$

The current circulating the pull down resistor $R_{OPPL}$ in this condition will be:

$$I_{R_{OPPL}} = \frac{V_{OPP}}{R_{OPPL}} = \frac{-0.2}{2.5\ k} = -80\ \mu A \quad \text{(eq. 21)}$$

The $R_{OPPU}$ value is therefore easily derived:

$$R_{OPPU} = \frac{V_{R_{OPPU}}}{I_{R_{OPPU}}} = \frac{-67.3}{-80\ \mu} \approx 841\ k\Omega \quad \text{(eq. 22)}$$

### Combining OVP and OTP

The OTP and Zener−based OVP can be combined together as illustrated by Figure 63. In nominal $V_{CC}$/output conditions, when the Zener is not activated, the NTC can drive the OPP pin and trigger the adapter in case of a fault. On the contrary, in nominal temperature conditions, if the loop is broken, the voltage runaway will be detected and acknowledged by the controller.

In case the OPP pin is not used for either OPP or OVP, it can simply be grounded.

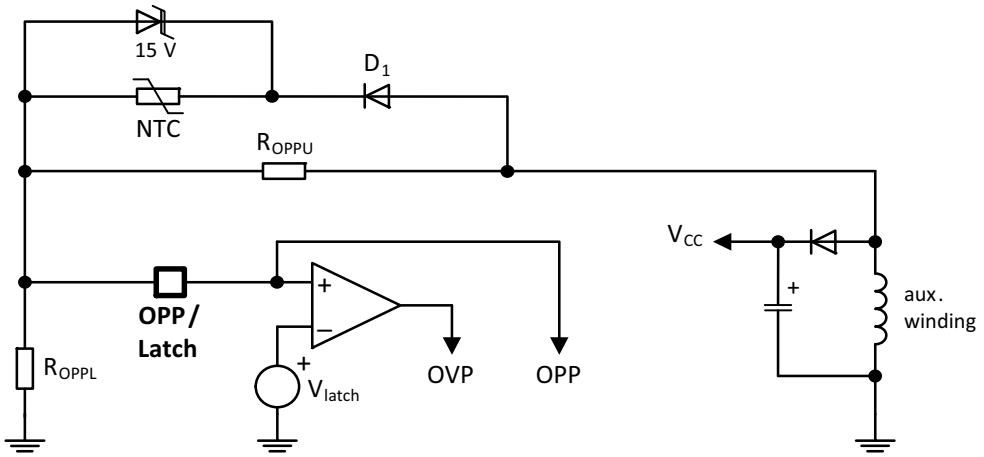



**Figure 63. With the NTC back in place, the circuit nicely combines OVP, OTP and OPP on the same pin.**

### Filtering the Spikes

The auxiliary winding is the seat of spikes that can couple to the OPP pin via the parasitic capacitances exhibited by the Zener diode and the series diode. To prevent an adverse triggering of the Over Voltage Protection circuitry, we recommend the installation of a small *RC* filter before the detection network as illustrated by Figure 64. The values of resistance and capacitance must be selected to provide the adequate filtering function without degrading the stand−by power by an excessive current circulation.

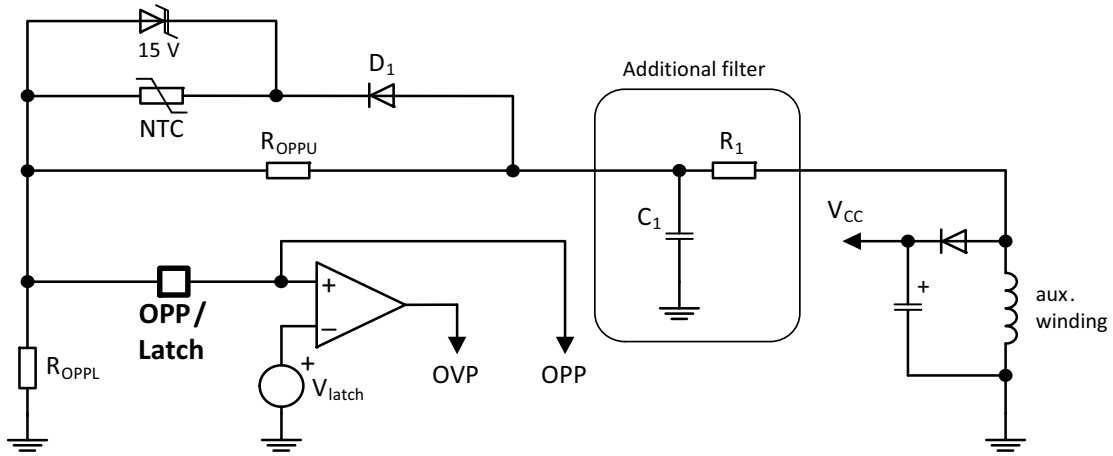
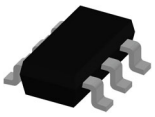


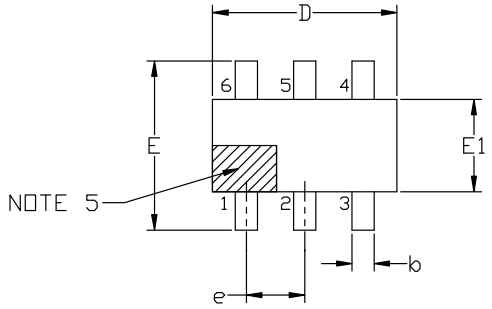

**Figure 64. A small *RC* filter prevents the fast rising spikes from reaching the protection pin OPP/latch in presence of energetic perturbations superimposed on the input line.**

# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

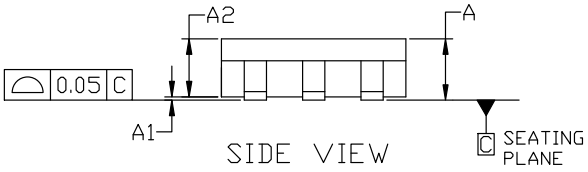


**TSOP−6 3.00x1.50x0.90, 0.95P**
CASE 318G
ISSUE W

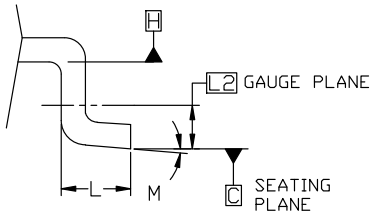
DATE 26 FEB 2024



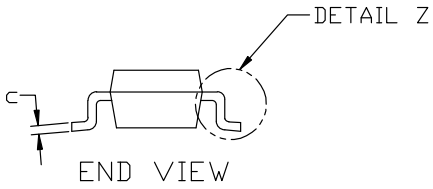

TOP VIEW




SIDE VIEW



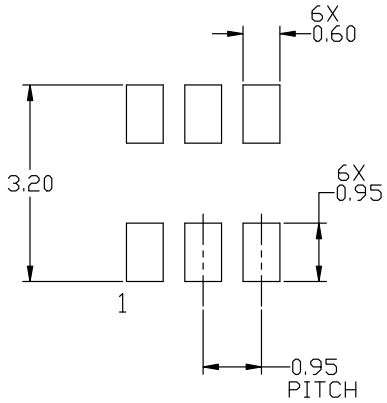

DETAIL Z
SCALE 3:1




END VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
5. PIN 1 INDICATOR MUST BE LOCATED IN THE INDICATED ZONE

| MILLIMETERS | | | |
|---|---|---|---|
| DIM | MIN | NOM | MAX |
| A | 0.90 | 1.00 | 1.10 |
| A1 | 0.01 | 0.06 | 0.10 |
| A2 | 0.80 | 0.90 | 1.00 |
| b | 0.25 | 0.38 | 0.50 |
| c | 0.10 | 0.18 | 0.26 |
| D | 2.90 | 3.00 | 3.10 |
| E | 2.50 | 2.75 | 3.00 |
| E1 | 1.30 | 1.50 | 1.70 |
| e | 0.85 | 0.95 | 1.05 |
| L | 0.20 | 0.40 | 0.60 |
| L2 | 0.25 BSC | | |
| M | 0° | --- | 10° |




RECOMMENDED MOUNTING FOOTPRINT

*For additional information on our Pb-Free strategy and soldering details, please download th e ON Semiconductor Soldering and Mounting Techniques Reference manual, SOLDERRM/D.

| | | | |
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| **DESCRIPTION:** | **TSOP−6 3.00x1.50x0.90, 0.95P** | | **PAGE 1 OF 2** |

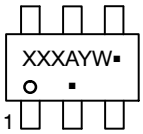
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**TSOP−6 3.00x1.50x0.90, 0.95P**
CASE 318G
ISSUE W

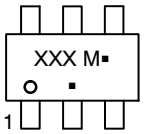
DATE 26 FEB 2024

**GENERIC**
**MARKING DIAGRAM***




**IC**

XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package




**STANDARD**

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 2:
PIN 1. EMITTER 2
2. BASE 1
3. COLLECTOR 1
4. EMITTER 1
5. BASE 2
6. COLLECTOR 2

STYLE 3:
PIN 1. ENABLE
2. N/C
3. R BOOST
4. Vz
5. V in
6. V out

STYLE 4:
PIN 1. N/C
2. V in
3. NOT USED
4. GROUND
5. ENABLE
6. LOAD

STYLE 5:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

STYLE 6:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

STYLE 7:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. N/C
5. COLLECTOR
6. EMITTER

STYLE 8:
PIN 1. Vbus
2. D(in)
3. D(in)+
4. D(out)+
5. D(out)
6. GND

STYLE 9:
PIN 1. LOW VOLTAGE GATE
2. DRAIN
3. SOURCE
4. DRAIN
5. DRAIN
6. HIGH VOLTAGE GATE

STYLE 10:
PIN 1. D(OUT)+
2. GND
3. D(OUT)−
4. D(IN)−
5. VBUS
6. D(IN)+

STYLE 11:
PIN 1. SOURCE 1
2. DRAIN 2
3. DRAIN 2
4. SOURCE 2
5. GATE 1
6. DRAIN 1/GATE 2

STYLE 12:
PIN 1. I/O
2. GROUND
3. I/O
4. I/O
5. VCC
6. I/O

STYLE 13:
PIN 1. GATE 1
2. SOURCE 2
3. GATE 2
4. DRAIN 2
5. SOURCE 1
6. DRAIN 1

STYLE 14:
PIN 1. ANODE
2. SOURCE
3. GATE
4. CATHODE/DRAIN
5. CATHODE/DRAIN
6. CATHODE/DRAIN

STYLE 15:
PIN 1. ANODE
2. SOURCE
3. GATE
4. DRAIN
5. N/C
6. CATHODE

STYLE 16:
PIN 1. ANODE/CATHODE
2. BASE
3. EMITTER
4. COLLECTOR
5. ANODE
6. CATHODE

STYLE 17:
PIN 1. EMITTER
2. BASE
3. ANODE/CATHODE
4. ANODE
5. CATHODE
6. COLLECTOR



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