QPA0708T

7.9 –8.4 GHz 60 Watt GaN Power Amplifier

Product Overview

Qorvo's QPA0708T is a power amplifier fabricated on Qorvo's 0.25um GaN on SiC process (QGaN25), mounted to a high thermal conductivity tab. Operating between 7.9 and 8.4 GHz, it achieves 36 dB small signal gain, 32 W linear power with −25 dBc intermodulation distortion products, and saturated output power of 72 W with a power-added efficiency of 49.3 %.

QPA0708T is ideally suited to support satellite communications.

To simplify system integration, the QPA0708T is fully matched to 50 ohms, with the DC shorted on the RF input port and integrated DC blocking caps on the RF output port.

The QPA0708T die is 100% DC and RF tested on-wafer to ensure compliance to electrical specifications.

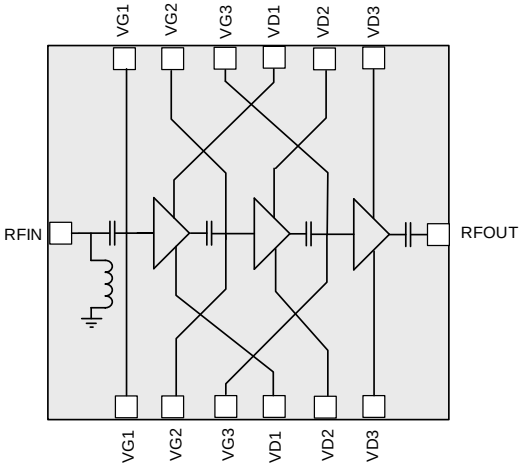
Lead-free and RoHS compliant.

Key Features

- Frequency Range: 7.9 – 8.4 GHz
- P_{SAT} (P_{IN}=18 dBm): 48.6 dBm
- PAE (P_{IN}=18 dBm): 49.3 %
- Power Gain (P_{IN}=18 dBm): 30.6 dB
- IMD3 (at 42 dBm/tone): −25 dBc
- Small Signal Gain: 36 dB
- Bias: V_D = 26 V, I_{DQ} = 904 mA
- Tab dimensions: 5.817 mm x 6.172 mm x 0.254 mm

Performance is typical across frequency. Please reference electrical specification table and data plots for more details.

Functional Block Diagram



Applications

- Satellite Communications

Ordering Information

Part No.	Description
QPA0708T	7.9 – 8.4 GHz GaN Amplifier (20 Pcs.)
QPA0708TEVB	QPA0708T Evaluation Board

Absolute Maximum Ratings

Parameter	Value / Range
Drain Voltage (V_D)	29.5 V
Gate Voltage Range (V_G)	−4 V to 0 V
Drain Current (I_{D1}), Stage 1	0.36 A
Drain Current (I_{D2}), Stage 2	1.6 A
Drain Current (I_{D2}), Stage 3	11.52 A
Gate Current (I_G)	See plot pg. 18
Power Dissipation (P_{DISS}), 85 °C	100 W
Input Power (P_{IN}), 50 Ω, V_D=22 V, I_{DQ}=280 mA, 85 °C	29 dBm
Input Power (P_{IN}), 3:1 VSWR, V_D=22 V, I_{DQ}=280 mA, 85 °C	25 dBm
Storage Temperature	−55 to +150 °C

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied.

Recommended Operating Conditions

Parameter	Value / Range
Drain Voltage (V_D)	26
Drain Current, Total (I_{DQ})	904 mA
Operating Temperature	−40 to +85 °C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Parameter		Min	Typ	Max	Units
Operational Frequency		7.9		8.4	GHz
Saturated Output Power (P_{IN}=18 dBm)[1]	7.90 GHz 8.15 GHz 8.40 GHz		48.6 48.7 48.6		dBm dBm dBm
Power Added Efficiency (P_{IN}=18 dBm)	7.90 GHz 8.15 GHz 8.40 GHz		49.3 49.4 48.6		% % %
Small Signal Gain	7.90 GHz 8.15 GHz 8.40 GHz		37.7 36.7 36.2		dB dB dB
Input Return Loss	7.90 GHz 8.15 GHz 8.40 GHz		18 20 23		dB dB dB
Output Return Loss	7.90 GHz 8.15 GHz 8.40 GHz		12 13 15		dB dB dB
IMD3 (P_{OUT}/Tone= 42 dBm, 10 MHz tone spacing)	7.90 GHz 8.15 GHz 8.40 GHz		−25.2 −27.2 −26.0		dBc dBc dBc
P_{OUT} Temp. Coeff. (85 °C to 25 °C, P_{IN} = 18 dBm))			−0.023		dB/°C
Sm. Sig. Gain Temp. Coefficient (85 °C to −40 °C)			−0.073		dB/°C

Test conditions, unless otherwise noted: T = +25 °C, V_D = 26 V, I_{DQ} = 904 mA
All performance data presented is for the bare die

Performance Plots – Large Signal

Test conditions, unless otherwise noted: V_D = 26 V, I_{DQ} = 904 mA, T=+25 °C, P_{IN} = 18 dBm
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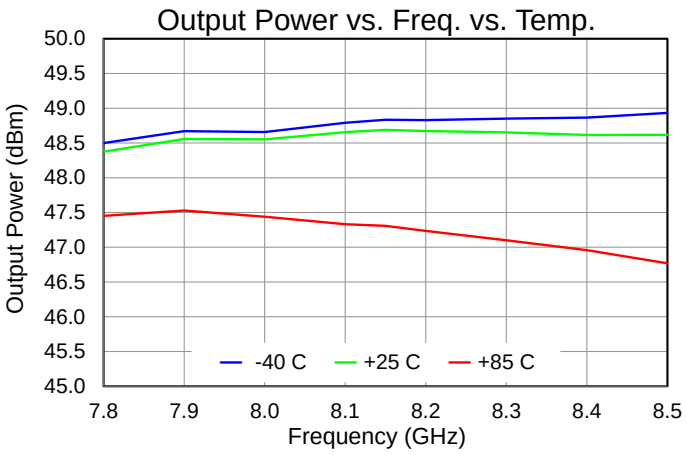

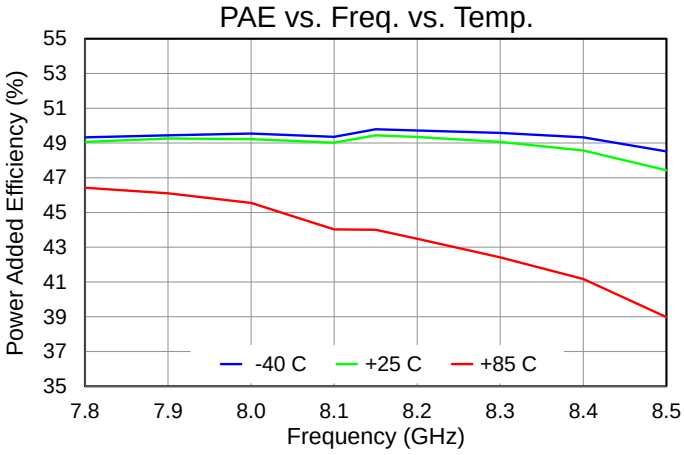

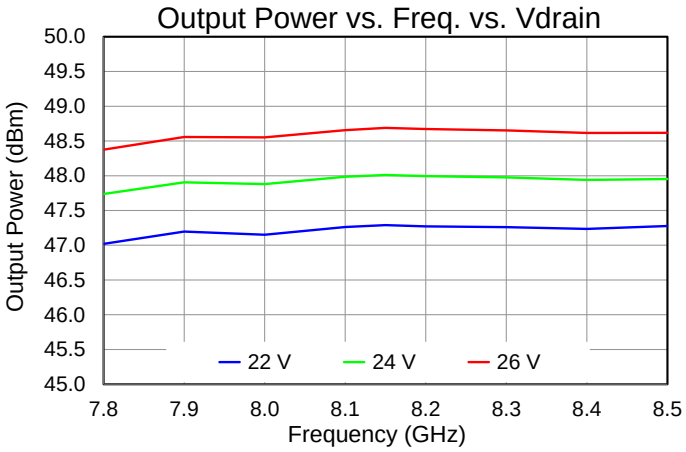

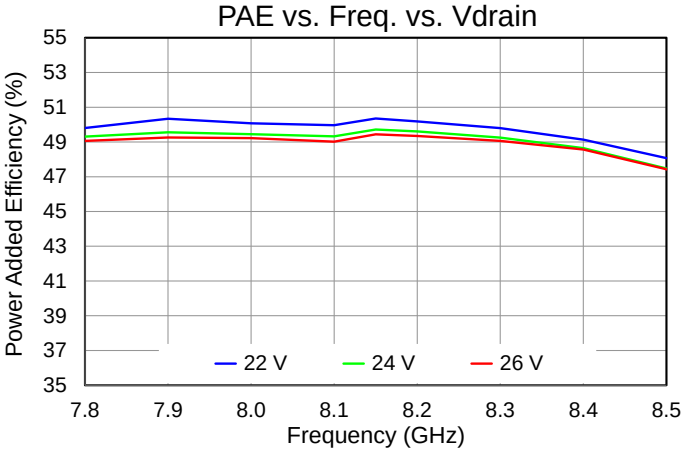

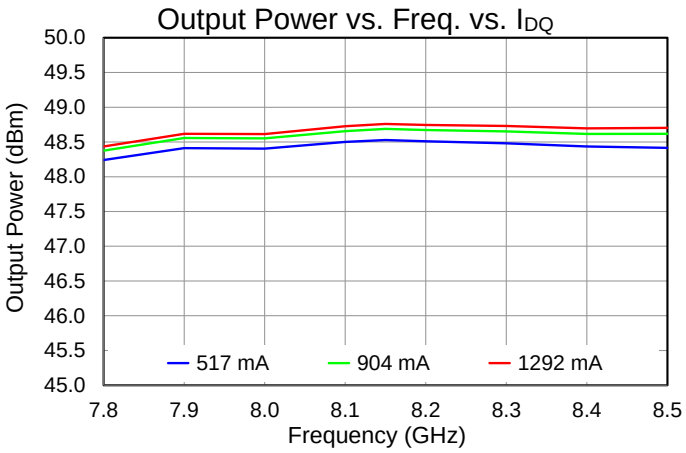

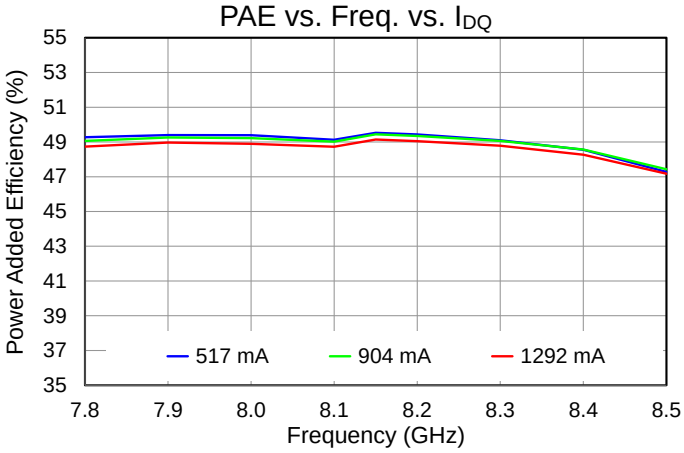

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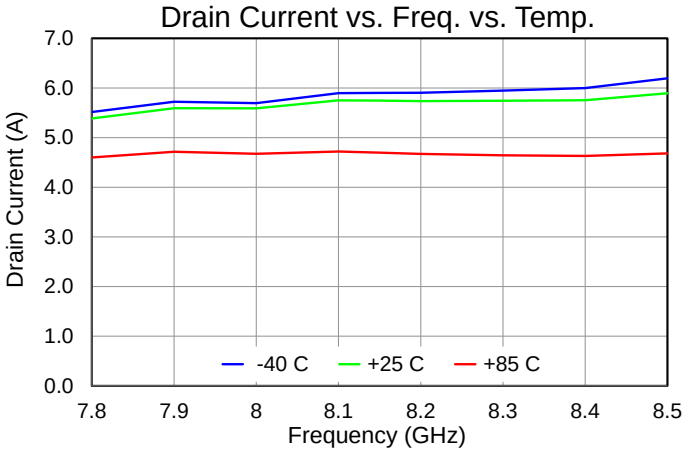

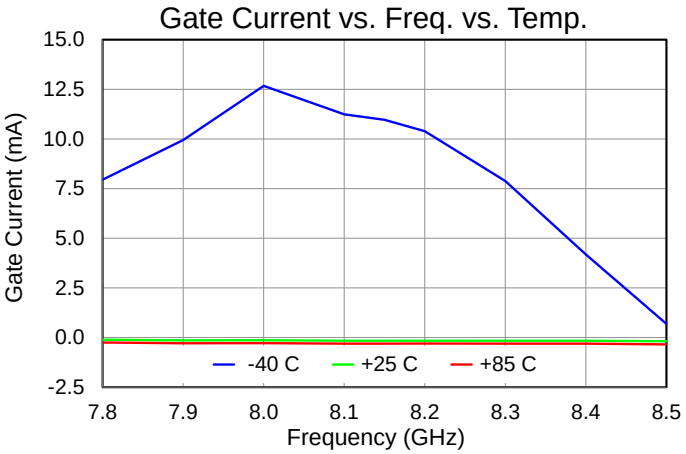

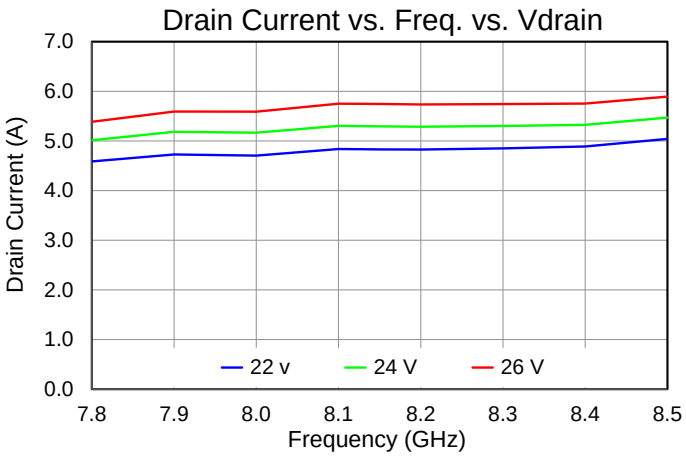

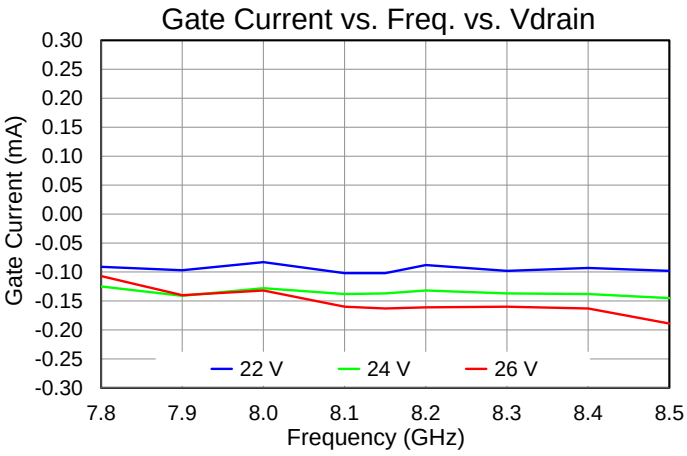

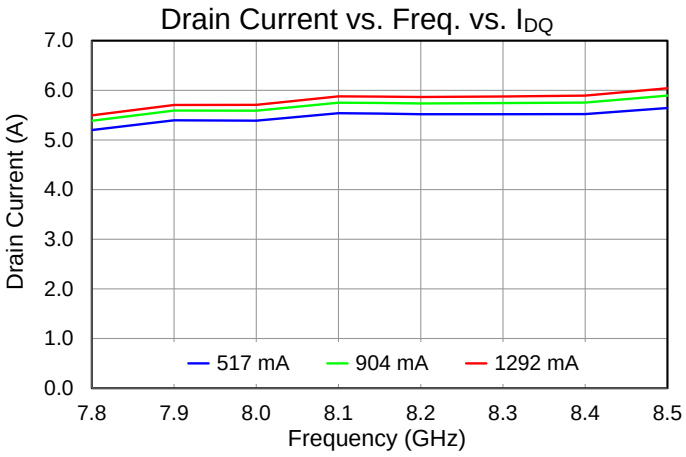

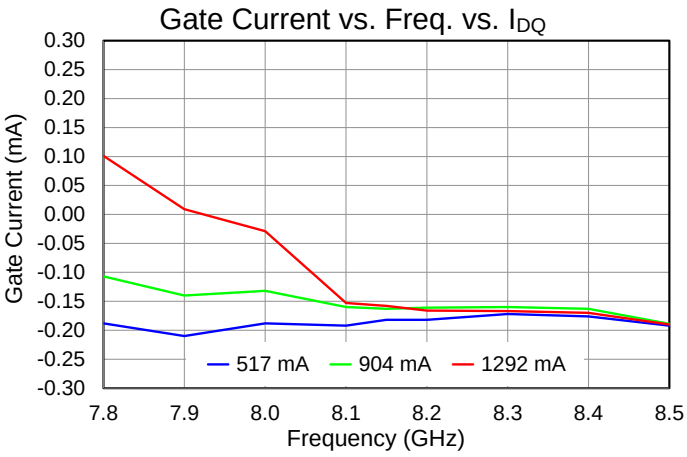

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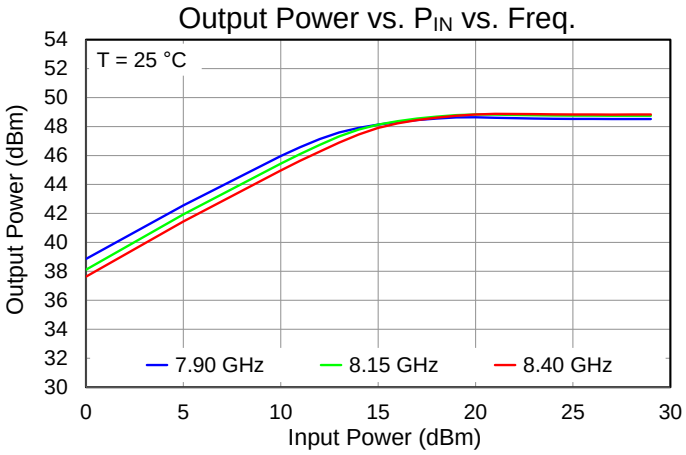

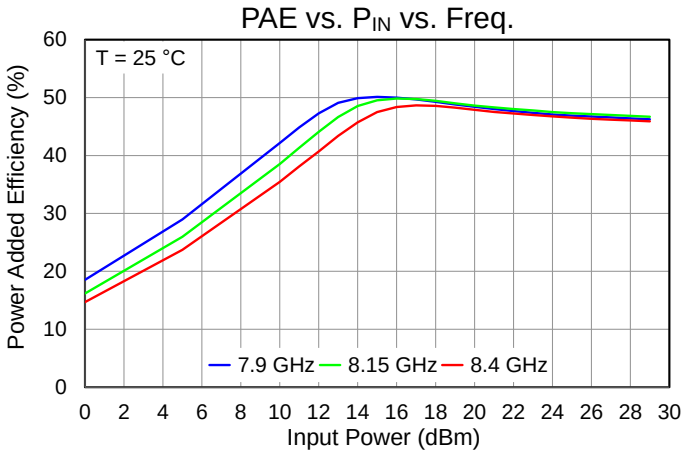

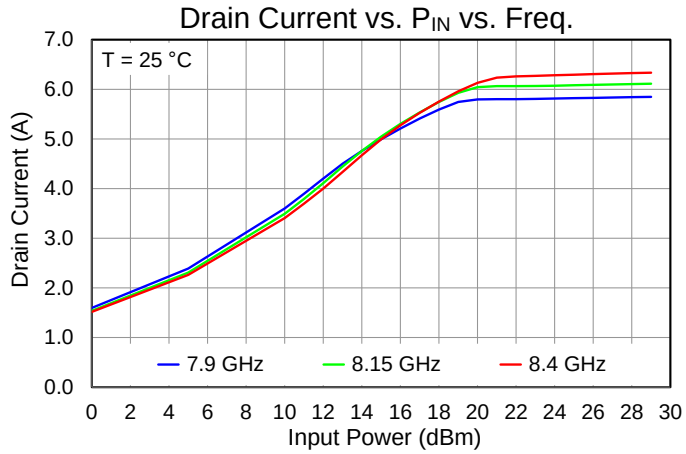

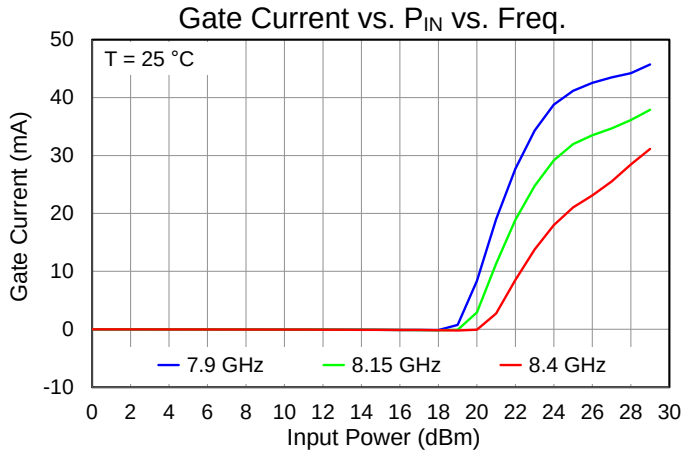

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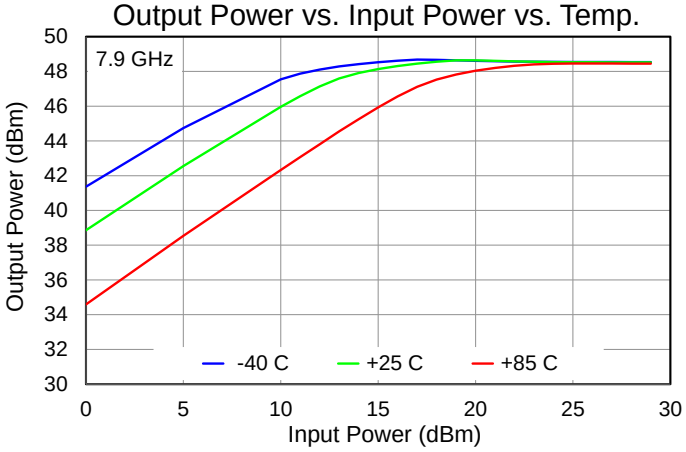
Output Power vs. Input Power vs. Temp.



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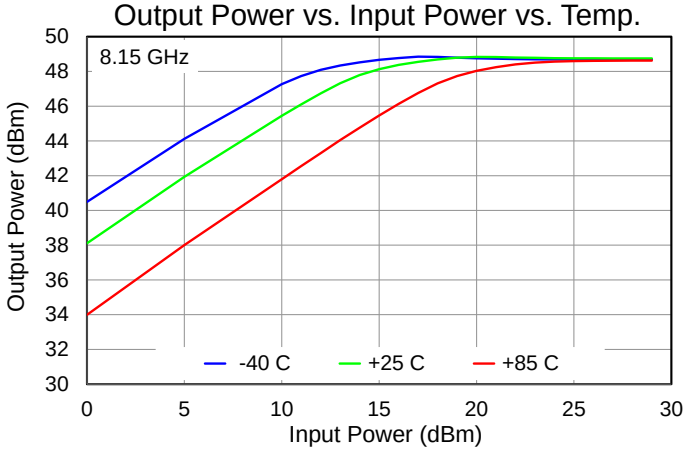
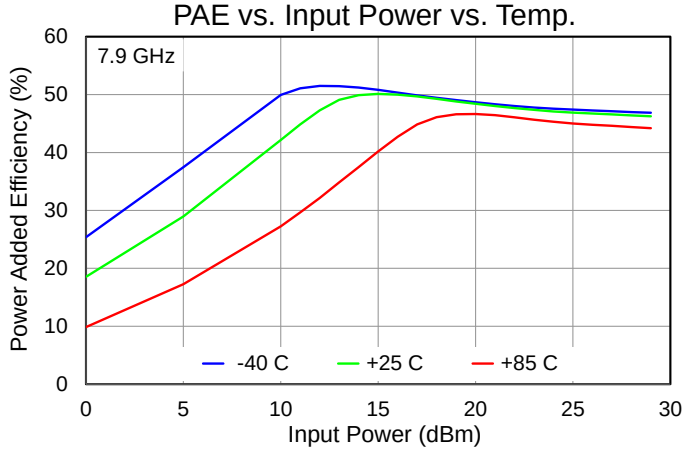


PAE vs. Input Power vs. Temp.



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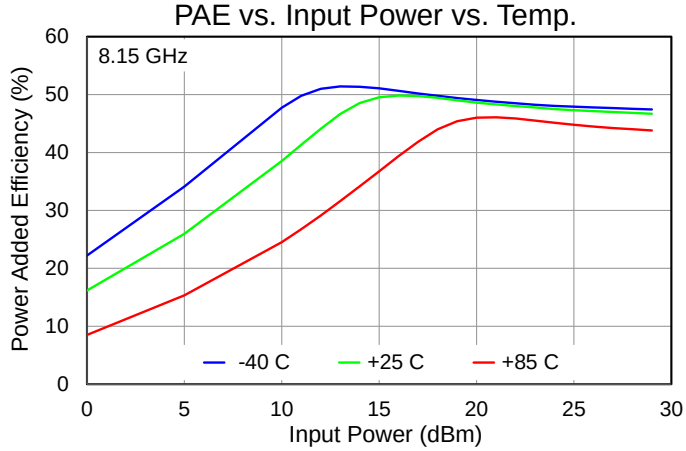
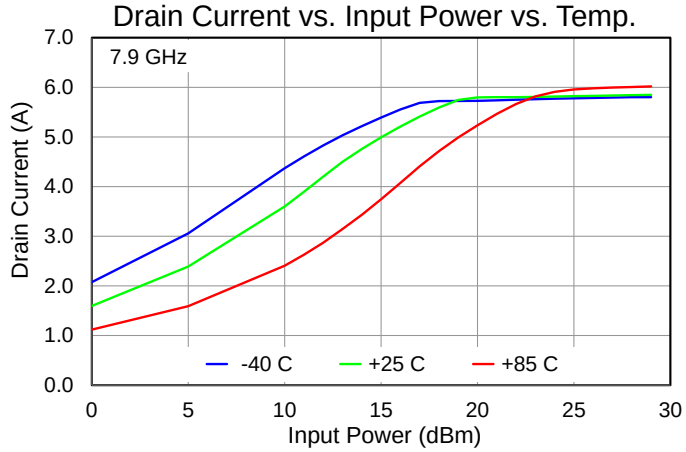


Drain Current vs. Input Power vs. Temp.



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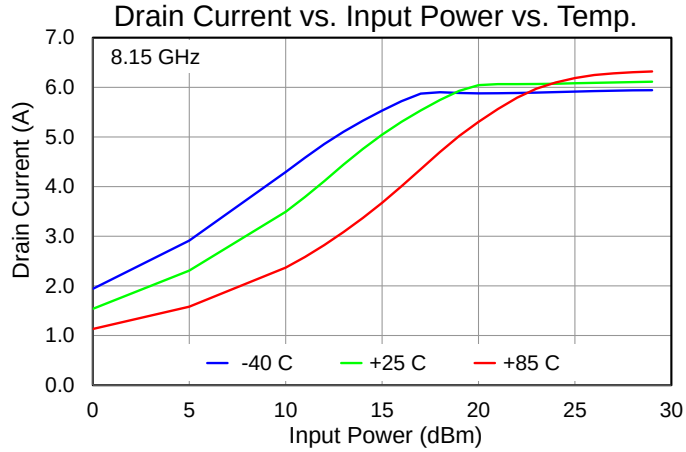

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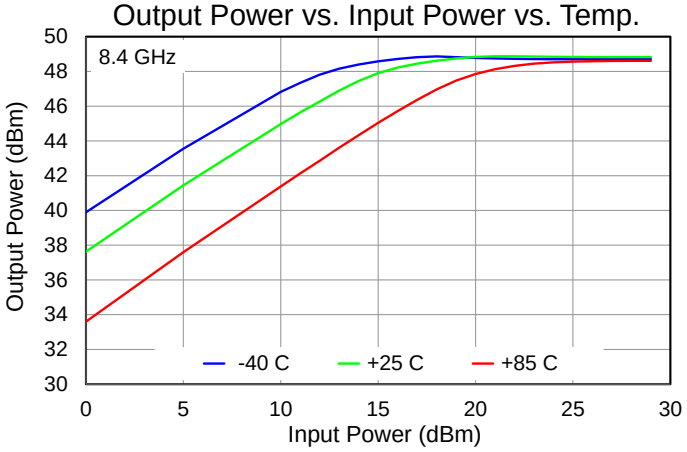
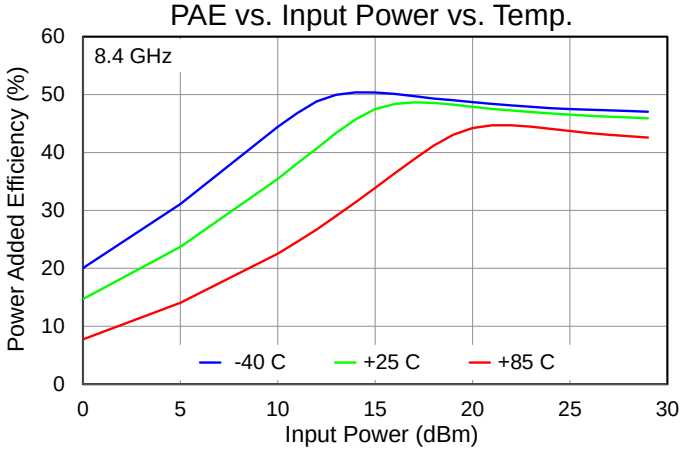


PAE vs. Input Power vs. Temp.



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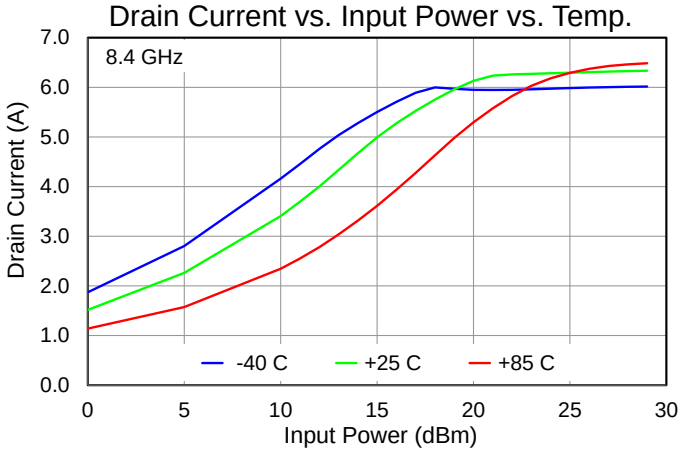

Performance Plots – Large Signal

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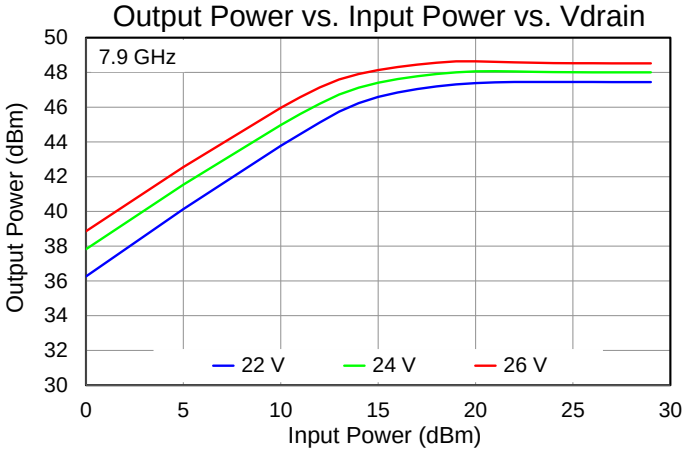
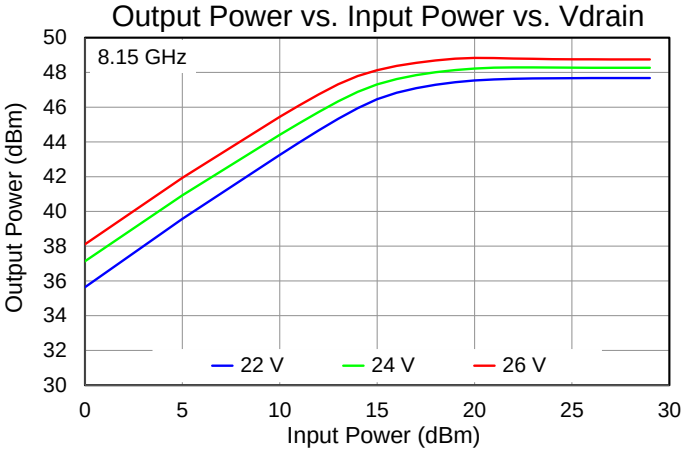
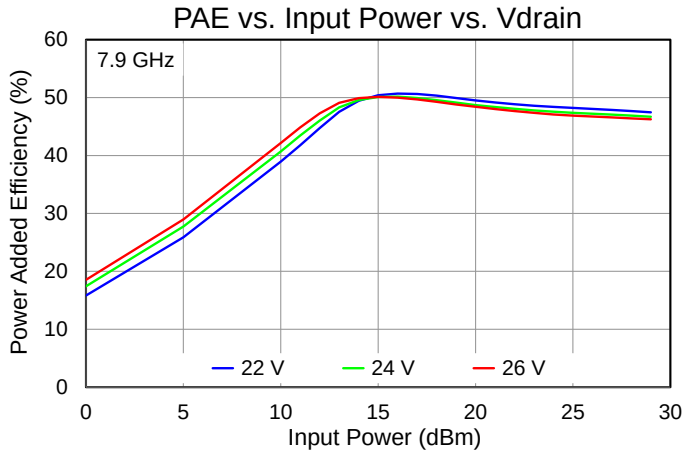
Output Power vs. Input Power vs. Vdrain



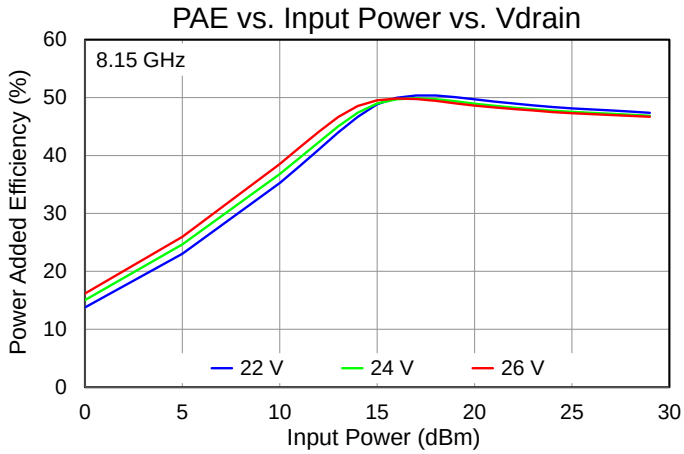
Output Power vs. Input Power vs. Vdrain



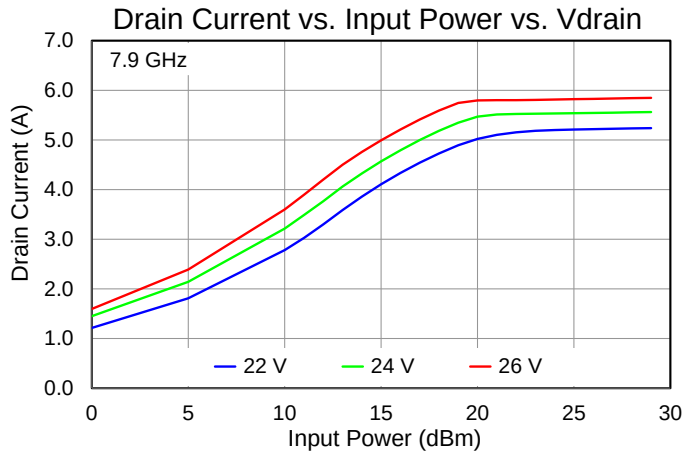
PAE vs. Input Power vs. Vdrain



PAE vs. Input Power vs. Vdrain



Drain Current vs. Input Power vs. Vdrain



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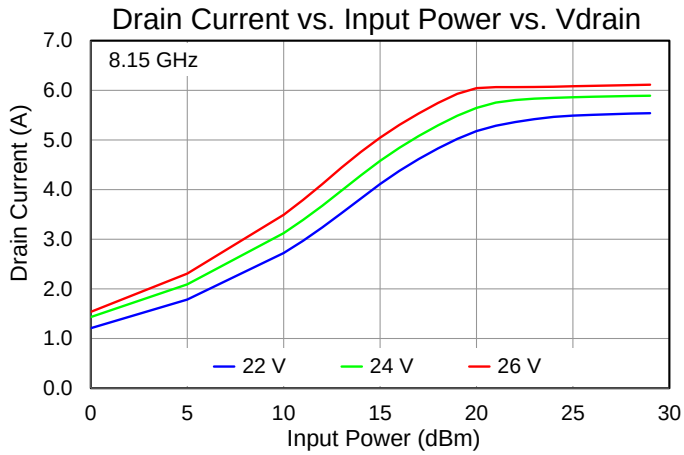

Performance Plots – Large Signal

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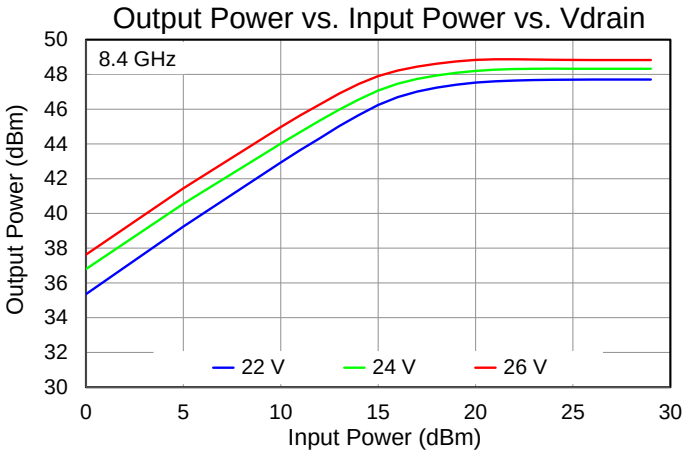

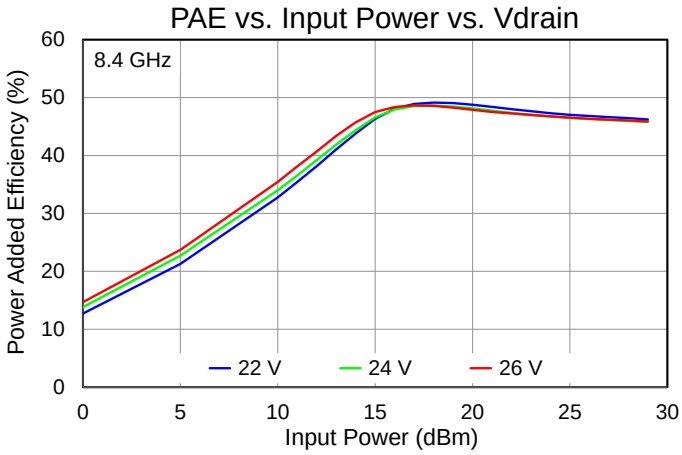

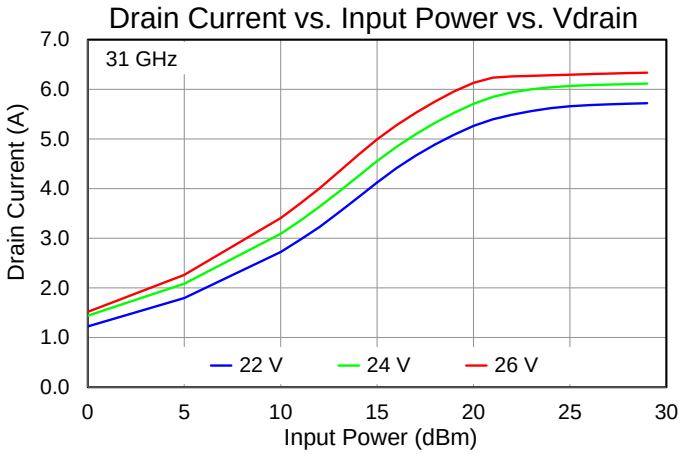

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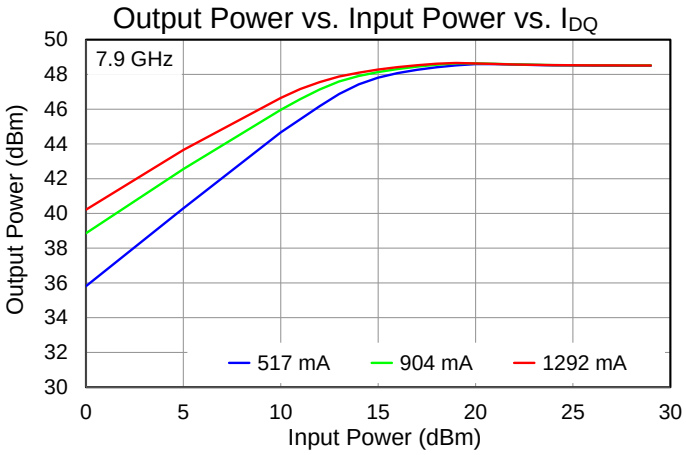

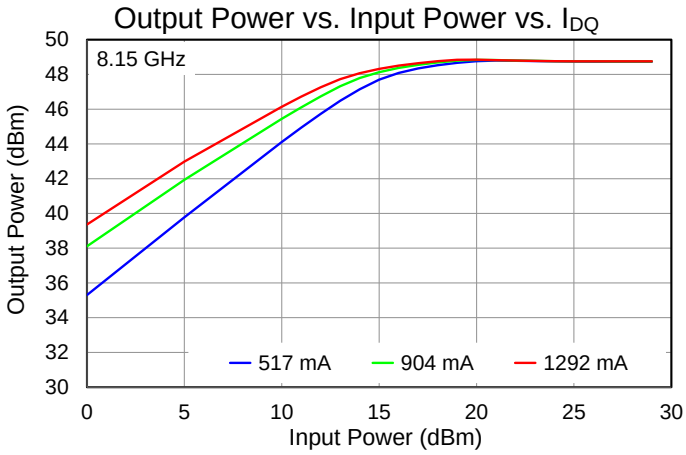

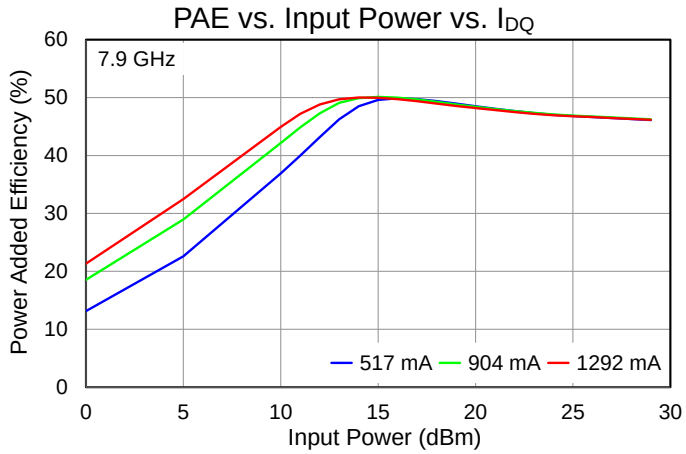

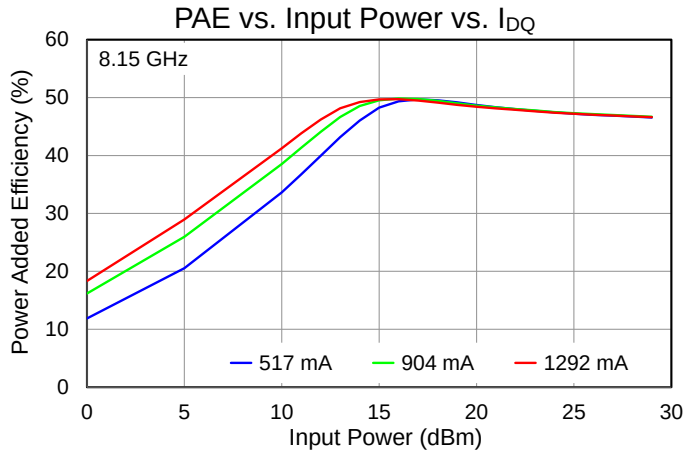

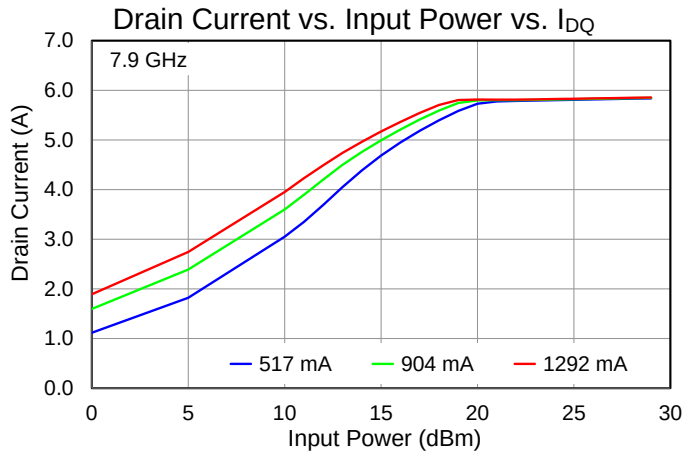

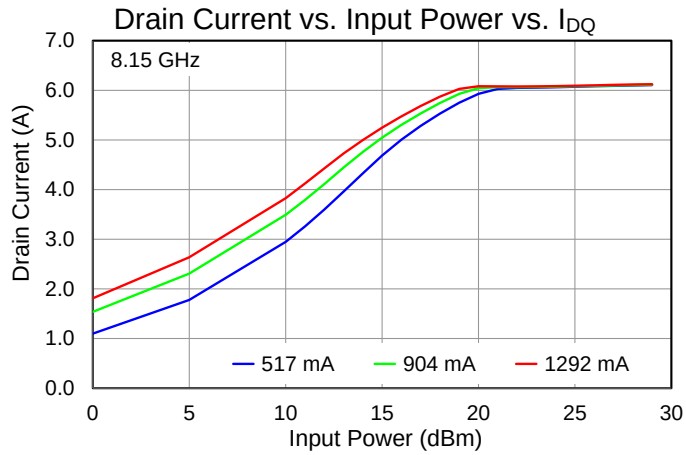

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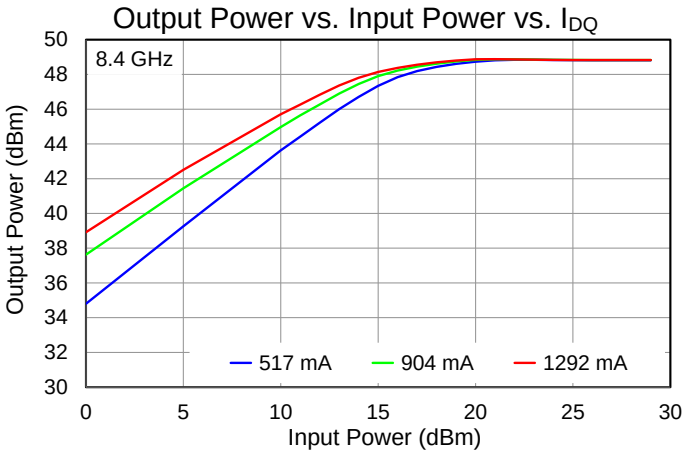

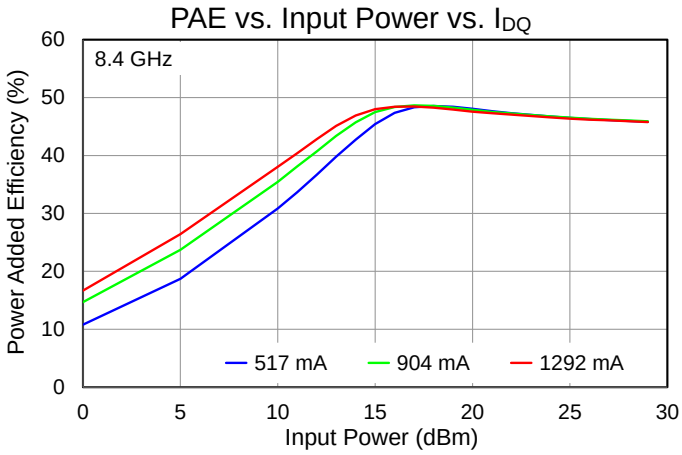

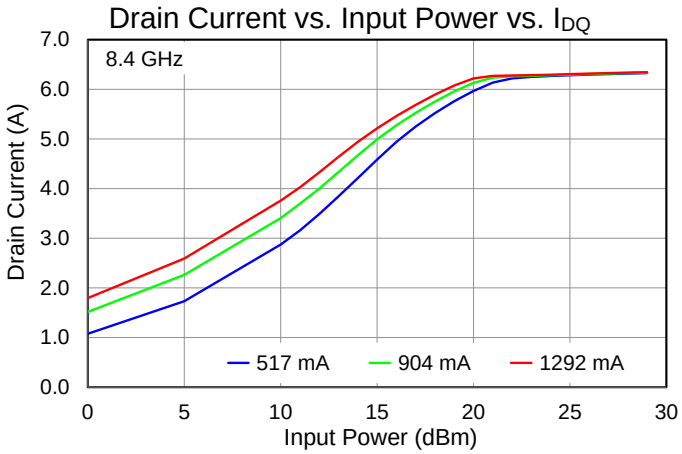

Performance Plots – 2ND Harmonic

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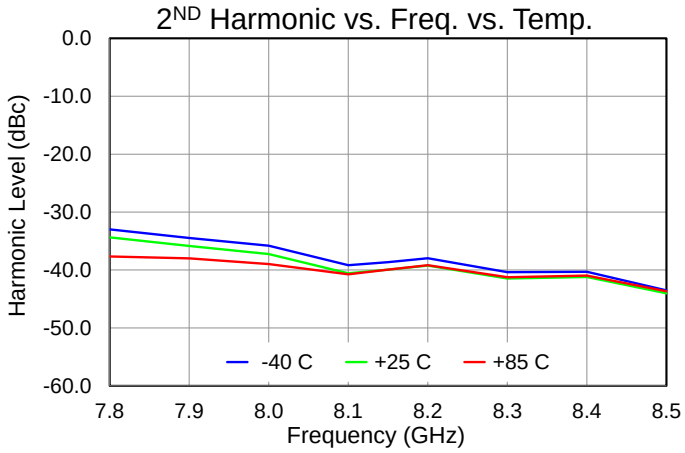
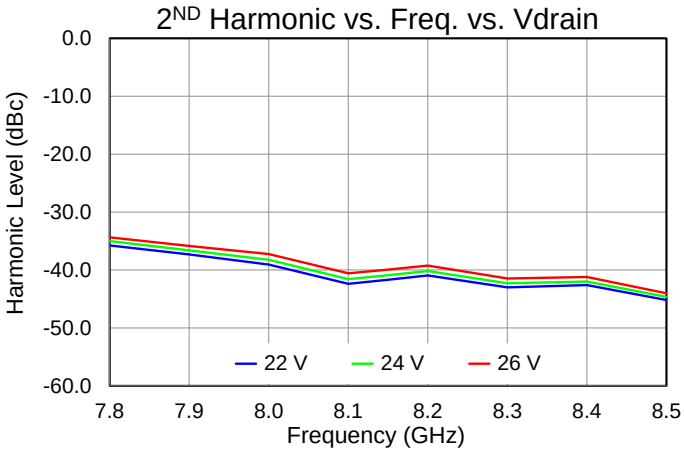
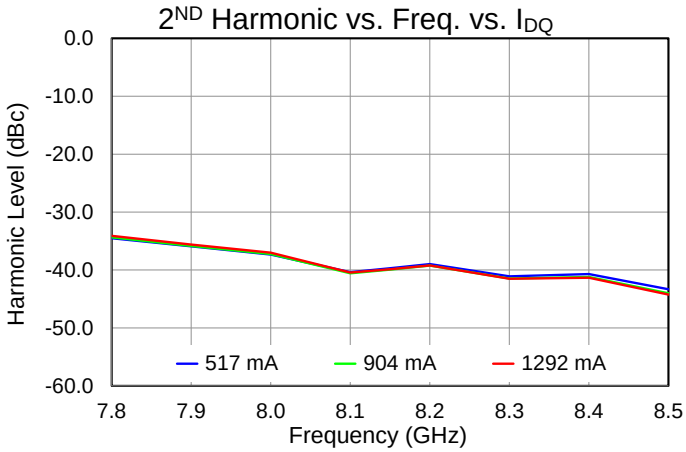
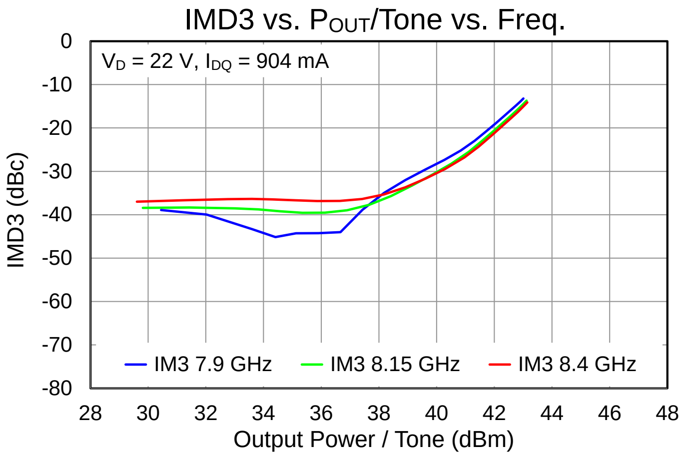


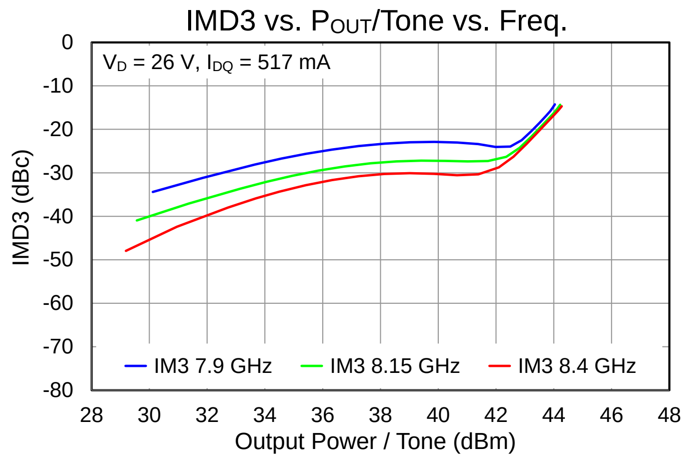


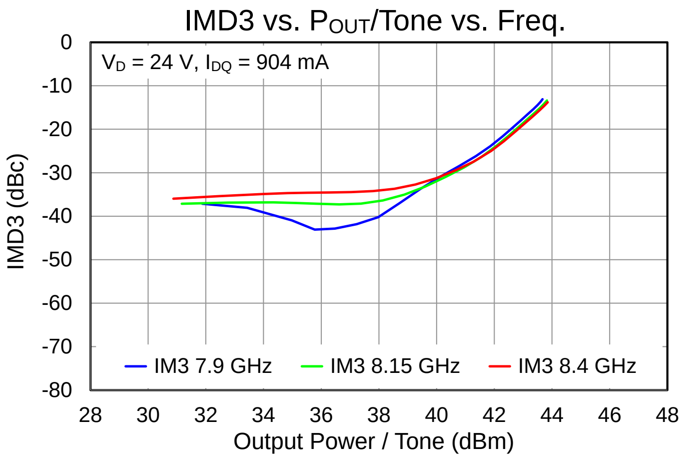


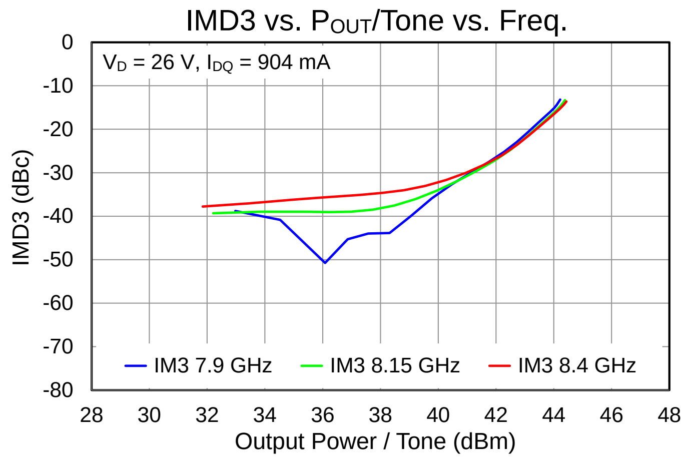
Performance Plots – Linearity

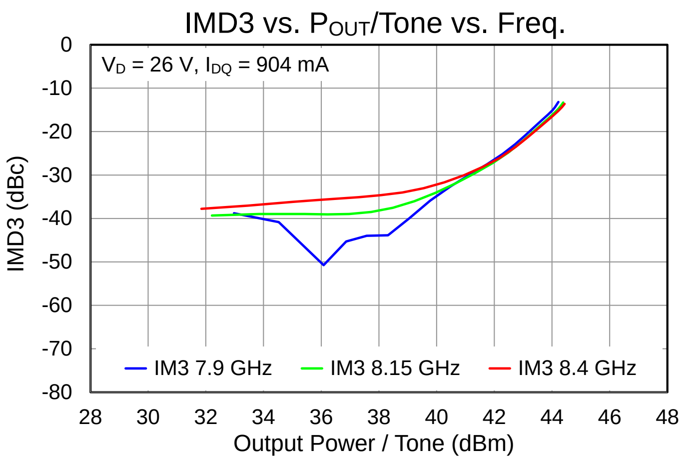
Test conditions, unless otherwise noted: V_D = 26 V, I_{DQ} = 904 mA, T=+25 °C, Tone Spacing = 10 MHz
All performance data presented is for the bare die

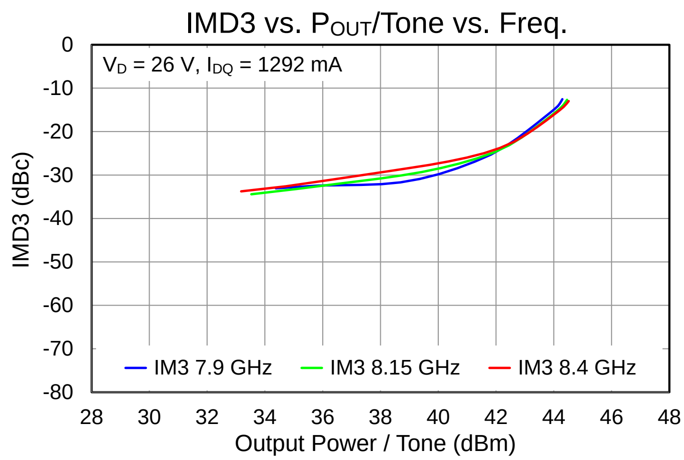








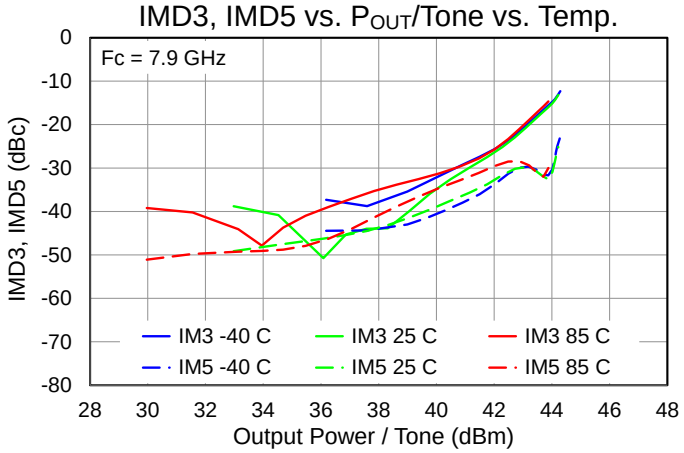




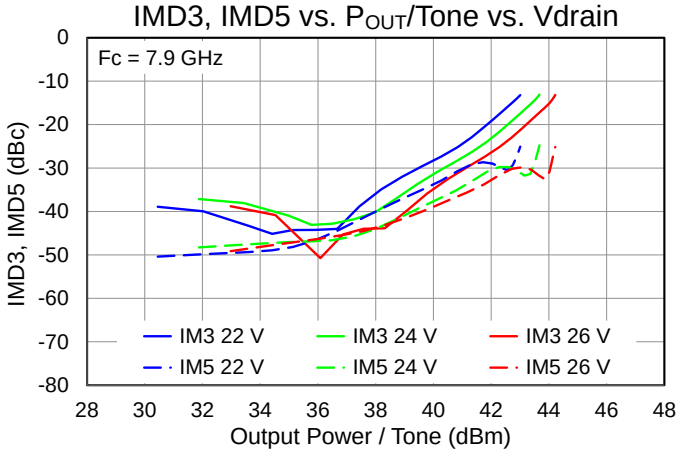
Performance Plots – Linearity

Test conditions, unless otherwise noted: V_D = 26 V, I_{DQ} = 904 mA, T=+25 °C, Tone Spacing = 10 MHz
All performance data presented is for the bare die

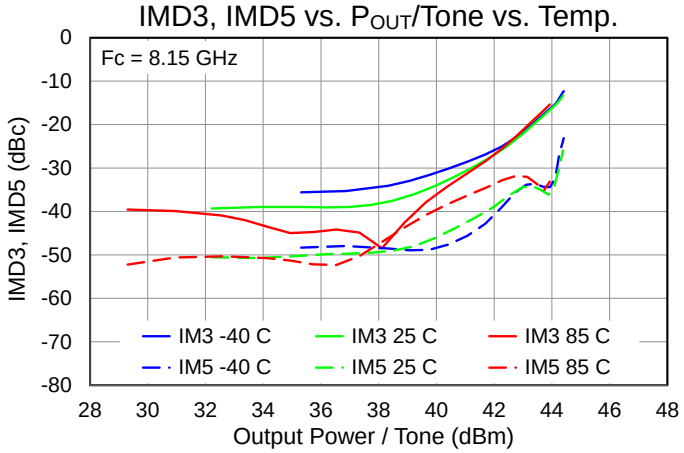
IMD3, IMD5 vs. P_{OUT}/Tone vs. Temp.



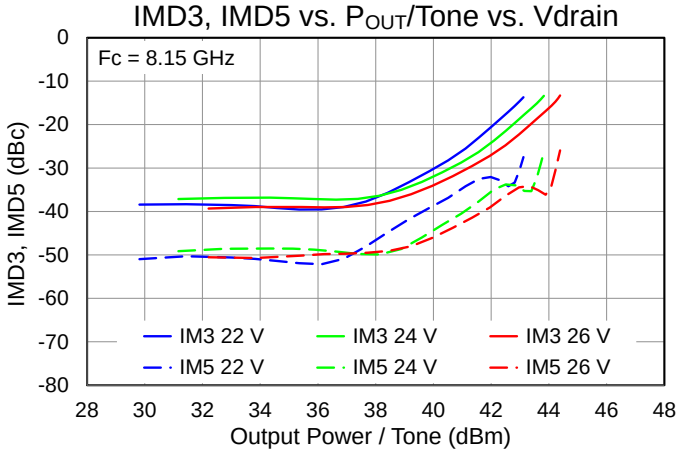
IMD3, IMD5 vs. P_{OUT}/Tone vs. Vdrain



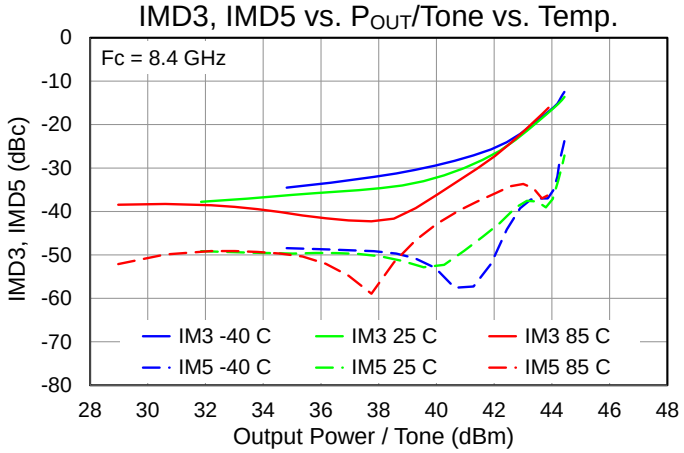
IMD3, IMD5 vs. P_{OUT}/Tone vs. Temp.



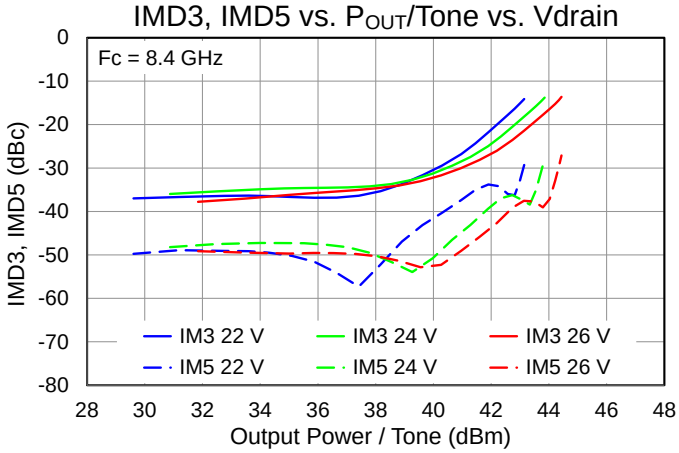
IMD3, IMD5 vs. P_{OUT}/Tone vs. Vdrain



IMD3, IMD5 vs. P_{OUT}/Tone vs. Temp.



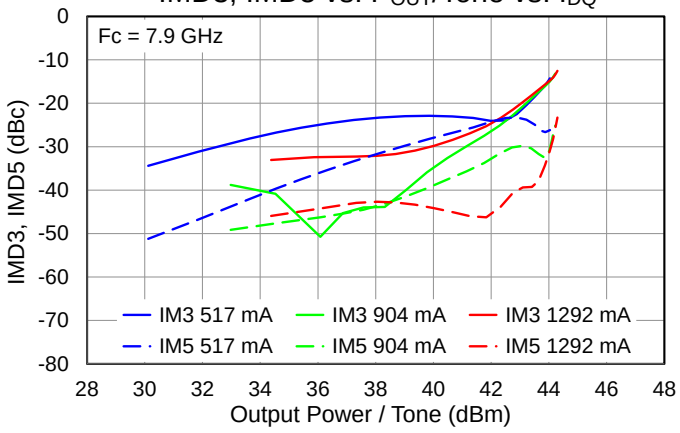
IMD3, IMD5 vs. P_{OUT}/Tone vs. Vdrain



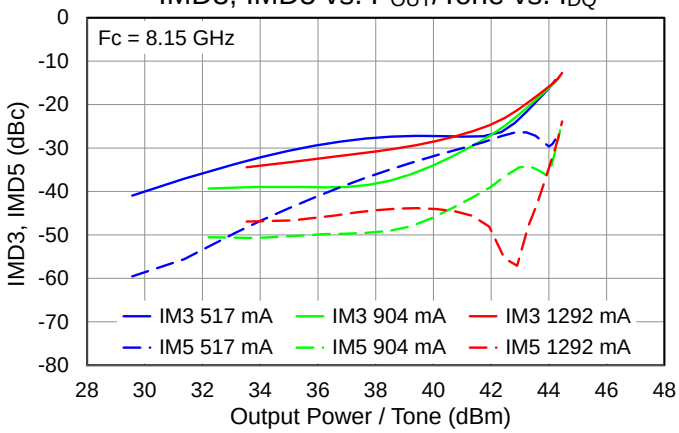
Performance Plots – Linearity

Test conditions, unless otherwise noted: V_D = 26 V, I_{DQ} = 904 mA, T=+25 °C, Tone Spacing = 10 MHz
All performance data presented is for the bare die

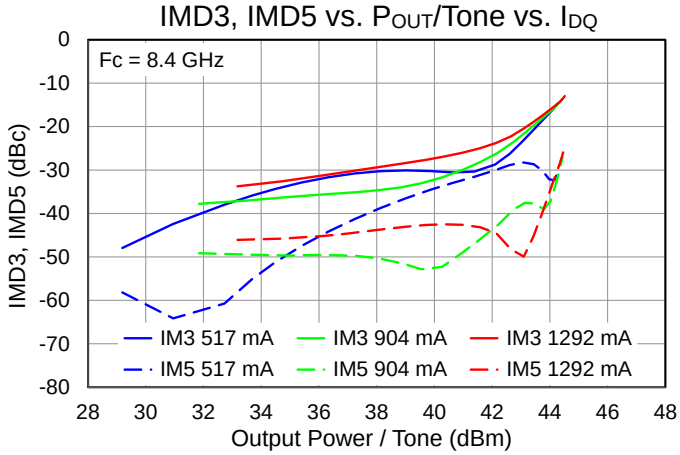
IMD3, IMD5 vs. P_{OUT}/Tone vs. I_{DQ}



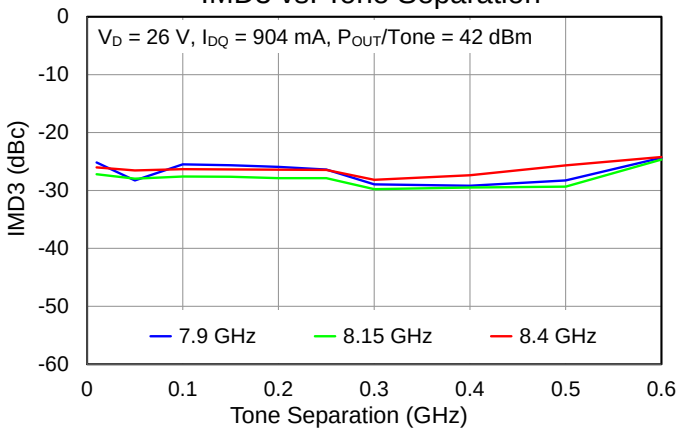
IMD3, IMD5 vs. P_{OUT}/Tone vs. I_{DQ}



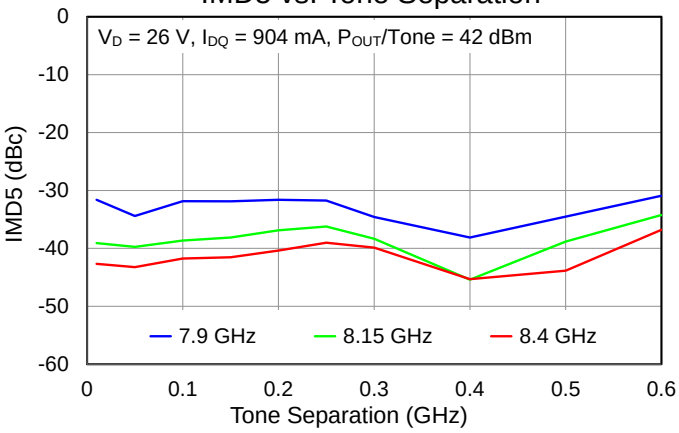
IMD3, IMD5 vs. P_{OUT}/Tone vs. I_{DQ}



IMD3 vs. Tone Separation



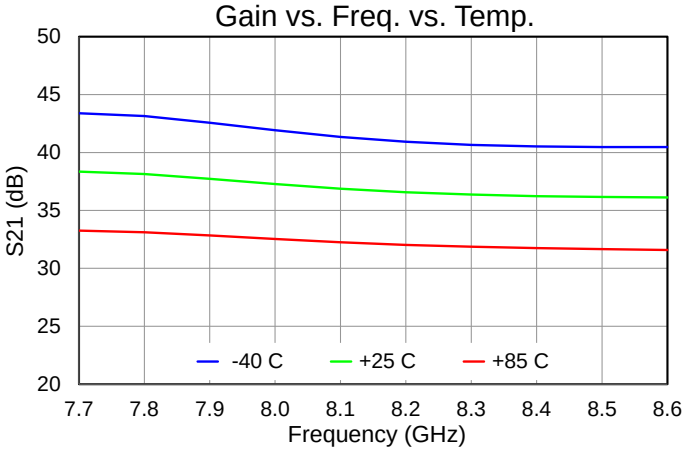
IMD5 vs. Tone Separation



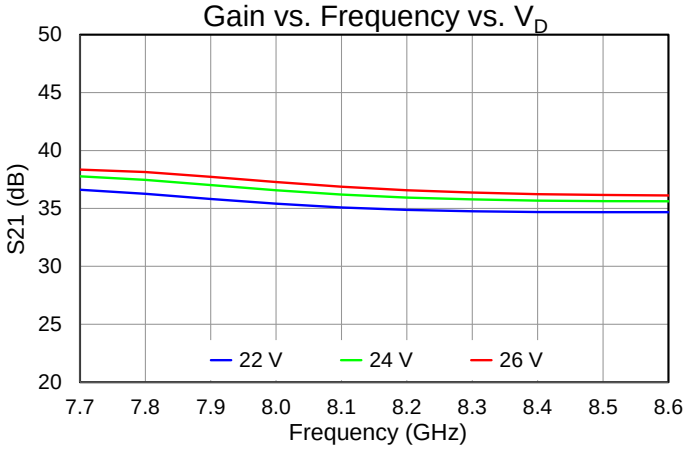
Performance Plots – Small Signal

Test conditions, unless otherwise noted: V_D = 26 V, I_{DQ} = 904 mA, T=+25 °C
All performance data presented is for the bare die

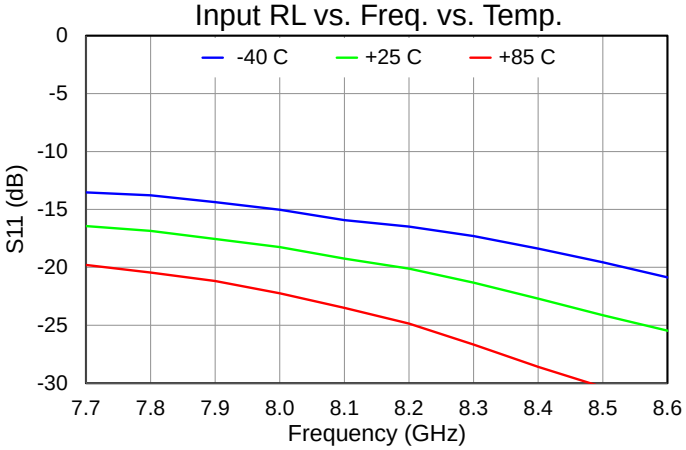
Gain vs. Freq. vs. Temp.



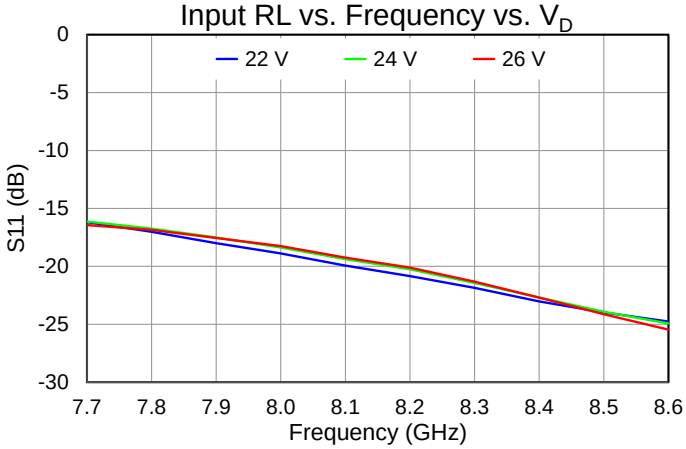
Gain vs. Frequency vs. V_D



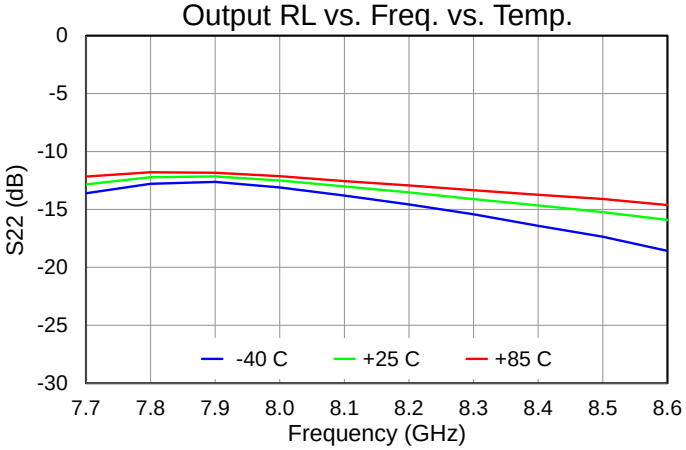
Input RL vs. Freq. vs. Temp.



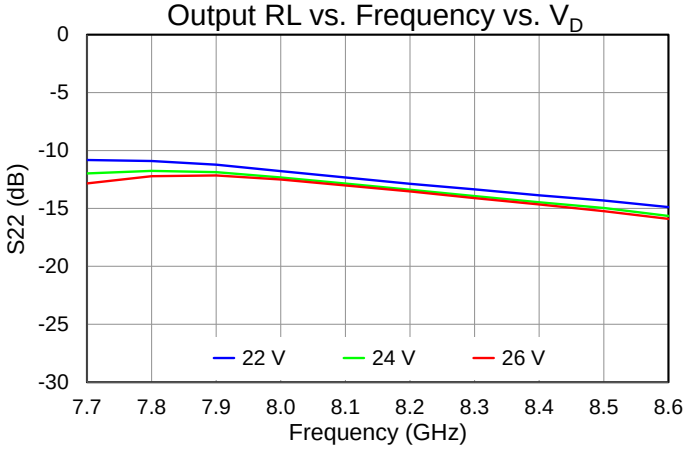
Input RL vs. Frequency vs. V_D



Output RL vs. Freq. vs. Temp.

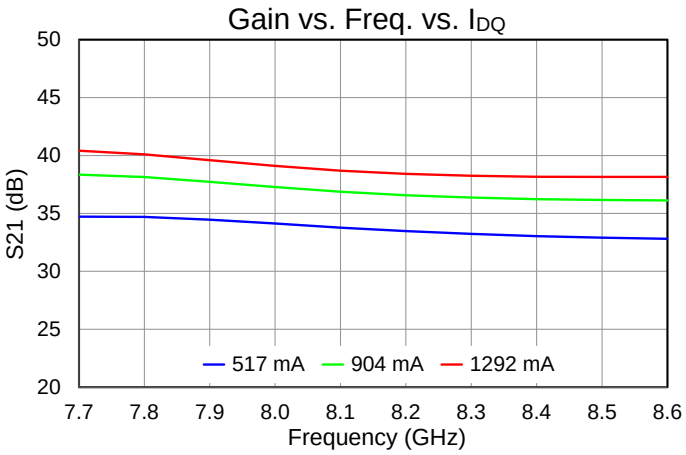


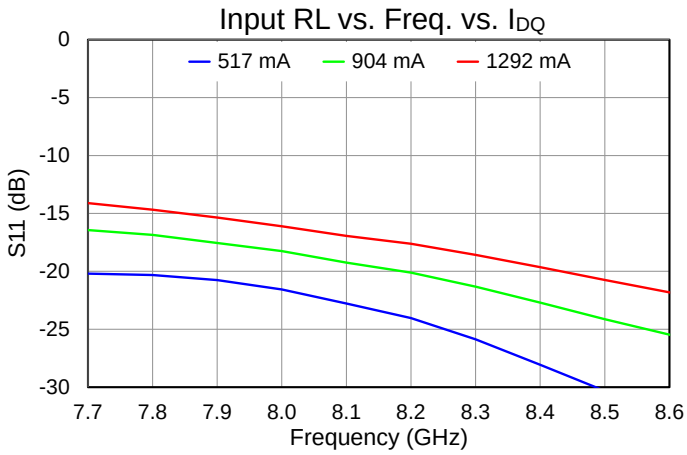
Output RL vs. Frequency vs. V_D

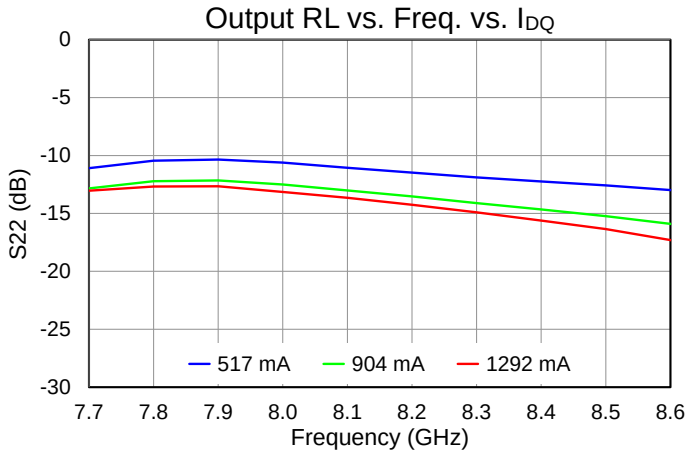


Performance Plots – Small Signal

Test conditions, unless otherwise noted: V_D = 26 V, I_{DQ} = 904 mA, T=+25 °C
All performance data presented is for the bare die





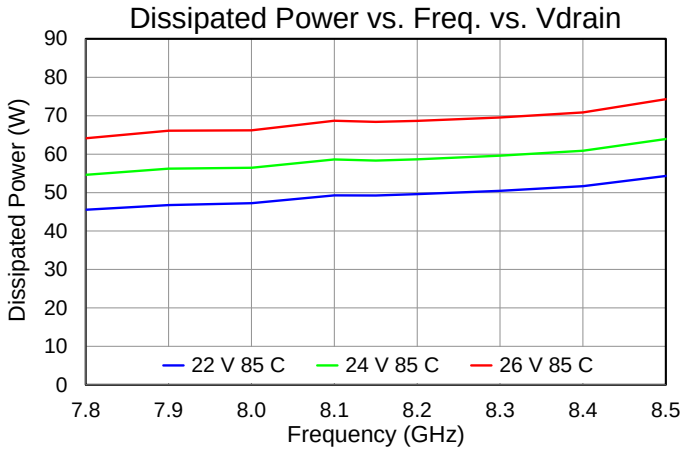


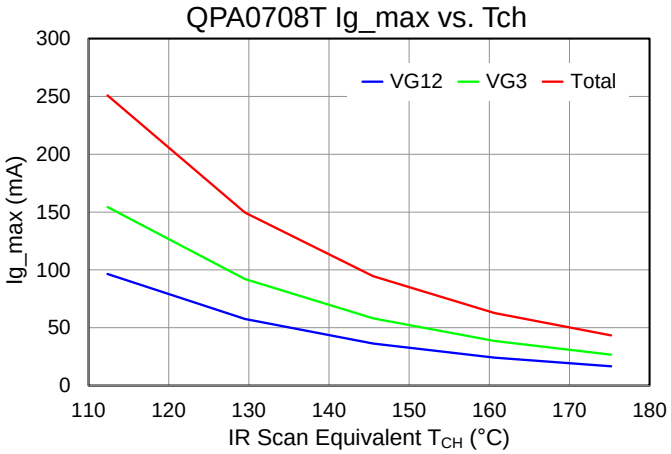
Thermal and Reliability Information

Parameter	Test Conditions	Value	Units
Thermal Resistance (θ_{JC}) (1)	T_{base} = 85 °C, V_D = 26 V, I_{DQ} = 904 mA, P_{DISS} = 23.504 W, No RF (quiescent DC operation)	0.6351	ºC/W
Channel Temperature, T_{CH} (No RF) (2)		99.93	°C
Thermal Resistance (θ_{JC}) (1)	T_{base} = 85 °C, V_D = 26 V, I_{DQ} = 940 mA, Freq = 8.4 GHz, I_{D_Drive} = 4631 mA, P_{IN} = 18 dBm, P_{OUT} = 46.96 dBm, P_{DISS} = 70.85 W	0.5699	ºC/W
Channel Temperature, T_{CH} (Under RF) (2)		125.4	°C

Notes:
1. Thermal resistance determined to the back of 20 mil CuMo carrier plate at 85 °C on die EVB
2. Data shown for bare die mounted onto 20 mil Cu-Mo carrier on the die EVB, not including the CMC tab
3. IR scan equivalent. Refer to the following document: GaN Device Channel Temperature, Thermal Resistance, and Reliability Estimates

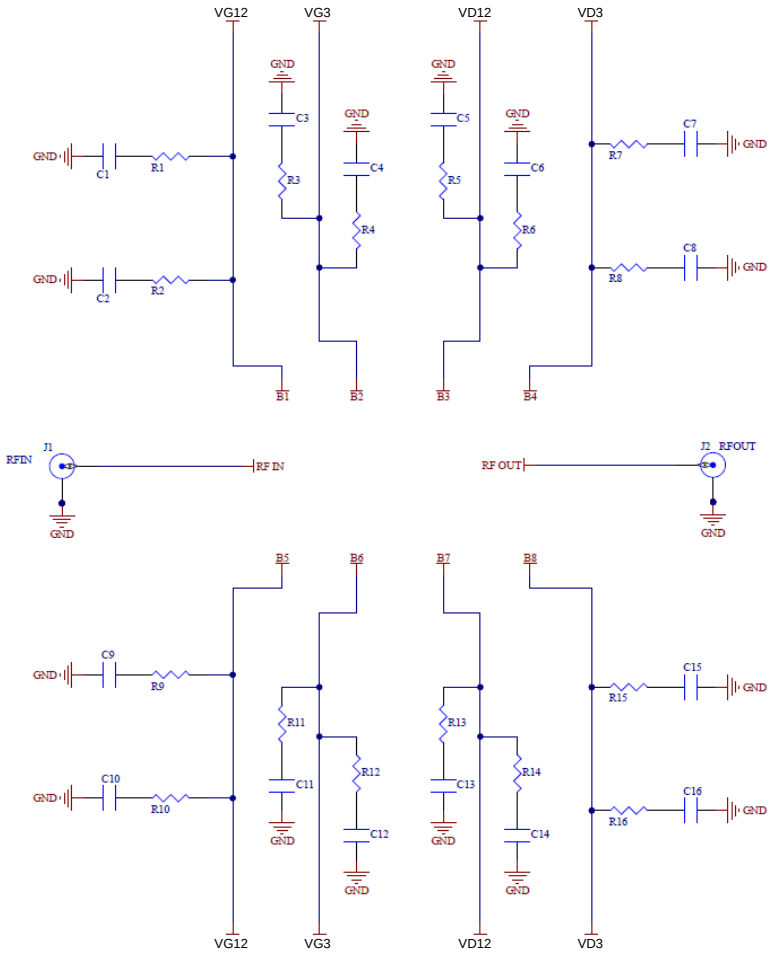
Dissipated Power and Maximum Gate Current





Test conditions, unless otherwise noted: V_D = 26 V, I_{DQ} = 904 mA, T=+85 °C, P_{IN} = 18 dBm
All performance data presented is for the bare die measured on the EVB

Applications Information



V_{G_TOP} and V_{G_BOTTOM} should be tied together (apply bias from both sides)
V_{D_TOP} and V_{D_BOTTOM} should be tied together (apply bias from both sides)
V_{G12} and V_{G3} can be separated in a customer's system, if desired, in an attempt to improve IMD performance

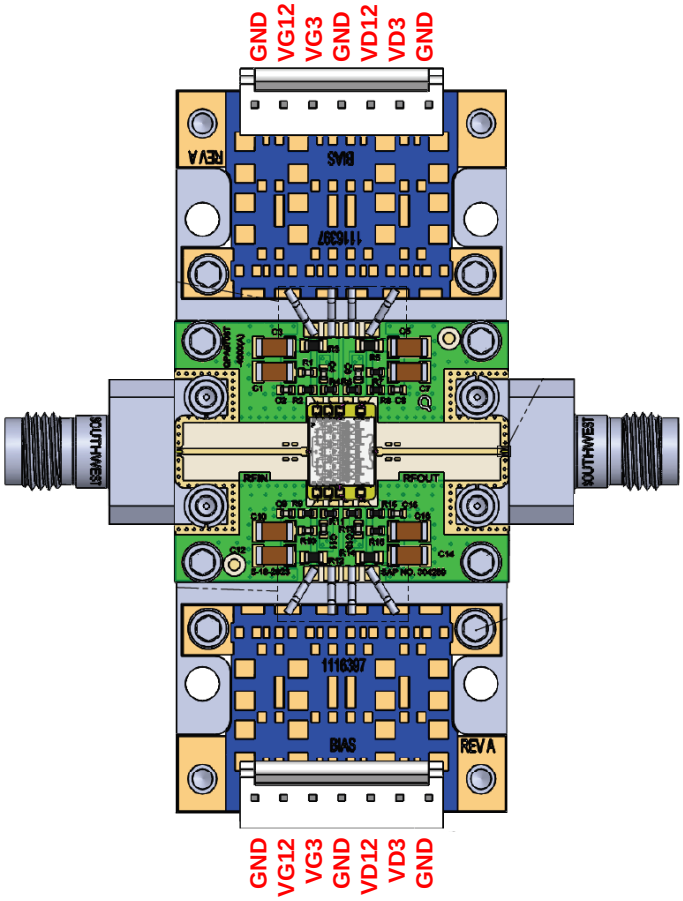
Bias-Up Procedure

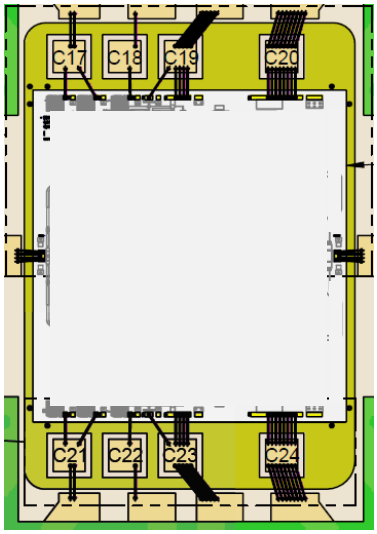
1. Set I_D limit to 7500 mA, I_G limit to 40 mA
2. Set V_G to −4.0 V
3. Set V_D +26 V
4. Adjust V_G more positive until $I_{DQ} \approx 904$ mA
5. Apply RF signal

Bias-Down Procedure

1. Turn off RF signal
2. Reduce V_G to −4.0 V. Ensure I_{DQ} ~ 0 mA
4. Set V_D to 0 V
5. Turn off V_D supply
6. Turn off V_G supply

Evaluation Board (EVB) Layout Assembly





Die and SLC mounting and bonding detail

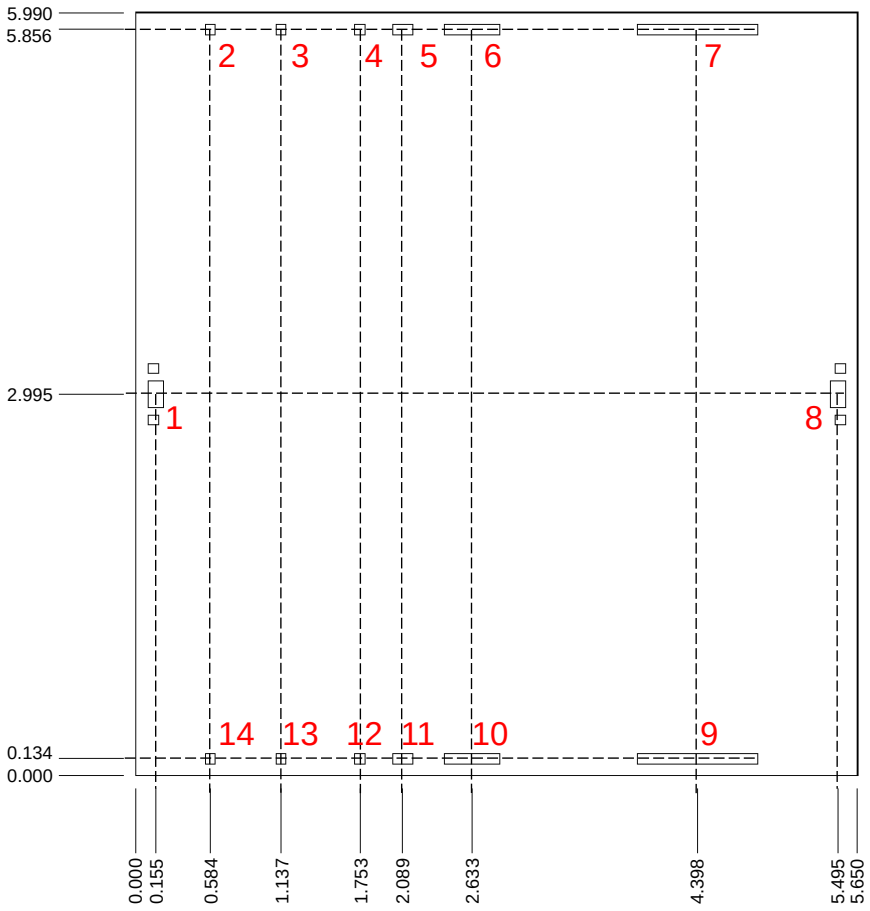
PCB is made from TACONICS RF-35HTC, 0.010 inch thick, 0.5 oz. copper both sides.
Note: EVB shown is for the bare die; there is no EVB available for the QPA0708T.

Bill of Materials

Reference Des.	Value	Description	Manuf.	Part Number
C1,C3,C5,C7,C10,C12,C14,C16	10 uF	CAP, 10uF, 20%, 50V, 20%, X5R, 1206	Various	
C2,C4,C6,C8,C9,C11,C13,C15	0.01 uF	CAP, 0.01uF, 10%, 50V, X7R, 0402	Various	
C17,C18,C19,C20,C21,C22,C23,C24	10 nF	CAP, 10nF, 15%, 30V,0303,SL Si WFR NO UV	Various	
R2,R4,R6,R7,R8,R9,R11,R13,R15,R16	0 Ω	RES, 0 OHM, JMPR, 0402	Various	
R3,R5,R12,R14	5.1 Ω	RES, 5.1 OHM, 1%, 1/10W, 0603	Various	
R1,R10	5.1 Ω	RES, 5.1 OHM, 1%, 1/10W, 0402	Various	
J1, J2		RF Connector, SMA	Southwest Microwave	292-04A-5

Note: Schematic, EVB layout, and components based on the EVB for the bare die

Mechanical Drawing and Bond Pad Description (MMIC Only)

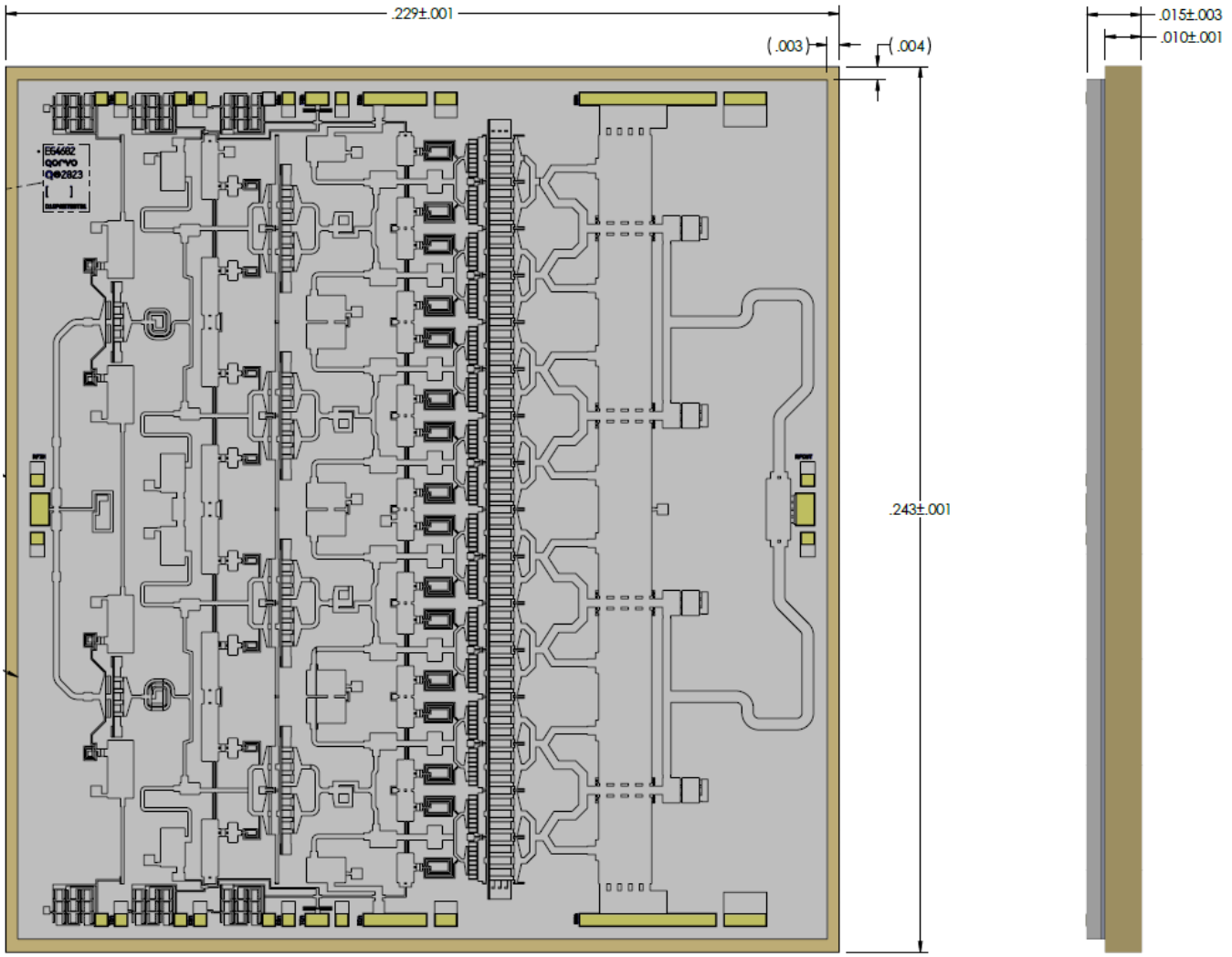


Dimensions are in mm
Thickness: 0.100
Die x, y size tolerance: ± 0.050
Ground is backside of die

Bond Pad Description

Pad No.	Symbol	Size (um x um)	Description
1	RF IN	119 x 213	RF input. 50 Ohms. DC blocked; DC grounded.
2, 14	V_{G1}	77 x 77	Gate voltage stage 1. Bypass network required; refer to page 19.
3, 13	V_{G2}	77 x 77	Gate voltage stage 2. Bypass network required; refer to page 19.
4, 12	V_{G3}	77 x 77	Gate voltage stage 3. Bypass network required; refer to page 19.
5, 11	V_{D1}	152 x 77	Drain voltage stage 1. Bypass network required; refer to page 19.
6, 10	V_{D2}	432 x 77	Drain voltage stage 2. Bypass network required; refer to page 19.
7, 9	V_{D3}	942 x 77	Drain voltage stage 3. Bypass network required; refer to page 19.
8	RF OUT	119 x 213	RF output. 50 Ohms. DC blocked.

Mechanical Drawing (Die on Tab)



Notes:

1. Dimensions are in inches
2. Thermal spreader material: Cu-Mo
3. Plating: Gold

Assembly Notes

Component placement and adhesive attachment assembly notes:

- Vacuum pencils and/or vacuum collets are the preferred method of pick up.
- Air bridges must be avoided during placement.
- The force impact is critical during auto placement.

Interconnect process assembly notes:

- Thermosonic ball bonding is the preferred interconnect technique.
- Force, time, and ultrasonic are critical parameters.
- Aluminum wire should not be used.
- Devices with small pad sizes should be bonded with 0.0007-inch wire.
- Maximum stage temperature is 200 °C.

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 1A	ANSI/ESD/JEDEC JS-001

Caution!

ESD-Sensitive Device

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_40_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com

Tel: 1-844-890-8163

Email: customer.support@qorvo.com

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