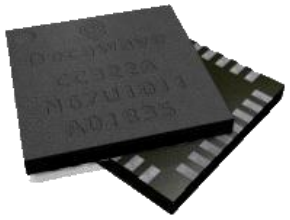
DW3300Q

ULTRA WIDEBAND (UWB) LOW-POWER TRANSCEIVER

Datasheet

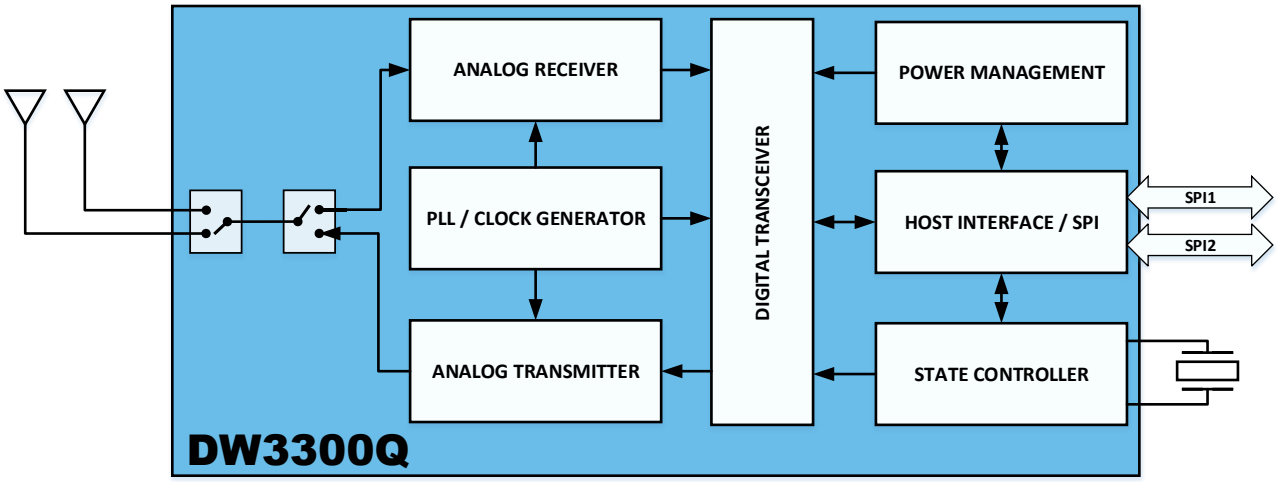
Product Overview

The DW3300Q is a fully integrated single chip Ultra-Wideband (UWB) low-power low-cost transceiver IC compliant to IEEE Std 802.15.4™-2020 and IEEE Std 802.15.4z™-2020 (BPRF mode) for automotive applications. It can be used in SS-TWR, DS-TWR, TDoA and PDoA systems to locate assets to an accuracy of 10 cm.



- Provides precision location and data transfer simultaneously
- Asset location to an accuracy of 10 cm
- High multipath fading immunity
- Secure ranging/distance measurement using STS (Scrambled-Timestamp)
- Supports high tag densities in real time location systems (RTLS)
- Low-cost precision location
- Suitable for coin cell applications
- Designed for automotive applications such as:
  - Precision Real Time Location Systems (RTLS) using SS-TWR, DS-TWR, TDoA or PDoA schemes in Automotive Applications
  - Presence Detection for Secure Entry and Secure Payment
  - Child/Passenger presence Detection, Occupancy Sensing
  - Parking Spot Detection and Positioning for Electrical Vehicle Wireless Charging as an example
  - Location aware Wireless sensor Networks
  - Car Connectivity Consortium Vehicle Access
  - FiRa Consortium Use Cases: Smart Cities and Mobility (Parking Garages, V2X, Ticket Validation, etc.)

1 Functional Block Diagram



2 Key Features

- Qualified to AEC-Q100 grade 2 (-40 to 105 C)
- IEEE Std 802.15.4™-2020 (Revision of IEEE Std 802.15.4-2015) UWB
- IEEE Std 802.15.4z™-2020 (Amendment to IEEE Std 802.15.4™-2020) (BPRF mode)
- Supports secure Time-of-Flight using STS
- Supports channels 5 & 9 (6489.6 MHz & 7987.2 MHz)
- Supports Single-Sided and Double-Sided Two-way Ranging (SS and DS TWR), Time Difference of Arrival (TDoA) and Phase Difference of Arrival (PDoA) location schemes
- Car Connectivity Consortium specification conform: Double Sided (DS) TWR
- Low external component count
- Supports enhanced security modes: payload encryption/decryption
- Integrated HW AES 256
- Worldwide UWB Radio Regulatory compliance
- Low power consumption
- Data rates of 850 Kbps and 6.8 Mbps
- Packet length from zero to 1023 bytes
- Integrated MAC support features
- Primary SPI interface to any automotive host MCU as a BLE SoC for CCC requirements: Supports rates up to 32 MHz
- Second SPI interface available for automotive applications requiring connection to another MCU: Supports rates up to 16 MHz
- Fast 20nS TX to RX internal RF switching speed

3 Ordering Information

Table 1: Ordering and Packaging Information

Part Number	Description	Packaging	Unit Quantity (Number of ICs)
DW3300QTR13	40 PIN LGA	13” Tape and Reel	2500
DW3300QSR		Sample Reel	100
DW3300QEVB	Customer EVB	EVB	1
DW3300QDK1	Anchor Kit includes EVB, Nucleo F429ZI , Ch5 Dual Antenna, Ch9 Dual Antenna, Stand	KIT	1
DW3300QDK2	Tag Kit includes EVB, Nucleo F429ZI , Ch5 Antenna, Ch9 Antenna, Stand	KIT	1
DW3300QDK3	Nearby Interaction Kit includes EVB, Nordic nRF52840, Ch5 Dual Antenna, Ch9 Dual Antenna, Stand	KIT	1

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4 IC Description

The DW3300Q is a fully integrated low-power, single chip CMOS RF 6.5GHz-8GHz IR-UWB transceiver IC compliant with the IEEE Std 802.15.4™-2020 (HRP UWB PHY), IEEE Std 802.15.4z™-2020 and IEEE 802.15.8 standards. It consists of an analog front end containing a receiver and a transmitter and a digital back end that interfaces to an off-chip host processor. A TX/RX switch is used to connect the receiver or transmitter to the antenna port. Temperature and voltage monitors are provided on-chip.

The receiver consists of an RF front end which amplifies the received signal in a low-noise amplifier before down-converting it directly to baseband. The receiver is optimized for wide bandwidth, high linearity, and low noise figure. This allows each of the supported IEEE Std 802.15.4™-2020 UWB channels to be down converted with minimum additional noise and distortion. The baseband signal is demodulated, and the resulting received data is made available to the host controller via SPI.

The transmit pulse train is generated by applying digitally encoded transmit data to the analog pulse generator. The pulse train is up-converted to a carrier generated by the synthesizer and centered on one of the permitted IEEE Std 802.15.4™-2020 UWB channels. The modulated RF waveform is amplified before transmission from the external antenna.

The Time-of-flight processing (Leading Edge and diagnostics block) analyses the preamble sequences both in the receiver and the transmitter and establishes the exact time of arrival of the signals to within < 100ps. The time-stamp generation and processing allow the devices then to provide the distance measurements to the user with minimal external effort.

The two RF antenna ports are used for Phase Difference of Arrival (PDoA) applications. The receiver switches between antenna ports to enable a PDoA measurement.

The IC has an on-chip One-Time Programmable (OTP) memory. This memory can be used to store calibration data such as TX power level and crystal initial frequency error adjustment. These adjustment values can be automatically retrieved when needed.

The IC includes a 20kHz oscillator for controlling wake cycles and system timing. The precision RF oscillator is used to derive the precise time-base of the device as well as being the reference for the RF transmissions.

A second SPI interface (SPI2) is available for cases where multiple hosts require time-interleaved access to the DW3300Q. This interface has enhanced security so that each SPI interface can work with the knowledge that the other interface will not have access to any of its data or settings. This interface is fully arbitrated for safe, conflict free operation.

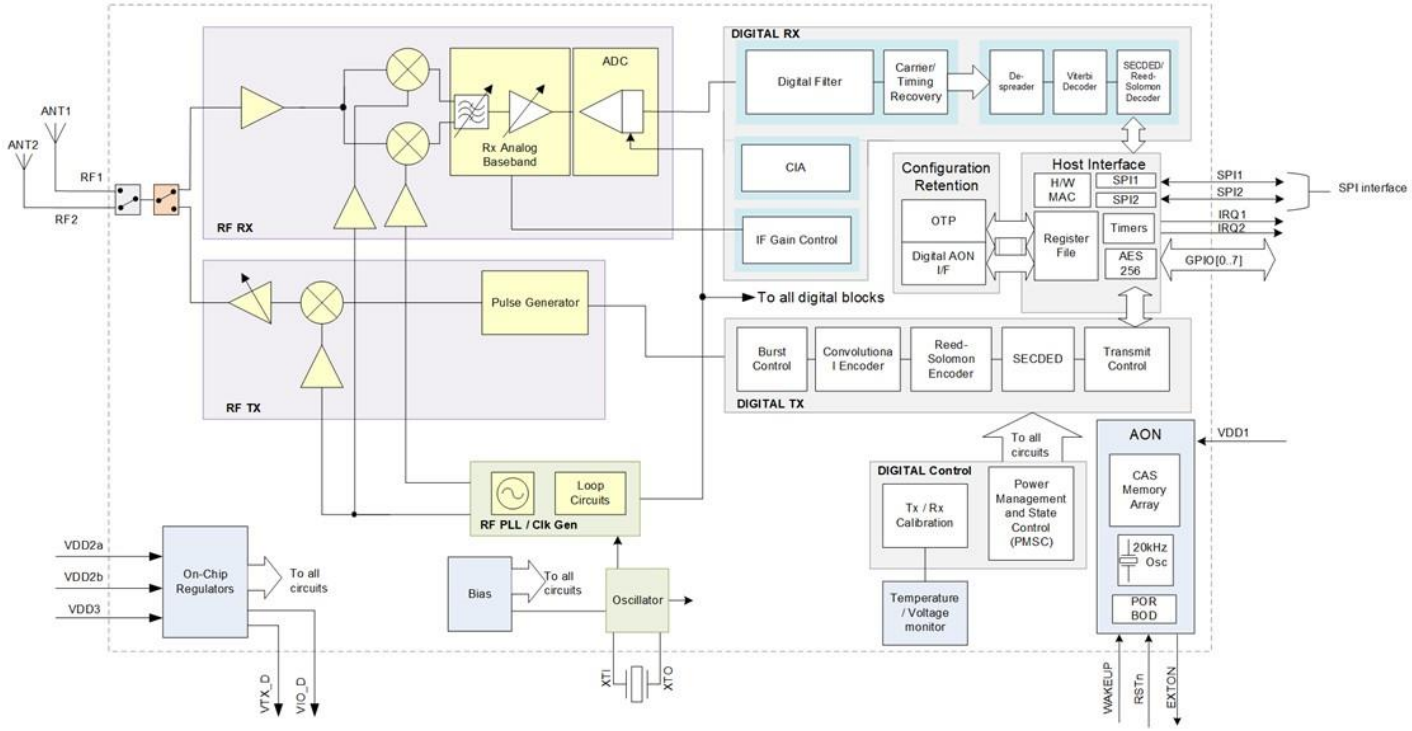


Figure 1: Block Diagram

The Always-On (AON) memory is 256 bytes and can be used to retain DW3300Q configuration data during the lowest power operational states. The AON can operate directly from battery. This data is downloaded during crystal start up automatically.

The DW3300Q contains a phase-locked-loop (PLL) with integrated loop filters. This PLL provides the RF local oscillator signals for the Rx Mixer and the Tx RF frequency carrier to the Tx mixer. The channel information signal defines the output channel frequency as follows; channel 5 = 6489.6 MHz, channel 9 = 7987.2 MHz

The DW3300Q has various debug and test options (RF loopback, event counters. test modes and more) and gives access to internal signals for on-the-bench debugging and to simplify production tests.

The DW3300Q incorporates Time Stamp system security features to prevent all known hacking type attacks such as ‘imposter’, ‘cicada’, ‘parasite’ ‘record & replay’ attacks etc. MAC features implemented include CRC generation, CRC checking and receive frame filtering.

4.1 DW3300Q Backward Compatibility with DW1000

DW3300Q is backward compatible with DW1000 on channel 5 and for data rates of 6.8 Mbps and 850 kbps. It is also compatible fully with the DW3000 products line, Mobile and IoT Chipsets.

4.2 Pin Configuration and Function Description

The DW3300Q IC is supplied in a 40 PIN LGA package. The pin assignments for package are illustrated in Figure 2 and the description is given in the Table 2 below.

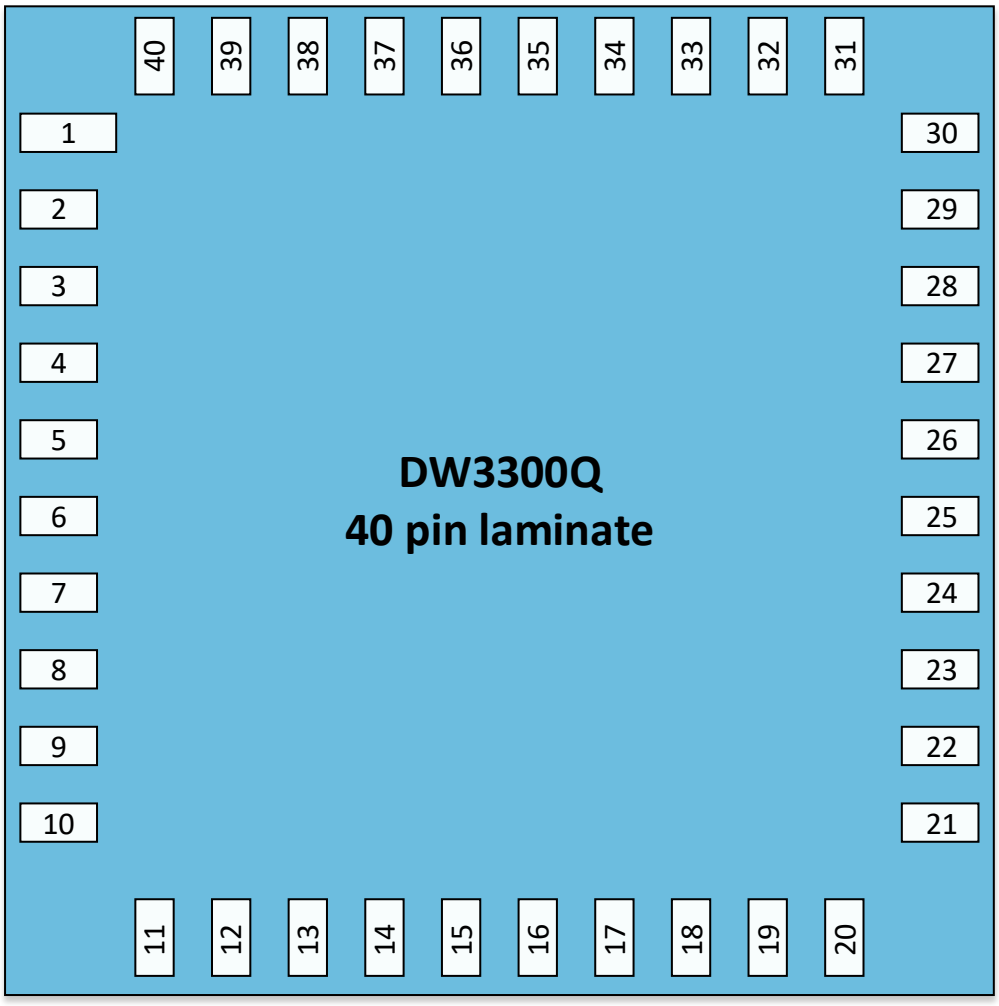


Figure 2: The 40 PIN LGA Top View Pin Assignments

Table 2: DW3300Q LGA Pin Functions

LGA Pin #	Signal Name	I/O Type (default)	Description
1	IRQ/GPIO8	DIO (O-L)	Interrupt Request output from the DW3300Q to the host processor. By default, IRQ is an active-high output but may be configured to be active-low if required. For correct operation in SLEEP and DEEPSLEEP modes, it should be configured for active-high operation. This pin will float in SLEEP and DEEPSLEEP states and may cause spurious interrupts unless pulled low. When the IRQ functionality is not being used the pin may be reconfigured as a general purpose I/O line, GPIO8.
2	GPIO6 / EXTRXE /	DIO (I)	General purpose I/O pin. After power-up, the pin will default to a General Purpose I/O pin. It may be configured for use as EXTRXE (External Receiver Enable). This pin goes high when the DW3300Q is in receive mode.
3	SPI2CLK	DI	SPI2 slave clock input
4	SPI2MISO	D0 (O-L)	SPI2 slave data output
5	GPIO5 / EXTTXE /	DIO (I)	General purpose I/O pin. It may be configured for use as EXTTXE (External Transmit Enable). This pin goes high when the DW3300Q is in transmit mode. After power-up, the pin will default to a General Purpose I/O pin.
6	IRQ2	DIO (I)	Interrupt signal for the 2nd SPI interface.
7	SPI2MOSI	DI	SPI2 Slave Data input
8	GPIO4/ EXTPA	DIO (I)	General purpose I/O pin. It may be configured for use as EXTPA (External Power Amplifier). This pin can enable an external Power Amplifier.
9	GPIO7/ SYNC	DIO (I)	The SYNC input pin is used for external synchronization. When the SYNC input functionality is not being used this pin may be reconfigured as a general purpose I/O pin, GPIO7.
10 11 12	GND	G	RF ground pin [1].
13	RF2	AIO	RF port for antenna 2 (50 Ω single-ended RF connection). When in use for PDoA, a 2 pF is required on the pin. In non PDoA chip variants, no 2 pF is required, but it should be grounded with 50 Ω.
14 15 16 17	GND	G	RF ground pin [1].
18	RF1	AIO	RF port for antenna 1 (50 Ω single ended connection). A 2pF is required on the pin.
19, 20	GND	G	RF ground pin [1].

LGA Pin #	Signal Name	I/O Type (default)	Description
21	XTI	AI	Reference crystal input or external reference overdrive pin.
22	XTO	AI	Reference crystal output.
23	VDD2b	P	Voltage Supply (2.4V to 3.6V) [1]. 23 requires isolation with a ferrite from 28.
24	VSS2	G	Ground return for VDD2.
25	VSS3	G	Ground return for VDD3.
26	VDD3	P	Voltage Supply (1.5V to 3.6V) [1].
27	VTX_D	PD	TX supply decoupling. Requires external capacitor to ground [1].
28	VDD2a	P	Voltage Supply (2.4V to 3.6V) [1]. 28 requires isolation with a ferrite from 23.
29	VDD1	P	Main power supply (1.62V – 3.6V). Should be Always ON [1]. The following I/Os are supplied by this pin: SPI2CS/WAKEUP, EXTON, RSTn, SPICLK, SPICSn, SPIMISO and SPIMOSI.
30	VSS1	G	Ground return for VDD1, also PSUB connection.
31	EXTON	DO (O-L)	External devices enable. Asserted during wake-up process and held active until device enters sleep mode. Can be used to control external DC-DC converters or other circuits that are not required when the device is in sleep mode to minimise power consumption.
32	SPI2CS/ WAKEUP	DI	Active-high SPI2 chip selects. If SPI2 is not being used then this pin will also function as a wakeup pin so that when asserted into its active-high state, the WAKEUP pin brings the DW3300Q out of SLEEP or DEEPSLEEP states into operational mode. This should be connected to ground if not used.
33	RSTn	DIO (O-H)	Reset pin. Active Low Output. May be pulled low by external open drain driver to reset the DW3300Q. Must not be pulled high by external source.
34	SPICLK	DI	Primary SPI slave clock input [2].
35	SPICDI (SPIMOSI)	DI	Primary SPI slave data input [2].
36	SPICDO (SPIMISO)	D0 (O-L)	Primary SPI slave data output [2].
37	SPICSn	DI	Primary SPI chip selects [2]. This is an active low enable input. The high-to-low transition on SPICSn signals the start of a new SPI transaction. SPICSn can also act as a wake-up signal to bring DW3300Q out of either SLEEP or DEEPSLEEP states.
38	VIO_D	PD	IO supply decoupling. Internally connected to the VDD1 with switch to allow disconnect from VDD1 for ultra-low power consumption mode.
39 40	VSS	G	Ground return for internal digital supply [1].

[1] Reference to the schematics and the layout.

[2] DW3300Q IC's will power up with full SPI access and interrupts on the primary SPI interface without the use of SPI2. To enable interrupts on the 2nd SPI interface (SPI2), the DUAL_SPI_INT_EN bit must be set. This can be set by either SPI master as it will only enable the interrupt vectoring to the 2nd SPI port, not the 2nd SPI port itself. This bit will be preserved and should be programmed as early as possible.

Table 3: Abbreviations

Abbreviation	Description
AI	Analog Input.
AIO	Analog Input / Output.
AO	Analog Output.
DI	Digital Input.
DIO	Digital Input / Output.
DO	Digital Output.
G	Ground.
P	Power Supply.
PD	Power Decoupling.
NC	No Connect.
O-L	Defaults to output, low level after reset.
O-H	Defaults to output, high level after reset.
I	Defaults to input.
Note: Any signal with the suffix 'n' indicates an active low signal.	

4.3 Off Chip Controls: Multi-functional IO

The following digital input-output signals can be configured in multiple modes as shown below.

Table 4: I/O Mode Mapping

I/O name	Mode 1	I/O type	Mode 2	I/O type	Mode 3	I/O type
IRQ	IRQ	DO	GPIO8	DIO	ext_ref	DO
SYNC	SYNC	DI	GPIO7	DIO	aoa_sw_3	DO
GPIO6	GPIO6	DIO	ext_sw_rx	DO	aoa_sw_2	DO
GPIO5	GPIO5	DIO	coex_out	DO	aoa_sw_1	DO
GPIO4	GPIO4	DIO	coex_in	DI	aoa_sw_0	DO
SPI2MOSI	SPI2MOSI	DI	led_3	DO	GPIO3	DIO
IRQ2	IRQ2	DO	led_2	DO	GPIO2	DIO
SPI2MISO	SPI2MISO	DIO	led_1	DO	GPIO1	DIO
SPI2CLK	SPI2CLK	DI	led_0	DO	GPIO0	DIO

Note that coex_out and coex_in can swap pins via register settings. Further details on configuring IO modes and their uses can be found in the DW3300Q User Manual.

Table 5: MFIO Special Mode Descriptions

MFIO	Description
coex_in	Input used to abort any ongoing TX or RX RF operations. Can be SW configured for “TX,RX,both”. This will trigger a coex_err interrupt flag to current granted host.
coex_out	Output flag that can configured via SW to indicate “RX, TX or either operation” are under way. Turn on time before active window is TBC.
aoa_sw_0	TX Switch enable, stays on during TX frame, turns on approx. 10us before TX
aoa_sw_1	Like ext_sw_rx but turns on 100ns before the start of RX.
aoa_sw_2	Ant1 en control. Used for AoA switching (within a frame)
aoa_sw_3	Ant2 en control. Used for AoA switching (within a frame)
GPIO [7:4]	GPIO [7:4] can also be bit banged under host (AP, MCU) control for antenna diversity control

Note: The AoA switch has a 1us window in which it should switch from one antenna to the other, any longer than this and we will be reducing the effective length of the STS.

5 Electrical Characteristics

5.1 Nominal Operating Conditions

Table 6: Nominal Operating Conditions

Parameter	Min.	Typ.	Max.	Units	Condition/Note
Operating temperature	-40		105	˚C	
Storage temperature	-65		150	˚C	
Supply voltage VDD1	1.62	3.0	3.6	V	
Supply voltage VDD2a and VDD2b	2.4	3.0	3.6	V	
Supply voltage VDD3	1.5	3.0	3.6	V	
Voltage on GPIO0-5, WAKEUP, RSTn, SPICSn, SPIMOSI, SPICLK, SPI2CSn, SPI2MOSI, SPI2CLK			3.6	V	Note that 3.6 V is the max voltage that should be applied to these pins.

Note: Unit operation is guaranteed by design when operating within these ranges. Sufficient headroom for any power supply voltage ripple should be considered in system designs.

5.2 DC Characteristics

T_{amb} = 25 ˚C, all supplies at 3.0V unless otherwise stated.

Table 7: DC Characteristics

Parameter	Min.	Typ.	Max.	Units	Condition/Note
Supply current DEEP SLEEP mode		210		nA	
Supply current SLEEP mode		810			
Supply current IDLE_PLL mode		16		mA	
Supply current IDLE_RC mode		6			
Supply current INIT mode		4			
Current single frame Tx/Rx with 47uF capacitor					
TX CH5		14		mA	Refer to section “Powering DW3300Q” for details of single TX frame configuration.
TX CH9		17			
RX CH5		16			Refer to section “Powering DW3300Q” for details of single RX frame configuration.
RX CH9		19			
Peak current continuous Tx/Rx over Temperature and Voltage					
TX CH5 (nominal power -41.3 dBm/MHz)		40		mA	Continuous TX only used as test mode. In typical operation TX is powered up for frame transmission then powered down
TX CH5 (max power -32.3 dBm/MHz)		52	70		
TX CH9 (nominal power -41.3 dBm/MHz)		50			
TX CH9 (max power -32.3 dBm/MHz)		63	86		
RX CH5		71	104		
RX CH9		86	119		

Parameter	Min.	Typ.	Max.	Units	Condition/Note
Digital input voltage high	0.7 * VDD1			V	
Digital input voltage low			0.3 * VDD1		
Digital output voltage high	0.7 * VDD1				Assumes 500 Ω load.
Digital output voltage low			0.3 * VDD1		Assumes 500 Ω load.
Digital output drive current					
GPIOx, IRQ	4	6		mA	
SPIMISO	8	10			
EXTON	3	4			

5.3 Receiver AC Characteristics

T_{amb} = 25 ˚C, all supplies at 3.0V unless otherwise stated.

Table 8: Receiver AC Characteristics

Parameter	Min.	Typ.	Max.	Units	Condition / Note
Center Frequency - Channel 5		6489.6		MHz	
Center Frequency - Channel 9		7987.2		MHz	
Channel bandwidth		499.2		MHz	Programmable.
Input P1dB compression point Channel 5		-25.4		dBm	
Input P1dB compression point. Channel 9		-27.1		dBm	
In-band blocking level		-84.3		dBm	Chip-referred (power at the pin) to give 1% PER with 3 dB desense.
Out-of-band blocking level		-18.3		dBm	Chip-referred (power at the pin) to give 1% PER with 3 dB desense (see Receiver Blocking).

5.4 Receiver Sensitivity Characteristics

Tamb = 25 ˚C, all supplies at 3.0V. 20-byte payload. Carrier frequency offset ±10 ppm. Measurement: Power level set to a nominal level @-10dBm; an attenuator is switched to reduce the power level to the device input; the power is measured after the attenuator; level set to limit where 1% PER (Packet Error Rate) is reached. Sensitivity is measured at the device pin with EVB trace loss de-embedded.

Table 9: Rx Sensitivity Characteristics (Channel 5)

Typical Receiver Sensitivity (dBm)	BPRF Mode	Data Rate	Preamble length (symbols)	STS length (symbols)	Description	Conditions
-92	BPRF1	6.8 Mbps	64	0	SP0	Measured at IC input
-92	BPRF2	6.8 Mbps	64	0	SP0	
-92	BPRF3	6.8 Mbps	64	64	SP1	
-98	BPRF4	No Data Mode	64	64	SP3	

Table 10: Rx Sensitivity Characteristics (Channel 9)

Typical Receiver Sensitivity (dBm)	BPRF Mode	Data Rate	Preamble length (symbols)	STS length (symbols)	Description	Conditions
-90	BPRF1	6.8 Mbps	64	0	SP0	Measured at IC input
-90	BPRF2	6.8 Mbps	64	0	SP0	
-90	BPRF3	6.8 Mbps	64	64	SP1	
-96	BPRF4	No Data Mode	64	64	SP3	

5.5 Reference Clock AC Characteristics

T_{amb} = 25 ˚C, all supplies at 3.0V

Table 11: Reference Clock AC Characteristics

Parameter	Min.	Typ.	Max.	Units	Condition / Note
Crystal oscillator reference frequency		38.4		MHz	A 38.4 MHz signal can be provided from an external reference in place of a crystal if desired.
Crystal specifications					
Load capacitance	0		35	pF	Depends on crystal used and PCB parasitic.
Shunt capacitance	0		4	pF	
Drive level			200	µW	Depends on crystal & load capacitance used.
Equivalent Series Resistance (ESR)			60	Ω	
Frequency tolerance			±20	ppm	DW3300Q includes circuitry to trim the crystal oscillator to reduce the initial frequency offset.
Crystal trimming range	-20		+20	ppm	Trimming range provided by on-chip circuitry. Depends on the crystal used and PCB design.

External Reference (For example a TCXO)

Amplitude	0.8		VDD2	Vpp	Must be AC coupled. A coupling capacitor value of 2200 pF is recommended.
SSB phase noise power density			-132	dBc / Hz	@1 kHz offset.
SSB phase noise power density			-145	dBc / Hz	@10 kHz offset.
Duty Cycle	40		60	%	Duty Cycle
Fast and Slow Oscillators					
Slow RC Oscillator	9	23	30	kHz	User programmable*. Minimum at VDD1=1.62 V, Maximum at VDD1=3.6 V
Fast RC Oscillator	105	115	130	MHz	Internally calibrated. Minimum at -40°C, maximum at +105°C

**Note: Chip start-up time depends on this clock. The typical frequency of the Slow RC oscillator is reflected in the chip start-up time of 913 us. With the time, required to download the AON after wake-up, the overall start-up time is ~1000 us. It is possible to trim the oscillator to the higher frequency in software, which would decrease the start-up time to ~770 us.*

5.6 Transmitter AC Characteristics

T_{amb} = 25 ˚C, all supplies at 3.0V

Table 12: Transmitter AC Characteristics

Parameter	Min.	Typ.	Max.	Units	Condition / Note
Center Frequency Channel 5		6489.6		MHz	
Center Frequency - Channel 9		7987.2		MHz	
Channel bandwidth		499.2		MHz	Programmable.
Maximum Output power spectral density Channel 5 (programmable)		-32		dBm / MHz	
Maximum Output power spectral density Channel 9 (programmable)		-33.5			
Max Output channel power Channel 5		-7		dBm / 500MHz	
Max Output channel power Channel 9		-8.4			
Load impedance		50		Ω	Single ended
Power level range		30		dB	See Transmit Power Adjustment
Output power variation with temperature		0.008		dB / °C	
Output power variation with voltage		0		dB / V	Internally regulated
Transmit bandwidth variation with temperature		0.2		MHz / °C	With internal calibration enabled

5.7 Link Budget

Using the receiver sensitivity above, expected transmission link budgets can be estimated with the following assumptions:

1. Receiver sensitivities as per Table below.
2. Transmitter and receiver antennas have 0 dBi gain.
3. No losses between the antenna and DW3300Q RF pins.
4. The transmitter is operating at an EIRP of -41.3 dBm/MHz (widely used regulatory limit).

Table 13: Typical Link Budget for DW3300Q

Typical Link Budget (dB)		Data Rate	Preamble length (symbols)	STS length (symbols)	Condition / Note
CH5	CH9				
87	83.5	6.8 Mbps	64	64	With 12 bytes data → max gating gain.
92	88.5		64	64	No data mode → max gating gain.

5.8 Temperature and Voltage Monitor Characteristics

Table 14: Temperature and Voltage Monitor Characteristics

Parameter	Min.	Typ.	Max.	Units	Condition / Note
Voltage Monitor Range*	1.62		3.6	V	
Voltage Monitor Accuracy		5		%	
Temperature Monitor Range	-40		105	°C	
Temperature Monitor Accuracy	-3		3	°C	

5.9 Location Functionality Characteristics

Table 15: Location Accuracy Characteristics

Parameter	Min.	Typ.	Max.	Units	Condition / Note
Ranging accuracy*	-6		6	cm	BPRF3 packet. In line-of-sight conditions.
Ranging standard deviation		3		cm	
PDoA accuracy[2]	-12.5		12.5	deg	Measured over +/- 180 degrees PDoA
PDoA standard deviation		5		deg	
Equivalent AoA Accuracy[2]	-6.25		6.25	deg	Measured over +/- 90 degrees AoA
Equivalent AoA Standard Deviation[2]		2.5		deg	

**After calibration is applied.*
2 Note: in a typical PDoA based system the computed angle of arrival (AoA) accuracy is better than the PDoA accuracy by a factor of approximately two i.e., if PDoA accuracy is ±12.5° then AoA accuracy is ±6.25°.

5.10 Absolute Maximum Rating

Table 16: Absolute Maximum Ratings

Parameter	Min.	Max.	Units
Supply voltage	-0.3	4.0	V
Receiver power		14	dBm
Storage Temperature	-65	+150	˚C
Operating Ambient Temperature	-40	+105	˚C
MSL (Moisture sensitivity level) for LGA packages JEDEC-JSTD-020 spec	MSL3		level
ESD (Human Body Model)	Class 2, 2000V		
ESD (Charged Device Model)	Class C3, 1000V		

5.11 Front-End Characteristics

T_{amb} = 25 ˚C, all supplies at 3.0V unless otherwise stated.

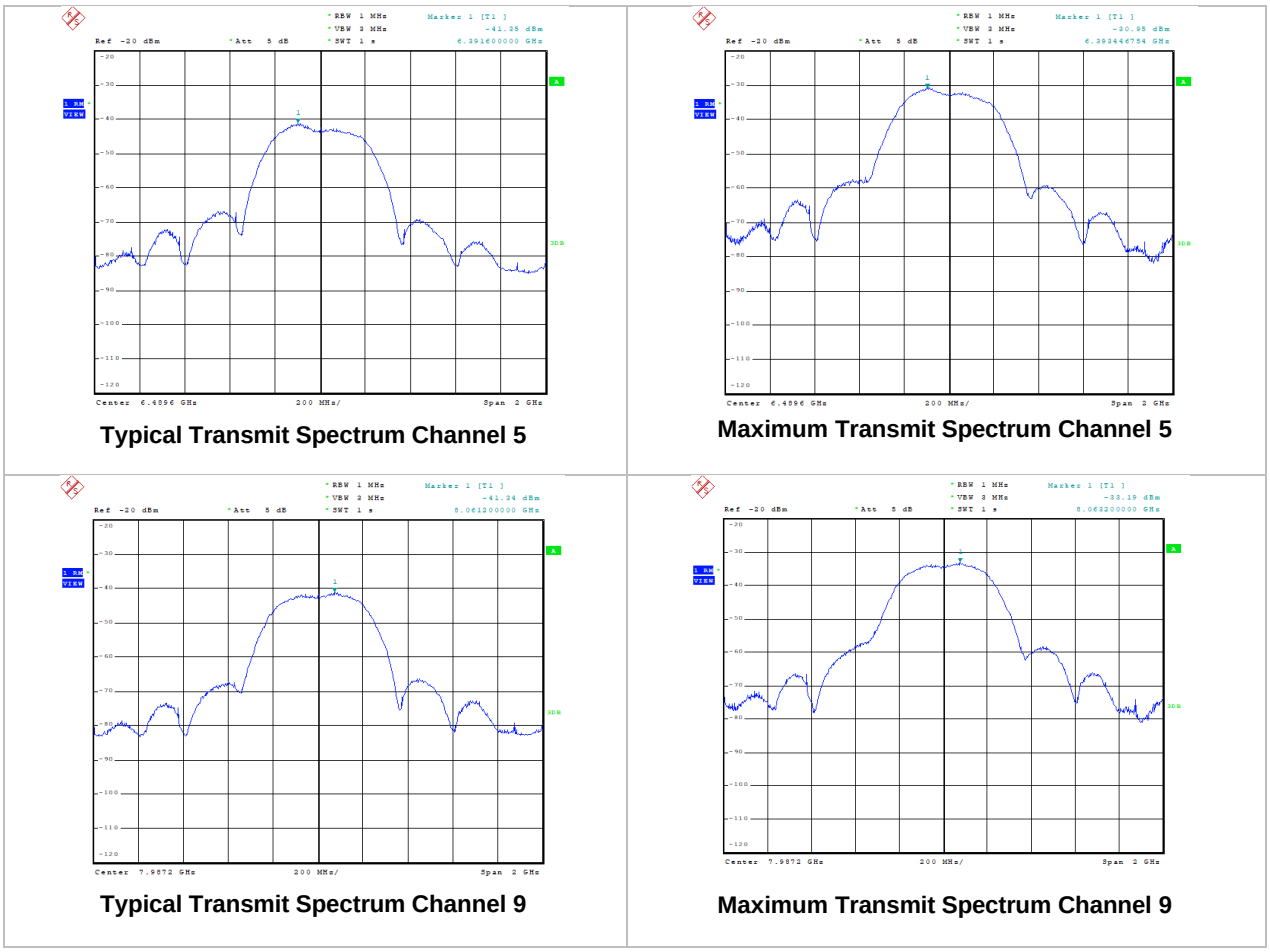
Table 17: Front-End Switch Characteristics

Parameter	Min.	Typ.	Max.	Units	Condition / Note
Switching Speed, RF1-RF2		20		nS	
Antenna Switch Isolation, RF1-RF2	20	27.5		dB	Channel 5; RF1 Active, Iso from RF2
Antenna Switch Isolation, RF2-RF1	10.5	16.5		dB	Channel 5; RF2 Active, Iso from RF1
Antenna Switch Isolation, RF1-RF2	6.5	12.5		dB	Channel 9; RF1 Active, Iso from RF2
Antenna Switch Isolation, RF2-RF1	12	22		dB	Channel 9; RF2 Active, Iso from RF1

5.12 Typical Performance

5.12.1 Transmit Spectrum

The typical transmit spectrums for channel 5 and channel 9 are in the pictures below.



Typical Transmit Spectrum Channel 5

Maximum Transmit Spectrum Channel 5

Typical Transmit Spectrum Channel 9

Maximum Transmit Spectrum Channel 9

Figure 3: Typical Transmit Spectrum

5.12.2 Transmit Power Adjustment

DW3300Q has a coarse TX power adjustment and a fine TX power adjustment. The plots below show the relationship between these adjustments for each channel. The y-axis, Power(dB), is the output power in dB below the maximum.

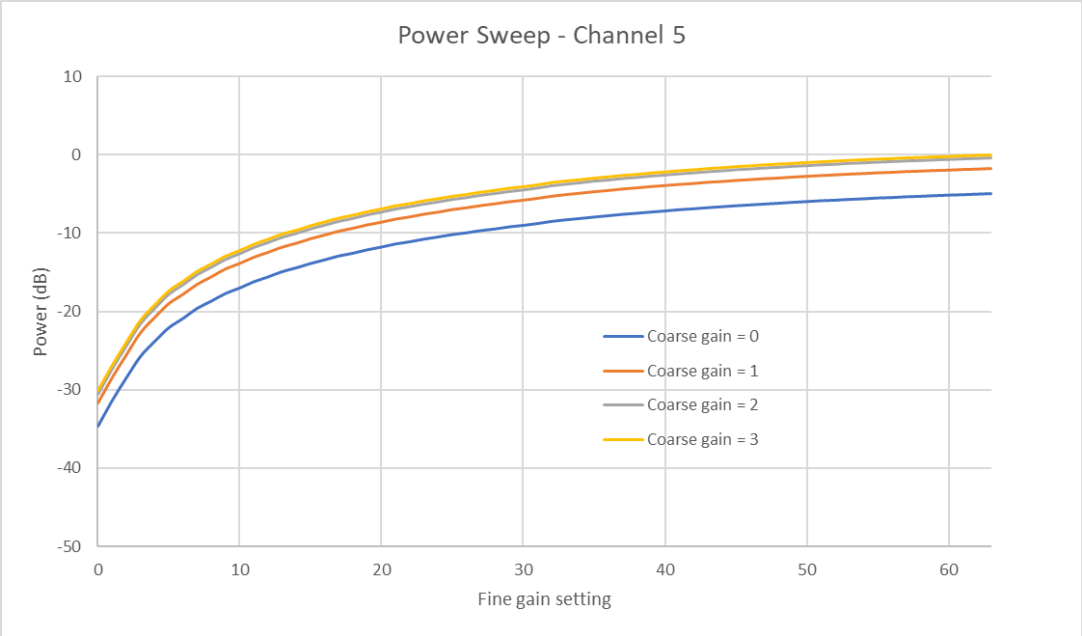


Figure 4: Tx power coarse and fine gain settings Channel 5

\

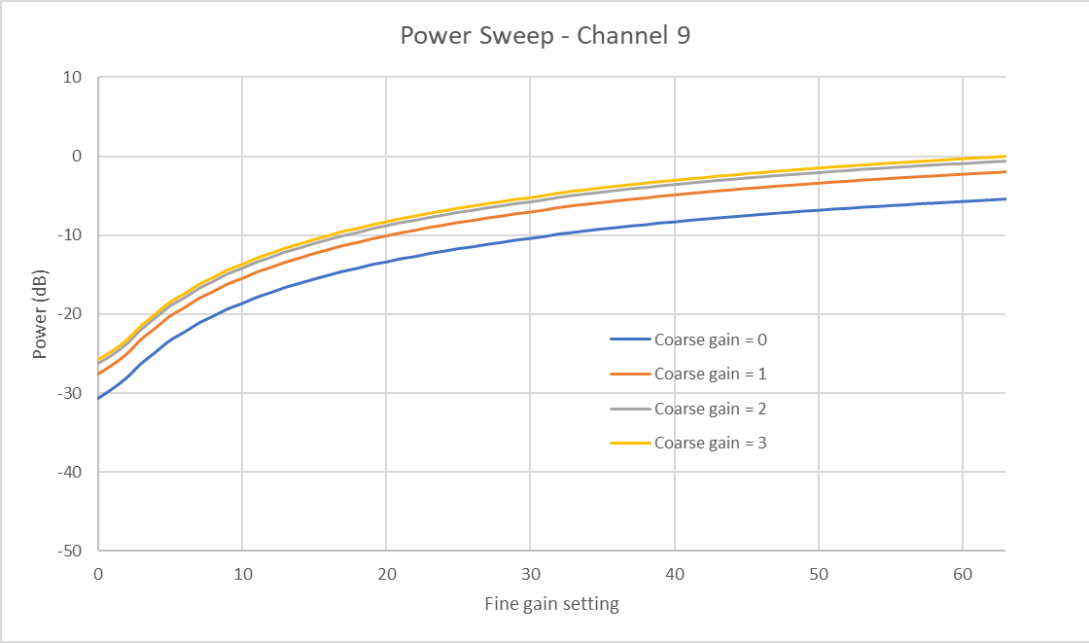


Figure 5: Tx power coarse and fine gain settings Channel 9

5.12.3 Receiver Blocking

The following plots show typical blocking levels to give 1% UWB PER at 3 dB back off from the sensitivity point. The UWB configuration is:

- PRF =64 MHz
- Preamble length = 64 symbols
- STS length = 64 symbols

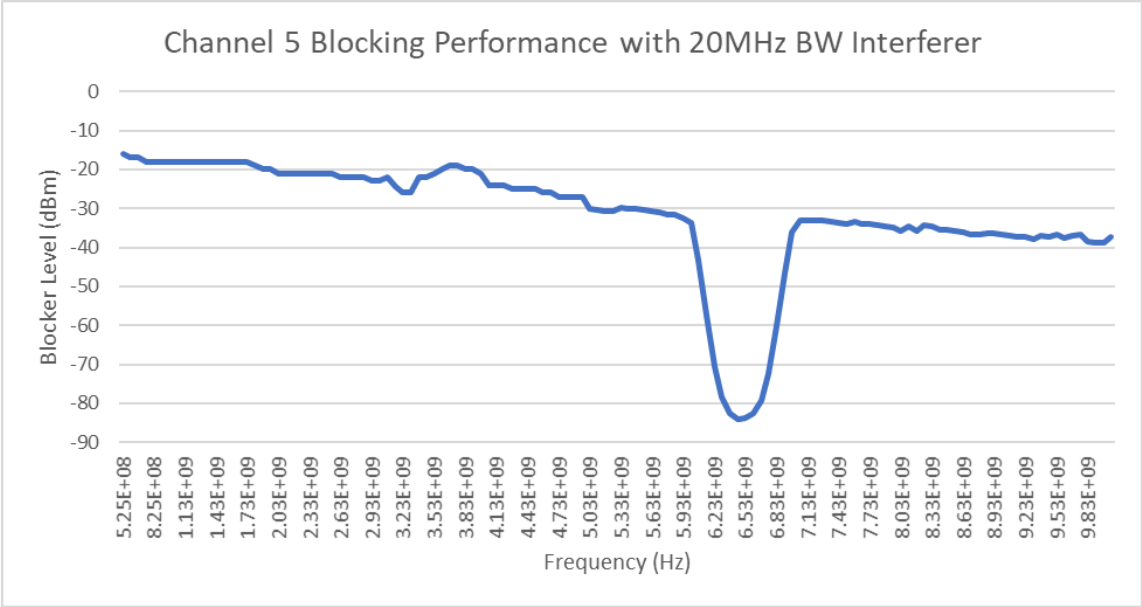


Figure 6: Blocking Performance Channel 5

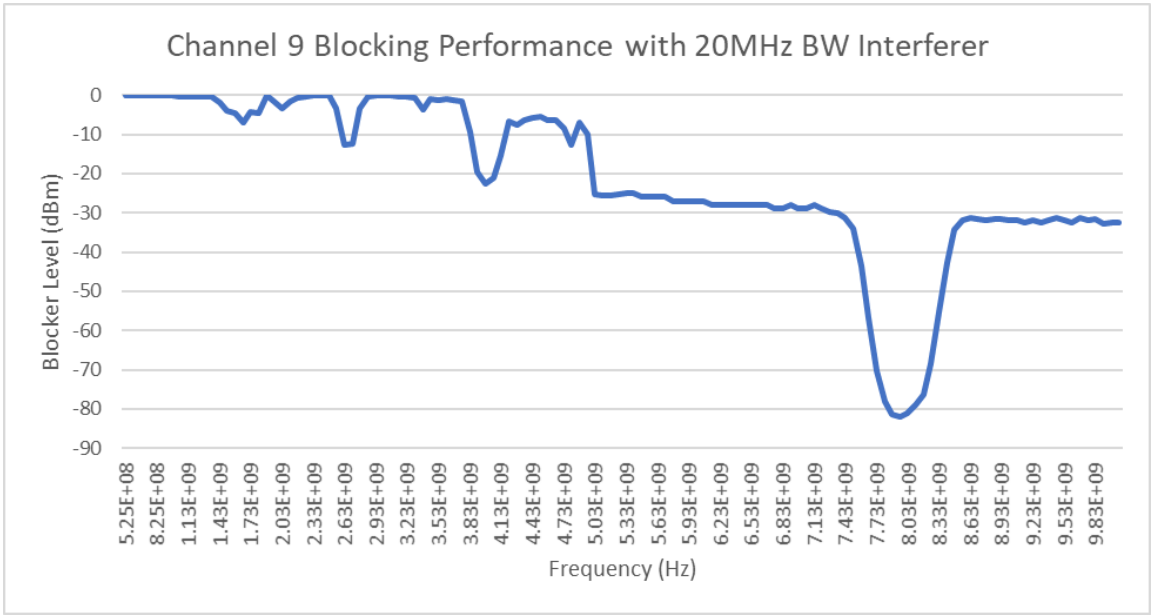


Figure 7: Blocking Performance Channel 9

5.12.4 Ranging

Typical measured distribution of double-sided TWR (DSR) performance.

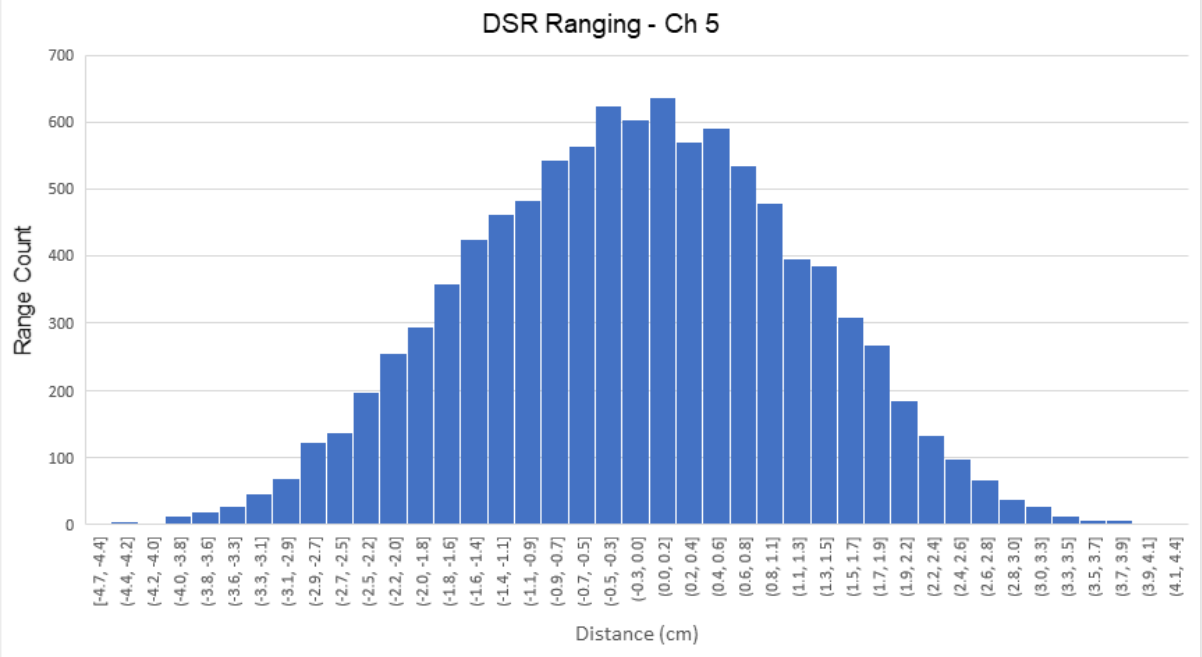


Figure 8: Ranging performance channel 5

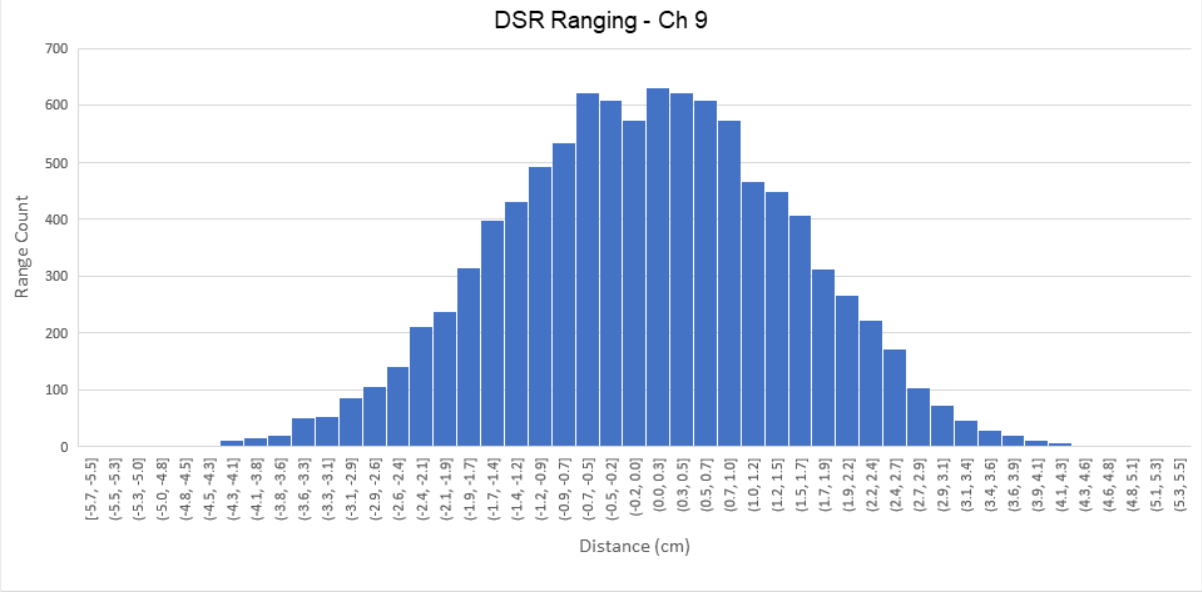
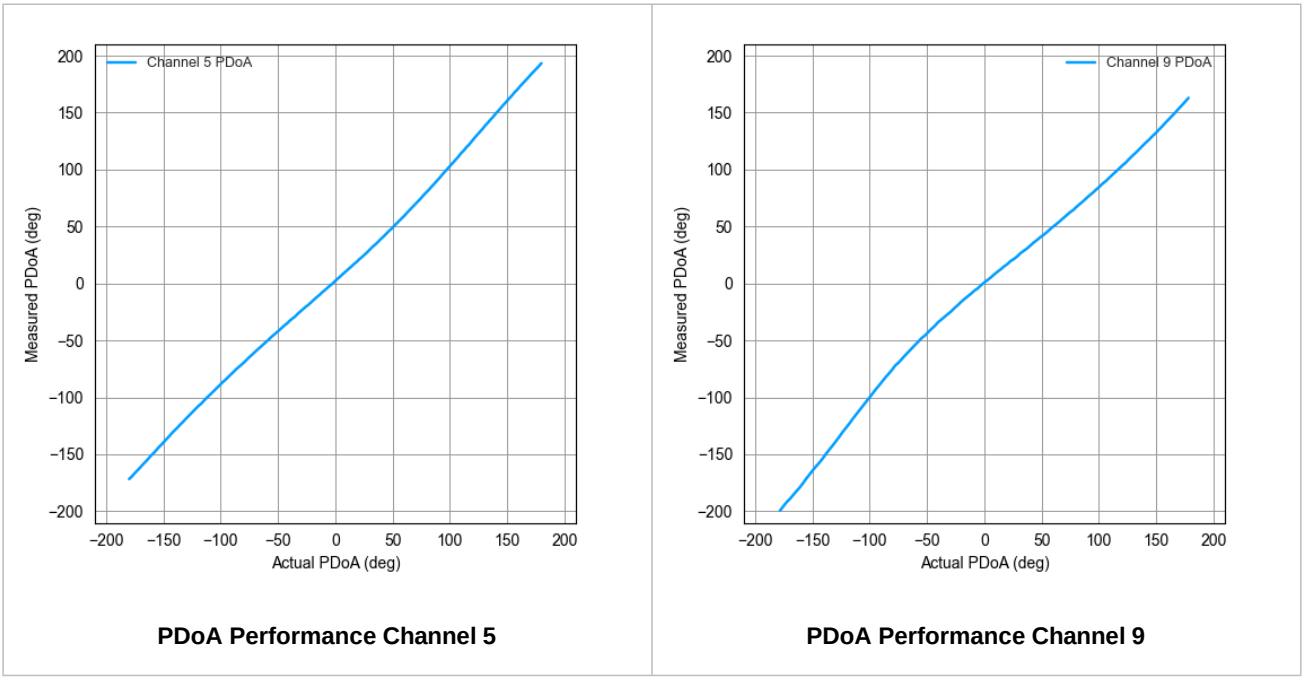


Figure 9: Ranging performance channel 9

5.12.5 PDoA

The following plots show typical measured PDoA performance. The UWB configuration is as follows:

- PRF = 64 MHz
- Preamble length = 128
- STS length = 256
- PDoA Mode = 3



PDoA Performance Channel 5

PDoA Performance Channel 9

Figure 10: DW3300Q PDoA Performance

6 Functional Description

6.1 Physical Layer Modes

Please refer to IEEE Std 802.15.4™-2020 and IEEE Std 802.15.4z™-2020 for the PHY specification.

6.2 Supported Channels and Bandwidths

The DW3300Q supports the following IEEE Std 802.15.4™-2020 and IEEE Std 802.15.4z™-2020 UWB channels:

Table 18: UWB Channels supported

UWB Channel Number	Center Frequency (MHz)	Bandwidth (MHz)
5	6489.6	499.2
9	7987.2	499.2

6.3 Supported Bit Rates and Pulse Repetition Frequencies (PRF)

The DW3300Q supports IEEE Std 802.15.4-2011, IEEE Std 802.15.4™-2020 UWB standard bit rates 850 kbps and 6.81 Mbps and nominal PRF values of 16 MHz and 64 MHz. The Base PRF (BPRF) mode of a newly defined draft standard IEEE Std 802.15.4z™-2020 is also supported.

Table 19: PRF and data rates supported

PRF (MHz)	Data Rate (Mbps)
16*	0.85
16*	6.81
64**	0.85
64**	6.81

Actual PRF mean values are slightly higher for SHR as opposed to the other portions of a frame. Mean PRF values are 16.1/15.6 MHz and 62.89/62.4 MHz, nominally referred to as 16 MHz and 64 MHz in this document. Refer to [1], [2] (UWB PHY rate-dependent and timing-related parameters) for full details of peak and mean PRFs.
** Backward-compatible for IEEE Std 802.15.4-2011 UWB devices*
*** Base PRF (BPRF) mode of IEEE Std 802.15.4z™-2020 and IEEE Std 802.15.4-2011*

In general, lower data rates give increased receiver sensitivity, increased link margin and longer range but due to longer frame lengths for a given number of data bytes they result in increased air occupancy per frame and a reduction in the number of individual transmissions that can take place per unit time.

16 MHz PRF gives a marginal reduction in transmitter power consumption over 64 MHz PRF (BPRF).

6.4 Symbol Timing

Timing durations in IEEE802.15.4 are expressed in an integer number of symbols. This convention is adopted in DW33300Q documentation. Symbol times vary depending on the data rate and PRF configuration of the device and the part of the frame. DW3300Q can transmit PHR on the 0.85 and 6.81 Mbps data rates. See the table below for symbol timings supported by DW3300Q.

Table 20: DW3300Q Symbol Timings Duration

PRF (MHz)	Data Rate (Mbps)	SHR (ns)	PHR 0.85 Mbps (ns)	PHR 6.81 Mbps (ns)	Data (ns)
16	0.85	993.59	1025.64	-	1025.64
16	6.81	993.59	1025.64	128.21	128.21
64	0.85	1017.63	1025.64	-	1025.64
64	6.81	1017.63	1025.64	128.21	128.21

6.5 Frame Format IEEE Std 802.15.4-2011, IEEE Std 802.15.4™-2020

IEEE Std 802.15.4-2011, IEEE Std 802.15.4™-2020 frames are structured as shown in. Detailed descriptions of the frame format are given in the standard. The frame consists of a synchronization header (SHR) which includes the preamble symbols and start frame delimiter (SFD), followed by the PHY header (PHR) and data. The data frame is usually specified in number of bytes and the frame format will include 48 Reed-Solomon parity bits following each block of 330 data bits (or less).

While zero length payloads and zero length PHR is supported the maximum frame length is 1023 bytes, including the 2-byte FCS.

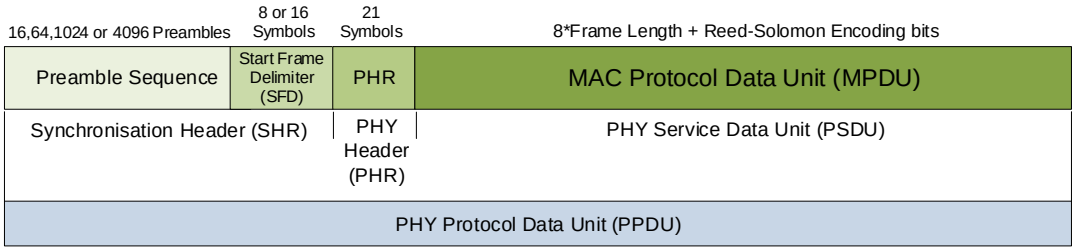
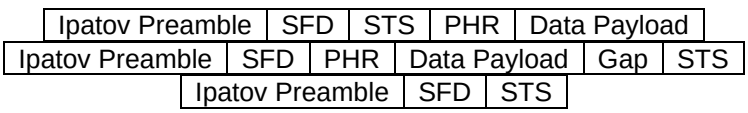


Figure 11: IEEE802.15.4-2011 PPDU Structure



6.6 Packet Formats of IEEE Std 802.15.4z™-2020

The 4z amendment added new packet formats to HRP UWB PHY incorporating a Scrambled Timestamp Sequence (STS) into the packet structure, defining four STS Packet Configurations as shown in Figure 7 below.

The STS is a random sequence of positive and negative pulses generated using an AES-128 based deterministic random bit generator (DRBG). Only valid transmitters and receivers have the correct seed (i.e., the key and IV) to generate the sequence for transmission and to validly cross correlate in the receiver to determine the receive timestamp. The STS provides for secure receive timestamping and secure ranging.

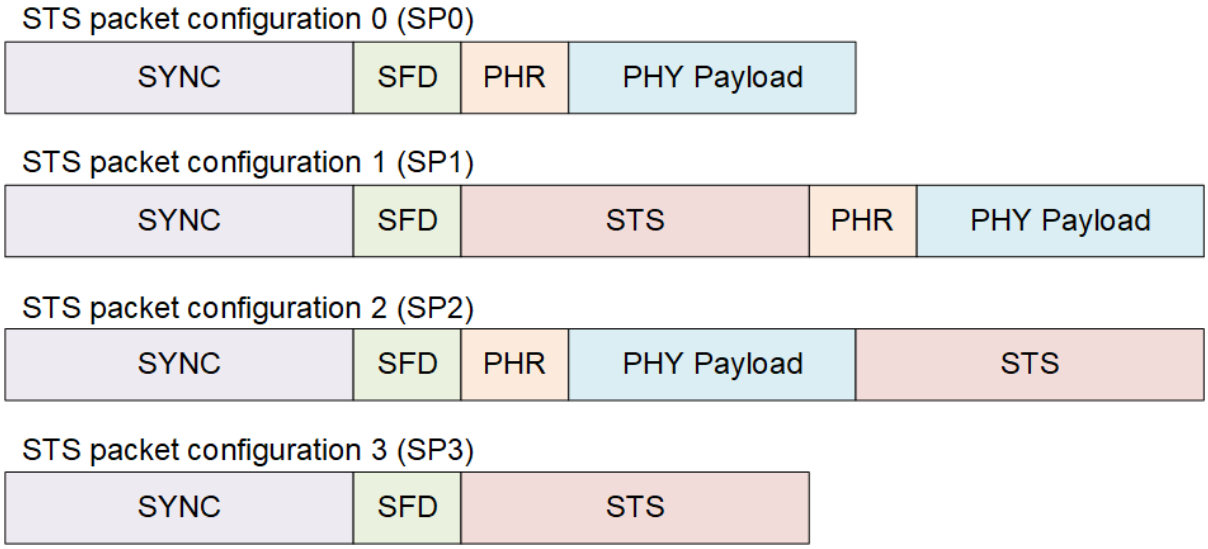


Figure 12: IEEE Std 802.15.4z™-2020 HRP UWB PHY PPDU Formats

6.7 Proprietary Long Frames

The DW3300Q offers a proprietary long frame mode where frames of up to 1023 bytes may be transferred. Refer to the DW3300Q user manual for full details.

6.8 No Data Frames

The DW3300Q offers zero length payloads and zero length PHR. This is for use cases where an alternative method of data communications is available.

6.9 Host Controller Interface

The primary interface DW3300Q is via a 4 wire SPI interface. DW3300Q will act a SPI slave device, in non-daisy-chain mode and operate at SPI clock frequencies up to 32MHz.

6.9.1 SPI1 Functional Description

The host interface to DW3300Q is a 4-wire SPI-compatible slave. The assertion of SPICSn low by the SPI master indicates the beginning of a transaction.
The SPI1 interface is used to read and write registers in the DW3300Q device. All data and address transfer on the SPI1 is most significant bit first. All address bytes are transmitted with MSB first, and all data is transmitted commencing with lowest addressed byte.

- Assertion low of SPICSn initializes transaction.
- De-assertion high of SPICSn ends the SPI transaction.
- The device supports direct and per-byte sub-addressing access to the full register space.
- Efficient block data reading/writing is allowed. Continuous, long transactions can be carried out while the addressed location is auto incremented on the DW3300Q side.

The SPIMISO I/O is required to go open drain when SPICSn is de-asserted, to allow interoperation with other slaves on the SPI bus.

SPI daisy chaining is not supported. This is the mode where the MISO, MOSI lines are passed through a device when it is not chip selected.

6.9.2 SPI Timing Parameters

The SPI1 slave complies with the Motorola SPI protocol within the constraints of the timing parameters listed in the Table below and illustrated in Figures below.

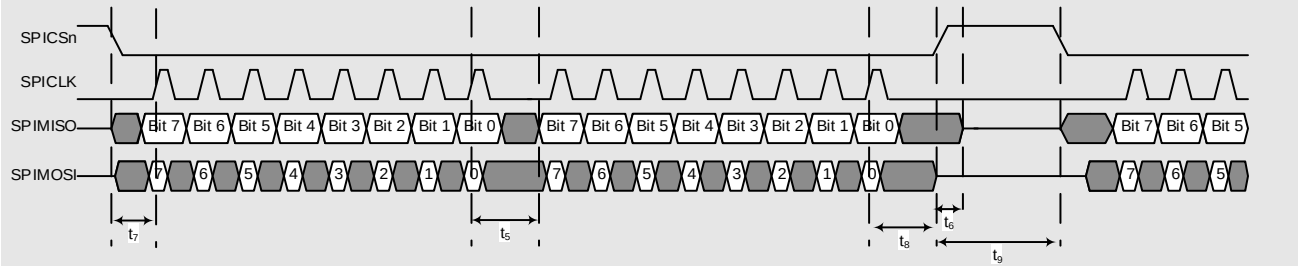


Figure 13: SPI Timing Diagram

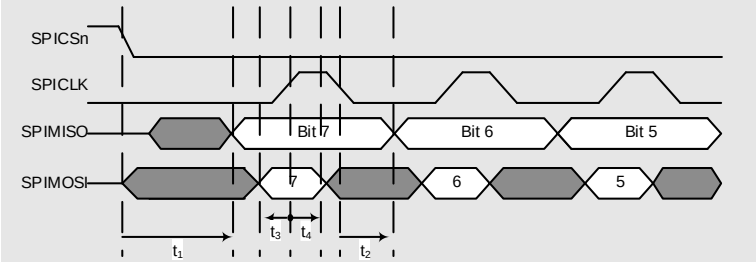


Figure 14: SPI Detailed Timing Diagram

Table 21: SPI Timing Parameters

Parameter	Min.	Typ.	Max.	Units	Description
t_1			N/A	ns	SPI select asserted low to valid slave output data.
T_2			9.5	ns	SCLK low to valid slave output data.
T_3	2.5			ns	Master data setup time.
T_4	0.7			ns	Master data hold time.
T_5		N/A		ns	LSB last byte to MSB next byte. (See maximum SPI frequency)
t_6			10	ns	SPI select deasserted high to MISO tristate.
T_7	10			ns	Start time; time from select asserted to first SCLK.
T_8	42			ns	Idle time between consecutive accesses.
T_9	40			ns	Last SCLK to SEL_n deasserted.
T_{10}			32	MHz	SPICLK SPI1 mode 0.
			16	MHz	SPICLK SP12 mode 0

6.9.3 SPI Operating Modes

Both clock polarities (SPIPOL=0/1) and phases (SPIPHA=0/1) are supported, as defined in the Motorola SPI protocol. The DW3300Q transfer protocols for each SPIPOL and SPIPHA setting are given in Figure 15 and Figure 16. Mode 0 is the default mode for both SP1 and SPI2. The mode can be changed by programming in the OTP memory or writing to the appropriate register, see User Manual.

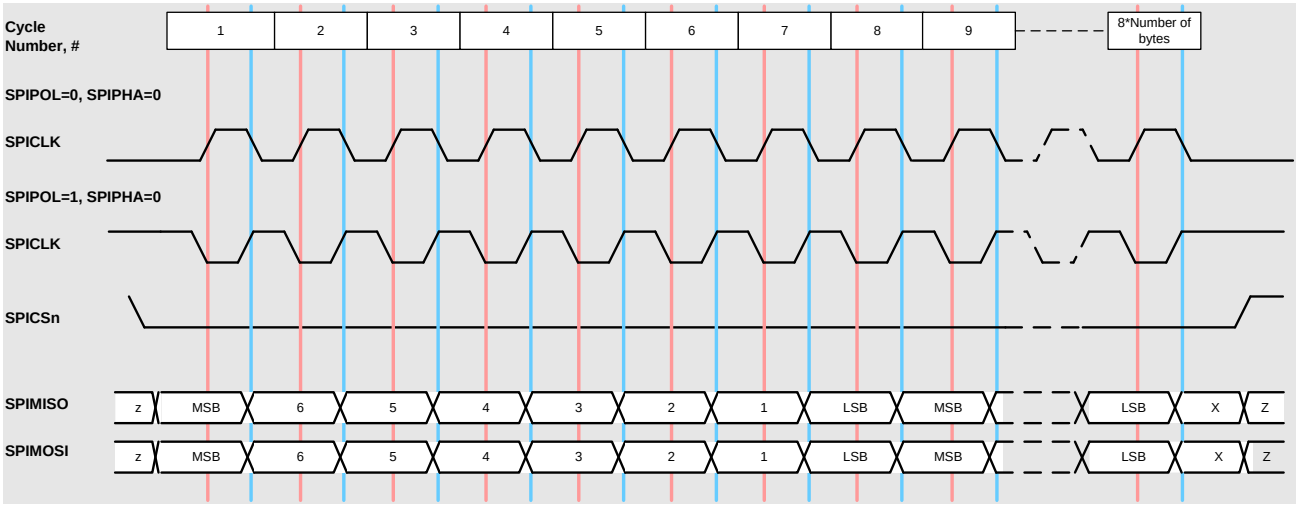


Figure 15: DW3300Q SPIPHA=0 Transfer Protocol

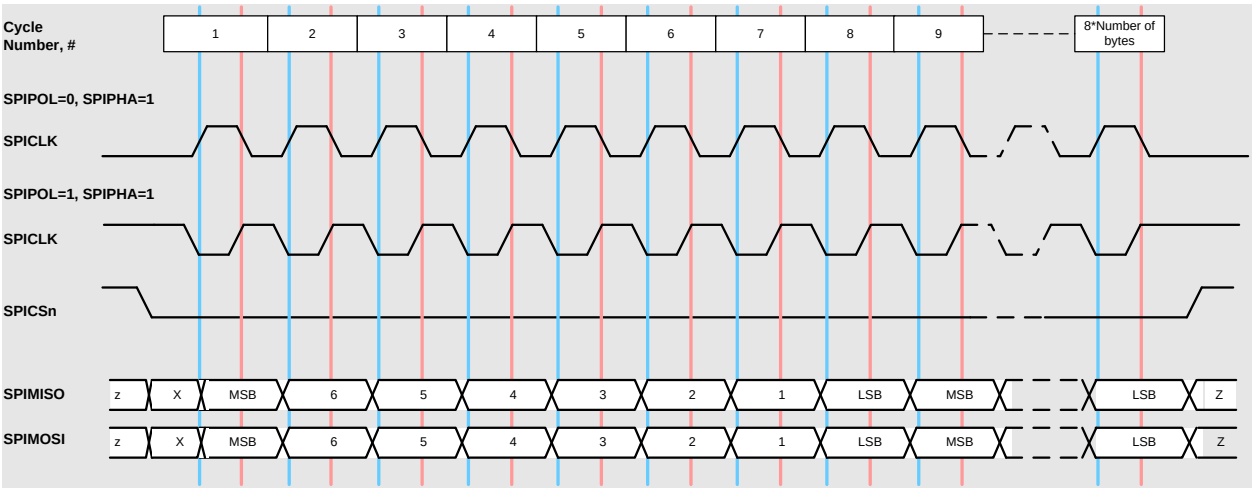


Figure 16: DW3300Q SPIPHA=1 Transfer Protocol

6.9.4 SPI Transaction Formatting

The SPI command structure allows for 4 different types of SPI command:

1. Fast, single byte commands. Up to 32 unique commands such as “TX now”, “TX/RX Off”.
2. Fast addressed mode. Allowing for read and write addressing to 32 master addresses. This command structure is padded by a trailing bit to allow the SPI address decoder time to fetch any read data. The length of the read is determined by the length of the SPI transaction.
3. Full addressed mode. Allowing for read and write addressing to 32 master addresses and up to 128 byte offset addressing. This command structure is padded by a trailing bit to allow the SPI address decoder time to fetch any read data. The length of the read or write is determined by the length of the SPI transaction.
4. Masked write transaction. These are intended to simplify read-modify-write operations by allowing the host to write to an address and apply a set, clear or toggle mask to 1, 2, or 4 bytes. The SPI command decoder then carries out the required read-modify-write instructions internally.

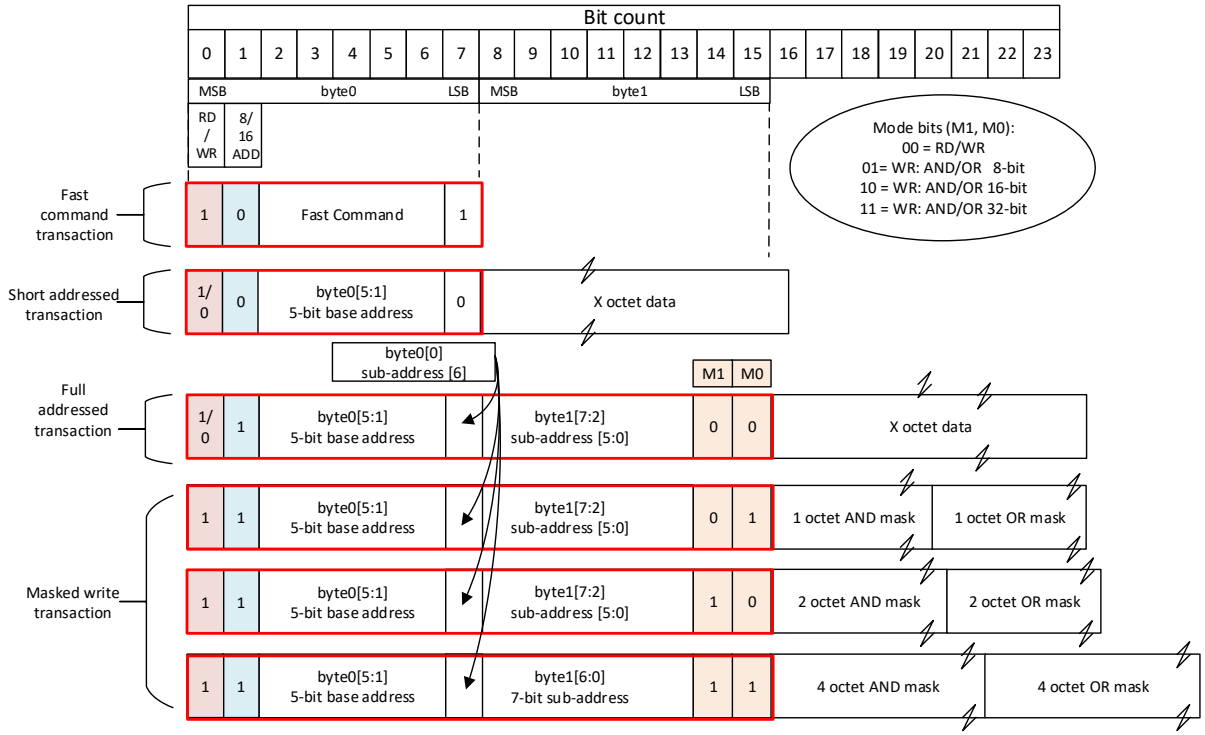


Figure 17: SPI Command Formatting

6.9.5 GPIO and SPI I/O Internal Pull Up/Down

All the GPIO pins have a software controllable internal pull up/down resistor to ensure safe operation when input pins are not driven. This defaults to enabled and pull-down except for the SPICSn pin which defaults to pull-up. The value of the pull up/down will vary with the VDD1 supply voltage over a range from 10 kΩ to 30 kΩ.

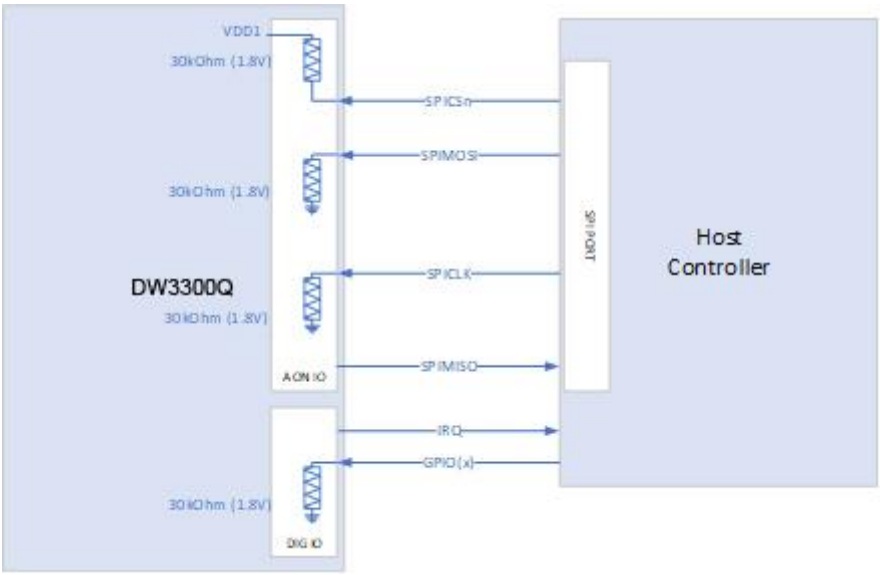


Figure 18: SPI and GPIO Pull Up/Down

6.9.6 SPI2 Interface

The DW3300Q also contains an additional SPI interface, this is to allow two external hosts to use the DW3300Q. Additional SPI control registers have been added that are unique for each SPI interface, this is to allow each interface to request access and to confirm if access has been granted.

The second SPI interface supports the following features:

- The same command set and timing as SPI1.
- Support for independent setting of the SPI2 mode (Phase and Polarity)
- Fully arbitration for access to the internal DW3300Q register and memory map via a semaphore req/ack control mechanism
- Independent external interrupt, INT2, only set if SPI2 has been granted access to device.
- Locking capability, SPI2 can lock out SPI1 to allow for full secure access.
- The default active level for the SPI2 chip select is active high.

6.10 Reference Crystal Oscillator

With the addition of an external 38.4 MHz crystal and appropriate loading capacitors, the on-chip crystal oscillator DW3300Q generates the reference frequency for the integrated frequency synthesizer's RFPLL.
The crystal oscillator is used to provide the reference clock to the internal PLL and provides a direct clock source to the digital core when operating in the lower power INIT_RC mode. The oscillator operates at a frequency of 38.4 MHz. A trim facility is provided which can be used to trim out crystal initial frequency error. Typically, a trimming range of ± 20 ppm is possible using a 6-bit trim range. This trimming in 0.125pF steps provides for up to 8 pF additional capacitance on the XTI and XTO crystal connections. A 7th bit of trim range is provided to be used to compensate the crystal for temperature extremes approaching 105C.

6.10.1 Calculation of External Capacitor Values for Frequency Trim

Ideally the value of external loading capacitors (Cext) should be calculated to give an equal trim range about the center trim value. To do this, one needs to estimate the parasitic capacitance (Cpar) between the crystal pads XTI/XTO and the crystal pads. A good starting estimate is usually about 3.6 pF however some trial and error may be required initially. The values of Cm, Lm, Rm and Co obtained from the crystal manufacturer are also required.

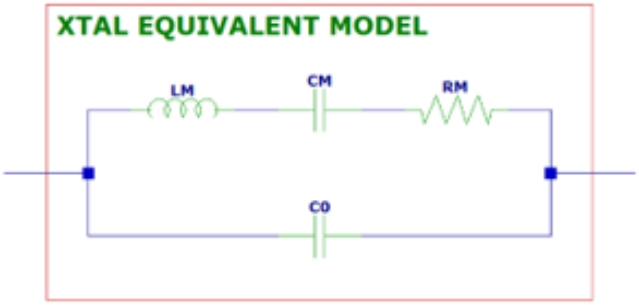


Figure 19: Crystal Model

Using the following formula, the required Cext and trim range can be estimated where:

fs = series frequency
fp = parallel frequency
Fl = loaded (desired) frequency

$$f_S = \frac{1}{2\pi\sqrt{C_M L_M}}$$

$$f_P = f_S\left(\sqrt{1+\frac{C_M}{C_0}}\right)$$

$$f_L = f_S\left(\sqrt{1+\frac{C_M}{C_L}}\right)$$

$$C_L = C_0+\frac{1}{2}\left(C_{TRIM}+C_{PAR}+C_{EXT}\right)$$

$$\Delta f_{ppm} = 10^6 \times \frac{f_L - f_{L_{NOM}}}{f_{L_{NOM}}}$$

A typical crystal trimming plot is shown below:

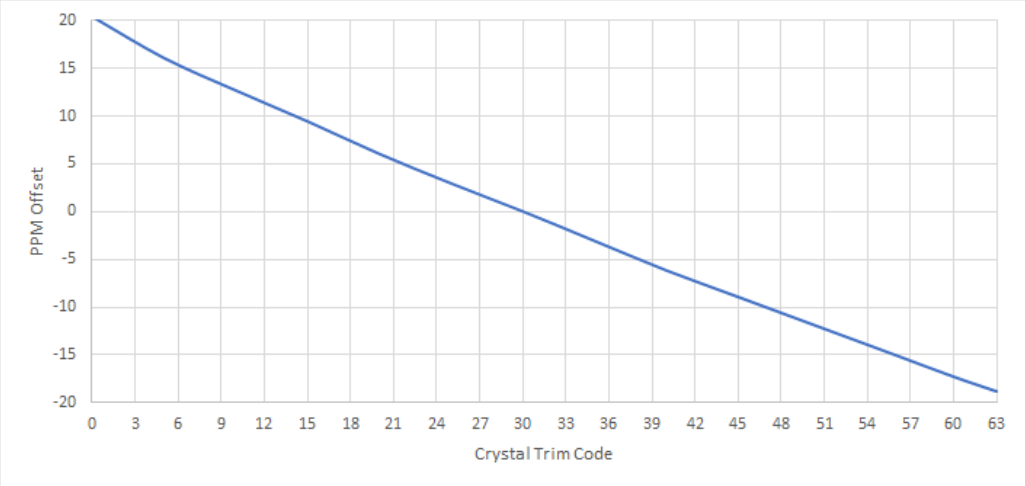


Figure 20: Crystal Trim Plot

7 Operational States

7.1 Overview

The DW3300Q has several basic operating states as described in Table below.

Table 17: Operating States

State	Description
OFF	Digital core is powered off, digital LDO is disabled. Reset is held low.
INIT_RC	System is clocked from 30MHz RC Osc, SPI comms @ 7MHz. AON download is performed. Automatically goes to IDLE_RC on completion.
IDLE_RC	System is clocked at ~120MHz to allow full speed SPI comms.
IDLE_PLL	System is clocked from the PLL at 124.8MHz.
TX_WAIT	TX blocks are sequenced on as required. Includes DELAYED_TX mode.
TX	Active TX state. Automatically reverts to IDLE_PLL after transmission.
RX_WAIT	RX blocks are sequenced on as required. Includes DELAYED RX mode.
RX	Active RX state. Can revert to IDLE_PLL if packet received or timeout triggers.
SLEEP	Low power state. Sleep counter is clocked from slow RC Osc at ~20kHz.
DEEPSLEEP	Low power state. All clocks off. Wakeup via IO event on WAKEUP or SPICSn, or by resetting the device (RSTn).

7.2 Operating State Transitions

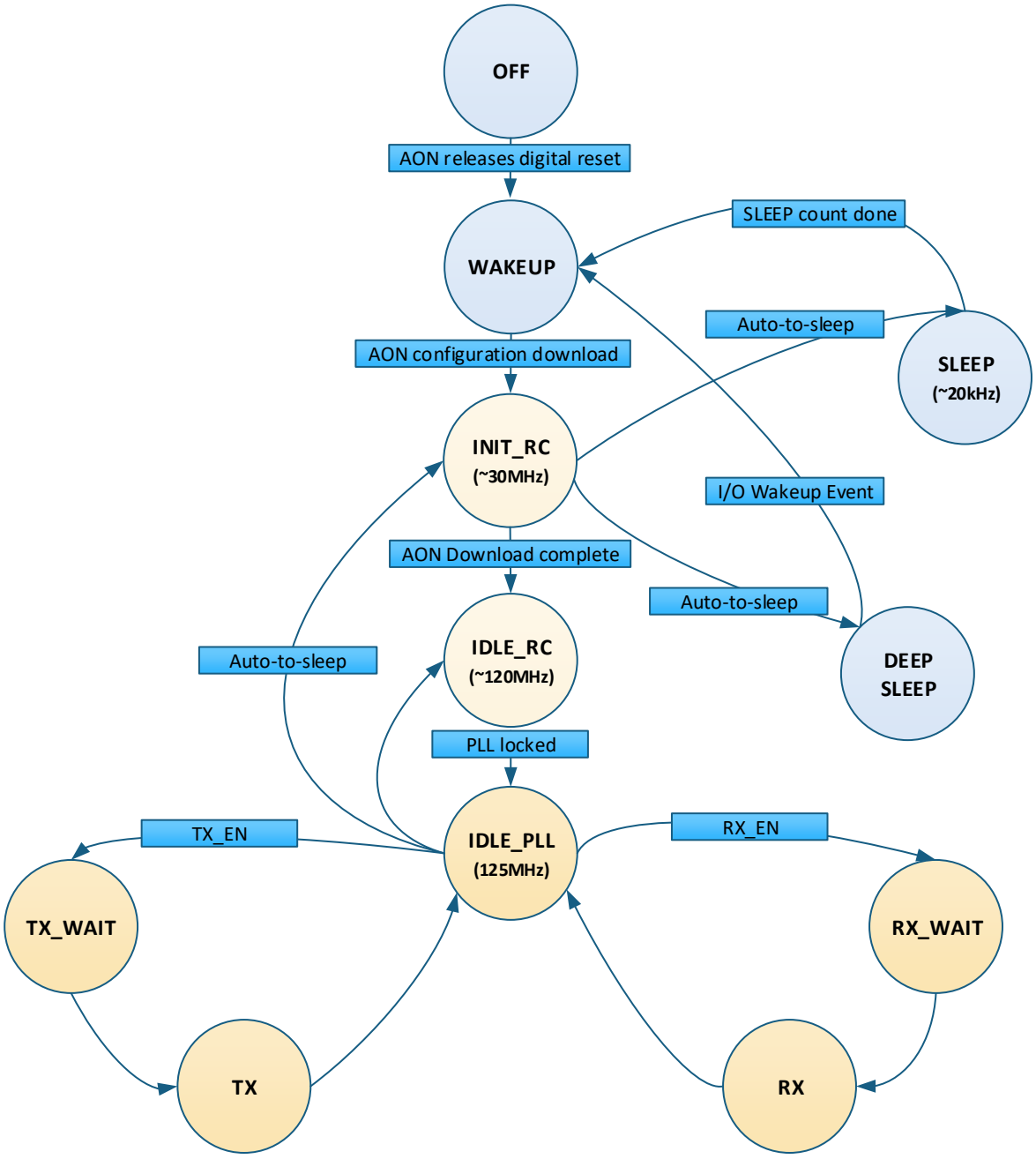


Figure 21: Operating State Transitions

8 Powering DW3300Q

DW3300Q is designed such that it can be powered in several different configurations depending on the application. These options are described below. Figure 22: Timing Diagram for Cold Start POR shows the power up sequence when external power sources are applied. The power supply design should ensure that VDD2a/b and VDD3 are stable less than 10ms after VDD1 (3.3V) comes up, otherwise a device reset is required.

When the external power source is applied to the DW3300Q for the first time (cold power up), the internal Power On Reset (POR) circuit compares the externally applied supply voltage (VDD1) to an internal power-on threshold (approximately 1.5V), and once this threshold is passed the AON block is released from reset and the external device enable pin EXTON is asserted.

Then the VDD2a/b and VDD3 supplies are monitored and once they are above the required voltage as specified in the Datasheet (2.2V and 1.4V respectively), the fast RC oscillator (FAST_RC) and crystal (XTAL Oscillator) will come on within 500 µs and 1 ms respectively.

The DW3300Q digital core will be held in reset until the crystal oscillator is stable. Once the digital reset is de-asserted the digital core wakes up and enters the INIT_RC state, (see Figure 22 and Figure 23). Then once the configurations stored in AON and OTP have been restored (into the configuration registers) the device will enter. Then the host can set the AINIT2IDLE configuration bit in SEQ_CTRL and the IC will enable the CLKPLL and wait for it to lock before entering the IDLE_PLL state.

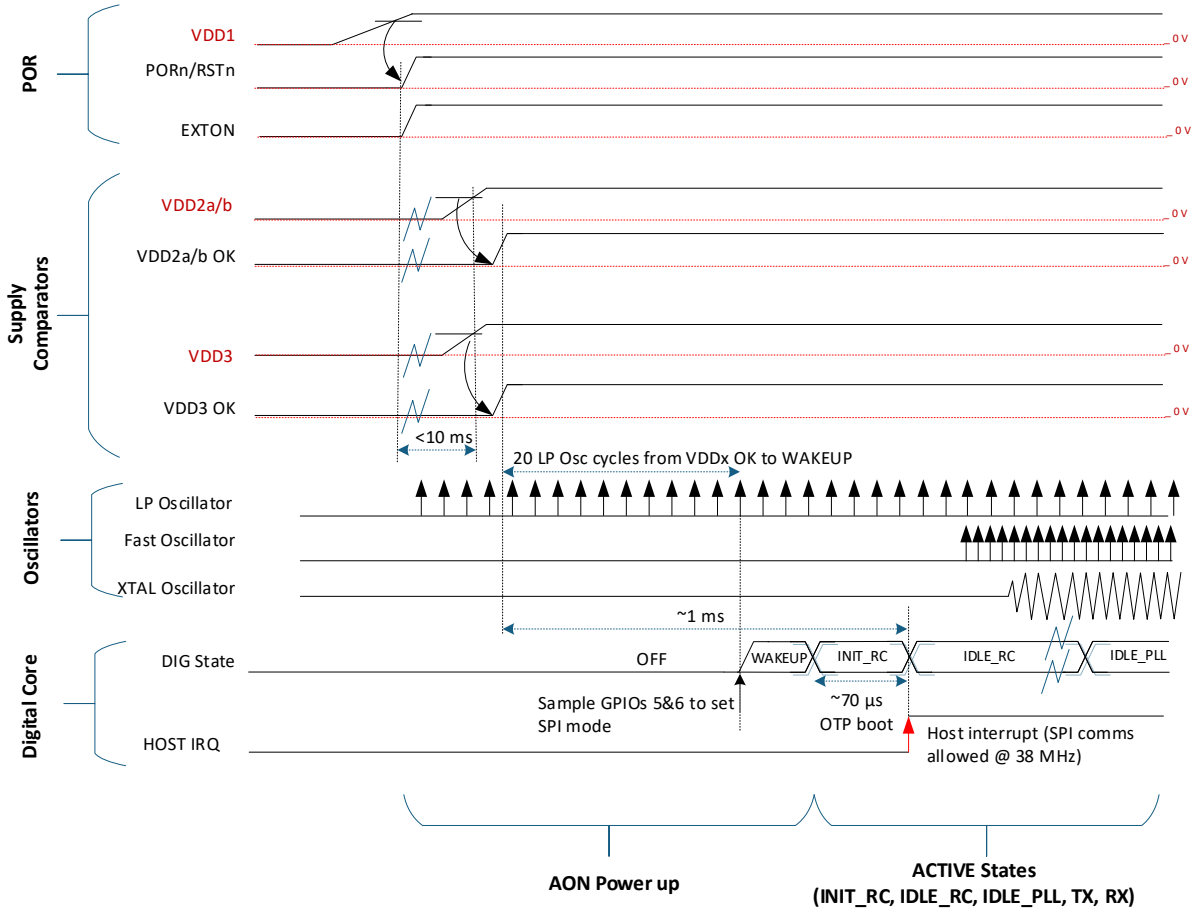


Figure 22: Timing Diagram for Cold Start POR

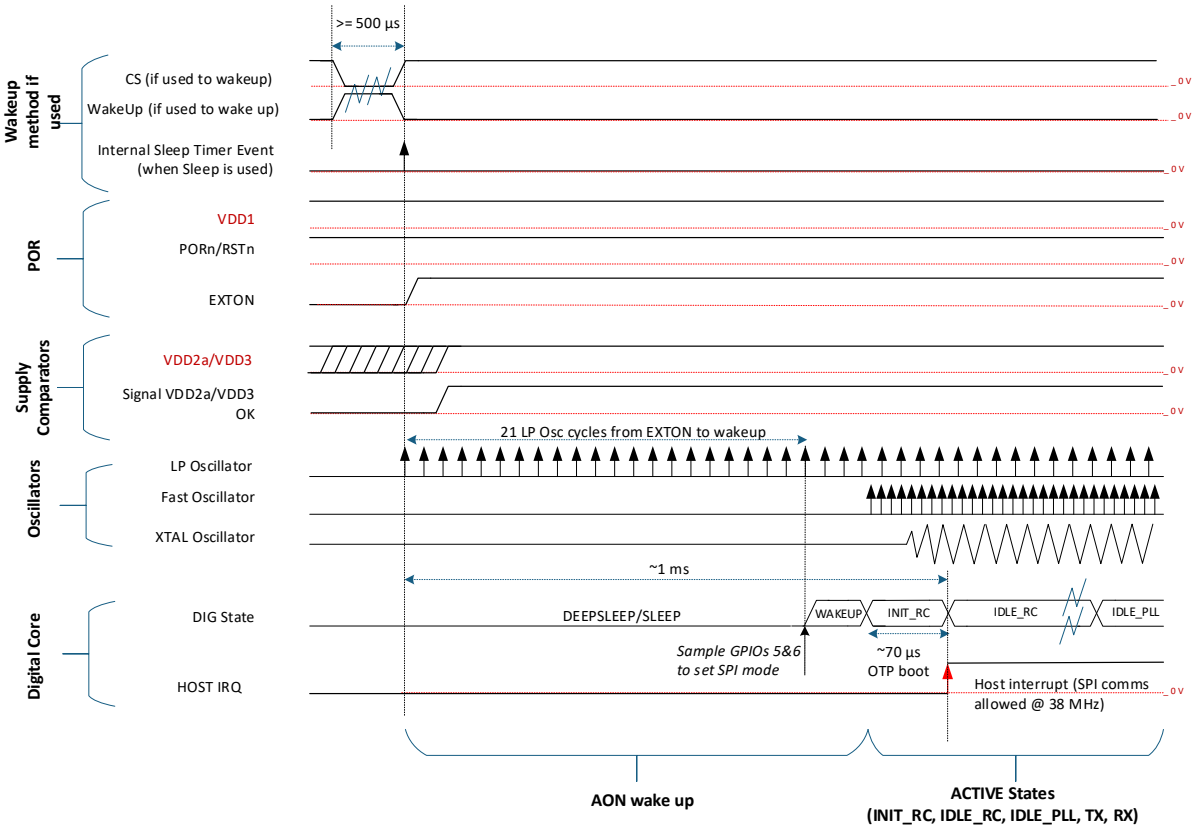


Figure 23: Timing Diagram for Warm Start

8.1 Lowest Bill of Materials (BOM) Powering Scheme

In the following configuration the DW3300Q is powered directly from a coin-cell battery. This is for applications that require the minimal BOM. The bulk capacitor is required to store energy. The value of capacitor depends on the time the transceiver is in the active Tx/Rx state, typically 47uF.

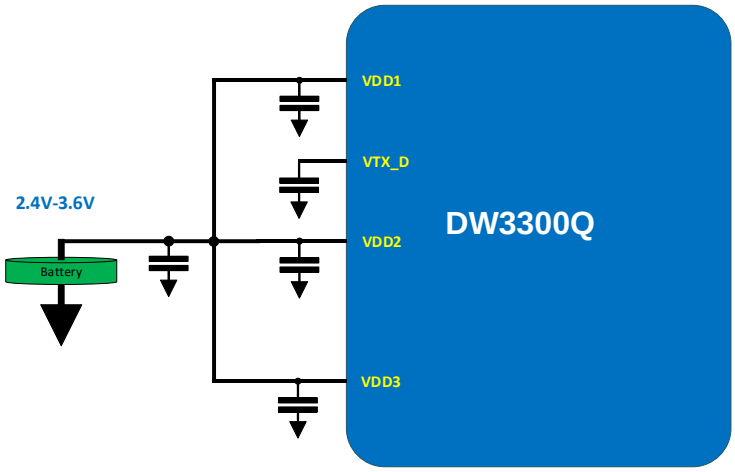


Figure 24: Lowest BOM Powering Option

8.2 Highest Efficiency Powering Scheme

In the following configuration the external Buck SMPS regulator is used. This is for applications that require the longest battery lifetimes. Depending on the use-case either the EXTON output or MCU can be used to control the Buck DC-DC.

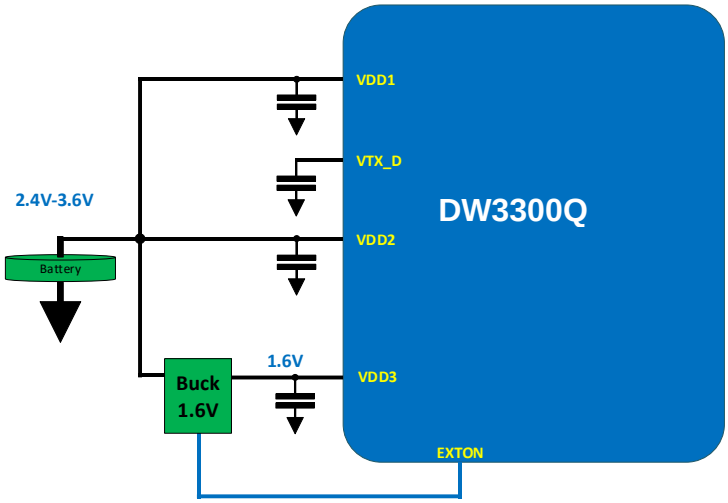


Figure 25: Single O/P Buck SMPS Option

8.3 PMIC Powering Scheme

In the following configuration the external PMIC circuit is used to provide all the power rails to the chip. The VDD1 is used to power Always-On memory and IO rail only, the current consumption for powering AON is negligible.

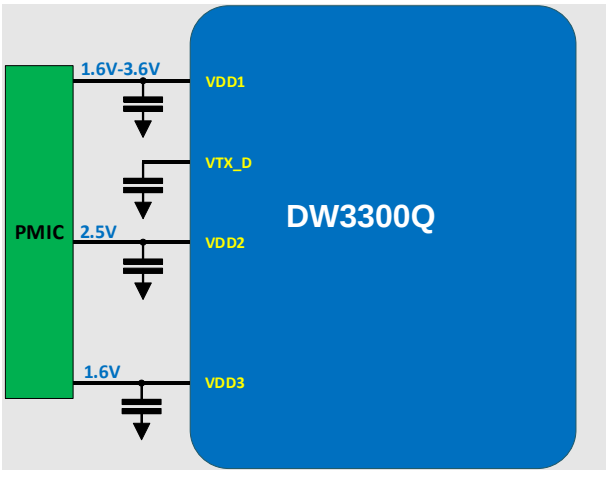


Figure 26: Keyfob Option with PMIC

8.4 Typical Transmit and Receive Power Profile

The current drawn during operation with DW3300Q will vary depending on supplies used, batteries used, use case etc. Figure 27 shows the current drawn from a CR2032 battery with typical TX frames transmitted and the reception of these frames by the receiver.

8.4.1 TX Current Profile for the Minimal BOM

Figure 27 below shows the current profiles during of frame transmission without secure preamble and 6.8Mbps TDoA tag frame. This mode is compatible to a DW1000 TDoA tag blink. All supplies are connected to the battery assumed to at 3.0V, ie. the lowest BOM option, see section 8.1 Lowest Bill of Material.

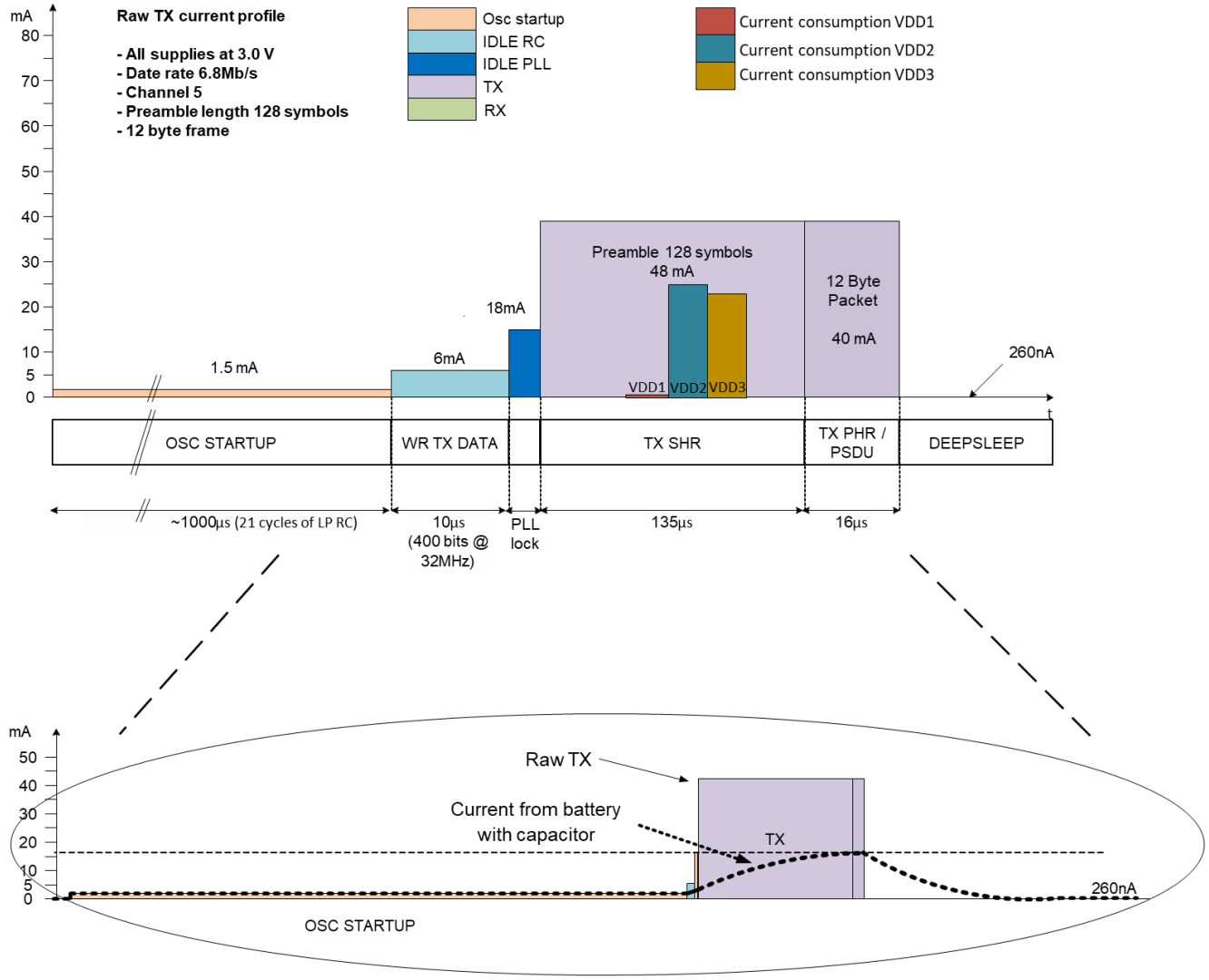


Figure 27: Current Profile when Transmitting a Frame (6.8Mbps) in Lowest BOM Use Case

8.4.2 TX Current Profile for High Efficiency Modes

In the high efficiency modes, i.e. when an external DC-DC/PMIC is used, the current consumption from VDD3 (1.6V) and VDD2a and VDD2b (2.5V) are different, therefore more efficient current consumption can be achieved using alternative powering schemes, illustrated in section 8.2 and 8.3. The VDD1 is used to power AON memory and IO rail only, the current consumption for powering AON is negligible.

For high efficiency schemes, the overall power consumption depends on the efficiency of external DC-DC and/or PMIC. For the DW3300Q device, the power consumption during different phases of operation as illustrated below.

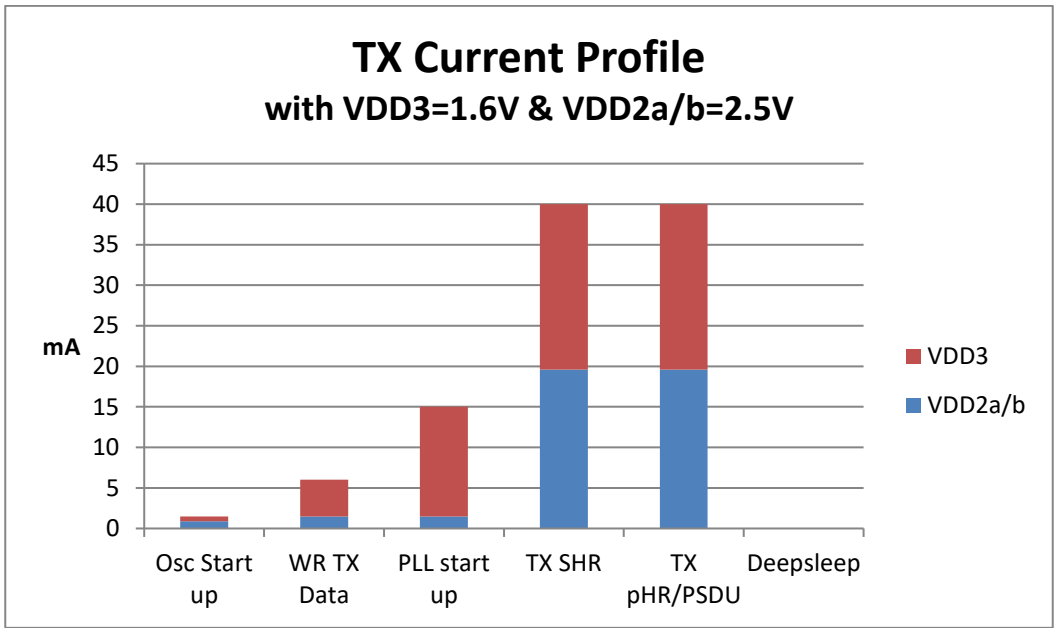


Figure 28: Current Consumption During TX for High Efficiency Powering Modes

8.4.3 RX Current Profile for Minimal BOM

Figure 29 illustrates the current profiles during the reception of a typical frame. All supplies are connected to the battery assumed to at 3.0V, ie. the lowest BOM option, see 8.1.

The example given for a case where a variable part of Preamble Hunt is ~30us. The preamble hunt can be minimized to 0 (zero) when using Delayed RX in the optimized Two Way Ranging (TWR) protocol (not illustrated), however with a Delayed RX the IDLE PLL should be maintained in between end of the transmission and start of the reception.

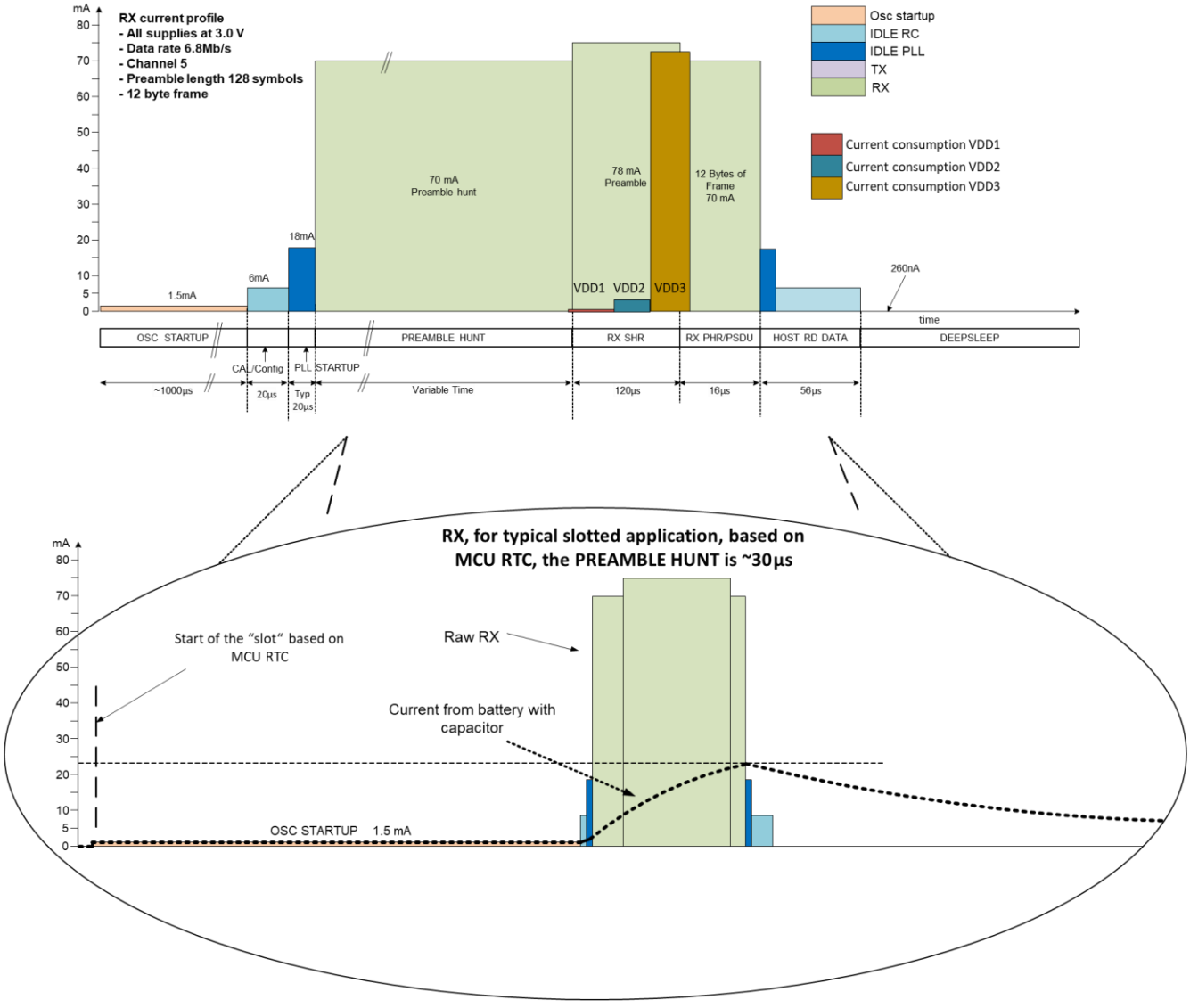


Figure 29: Typical Current Profiles When Receiving a Frame for Different Types of Applications

RX Current Profile for High Efficiency BOMs

In the high efficiency modes, i.e. when an external DC-DC/PMIC is used, the current consumption from VDD2 (2.5V) and VDD3 (1.6V) are different, therefore more efficient current consumption can be achieved using alternative powering schemes, illustrated in section 8.2 and 8.3. The VDD1 is used to power AON memory and IO only, the current consumption for powering AON is negligible.

For high efficiency schemes, the overall power consumption depends on the efficiency of external the DC-DC and/or PMIC. For the DW3300Q device, the power consumption during different phases of operation as illustrated below.

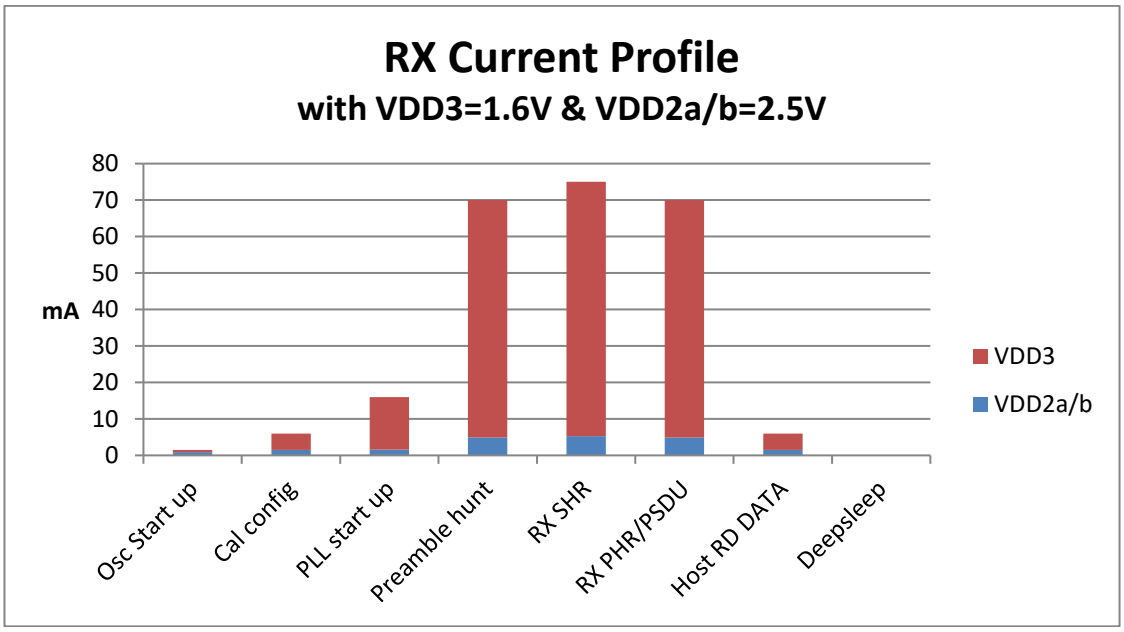


Figure 30: Current Consumption During RX for High Efficiency Powering Modes

8.5 Internal Power Supply Distribution

The block diagram shows the power distribution within the DW3300Q device.

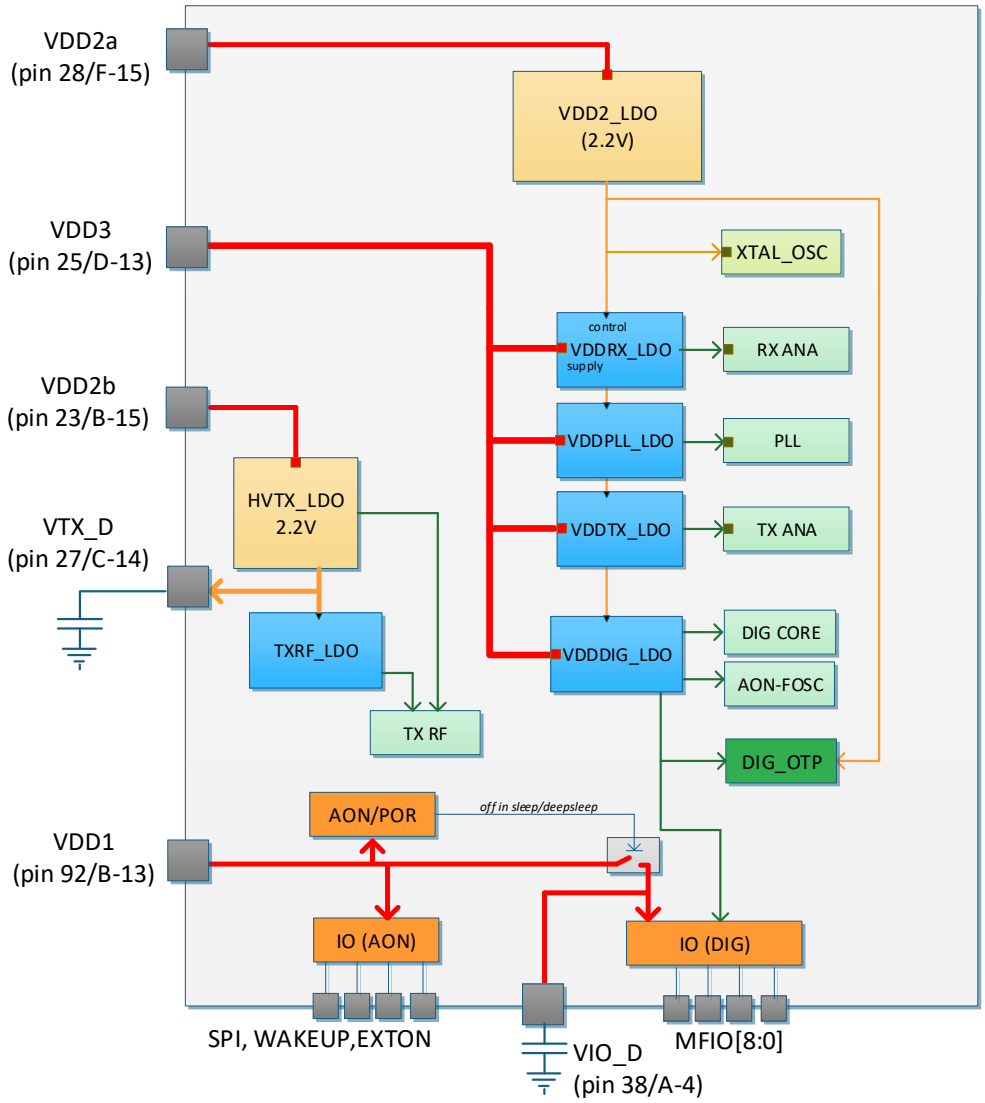


Figure 31: Internal Power Distribution

9 Application Information

9.1 Application Circuit Diagram

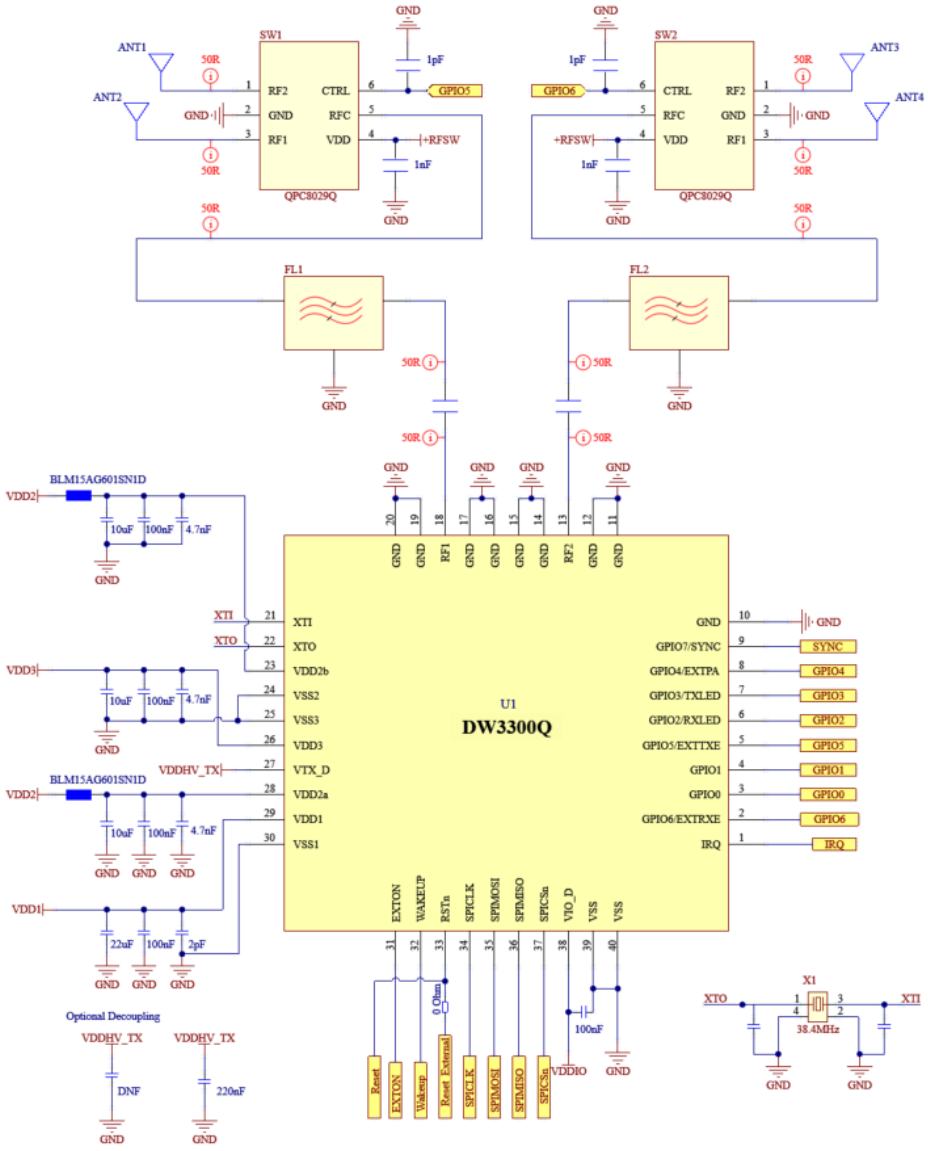


Figure 32: DW3300Q 40 Pin LGA Application Circuit

9.2 EVB Circuit Diagram

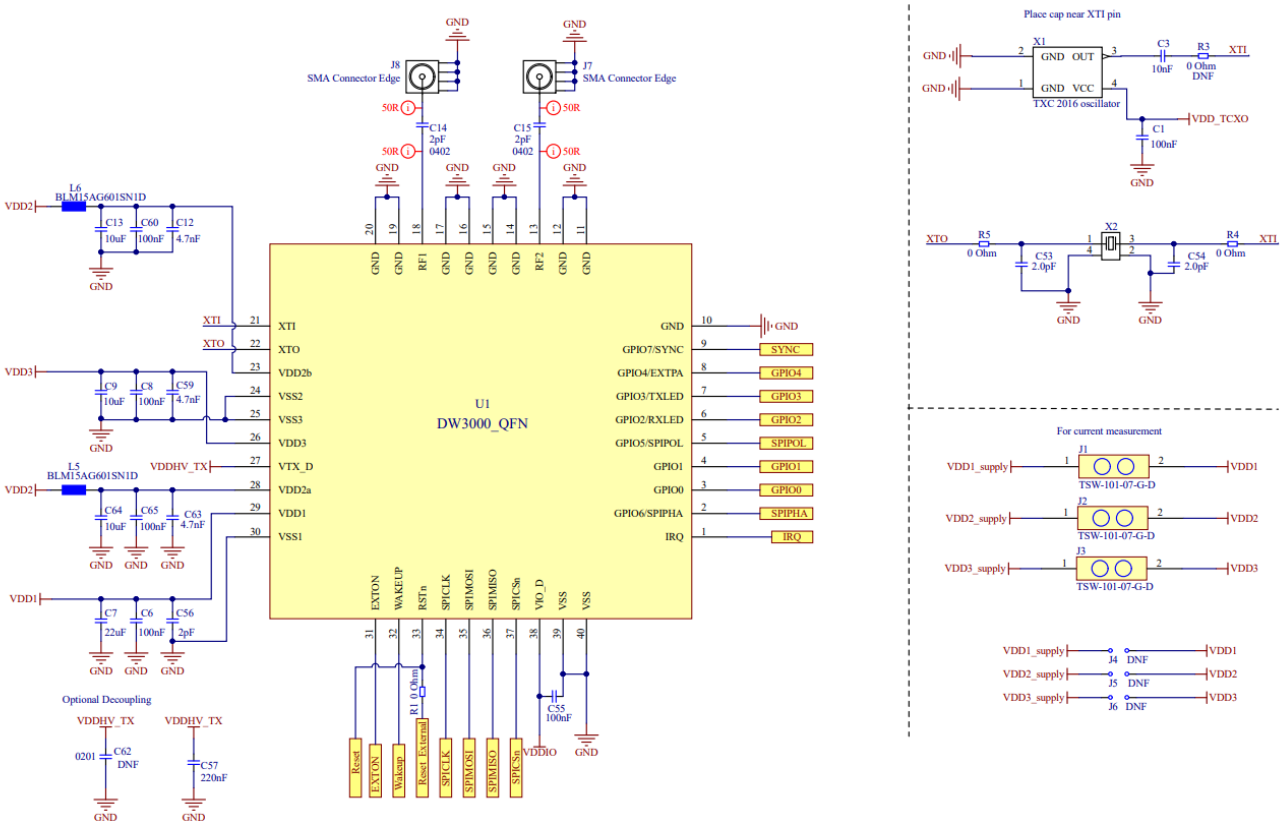
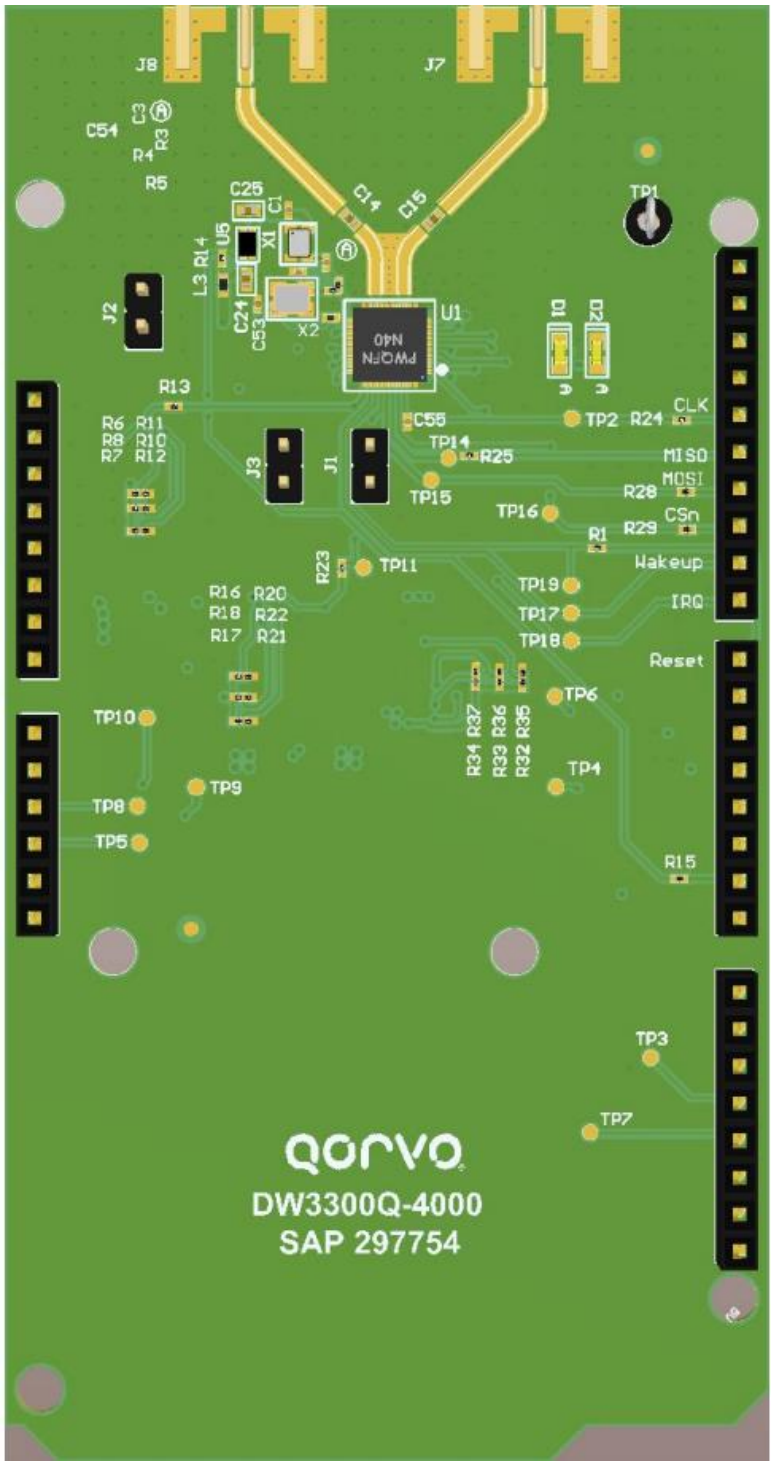


Figure 33: EVB Circuit Diagram

Note, the suggested crystal loading will vary depending on board layout and actual crystal used. C14 and C15 are not only DC blocking capacitors but are part of the RF transmission line. This line was simulated in design and this capacitance value was chosen as the result of the simulation. Terminate unused RF1 or RF2 ports in 50 ohms. RF1 is the default position for non-PDOA mode.

9.3 EVB Board


J8
J7
C54
C3
R3
R4
R5
C25
C1
C14
C15
TP1
U5
X1
L3
R14
C24
C53
X2
J2
U1
D1
D2
R13
C55
TP2
R24
CLK
R6
R11
R8
R10
R7
R12
TP14
R25
MISO
MOSI
J3
J1
TP15
R28
TP16
CSn
R29
R1
TP11
R23
Wakeup
R16
R20
R18
R22
R17
R21
TP19
TP17
IRQ
TP18
Reset
TP6
TP10
R34
R37
R36
R33
R32
R35
TP4
TP9
TP8
TP5
R15
TP3
TP7
DW3300Q-4000
SAP 297754

9.4 Recommended Components

The list of components in test by Qorvo are shown in the table below. The use of DC-DC regulators and TCXO's is optional.

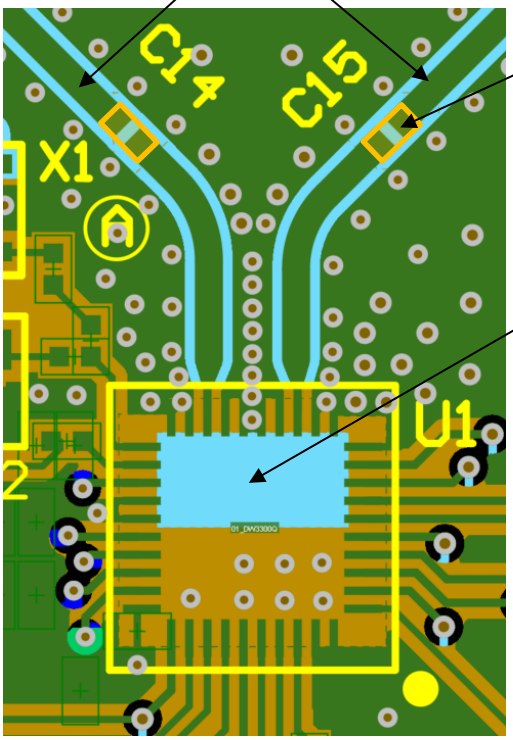
Table 18: Recommended Components

Function	Manufacturer	Part Number	Web Link
Antenna	Partron	ACS5200HFAUWB	www.partron.co.kr
Crystal (38.4 MHz +/-10 ppm at room; +/-25 to 30 ppm over temp)	Geyer	KX-5E	www.geyer-electronic.de
	KYOCERA	CX2016SA38400H0FRNC1	https://global.kyocera.com
DC-DC 3V3	Torex	XC9258B33CER-G	www.torexsemi.com
DC-DC 2V5		XC9282B25D0R-G	
DC-DC 1V6		XC9282B16D0R-G	
DC-DC	TI	TPS62743	www.ti.com

9.5 Recommended PCB layout and Stackup

The recommendation for the device layout.

- Keep all the traces as short as possible.
- Avoid mixing Analog (RF1,RF2,XIN,XOUT), Power (VDD1,VDD2a/b,VDD3,VDD decoupling) and Digital (SPI etc) groups together.
- Place all the decoupling capacitors as close to the corresponding device pads as possible, the smaller value capacitor should be closer to the pad. Connect the ground pad of each capacitor to the ground plane directly to minimize ESR and ESL of the return current path.
- RF1 and RF2 lines should be 50 Ohm impedance-controlled lines. The DC-blocking 2pF capacitor pads should be embedded into the track (have the same width) to remove any possible discontinuities.
- The ground copper should be removed from under the device in the areas shown in the picture below (Top layer and Layer2). The first solid ground copper should be on Layer 3. If different stack-up will be used – this first solid copper layer should be at least 0.45mm away from the Top Layer, and inner layers close to the Top Layer should have the ground removed in the same manner as in Layer 1 below.



PCB Stackup *(Dimensions in Mils)*

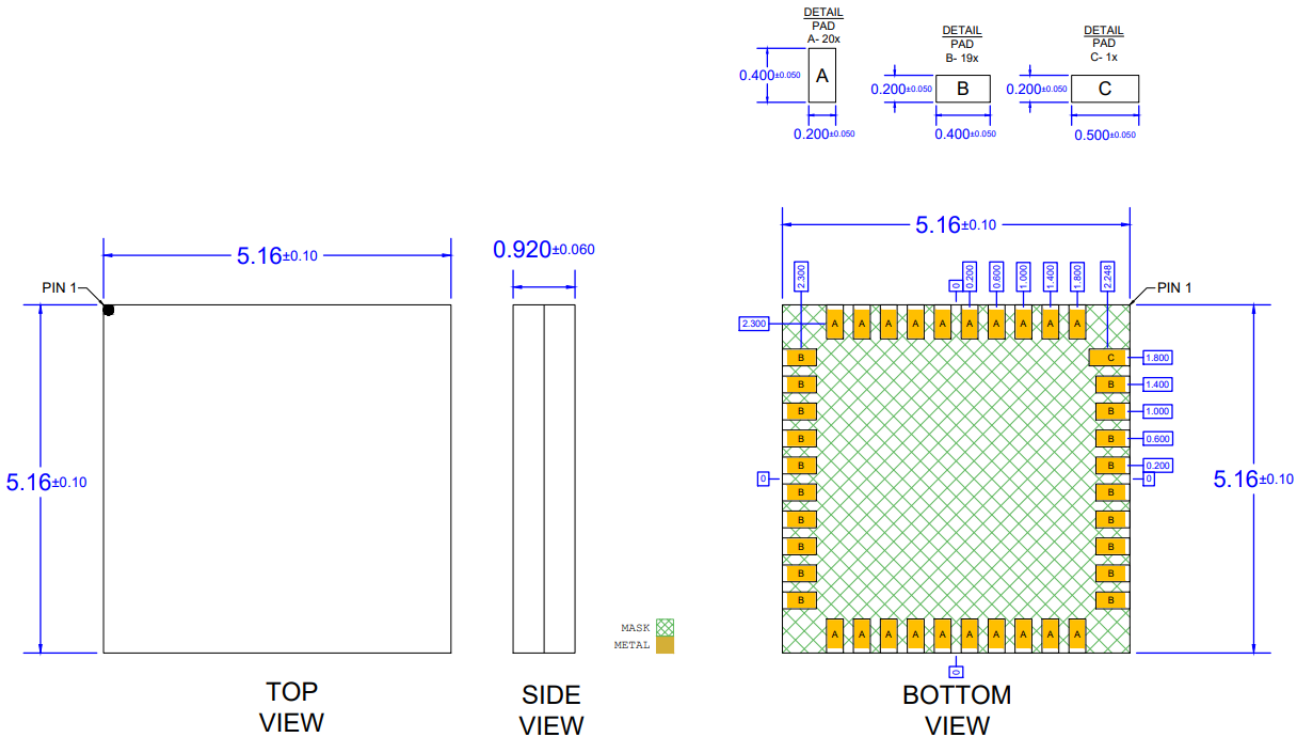
Layer	Cust Thickness	Calc Thickness	Primary Stack	Description
		0.0010		Taiyo 4000-HFX DI
Layer - 1		0.0020		1/4oz Mix (Std Plt)
	0.0039	0.0036	2113 - 59%	370H
Layer - 2		0.0012		1oz P/G
	0.0140	0.0142	0.0140 (2-7628)	370H
Layer - 3		0.0012		1oz Mix
		0.0049	106 - 71% / 1080 - 66%	370H
		0.0080	0.0080B (1-7628)	370H
		0.0049	1080 - 66% / 106 - 71%	370H
Layer - 4		0.0012		1oz Mix
	0.0140	0.0142	0.0140 (2-7628)	370H
Layer - 5		0.0012		1oz P/G
	0.0039	0.0037	2113 - 59%	370H
Layer - 6		0.0020		1/4oz Mix (Std Plt)
		0.0010		Taiyo 4000-HFX DI

10 Packaging & Ordering Information

10.1 40 Pin LGA IC Variant

The product packaging complies with IPC standard 6012D/DS Class 3A.

10.1.1 Package Dimensions



All dimensions are in millimeters [mm]

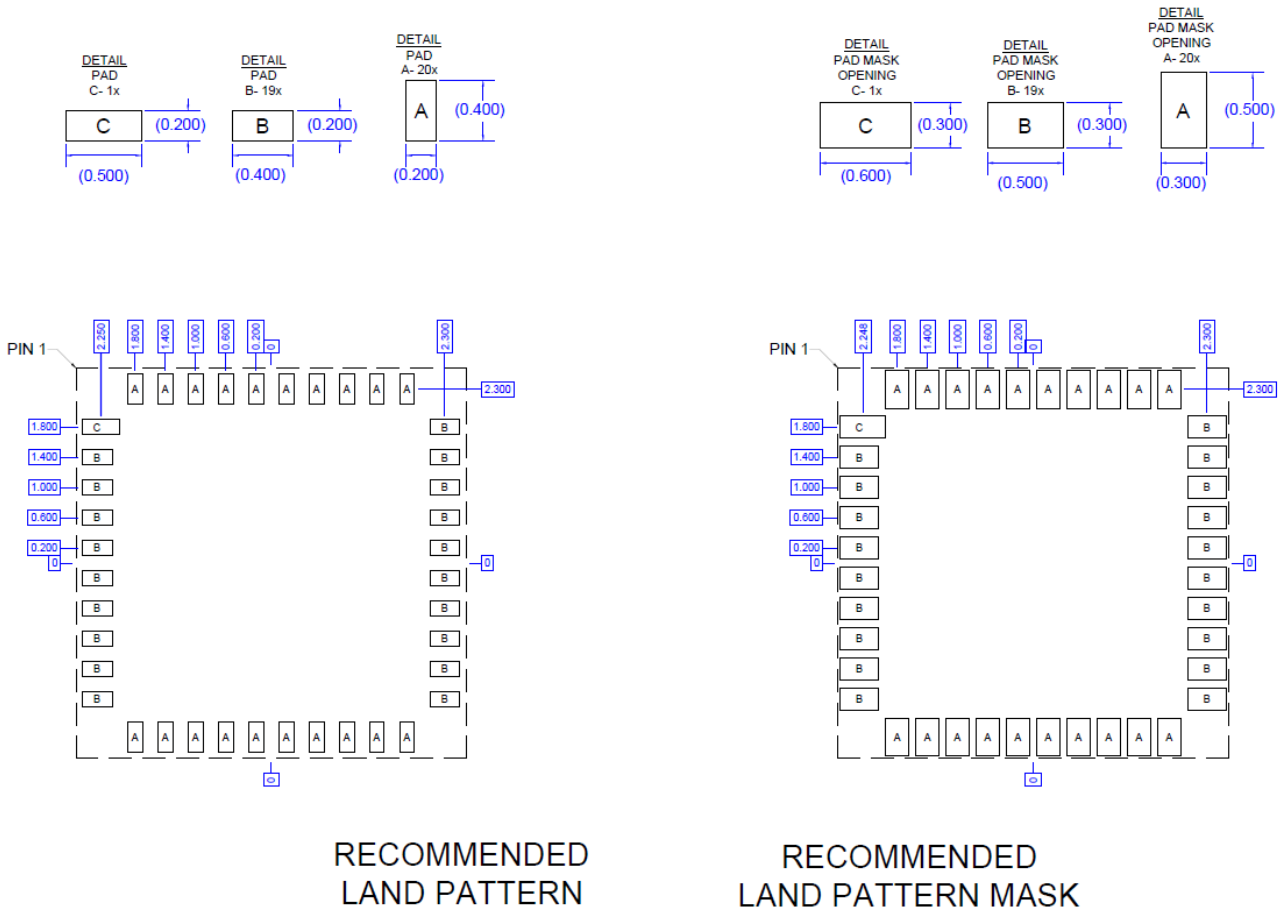
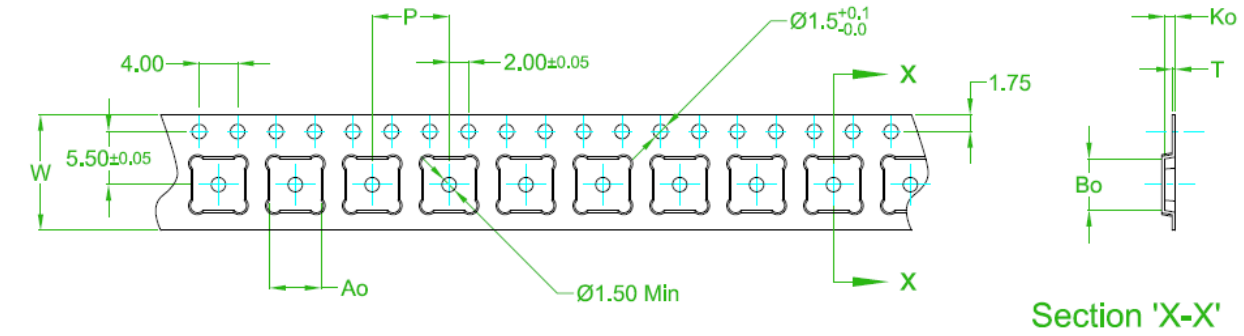


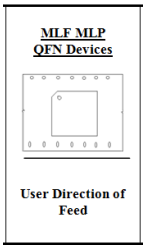
Figure 34: Package Dimensions LGA

All dimensions are in millimeters [mm]

10.1.2 Tape and Reel Packaging Information

Tape orientation and dimensions:





DIMENSIONS	
Ao	5.25 ±0.10
Bo	5.25 ±0.10
Ko	1.10 ±0.10
P	8.00 ±0.10
T	0.30 ±0.05
W	12.00 +0.30/-0.10

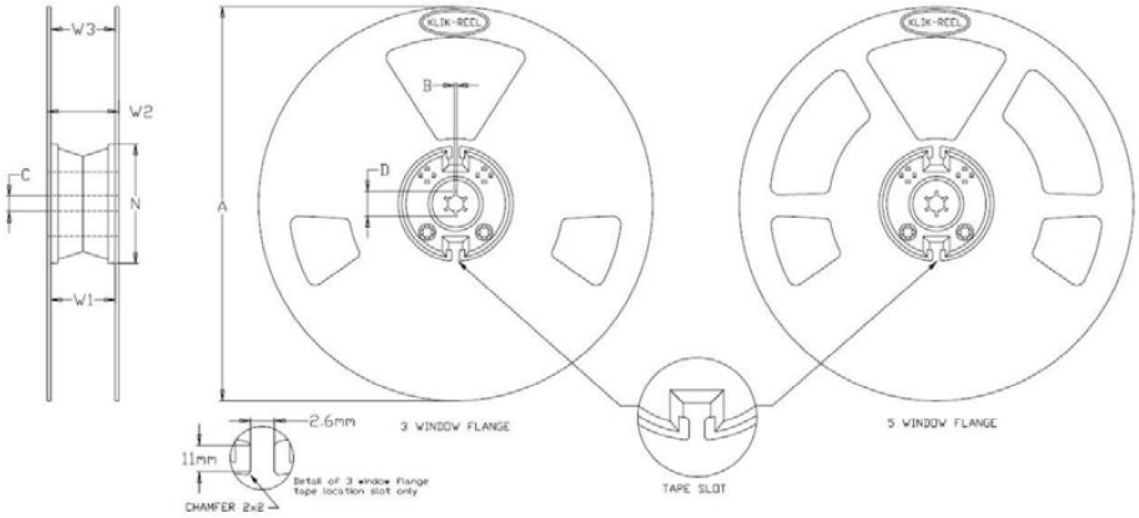
NOTES:

ALL DIMENSIONS IN MILLIMETRES.
10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ± 0.20.
MATERIAL: CONDUCTIVE POLYSTYRENE.
CAMBER NOT TO EXCEED 1.0mm IN 250mm.

Figure 35: LGA Tape Orientation and Dimensions

REEL INFORMATION: 330mm REEL (13")

Base material: High Impact Polystyrene with Integrated Antistatic Additive.
Surface resistivity: Antistatic with surface resistivity less than 1 x 10e12ohms per square.



Tape width	A Diameter	B (min)	C	D (min)	N Hub	W1 (max)	W2 (max)	W3 (min)	W3 (max)
12	330/380	1.5	13 +/-0.2	20.2	100 +/-1	12.4 +2/-0	18.4	11.9	15.4

Figure 36: LGA Reel Information

All dimensions and tolerances are fully compliant with EIA 481-C and are specified in millimeters (mm). Quantity per reel = 2500 units.

10.1.3 Device Package Marking

The diagram below shows the package markings for the DW3300Q.

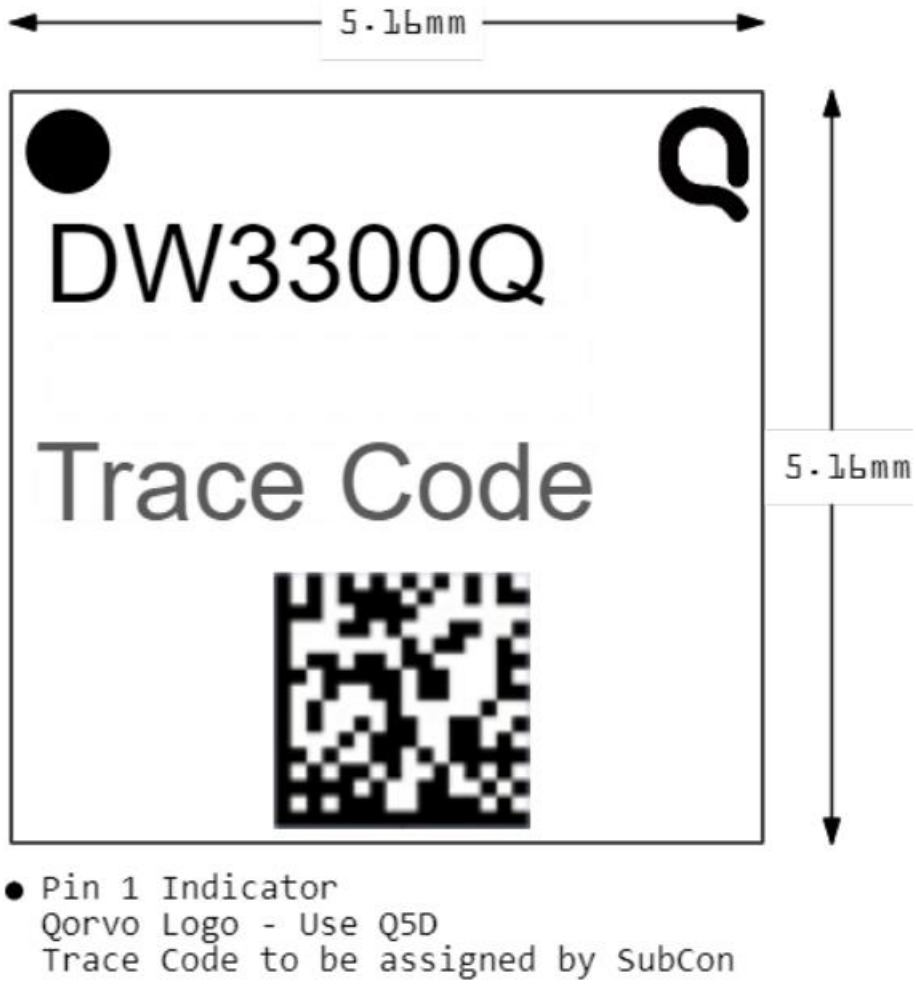


Figure 37: Device Package Marking

Legend:

DW3300Q	Part number
Trace Code	2DID

11 Glossary

Table 24: Glossary of Terms

Abbreviation	Full Title	Explanation
EIRP	Equivalent Isotropically Radiated Power	The amount of power that a theoretical isotropic antenna (which evenly distributes power in all directions) would emit to produce the peak power density observed in the direction of maximum gain of the antenna being used.
BPRF	Base PRF mode	64MHz PRF Mode
GPIO	General Purpose Input / Output	Pin of an IC that can be configured as an input or output under software control and has no specifically identified function.
IEEE	Institute of Electrical and Electronic Engineers	Is the world's largest technical professional society. It is designed to serve professionals involved in all aspects of the electrical, electronic, and computing fields and related areas of science and technology.
LoS	Line of Sight	Physical radio channel configuration in which there is a direct line of sight between the transmitter and the receiver.
Open Drain	Open Drain	A technique allowing a signal to be driven by more than one device. Generally, each device is permitted to pull the signal to ground but when not doing so it must allow the signal to float. Devices should not drive the signal so high as to prevent contention with devices attempting to pull it low.
NLoS	Non-Line of Sight	Physical radio channel configuration in which there is no direct line of sight between the transmitter and the receiver.
PLL	Phase Locked Loop	Circuit designed to generate a signal at a particular frequency whose phase is related to an incoming "reference" signal.
PPM	Parts Per Million	Used to quantify very small relative proportions. Just as 1% is one out of a hundred, 1 ppm is one part in a million.
RF	Radio Frequency	Generally used to refer to signals in the range of 3 kHz to 300 GHz. In the context of a radio receiver, the term is generally used to refer to circuits in a receiver before down-conversion takes place and in a transmitter after up-conversion takes place.
RTLS	Real Time Location System	System intended to provide information on the location of various items in real-time.
SFD	Start of Frame Delimiter	Defined in the context of the IEEE Std 802.15.4-2011 standard.
SPI	Serial Peripheral Interface	An industry standard method for interfacing between IC's using a synchronous serial scheme first introduced by Motorola.
TWR	Two Way Ranging	Method of measuring the physical distance between two radio units by exchanging messages between the units and noting the times of transmission and reception. Refer to Decawave Is Now Qorvo's website for further information.
TDoA	Time Difference of Arrival	Method of deriving information on the location of a transmitter. The time of arrival of a transmission at two physically different locations whose clocks are synchronized is noted and the difference in the arrival times provides information on the location of the transmitter. A few such TDoA measurements at different locations can be used to uniquely determine the position of the transmitter. Refer to Decawave Is Now Qorvo's website for further information.
PDoA	Phase Difference of Arrival	Method of determining the direction of propagation of a radio-frequency wave incident on an antenna array using the phase difference between the signal received on each antenna array element.

12 References

[1] IEEE Std 802.15.4-2011 or "IEEE Std 802.15.4™-2011" (Revision of IEEE Std 802.15.4-2006). IEEE Standard for Local and metropolitan area networks – Part 15.4: Low-Rate Wireless Personal Area Networks (LR-WPANs). IEEE Computer Society Sponsored by the LAN/MAN Standards Committee. Available from http://standards.ieee.org/

[2] IEEE Std 802.15.4-2015 or "IEEE Std 802.15.4™-2015" (Revision of IEEE Std 802.15.4-2011). IEEE Standard for Local and metropolitan area networks – Part 15.4: Low-Rate Wireless Personal Area Networks (LR-WPANs). IEEE Computer Society Sponsored by the LAN/MAN Standards Committee. Available from http://standards.ieee.org/

[3] IEEE Std 802.15.4™-2020 (Revision of IEEE Std 802.15.4-2015) "IEEE Standard for Low-Rate Wireless Networks". IEEE Computer Society Sponsored by the LAN/MAN Standards Committee. Available from http://standards.ieee.org/

[4] IEEE Std 802.15.4z™-2020 (Amendment to IEEE Std 802.15.4™-2020) "Amendment 1: Enhanced Ultra-Wideband (UWB) Physical Layers (PHYs) and Associated Ranging Techniques". IEEE Computer Society Sponsored by the LAN/MAN Standards Committee. Available from http://standards.ieee.org/

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU. This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Product Status

Marking	Product Status	Definition
ADVANCE INFO	Formative / In Design	Datasheet contains design specifications for product development. Specifications may change in any manner without notice.
PRELIMINARY	First Production	Datasheet contains preliminary data; supplementary data will be published later. Qorvo reserves the right to make changes at any time without notice to improve the design.
(none)	Full Production	Datasheet contains final specifications. Qorvo reserves the right to make changes at any time without notice to improve the design.
OBSOLETE	Not in Production	Datasheet contains specifications on a product that is discontinued. The datasheet is for reference information only.

Document History

Version	Date	Section	Changes
A	11/3/21		Initial PDE release
B	4/25/22		Updated Table 13 TX AC Power Characteristics with values moved to correct column. Removed reference to spi mode selection using GPIO5/6 not supported. Added rows for equivalent AoA accuracy and standard deviation. Added row for SPICLK SPI2 max frequency. Lowered SPI clk from 38MHz to 32MHz in Key Features on page 3. Lowered to 32MHz max SPI clk on Host Interface. Updated MSL LGA package update. Add min/max TBDs to peak current specs. Added EVB schematic and layout/stackup. Updated Apps circuit schematic with filters/switches. Removed references to DW3310Q non-PDoA variant. Added MSL3. Updated typ sensitivity measurements in Sec 5.4. Moved TX AC power to MAX column. Updated typ blocking measurements in 5.3. In sec 6.10 added 7th bit use.
C	9/30/22		Added RoHS compliance section on page 62. Updated Rx sensitivity measurement description of para 5.4 for clarity. Added Kyocera Xtal recommendation in 9.4, removed Rakon. Improved images for EVB schematic. Updated Device Packaging Marking. Added TX to RX typ switching speed in section 2. Added Packaging IPC standard to section 10.
D.1	11/22/22		Updated ESD; Updated TR13 from 4000 to 2500 pieces. Moved packaging note on 10.1. (Not released)
D	12/8/22		Updated orderable parts.
E	4/19/23		Added max currents, prepared for PR removing Preliminary header. Added RF port isolation spec + switching speed in para 5.11. Added note in APPS section for terminating unused RF port. Updated CDM from Class 3 to C3.
F	4/19/24		Changing % to degrees for Temperature monitoring in Table 14. Updating Tables 9/10 with conditions. Added RF1 default position in Figure 33.

Important Notices

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