GLF71320, GLF71321, GLF71322, GLF71323

4 A, Low R_{ON} I_QSmart™ Power Load Switch with Slew Rate Control

Product Specification

DESCRIPTION

The GLF7132x is an ultra-efficiency, 4 A rated, integrated load switch with integrated slew rate control.

The GLF7132x features an ultra-efficient I_QSmart™ technology that supports the lowest R_{ON}, quiescent current (I_Q) and shutdown current (I_{SD}) in the industry. Low R_{ON} reduces conduction losses, while low I_Q and I_{SD} solutions help designers to reduce parasitic leakage current, improve system efficiency, and increase battery lifetime.

The GLF7132x integrated slew rate control greatly enhances system reliability by mitigating bus voltage swings during switching events. Where uncontrolled switches can generate high inrush currents that result in voltage droop and/or bus reset events, the GLF7132x slew rate control specifically limits inrush current during turn-on to minimize voltage droop.

GLF7132x Load Switch device supports an industry leading wide input voltage range and helps to improve operating life and system robustness. Furthermore, one device can be used in multiple voltage rail applications which helps to simplify inventory management and reduces operating cost.

GLF7132x Load Switch device is small utilizing a chip scale package with 6 bumps in a 0.97 mm x 1.47 mm x 0.55 mm die size and a 0.5 mm pitch.

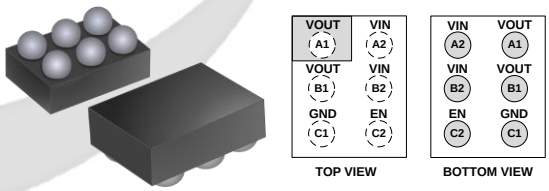
FEATURES

- Low R_{ON} : 15 mΩ Typ 5.5 V_{IN}
- Ultra-Low I_Q:
  3 nA Typ at 5.5 V_{IN} GLFL71320, GLF71321
  570 nA Typ at 5.5 V_{IN} GLFL71322, GLF71323
- Ultra-Low I_{SD}: 50 nA Typ at 5.5 V_{IN}
- I_{OUT} Max: 4 A
- Wide Input Range: 1.1 V to 5.5 V
  6 Vabs max
- Controlled Rise Time: 400 µs at 3.3 V_{IN}
- Internal EN Pull-Down or Pull-Up Resistor
- Integrated Output Discharge Switch
  GLF71321 and GLF71323
- Wide Operating Temperature Range:
  -40 °C ~ 85 °C
- HBM: 6 kV, CDM: 2 kV
- Ultra-Small: 0.97 mm x 1.47 mm WLCSP

APPLICATIONS

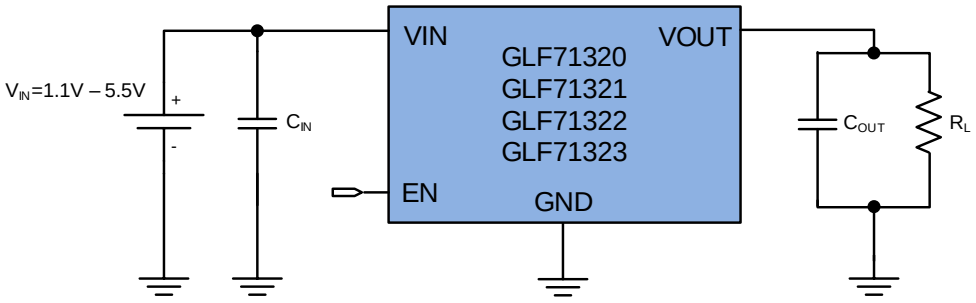
- Mobile Devices
- Data Storage, SSD
- Wearables
- Low Power Subsystems

PACKAGE



0.97 mm x 1.47 mm x 0.55 mm
0.5 mm pitch WLCSP

APPLICATION DIAGRAM



ALTERNATE DEVICE OPTIONS

Part Number	Top Mark	R_{ON} (Typ) at 5.5 V	Output Discharge	EN Activity
GLF71320	AA	15 mΩ	NA	High
GLF71321	BB	15 mΩ	80 Ω	High
GLF71322	CC	15 mΩ	NA	Low
GLF71323	DD	15 mΩ	80 Ω	Low

FUNCTIONAL BLOCK DIAGRAM

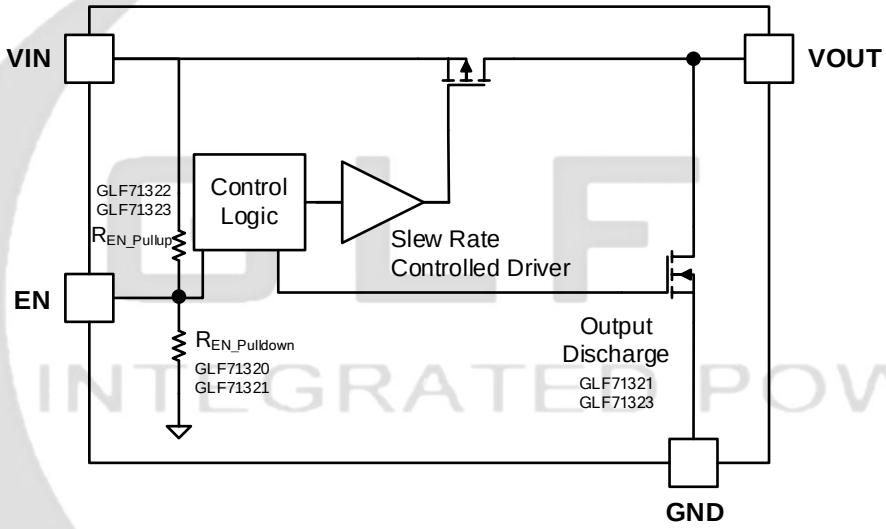


Figure 1. Functional Block Diagram

PIN CONFIGURATION

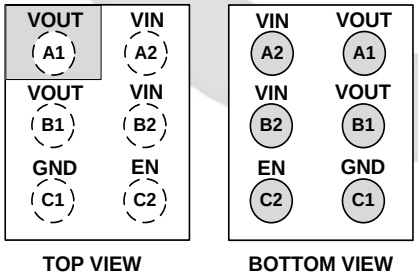


Figure 2. 0.97 mm x 1.47 mm x 0.55 mm WLCSP

PIN DEFINITION

Pin #	Name	Description
A1, B1	VOUT	Switch Output
A2, B2	VIN	Switch Input. Supply Voltage for IC
C1	GND	Ground
C2	EN	Enable to control the switch

ABSOLUTE MAXIMUM RATINGS

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions; extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{IN}, V_{OUT}, V_{EN}	Each Pin Voltage Range to GND		-0.3	6	V
I_{OUT}	Maximum Continuous Switch Current			4	A
P_D	Power Dissipation at T_A = 25 °C			1.2	W
T_{STG}	Storage Junction Temperature		-65	150	°C
T_A	Operating Temperature Range		-40	85	°C
θ_{JA}	Thermal Resistance, Junction to Ambient (Measured using 2S2P JEDEC std. PCB.)			85	°C/W
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22-A114	6		kV
		Charged Device Model, JESD22-C101	2		

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Max.	Unit
V_{IN}	Supply Voltage	1.1	5.5	V
T_A	Ambient Operating Temperature	-40	+85	°C

ELECTRICAL CHARACTERISTICS

V_{IN} = 1.1 V to 5.5 V, typical values are at V_{IN} = 3.3 V and T_A = 25 °C. Unless otherwise noted

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Basic Operation						
V_{IN}	Supply Voltage		1.1		5.5	V
I_Q	Quiescent Current GLF71320, GLF71321	EN = Enable, I_{OUT}=0 mA, V_{IN} = V_{EN} =5.5 V		3		nA
		EN = Enable, I_{OUT}=0 mA, V_{IN}=V_{EN}=5.5 V, T_A=85 °C (5)		10		
	Quiescent Current (1) GLF71322, GLF71323	EN = 0 V, I_{OUT}=0 mA, V_{IN} = 5.5 V		570		
		EN = 0 V, I_{OUT}=0 mA, V_{IN} = 5.5 V, T_A=85 °C (5)		810		
I_{SD}	Shut Down Current, GLF71320, GLF71321	EN = Disable, V_{OUT}= 0 V, V_{IN}= 1.1 V		9		nA
		EN = Disable, V_{OUT}= 0 V, V_{IN}= 1.8 V		11		
		EN = Disable, V_{OUT}= 0 V, V_{IN}= 3.3 V		16		
		EN = Disable, V_{OUT}= 0 V, V_{IN}= 4.5 V		20		
		EN = Disable, V_{OUT}= 0 V, V_{IN}= 5.5 V		50	100	
		EN = Disable, V_{OUT}= 0 V, V_{IN}= 5.5 V, T_A=55 °C (5)		250		
		EN = Disable, V_{OUT}= 0 V, V_{IN}= 5.5 V, T_A=85 °C (5)		1.7		µA
	Shut Down Current, GLF71322, GLF71323	EN = Disable, V_{OUT}=0 V, V_{IN} = V_{EN} =1.1 V		5		nA
		EN = Disable, V_{OUT}=0 V, V_{IN} = V_{EN} =1.8 V		6		
		EN = Disable, V_{OUT}=0 V, V_{IN} = V_{EN} =3.3 V		9		
		EN = Disable, V_{OUT}=0 V, V_{IN} = V_{EN} =4.5 V		18		
		EN = Disable, V_{OUT}=0 V, V_{IN} = V_{EN} =5.5 V		40	80	
		EN = Disable, V_{OUT}= 0 V, V_{IN} = V_{EN} =5.5 V, T_A=55 °C (5)		150		
		EN = Disable, V_{OUT}= 0 V, V_{IN} = V_{EN} =5.5 V, T_A=85 °C (5)		0.9		µA

ELECTRICAL CHARACTERISTICS (Continued)

V_{IN} = 1.1 V to 5.5 V, typical values are at V_{IN} = 3.3 V and T_A = 25 °C. Unless otherwise noted

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
R_{ON}	On-Resistance	V_{IN}=5.5 V I_{OUT}= 500 mA	T_A=25 °C		15	17	mΩ
			T_A=85 °C (5)		17		
		V_{IN}=3.3 V, I_{OUT}= 500 mA	T_A=25 °C		18	21	
			T_A=85 °C (5)		21		
		V_{IN}=1.8 V, I_{OUT}= 300 mA	T_A=25 °C		28		
		V_{IN}=1.1 V, I_{OUT}= 100 mA	T_A=25 °C		55		
R_{DSC}	Output Discharge Resistance	EN=Disable, I_{FORCE}= 10 mA, GLF71321, GLF71323			80	100	Ω
V_{IH}	EN Input Logic High Voltage	V_{IN}=1.1 - 1.8 V		0.9			V
		V_{IN}=1.8 - 5.5 V		1.2			
V_{IL}	EN Input Logic Low Voltage	V_{IN}=1.1 - 1.8 V				0.3	
		V_{IN}=1.8 - 5.5 V				0.4	
R_{EN}	EN Pull-down / Pull-up Resistance	EN=5.5 V, GLF71320, GLF71321 EN=0 V, GLF71322, GLF71323		7	10.1	13	MΩ
I_{EN}	EN Current					0.8	µA
Switching Characteristics							
t_{dON}	Turn-On Delay(2)	R_{OUT}=150 Ω, C_{OUT}=0.1 µF			250		µs
t_R	V_{OUT} Rise Time(2)				400		µs
t_{dON}	Turn-On Delay(2,5)	R_{OUT}=500 Ω, C_{OUT}=0.1 µF			240		µs
t_R	V_{OUT} Rise Time(2,5)				390		µs
t_{dOFF}	Turn-Off Delay(3,4,5)	R_{OUT}=10 Ω, C_{OUT}=0.1 µF, GLF71320, GLF71322			0.6		µs
t_F	V_{OUT} Fall Time(3,4,5)				2.3		µs
t_{dOFF}	Turn-Off Delay(3,4,5)	R_{OUT}=10 Ω, C_{OUT}=0.1 µF, GLF71321, GLF71323			0.4		µs
t_F	V_{OUT} Fall Time(3,4,5)				1.5		µs
t_{dOFF}	Turn-Off Delay(3,4,5)	R_{OUT}=500 Ω, C_{OUT}=0.1 µF, GLF71320, GLF71322			3.7		µs
t_F	V_{OUT} Fall Time(3,4,5)				106		µs
t_{dOFF}	Turn-Off Delay(3,4,5)	R_{OUT}=500 Ω, C_{OUT}=0.1 µF, GLF71321, GLF71323			1.3		µs
t_F	V_{OUT} Fall Time(3,4,5)				16		µs

Notes:
1. I_Q for GLF71322 / GLF71323 includes the shunt current through the internal pull-up resistor R_{EN} of EN Pin.
2. $t_{ON} = t_{dON} + t_R$
3. $t_{OFF} = t_{dOFF} + t_F$
4. Output discharge path is enabled during off.
5. By design; characterized, not production tested.

TIMING DIAGRAM

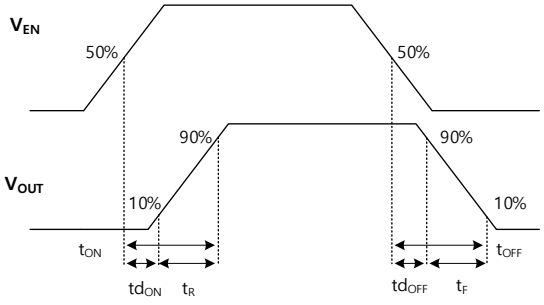


Figure 3. Timing Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

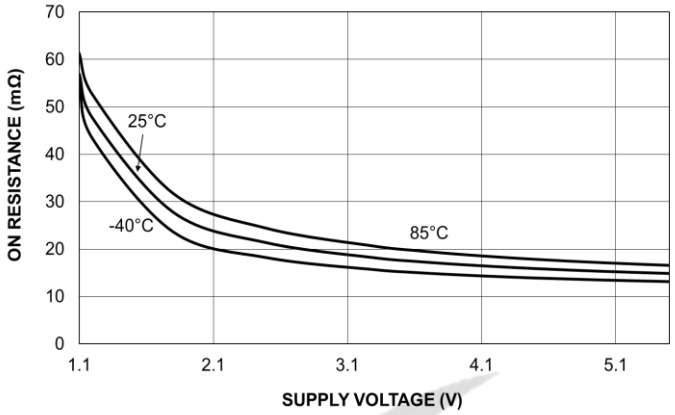


Figure 4. On-Resistance vs. Supply Voltage

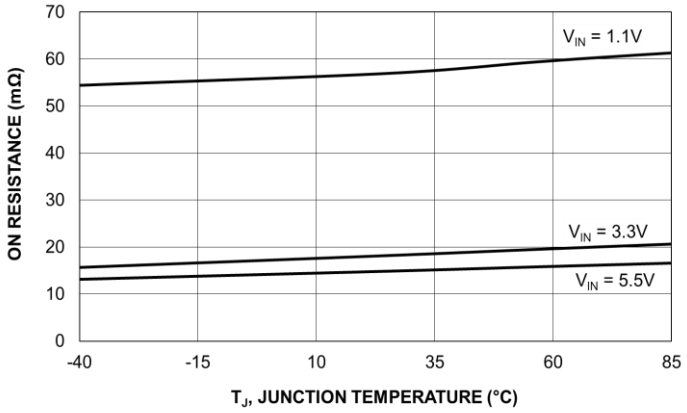


Figure 5. On-Resistance vs. Temperature

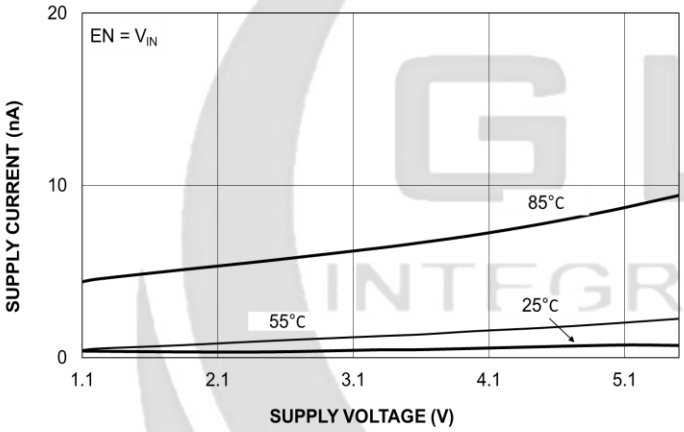


Figure 6. Quiescent Current vs. Supply Voltage GLF71320 / GLF71321

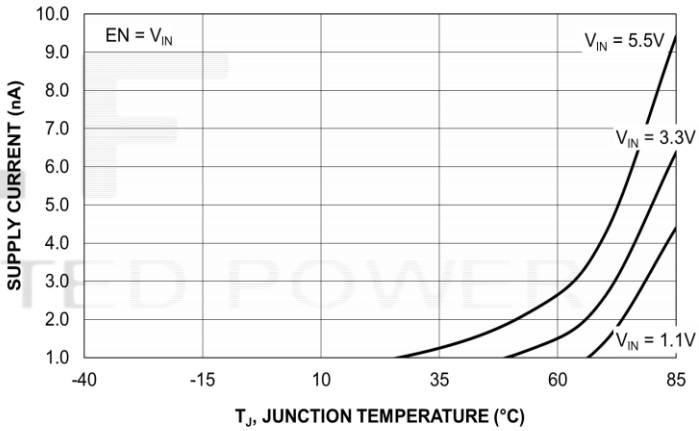


Figure 7. Quiescent Current vs. Temperature GLF71320 / GLF71321

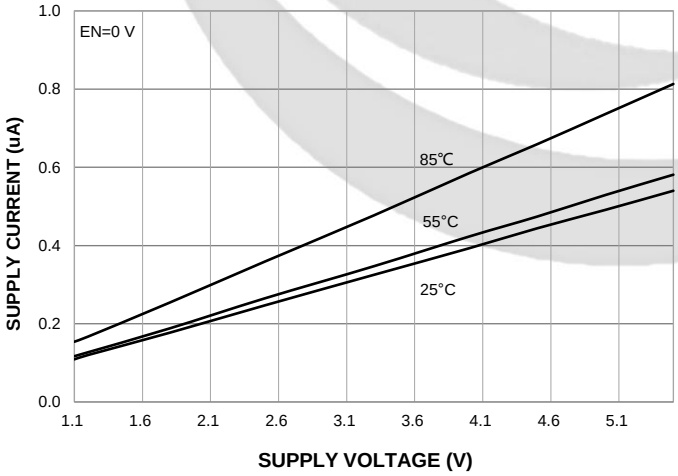


Figure 8. Quiescent Current vs. Supply Voltage GLF71322 / GLF71323

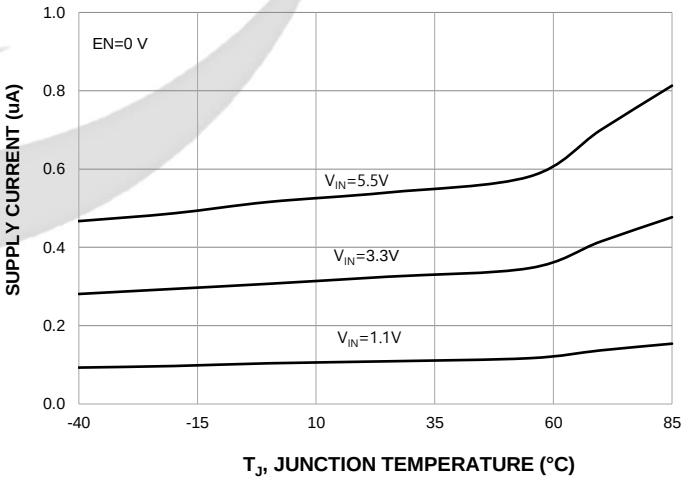


Figure 9. Quiescent Current vs. Temperature GLF71322 / GLF71323

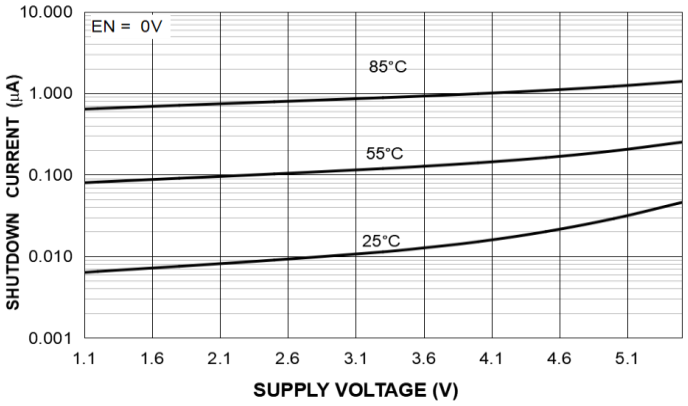


Figure 10. Shutdown Current vs. Supply Voltage GLF71320 / GLF71321

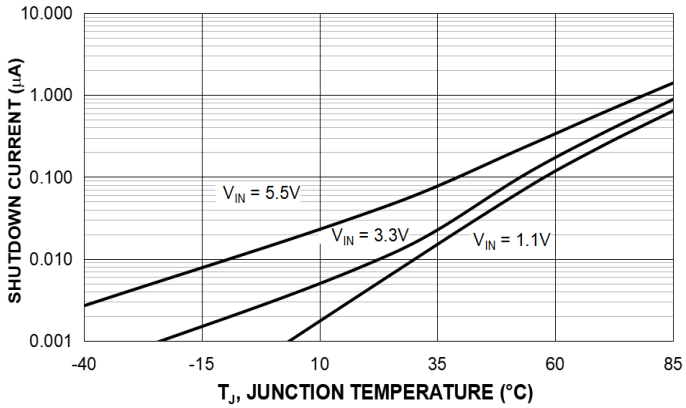


Figure 11. Shutdown Current vs. Temperature GLF71320 / GLF71321

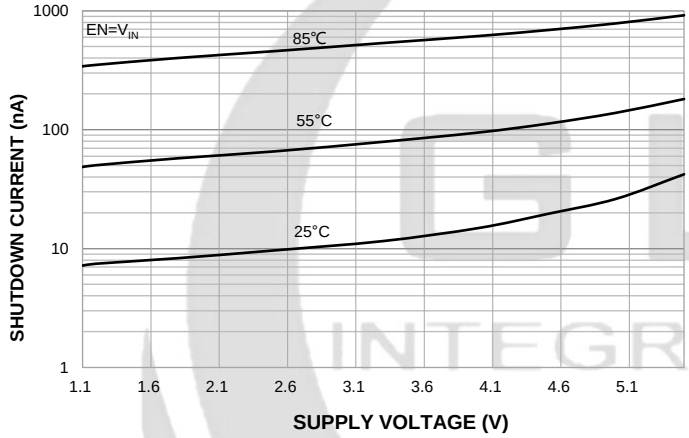


Figure 12. Shutdown Current vs. Supply Voltage GLF71322 / GLF71323

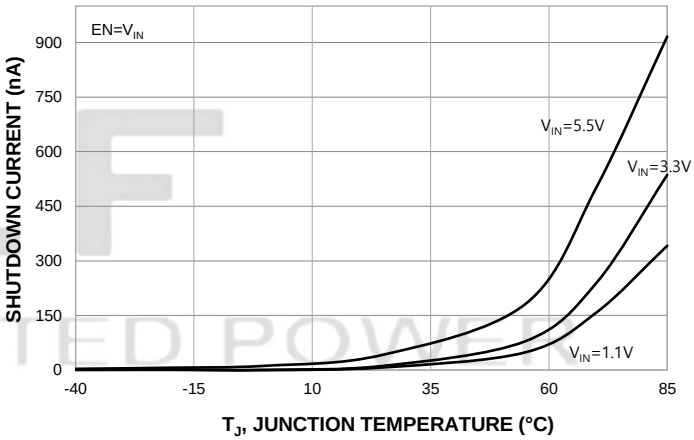


Figure 13. Shutdown Current vs. Supply Voltage GLF71322 / GLF71323

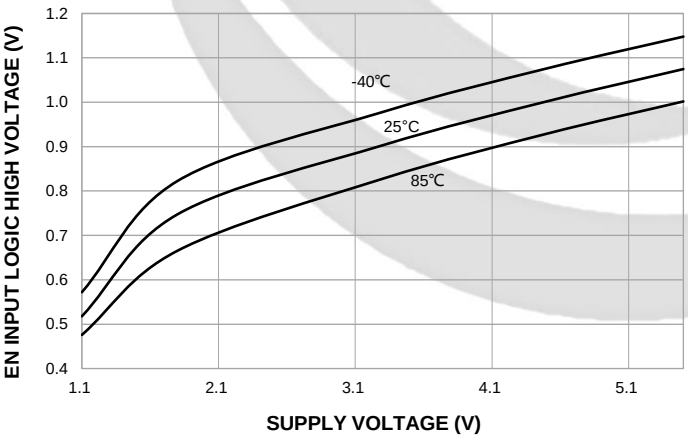


Figure 14. EN Input Logic High Threshold

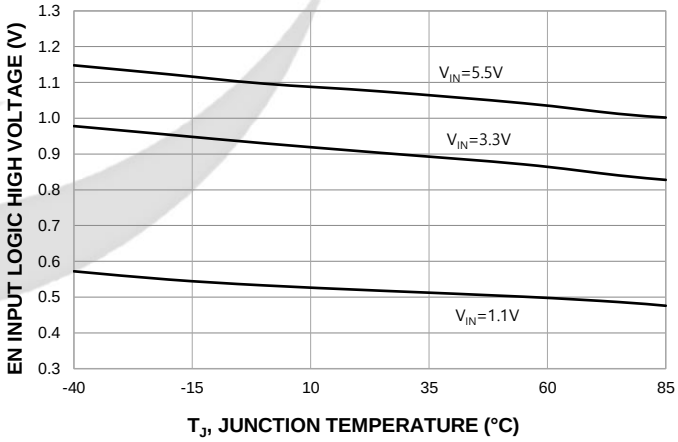


Figure 15. EN Input Logic High Threshold Vs. Temperature

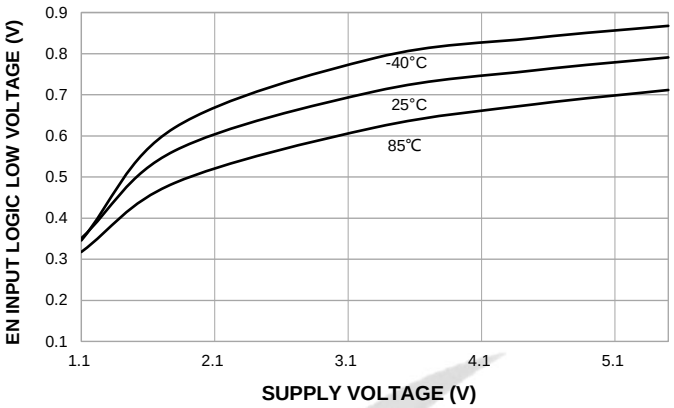


Figure 16. EN Input Logic Low Threshold

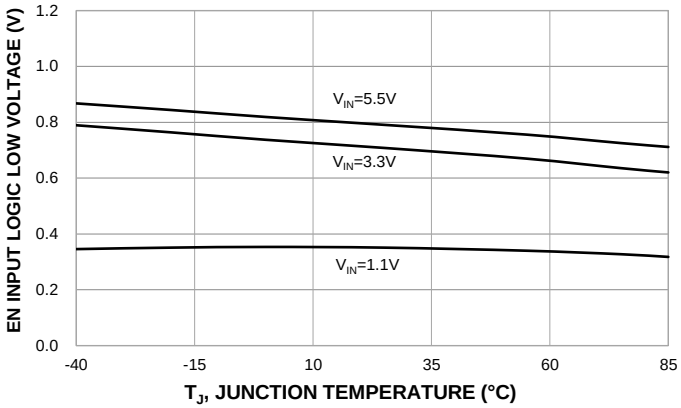


Figure 17. EN Input Logic Low Threshold Vs. Temperature

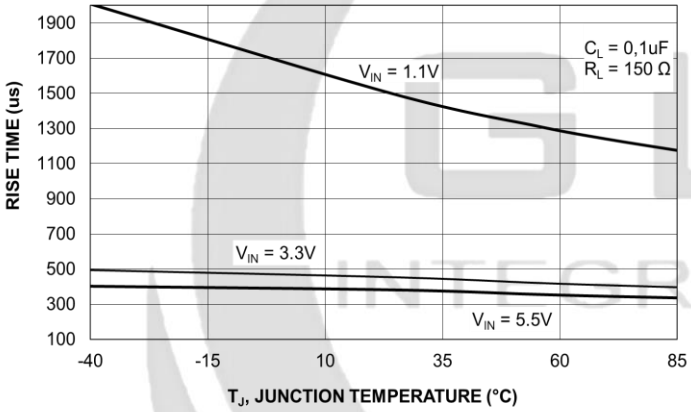


Figure 18. V_{OUT} Rise Time vs. Temperature

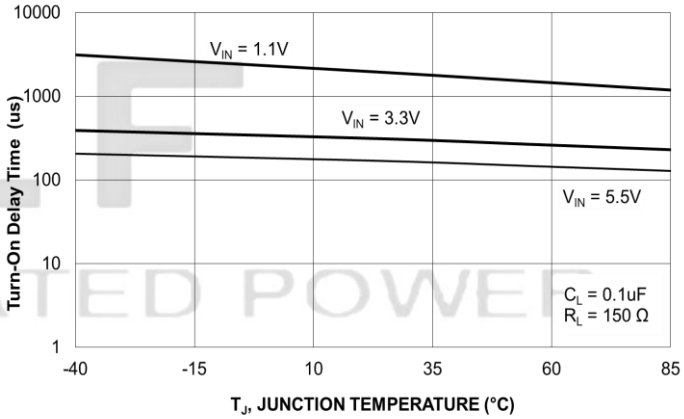


Figure 19. Turn-On Delay Time vs. Temperature

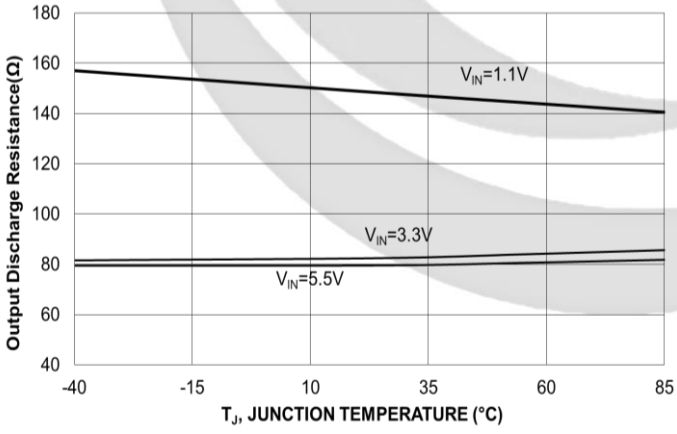


Figure 20. V_{OUT} Discharge Resistance vs. Temperature GLF71321 / GLF71323

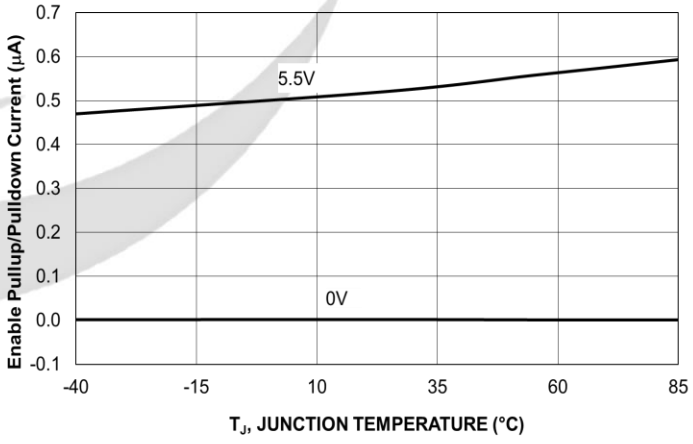


Figure 21. Enable Pullup / Pulldown Current vs. Temperature

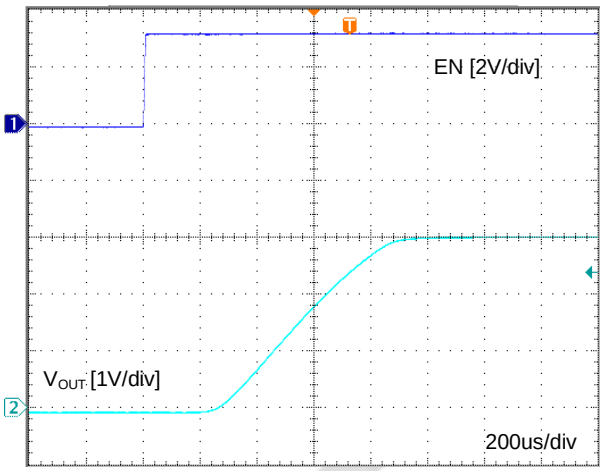


Figure 22. Turn-On Response, GLF71320 / GLF71321
V_{IN}=3.3 V, C_{IN}=10 µF, C_{OUT}=0.1 µF, R_L=10 Ω

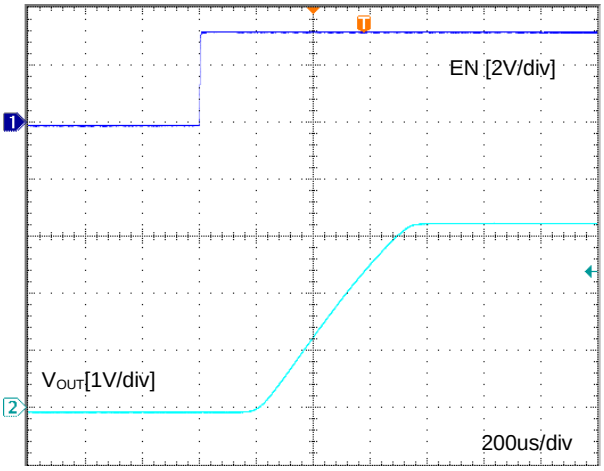


Figure 23. Turn-On Response, GLF71320 / GLF71321
V_{IN}=3.3 V, C_{IN}=10 µF, C_{OUT}=0.1 µF, R_L=500 Ω

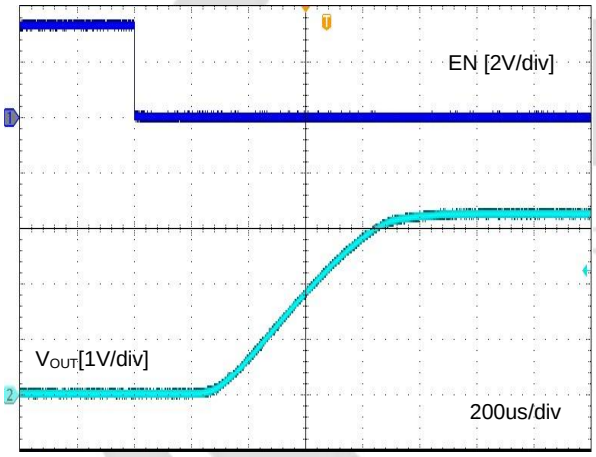


Figure 24. Turn-On Response, GLF71322 / GLF71323
V_{IN}=3.3 V, C_{IN}=10 µF, C_{OUT}=0.1 µF, R_L=10 Ω

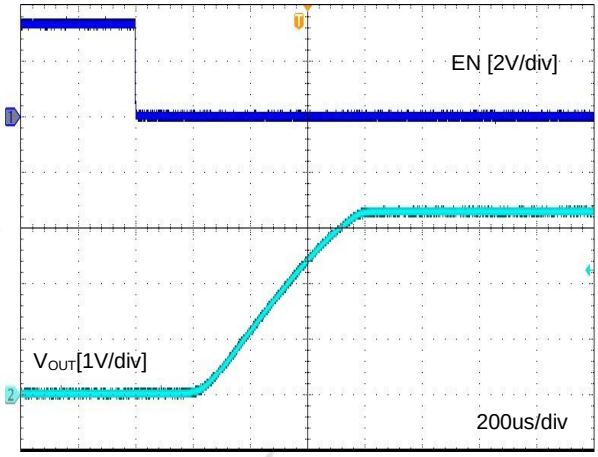


Figure 25. Turn-On Response, GLF71322 / GLF71323
V_{IN}=3.3 V, C_{IN}=10 µF, C_{OUT}=0.1 µF, R_L=500 Ω

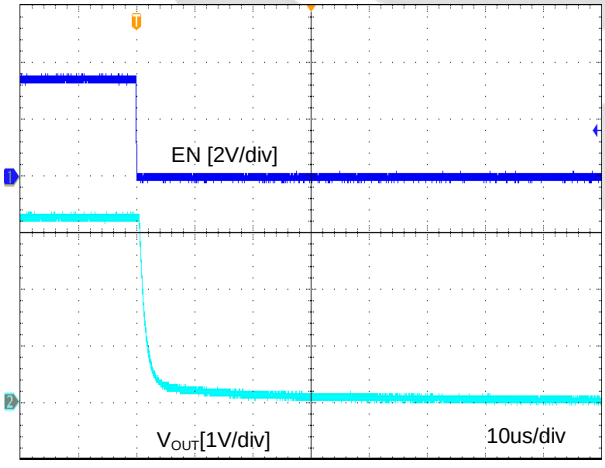


Figure 26. Turn-Off Response, GLF71320
V_{IN}=3.3 V, C_{IN}=10 µF, C_{OUT}=0.1 µF, R_L=10 Ω

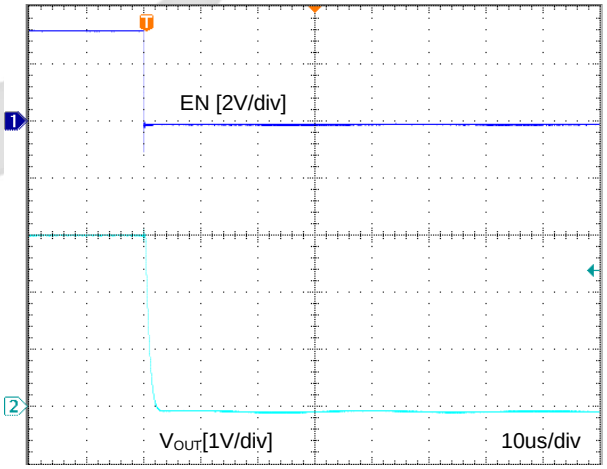


Figure 27. Turn-Off Response, Output Discharge, GLF71321
V_{IN}=3.3 V, C_{IN}=10 µF, C_{OUT}=0.1 µF, R_L=10 Ω

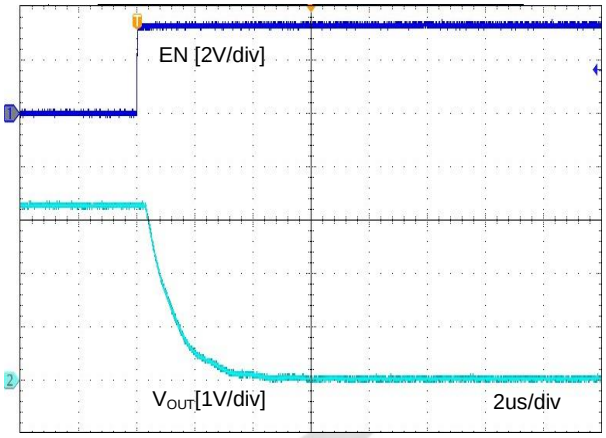


Figure 28. Turn-Off Response, GLF71322
V_{IN}=3.3 V, C_{IN}=10 µF, C_{OUT}=0.1 µF, R_L=10 Ω

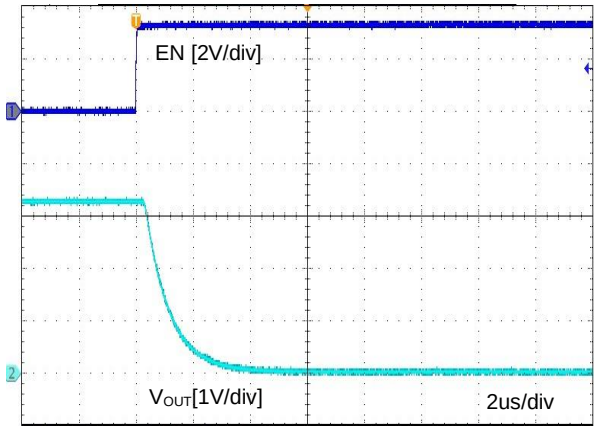


Figure 29. Turn-Off Response, Output Discharge, GLF71323
V_{IN}=3.3 V, C_{IN}=10 µF, C_{OUT}=0.1 µF, R_L=10 Ω

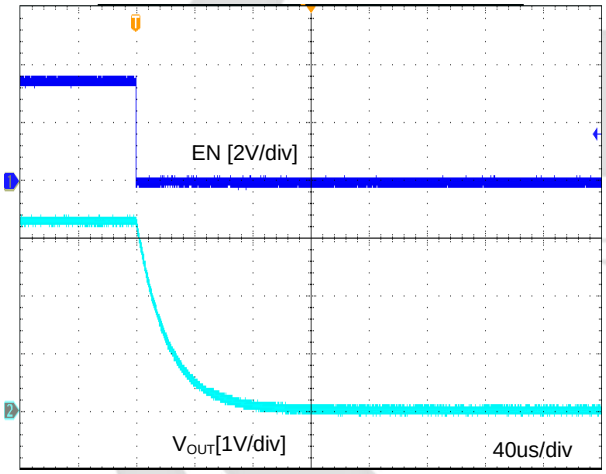


Figure 30. Turn-Off Response, GLF71320
V_{IN}=3.3 V, C_{IN}=10 µF, C_{OUT}=0.1 µF, R_L=500 Ω

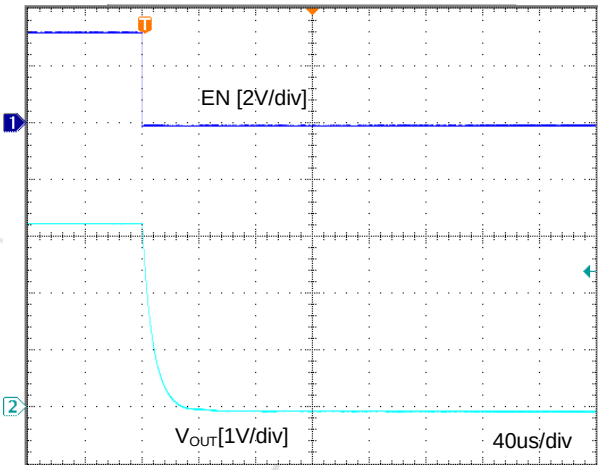


Figure 31. Turn-Off Response, Output Discharge, GLF71321
V_{IN}=3.3 V, C_{IN}=10 µF, C_{OUT}=0.1 µF, R_L=500 Ω

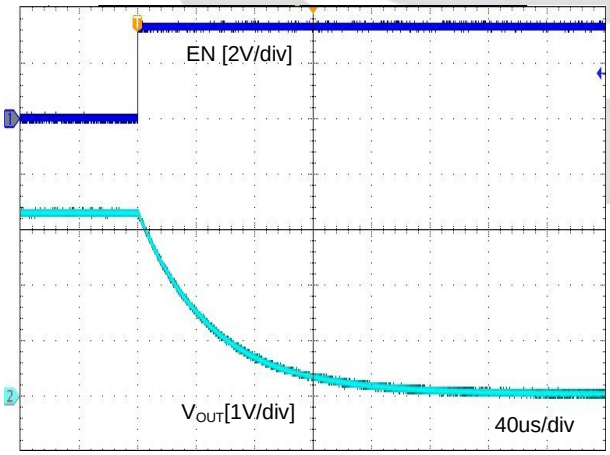


Figure 32. Turn-Off Response, GLF71322
V_{IN}=3.3 V, C_{IN}=10 µF, C_{OUT}=0.1 µF, R_L=500 Ω

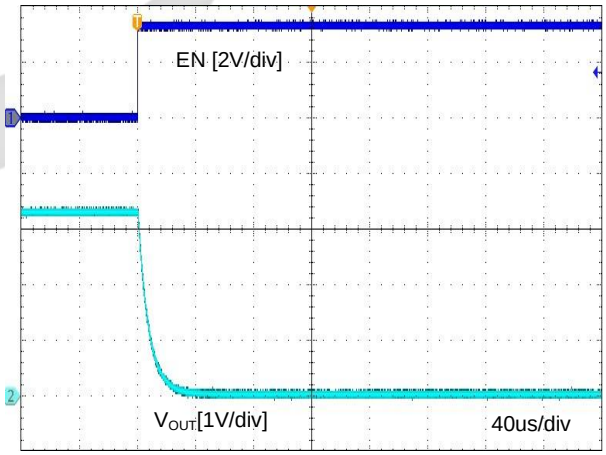


Figure 33. Turn-Off Response, Output Discharge, GLF71323
V_{IN}=3.3 V, C_{IN}=10 µF, C_{OUT}=0.1 µF, R_L=500 Ω

APPLICATION INFORMATION

The GLF7132x family of devices are integrated 4 A, Ultra-efficient I_QSmart™ Load Switch devices with a fixed slew rate control to limit the inrush current during turn on. Each device is capable of operating over a wide input range from 1.1 V to 5.5 V with very low on-resistance to reduce conduction loss. In the off state, these devices consume very low leakage current to avoid unwanted standby current and save limited input power. The package is a 0.97 mm x 1.47 mm x 0.55 mm wafer level chip scale package, saving space in compact applications. It is constructed using 6 bumps, with a 0.5 mm pitch for manufacturability.

Input Capacitor

The GLF7132x family of devices do not require an input capacitor. However, to reduce the voltage drop on the input power rail caused by transient inrush current at start-up, a 0.1µF capacitor is recommended to be placed close to the V_{IN} pin. A higher input capacitor value can be used to further attenuate the input voltage drop.

Output Capacitor

The GLF7132x family of devices do not require an output capacitor. However, use of an output capacitor is recommended to mitigate voltage undershoot on the output pin when the switch is turning off. Undershoot can be caused by parasitic inductance from board traces or intentional load inductances. If load inductances do exist, use of an output capacitor can improve output voltage stability and system reliability. The C_{OUT} capacitor should be spaced close to the VOUT and GND pins.

EN pin

The GLF71320 and GLF71321 can be activated by EN pin high level and GLF71322 and GLF71323 by EN pin low level. Note that the EN pin has an internal pull-down or pull-up resistor to help pull the main switch to a known “off state” when no EN signal is applied from an external controller.

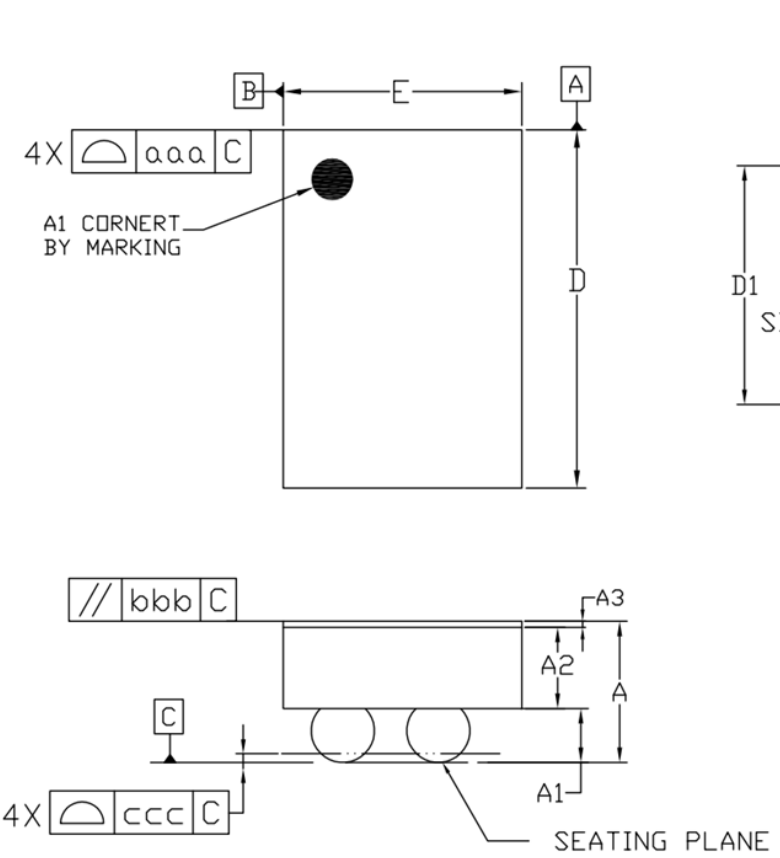
Output Discharge Function

The GLF71321 and GLF71323 have an internal discharge N-channel FET switch on the VOUT pin. When EN signal turns the main power FET to an off state, the N-channel switch turns on to discharge an output capacitor quickly.

Board Layout

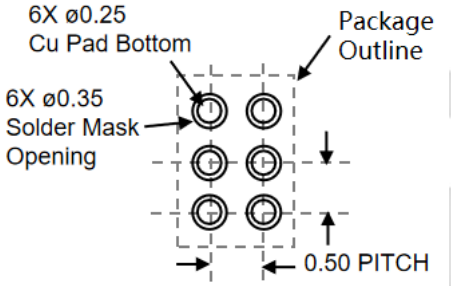
All traces should be as short as possible to minimize parasitic inductance effects. Wide traces for VIN, VOUT, and GND will help reduce voltage drops and parasitic effects during dynamic operation as well as improve the thermal performance at high load currents.

PACKAGE OUTLINE



Dimensional Ref.			
REF.	Min.	Nom.	Max.
A	0.500	0.550	0.600
A1	0.225	0.250	0.275
A2	0.250	0.275	0.300
A3	0.020	0.025	0.030
D	1.460	1.470	1.485
E	0.960	0.970	0.985
D1	0.950	1.000	1.050
E1	0.450	0.500	0.550
b	0.260	0.310	0.360
e	0.500 BSC		
SD	0.000 BSC		
SE	0.250 BSC		
Tol. of Form&Position			
aaa	0.10		
bbb	0.10		
ccc	0.05		
ddd	0.05		

Recommended Footprint

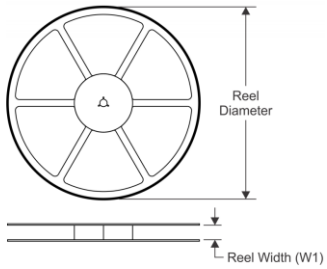


Notes

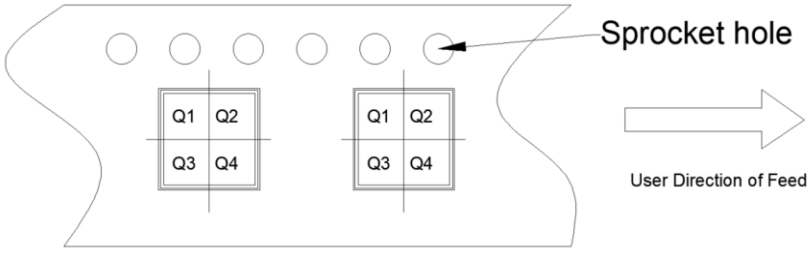
1. ALL DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGRESS)
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.
3. A3: BACKSIDE LAMINATION

TAPE AND REEL INFORMATION

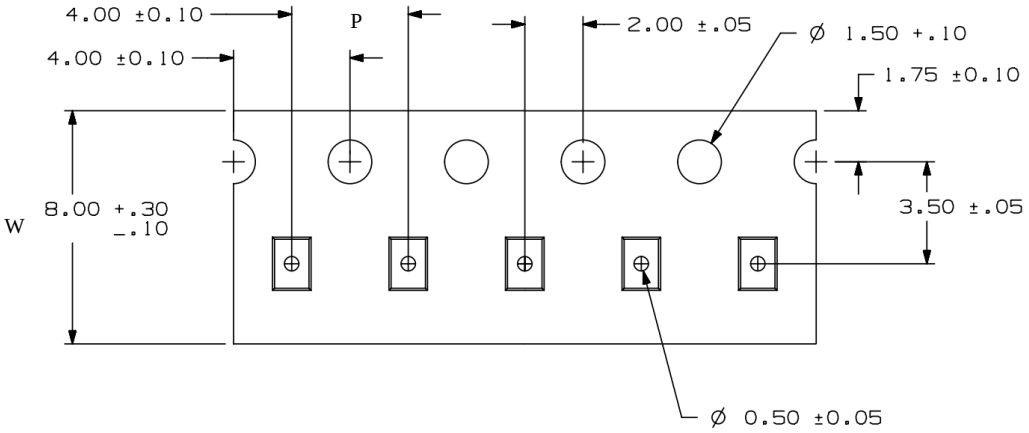
REEL DIMENSIONS

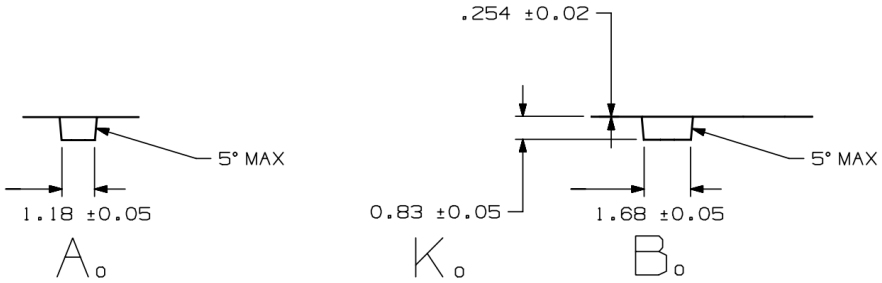


QUADRANT ASSIGNMENTS PIN 1 ORIENTATION TAPE



TAPE DIMENSIONS





Device	Package	Pins	SPQ	Reel Diameter (mm)	Reel Width W1	A0	B0	K0	P	W	Pin1
GLF71320	WLCSP	6	3000	180	9	1.18	1.68	0.83	4	8	Q1
GLF71321	WLCSP	6	3000	180	9	1.18	1.68	0.83	4	8	Q1
GLF71322	WLCSP	6	3000	180	9	1.18	1.68	0.83	4	8	Q1
GLF71323	WLCSP	6	3000	180	9	1.18	1.68	0.83	4	8	Q1

Remark:

A0: Dimension designed to accommodate the component width

B0: Dimension designed to accommodate the component length

C0: Dimension designed to accommodate the component thickness

W: Overall width of the carrier tape

P: Pitch between successive cavity centers

SPECIFICATION DEFINITIONS

Document Type	Meaning	Product Status
Target Specification	This is a target specification intended to support exploration and discussion of critical needs for a proposed or target device. Spec limits including typical, minimum, and maximum values are desired, or target, limits. GLF reserves the right to change limits at any time without warning or notification. A target specification in no way guarantees future production of the device in question.	Design / Development
Preliminary Specification	This is a draft version of a product specification. The specification is still under internal review and subject to change. GLF reserves the right to change the specification at any time without warning or notification. A preliminary specification in no way guarantees future production of the device in question.	Qualification
Product Specification	This document represents the anticipated production performance characteristics of the device.	Production

DISCLAIMERS

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