Features

- ESD Protect for 8 high-speed I/O channels
- Provide ESD protection for each channel to
  IEC 61000-4-2 (ESD) ±26kV (air), ±20kV (contact)
  IEC 61000-4-5 (Lightning) 14A (8/20μs)
- **For low operating voltage of 3.3V and below**
- **Low capacitance: 1.5pF typical**
- Fast turn-on and low clamping voltage
- Array of ESD rated diodes with internal equivalent TVS (Transient Voltage Suppression) diode
- Solid-state silicon-avalanche and active circuit triggering technology
- Simplified layout for high-speed differential signaling channels
- ***Green part***

Applications

- USIT Interface
- LVDS interface
- Monitors and Flat Panel Displays
- Video Graphics Cards
- Notebook and PC Computers

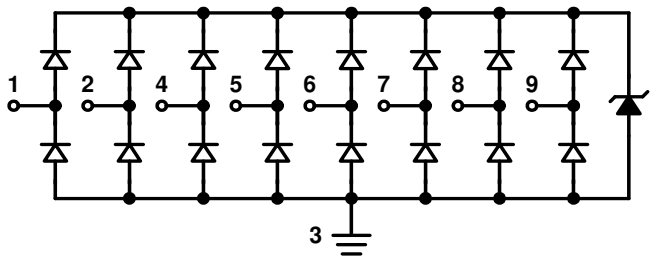
Description

AZ1013-08F is a design which includes ESD rated clamping cell arrays to protect high speed data interfaces. The AZ1013-08F has been specifically designed to protect sensitive components which are connected to data and transmission lines from over-voltage damage caused by Electrostatic Discharging (ESD) and Lightning.

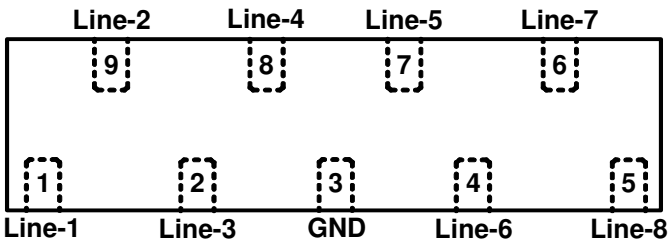
AZ1013-08F is a unique design which includes ESD rated, low capacitance steering diodes and a unique design of clamping cell which is an equivalent TVS diode in a single package. During transient conditions, the steering diodes direct the transient to either the internal ESD line or ground line. The internal unique design of clamping cell prevents over-voltage on the internal ESD line and on the I/O line, which is protecting any downstream components.

AZ1013-08F may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 (±15kV air, ±8kV contact discharge).

Circuit Diagram



Pin Configuration



DFN3810P9E
(Top View)

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS			
PARAMETER	**SYMBOL**	**RATING**	**UNITS**
Peak Pulse Current (tp = 8/20μs)	I_{PP}	14	A
Operating Supply Voltage	V_{DC}	3.6	V
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD-1} V_{ESD-2}	±26 ±20	kV
Lead Soldering Temperature	T_{SOL}	260 (10 sec.)	°C
Operating Temperature	T_{OP}	-55 to +85	°C
Storage Temperature	T_{STO}	-55 to +150	°C

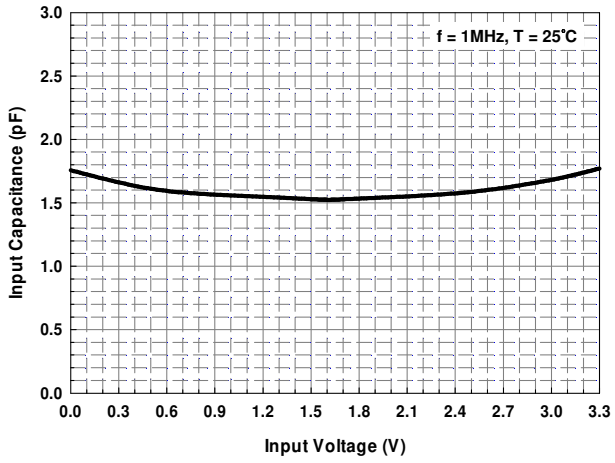
ELECTRICAL CHARACTERISTICS						
PARAMETER	**SYMBOL**	**CONDITIONS**	**MINI**	**TYP**	**MAX**	**UNITS**
Reverse Stand-Off Voltage	V_{RWM}	Pin-1, -2, -4, -5, -6, -7, -8, -9 to pin-3, T = 25 °C.			3.3	V
Reverse Leakage Current	$I_{CH-Leak}$	$V_{Pin-1,-2,-4,-5,-6,-7,-8,-9}$ = 3.3V, V_{Pin-3} = 0V, T = 25 °C.			1	μA
Reverse Breakdown Voltage	V_{BV}	I_{BV} = 1mA, pin-1, -2, -4, -5, -6, -7, -8, -9 to pin-3, T = 25 °C.	4.5			V
Forward Voltage	V_F	I_F = 15mA, pin-3 to pin-1, -2, -4, -5, -6, -7, -8, -9, T = 25 °C.	0.6		1.2	V
Surge Clamping Voltage	$V_{CL-surge}$	I_{PP} = 5A, tp = 8/20μs, any I/O pin to Ground, T = 25 °C.		6.0		V
ESD Clamping Voltage (Note 1)	V_{clamp}	IEC 61000-4-2 +8kV (I_{TLP} = 16A), Contact mode, any I/O pin to Ground, T = 25 °C.		8.2		V
ESD Dynamic Turn-on Resistance	$R_{dynamic}$	IEC 61000-4-2 0~+8kV, T = 25 °C, Contact mode, any I/O pin to Ground.		0.2		Ω
Channel Input Capacitance	C_{IN}	V_{pin-3} = 0V, V_{IN} = 1.65V, f =1MHz, T = 25 °C, any I/O pin to Ground.		1.5	2.0	pF
Channel to Channel Input Capacitance	C_{CROSS}	V_{pin-3} = 0V, V_{IN} = 1.65V, f =1MHz, T = 25 °C, between I/O pins.		0.12	0.2	pF

Note 1: ESD Clamping Voltage was measured by Transmission Line Pulsing (TLP) System.

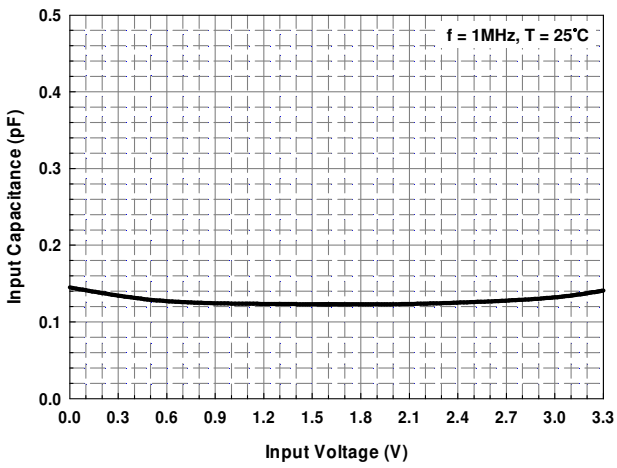
TLP conditions: Z_0= 50Ω, t_p= 100ns, t_r= 1ns.

Typical Characteristics

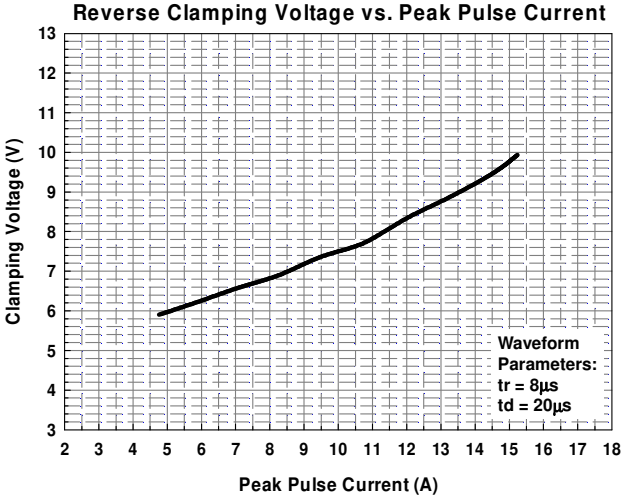
Typical Variation of C_{IN} vs. V_{IN}



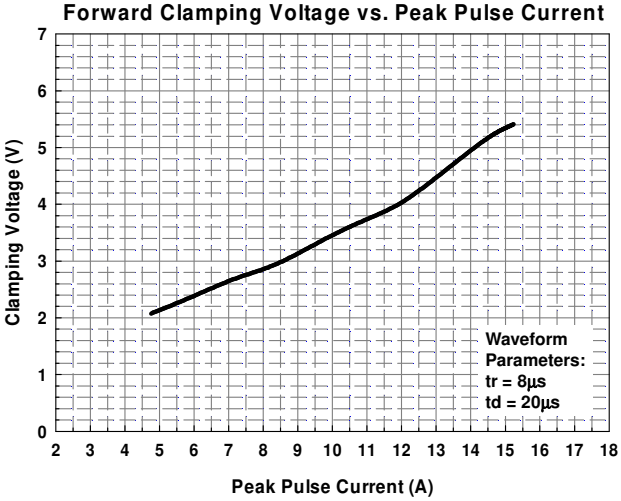
Typical Variation of $C_{IO\text{-}to\text{-}IO}$ vs. V_{IN}



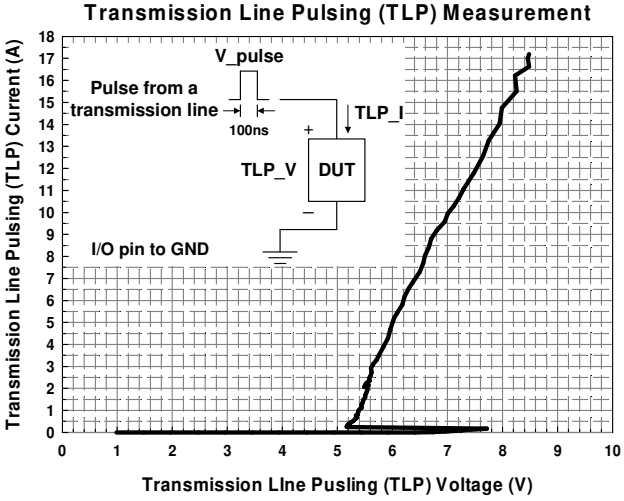
Reverse Clamping Voltage vs. Peak Pulse Current



Forward Clamping Voltage vs. Peak Pulse Current



Transmission Line Pulsing (TLP) Measurement



Applications Information

The AZ1013-08F is designed to protect 8 high-speed data lines from transient over-voltage (such as ESD stress pulse). The device connection of AZ1013-08F is shown in the Fig. 1. In Fig. 1, the 8 protected high-speed data lines are connected to the ESD protection pins (pin1, pin2, pin4, pin5, pin6, pin7, pin8, and pin9) of AZ1013-08F. The AZ1013-08F is designed for allowing the traces to run straight through the device to simplify the PCB layout. The ground pin (pin3) of AZ1013-08F is a negative reference pin. This pin should be directly connected to the GND rail of PCB. To get minimum parasitic inductance, the path length should keep as short as possible.

AZ1013-08F can provide ESD protection for 8 I/O signal lines simultaneously. If the number of I/O signal lines is less than 8, the unused I/O pins can be simply left as NC pins.

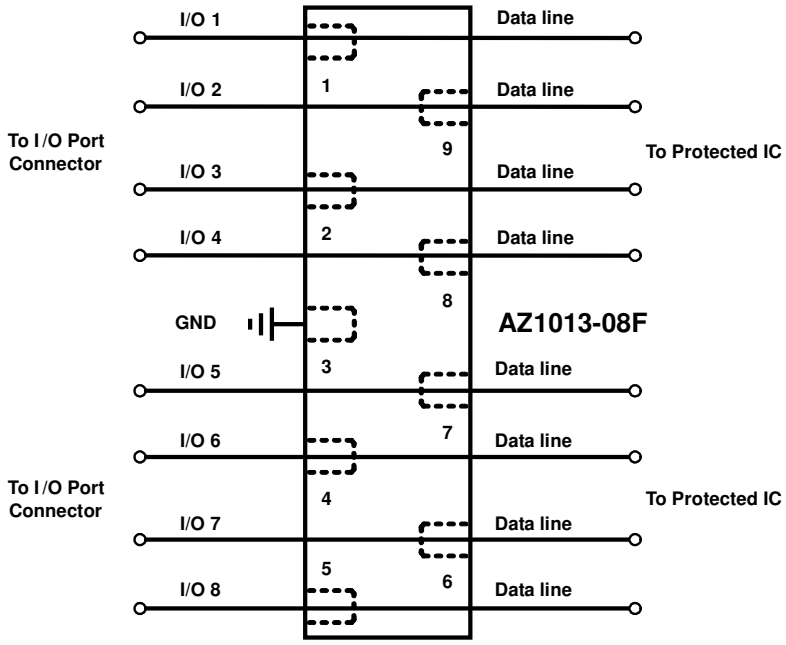
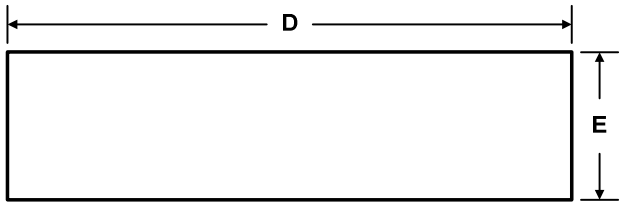


Fig. 1 Data lines connection of AZ1013-08F.

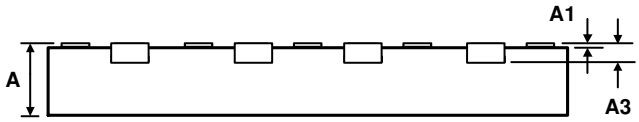
Mechanical Details

DFN3810P9E
PACKAGE DIAGRAMS

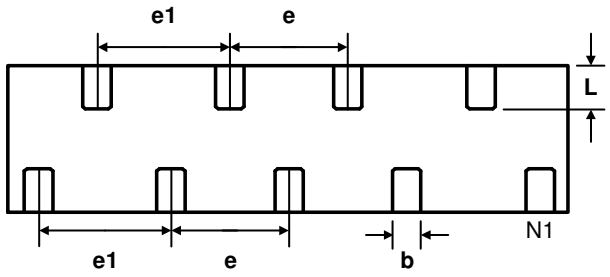
TOP VIEW



SIDE VIEW



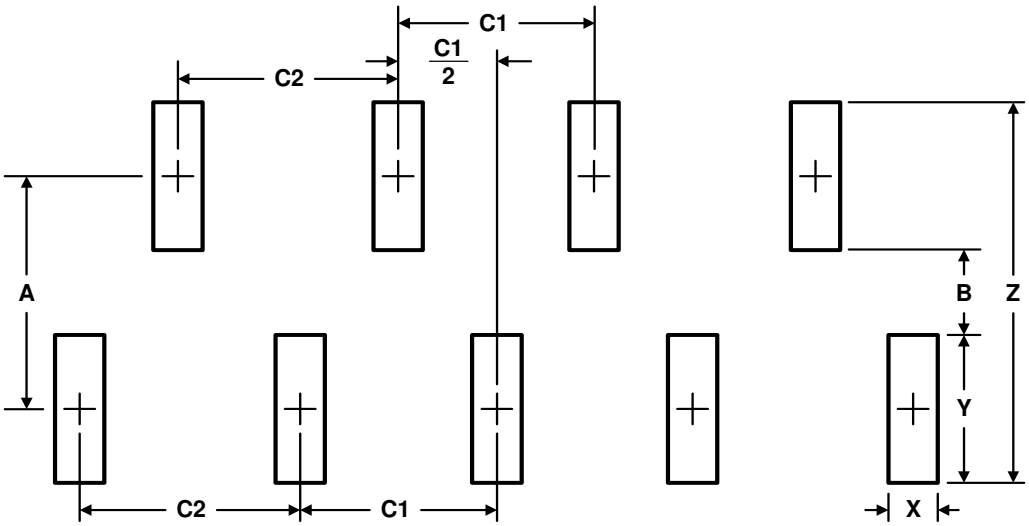
BOTTOM VIEW



PACKAGE DIMENSIONS

SYMBOL	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	0.450	0.550	0.018	0.022
A1	0.000	0.050	0.000	0.002
A3	0.150REF.		0.006REF.	
D	3.700	3.900	0.146	0.154
E	0.900	1.100	0.035	0.043
b	0.150	0.250	0.006	0.010
e	0.800TYP.		0.031TYP.	
e1	0.900TYP.		0.035TYP.	
L	0.200	0.400	0.008	0.016

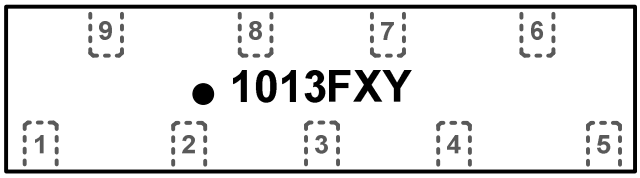
LAND LAYOUT



Notes:
This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.

Dimensions	
Index	**Millimeters**
A	0.95
B	0.35
C1	0.80
C2	0.90
X	0.20
Y	0.60
Z	1.55

MARKING CODE



1013F=Device Code
X=Date Code
Y=Control Code

Part Number	Marking Code
AZ1013-08F.R7G (Green Part)	1013FXY

Note. Green means Pb-free, RoHS, and Halogen free compliant.

Ordering Information

PN#	Material	Type	Real Size	MOQ	MOQ / internal box	MOQ / carton
AZ1013-08F.R7G	Green	T/R	7 inch	3,000/reel	3 reels = 9,000/box	6 boxes = 54,000/carton

Revision History

Revision	Modification Description
Revision 2015/12/15	Preliminary Release.
Revision 2017/05/15	Formal Release.