# IS31FL3292

## 4-RGB/12-LED LED DRIVER

**June 2024**

### GENERAL DESCRIPTION

The IS31FL3292 is a 12 LED current sink LED driver with 1MHz I2C compatible programming interface. Each LED can be dimmed individually with 12-bit PWM data and color calibrated with 8-bit DC scaling data, which provides 4096 steps of linear PWM dimming and 256 steps of DC current adjustable levels. All channels output current can be further globally adjusted in 64 steps.

The IS31FL3292 operates from 2.7V to 5.5V and features a very low operational and shutdown current.

Each channel of IS31FL3292 can operate in “PWM mode” or “Pattern mode” or “Current Level mode”. In “PWM mode”, the output current is set by 12-bit PWM registers and 8-bit current level registers. In “Pattern mode”, the timing characteristics for RGB channels output can be individually adjusted to maintain a pre-established pattern sequence without requiring any additional MCU interaction, thus saving valuable system resources. In “Current Level mode”, the output current is set by 8-bit current level register.

IS31FL3292 is available in QFN-20 (3mm×3mm) package. It operates from 2.7V to 5.5V over the temperature range of -40°C to +125°C.

### FEATURES

- Supply voltage range: 2.7V to 5.5V
- 12 current sinks, $I_{OUT}$= 40mA (Max.)
- Ultra-low operational current (310μA Typ. at $V_{CC}$=3.6V)
- Sleep mode: 1μA (Typ.) with SDB pulled high and all LEDs off
- Accurate color rendition
  - 12-bit/8+4-bit PWM/channel
  - 8-bit correction current/channel
  - 6-bit global current adjust
- SDB rising edge reset I2C module
- 1MHz I2C-compatible interface
- Auto breath function:
  - 4 patterns for auto breath.
  - Fade IN/ Fade OUT time up to 10s
  - 3 colors pre-configure registers for color breath
- 23kHz PWM frequency (8+4-bit PWM mode)
- QFN-20 (3mm×3mm) package
- RoHS & Halogen-Free Compliance
- TSCA Compliance

### APPLICATIONS

- Hand-held devices for LED display
- Gaming device (Mouse, Mouse Pad etc.)
- IOT device (AI speaker etc.)
- Portable Medical Devices

## TYPICAL APPLICATION CIRCUIT

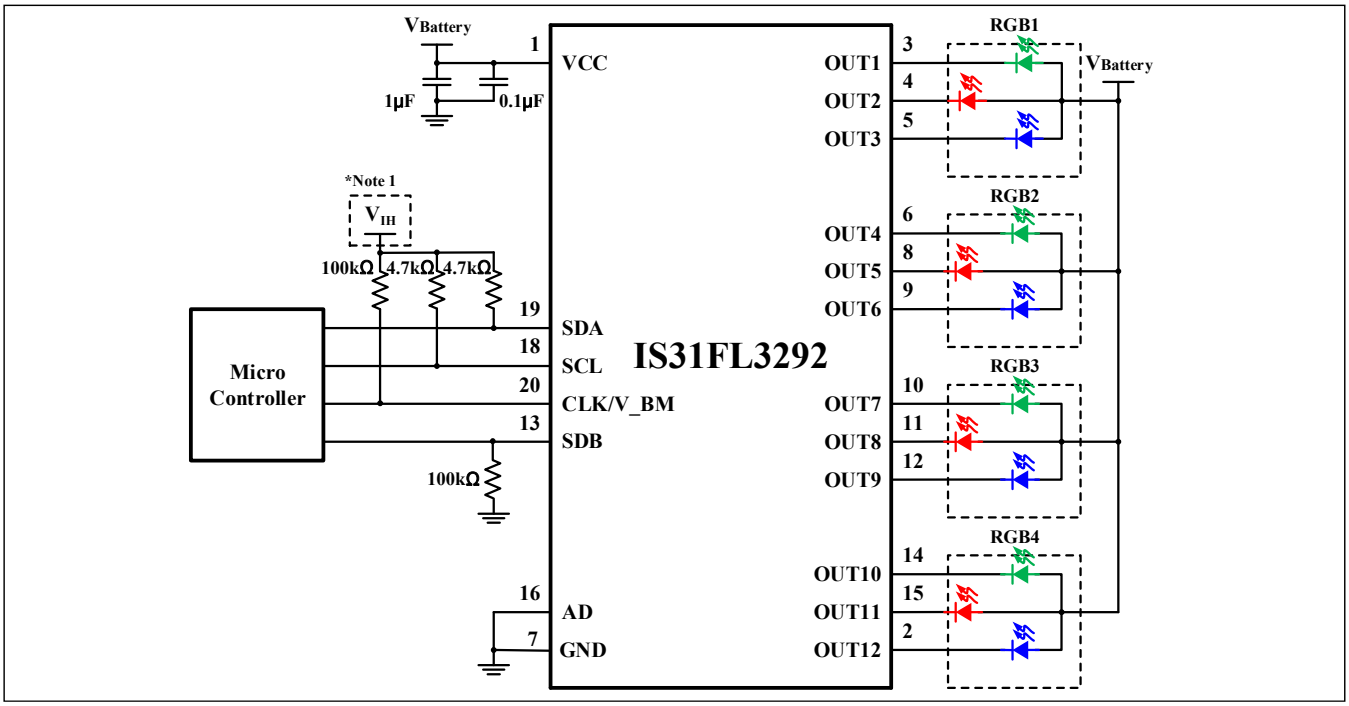



**Figure 1** Typical Application Circuit: 4-RGBs

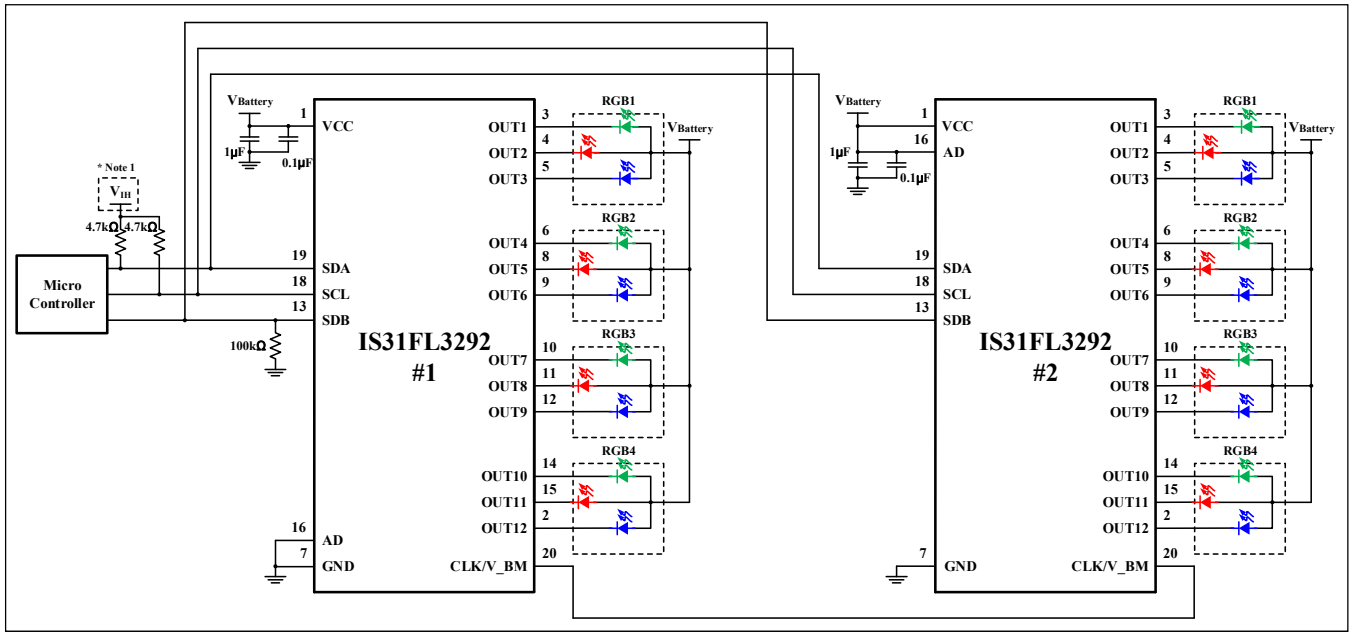
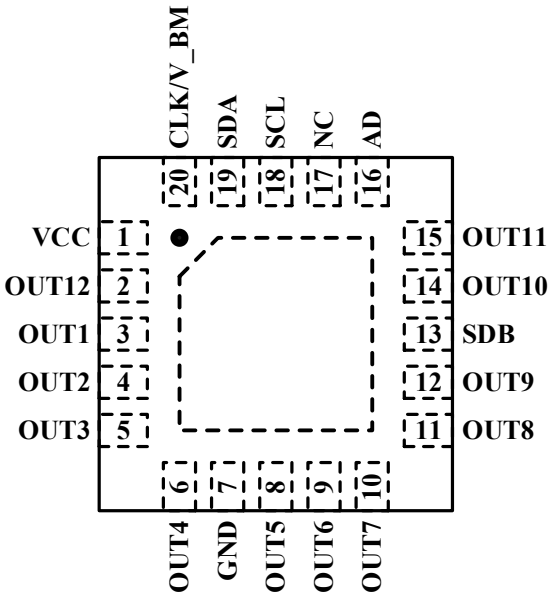



**Figure 2** Typical Application Circuit (Cascade Mode)

**Note 1**: $V_{IH}$ is the high-level voltage for IS31FL3292, which is usually same as VCC of Micro Controller, e.g. if $V_{CC}$ of Micro Controller is 3.3V, $V_{IH}$= 3.3V. If $V_{CC}$= 5V and $V_{IH}$ is lower than 2.8V, recommend to add level shift circuit.

## PIN CONFIGURATION

| Package | Pin Configuration (Top View) |
|---|---|
| QFN-20 |  |



## PIN DESCRIPTION

| No. | Pin | Description |
|---|---|---|
| 1 | VCC | Power supply |
| 2 | OUT12 | Current sink channel |
| 3~6 | OUT1~OUT4 | Current sink channels |
| 7 | GND | Ground |
| 8~12 | OUT5~OUT9 | Current sink channels |
| 13 | SDB | Shutdown the chip when pulled to low |
| 14,15 | OUT10~OUT11 | Current sink channels |
| 16 | AD | I2C address setting |
| 17 | NC | No connect |
| 18 | SCL | I2C serial clock |
| 19 | SDA | I2C serial data |
| 20 | CLK/V_BM | CLK input or output for cascade connection.<br>When breathing mark function is enabled, this pin is V_BM pin. |
| | Thermal Pad | Connect to GND |

## ORDERING INFORMATION

**Industrial Range: -40°C to +125°C**

| Order Part No. | Package | QTY/Reel |
|---|---|---|
| IS31FL3292-QFLS4-TR | QFN-20, Lead-free | 2500 |

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply voltage, $V_{CC}$ | -0.3V ~+6.0V |
| Voltage at any input pin | -0.3V ~ $V_{CC}$+0.3V |
| Maximum junction temperature, $T_{JMAX}$ | +150°C |
| Storage temperature range, $T_{STG}$ | -65°C ~+150°C |
| Operating temperature range, $T_A$=$T_J$ | -40°C ~ +125°C |
| Package thermal resistance, junction to ambient (4-layer standard test PCB based on JESD 51-2A), $\theta_{JA}$ | 57.5°C/W |
| ESD (HBM)<br>ESD (CDM) | ±4kV<br>±750V |

**Note 2:** Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

The following specifications apply for $V_{CC}$= 5V, $T_A$= 25°C, unless otherwise noted.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 2.7 | | 5.5 | V |
| $I_{CC}$ | Quiescent power supply current | $V_{CC}$=3.6V, $V_{SDB}$=$V_{CC}$, ALL channels enable, PWM=0x00, 12-bit mode, PFS= 220Hz | | 0.31 | 0.35 | mA |
| | | $V_{CC}$=5V, $V_{SDB}$=$V_{CC}$, ALL channels enable, PWM=0x00, 12-bit mode, PFS= 220Hz | | 0.36 | 0.45 | |
| | | $V_{CC}$=3.6V, $V_{SDB}$=$V_{CC}$, ALL channels enable, PWM=0x00, 8+4-bit mode, PFS= 23kHz | | 0.76 | 0.95 | |
| | | $V_{CC}$=5V, $V_{SDB}$=$V_{CC}$, ALL channels enable, PWM=0x00, 8+4-bit mode, PFS= 23kHz | | 1 | 1.3 | |
| $I_{SD}$ | Shutdown current | $V_{CC}$=5V, $V_{SDB}$=0V | | 0.4 | 2 | μA |
| | | $V_{CC}$=3.6V, $V_{SDB}$=0V | | 0.3 | 1 | |
| | | $V_{SDB}$= $V_{CC}$=5V, Configuration Register written "0000 0000 | | 0.4 | 2 | |
| | | $V_{SDB}$= $V_{CC}$=3.6V, Configuration Register written "0000 0000 | | 0.3 | 1 | |
| $I_{OUT}$ | Constant current of channel | GCC=0x3F, CL=0xFF, IMAX=0 | 27.5 | 30 | 32.5 | mA |
| | | GCC=0x3F, CL=0xFF, IMAX=1 | | 40 | | mA |
| $f_{OUT}$ | PWM frequency of output | OSC= 1.8MHz, PFS=00, PWM Resolution= 12-bit | 200 | 220 | 240 | Hz |
| | | OSC= 1.8MHz, PFS=01, PWM Resolution= 12-bit | 400 | 440 | 480 | Hz |
| | | OSC= 6MHz, PFS=10, PWM Resolution= 8+4-bit | 21 | 23 | 25.3 | kHz |
| $\Delta I_{MAT}$ | Between channels | $I_{OUT}$=30mA (Note 3) | -6.5 | | 6.5 | % |
| $\Delta I_{ACC}$ | Between device to device | $I_{OUT}$=30mA (Note 4) | -6.5 | | 6.5 | % |
| $\Delta I_{MAT}$ | Between channels | $I_{OUT}$=3mA (LCAI=1) (Note 3) | -7 | | 7 | % |
| $\Delta I_{ACC}$ | Between device to device | $I_{OUT}$=3mA (LCAI=1) (Note 4) | -7 | | 7 | % |

## ELECTRICAL CHARACTERISTICS (CONTINUE)

The following specifications apply for $V_{CC}$= 5V, $T_A$= 25°C, unless otherwise noted.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{HR}$ | Current sink headroom voltage | $I_{OUT}$= 30mA | | 250 | 350 | mV |
| $T_{SD}$ | Thermal shutdown | (Note 5) | | 165 | | °C |
| $T_{SD\_HY}$ | Thermal shutdown hysteresis | (Note 5) | | 18 | | °C |
| **Logic Electrical Characteristics (SDA, SCL, SDB, AD)** | | | | | | |
| $V_{IL}$ | Logic “0” input voltage | $V_{CC}$= 2.7V~5.5V | GND | | 0.4 | V |
| $V_{IH}$ | Logic “1” input voltage | $V_{CC}$= 2.7V~5.5V | 1.4 | | $V_{CC}$ | V |
| $I_{IL}$ | Logic “0” input current | $V_{INPUT}$= 0V (Note 5) | | 5 | | nA |
| $I_{IH}$ | Logic “1” input current | $V_{INPUT}$= $V_{CC}$ (Note 5) | | 5 | | nA |
| $V_{OL-SDA}$ | Low-level output voltage of SDA | $I_{LOAD}$= 5mA | | | 0.4 | V |
| $V_{OL-CLK}$ | Low-level output voltage of CLK/V_BM | $I_{LOAD}$= -5mA | | | 0.4 | V |
| $V_{OH-CKL}$ | High-level output voltage of CLK/V_BM | $I_{LOAD}$= 5mA | $V_{CC}$-0.4 | | | V |

## DIGITAL INPUT I2C SWITCHING CHARACTERISTICS (NOTE 5)

| Symbol | Parameter | Fast Mode | | | Fast Mode Plus | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| $f_{SCL}$ | Serial-clock frequency | - | | 400 | - | | 1000 | kHz |
| $t_{BUF}$ | Bus free time between a STOP and a START condition | 1.3 | | - | 0.5 | | - | µs |
| $t_{HD, STA}$ | Hold time (repeated) START condition | 0.6 | | - | 0.26 | | - | µs |
| $t_{SU, STA}$ | Repeated START condition setup time | 0.6 | | - | 0.26 | | - | µs |
| $t_{SU, STO}$ | STOP condition setup time | 0.6 | | - | 0.26 | | - | µs |
| $t_{HD, DAT}$ | Data hold time | - | | - | - | | - | µs |
| $t_{SU, DAT}$ | Data setup time | 100 | | - | 50 | | - | ns |
| $t_{LOW}$ | SCL clock low period | 1.3 | | - | 0.5 | | - | µs |
| $t_{HIGH}$ | SCL clock high period | 0.7 | | - | 0.26 | | - | µs |
| $t_R$ | Rise time of both SDA and SCL signals, receiving (Note 6) | - | | 300 | - | | 120 | ns |
| $t_F$ | Fall time of both SDA and SCL signals, receiving (Note 6) | - | | 300 | - | | 120 | ns |

**Note 3:** $I_{OUT}$ mismatch (bit to bit) $\triangle I_{MAT}$ is calculated:

$$\Delta I_{MAT} = \left( \frac{I_{OUTn}(n = 1 \sim 12)}{\left( \frac{I_{OUT1}+I_{OUT2}+I_{OUT3}+I_{OUT4}+I_{OUT5}+I_{OUT6}+I_{OUT7}+I_{OUT8}+I_{OUT9}+I_{OUT10}+I_{OUT11}+I_{OUT12}}{12} \right)} - 1 \right) \times 100\%$$

**Note 4:** $I_{OUT}$ accuracy (device to device) $\triangle I_{ACC}$ is calculated:

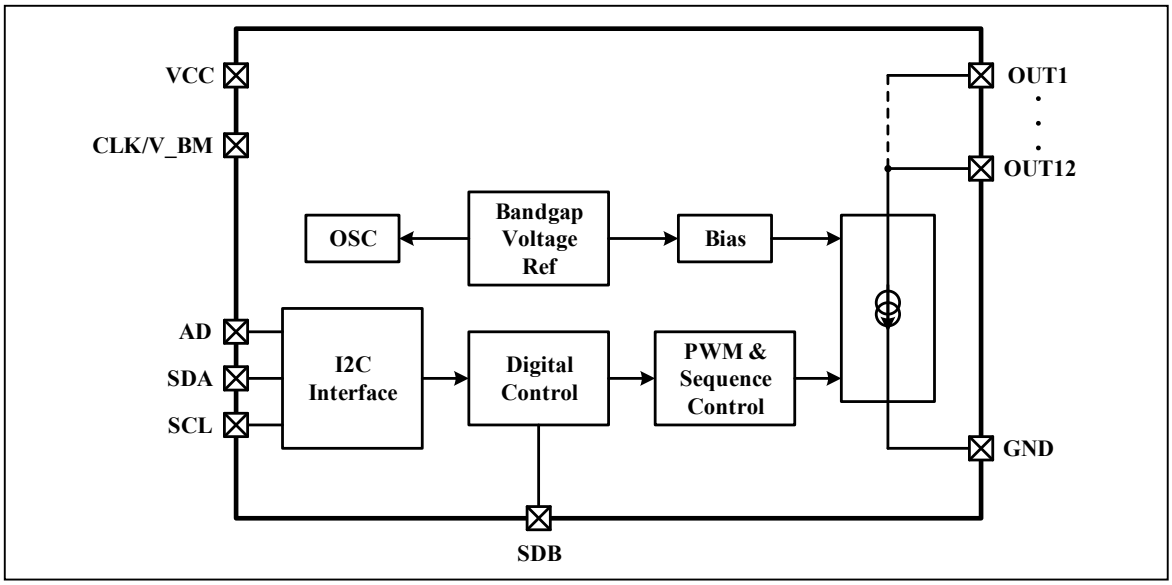
$$\Delta I_{ACC} = \left( \frac{\left( \frac{I_{OUT1}+I_{OUT2}+I_{OUT3}+I_{OUT4}+I_{OUT5}+I_{OUT6}+I_{OUT7}+I_{OUT8}+I_{OUT9}+I_{OUT10}+I_{OUT10}+I_{OUT12}}{12} - I_{OUT(IDEAL)} \right)}{I_{OUT(IDEAL)}} \right) \times 100\%$$

Where $I_{OUT(IDEAL)}$= 30mA or 3mA.

**Note 5:** Guaranteed by design.

**Note 6:** $t_R$ and $t_F$ measured between 0.3×$V_{CC}$ and 0.7×$V_{CC}$.

## FUNCTION BLOCK DIAGRAM



## DETAILED DESCRIPTION

### I2C INTERFACE

IS31FL3292 uses a serial bus, which conforms to the I2C protocol, to control the chip's functions with two wires: SCL and SDA. The IS31FL3292 has a 7-bit slave address (A7:A1), followed by the R/W bit, A0. Set A0 to "0" for a write command and set A0 to "1" for a read command. The value of bits A1 and A2 are decided by the connection of the AD pin.

**Table 1 Slave Address**

| AD | A7:A3 | A2:A1 | A0 |
|---|---|---|---|
| GND | 1001 1 | 00 | 0/1 |
| SCL | | 01 | |
| SDA | | 10 | |
| VCC | | 11 | |

AD connected to GND, A2:A1=00;

AD connected to VCC, A2:A1=11;

AD connected to SCL, A2:A1=01;

AD connected to SDA, A2:A1=10;

The SCL line is uni-directional. The SDA line is bi-directional (open-drain) with a pull-up resistor (typically 2kΩ). The maximum clock frequency specified by the I2C standard is 1MHz. In this discussion, the master is the microcontroller and the slave is the IS31FL3292.

The timing diagram for the I2C is shown in Figure 3. The SDA is latched in on the stable high level of the SCL. When there is no interface activity, the SDA line should be held high.

The "START" signal is generated by lowering the SDA signal while the SCL signal is high. The start signal will alert all devices attached to the I2C bus to check the incoming address against their own chip address.

The 8-bit chip address is sent next, most significant bit first. Each address bit must be stable while the SCL level is high.

After the last bit of the chip address is sent, the master checks for the IS31FL3292's acknowledge. The master releases the SDA line high (through a pull-up resistor). Then the master sends an SCL pulse. If the IS31FL3292 has received the address correctly, then it holds the SDA line low during the SCL pulse. If the SDA line is not low, then the master should send a "STOP" signal (discussed later) and abort the transfer.

Following acknowledge of IS31FL3292, the register address byte is sent, most significant bit first. IS31FL3292 must generate another acknowledge indicating that the register address has been received.

Then 8-bit of data byte are sent next, most significant bit first. Each data bit should be valid while the SCL level is stable high. After the data byte is sent, the IS31FL3292 must generate another acknowledge to indicate that the data was received.

The "STOP" signal ends the transfer. To signal "STOP", the SDA signal goes high while the SCL signal is high.

### ADDRESS AUTO INCREMENT

To write multiple bytes of data into IS31FL3292, load the address of the data register that the first data byte is intended for. During the IS31FL3292 acknowledge of receiving the data byte, the internal address pointer will increment by one. The next data byte sent to IS31FL3292 will be placed in the new address, and so on. The auto increment of the address will continue as long as data continues to be written to IS31FL3292 (Figure 6).

### READING OPERATION

Most of the registers can be read.

To read the register, after I2C start condition, the bus master must send the IS31FL3292 device address with the R/ bit set to "0", followed by the register address which determines which register is accessed. Then restart I2C, the bus master should send the IS31FL3292 device address with the R/ bit set to "1". Data from the register defined by the command byte is then sent from the IS31FL3292 to the master (Figure 7).

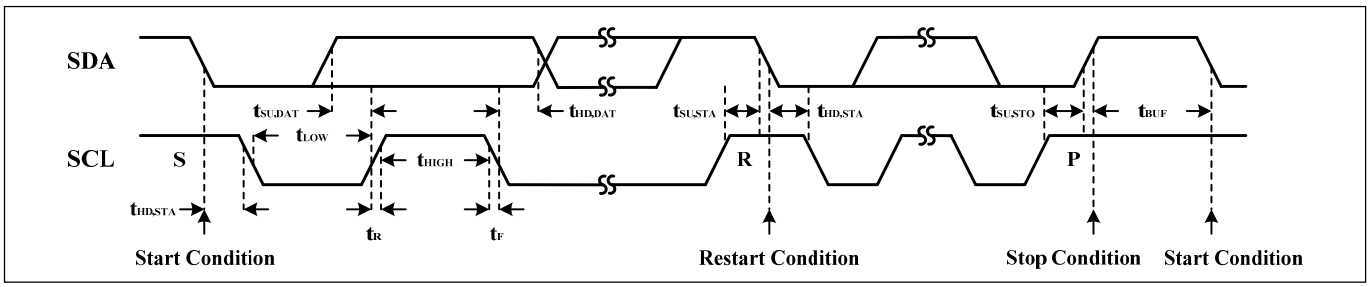



**Figure 3** I2C Interface Timing

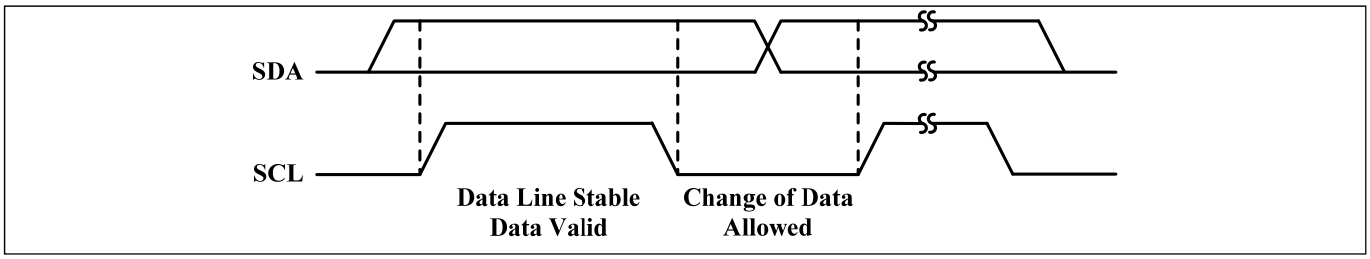



**Figure 4** I2C Bit Transfer

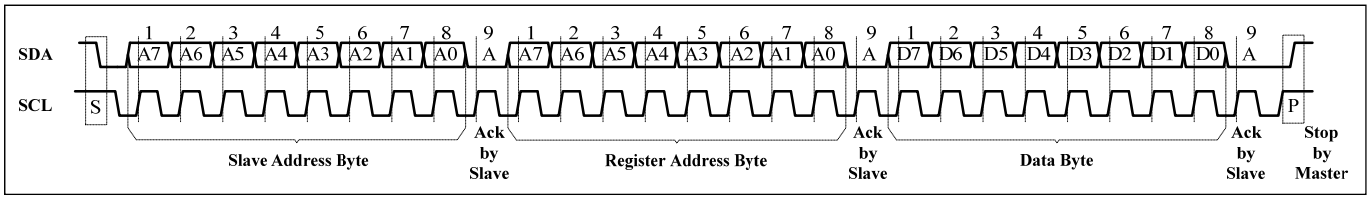



**Figure 5** I2C Writing to IS31FL3292 (Typical)

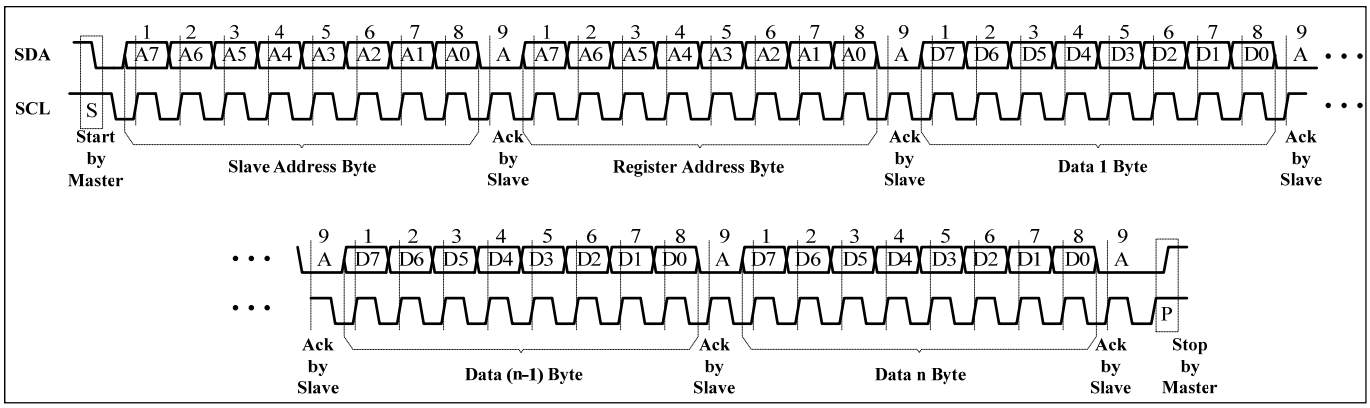



**Figure 6** I2C Writing to IS31FL3292 (Automatic Address Increment)

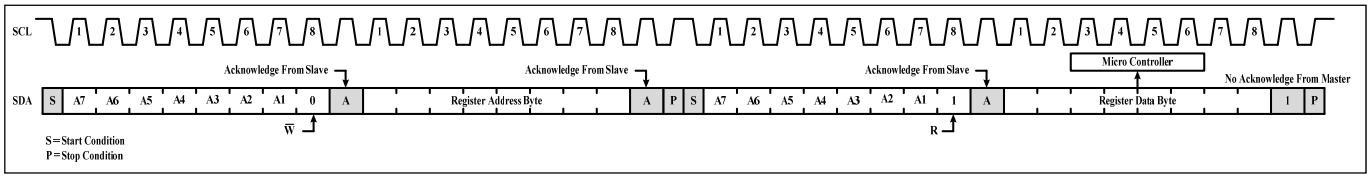



**Figure 7** I2C Reading from IS31FL3292

**Table 2 Registers Definitions**

| Address | Name | Function | R/W | Table | Default |
|---|---|---|---|---|---|
| 00h | Product ID | For read only, read result is Slave address | R | - | - |
| 01h | Shutdown Control Register | Set power down mode and outputs shutdown control | R/W | 3 | 0010 0000 |
| 02h | Output Enable Register 1 | Enable output 1~8 | R/W | 4 | 1111 1111 |
| 03h | Output Enable Register 2 | Enable output 9~12 | R/W | 5 | 0000 1111 |
| 04h | Operation Configure Register 1 | Set output 1~4 operation mode | R/W | 6 | 0000 0000 |
| 05h | Operation Configure Register 2 | Set output 5~8 operation mode | R/W | 7 | 0000 0000 |
| 06h | Operation Configure Register 3 | Set output 9~12 operation mode | R/W | 8 | 0000 0000 |
| 07h | Global Current Control Register | Set global current | R/W | 9 | 0011 1111 |
| 08h | Hold Function Register | Set the hold function of each Output | R/W | 10 | 0000 0000 |
| 09h | V_BM Function Register | Clock and V_BM mark | R/W | 11 | 0000 0000 |
| 0Ah | PWM Frequency Adjust Unlock Register | Unlock the 0Ch | W | - | 0000 0000 |
| 0Bh | PWM Frequency Adjust and Spread Spectrum Register | Adjust the PWM Frequency | R/W | 12 | 0000 0000 |
| 0C~0Fh | 3 Pattern State Registers | For reading the pattern running state | R | 13 | 0000 0000 |
| 10h~1Bh | OUT1~OUT12 Current Level Register | Output current level data register | R/W | 14 | 0000 0000 |
| 10h~1Bh | Color 1 Setting Register of Pattern | Output current level data register-Color 1 | R/W | 15 | 0000 0000 |
| 20h~2Bh | Color 2 Setting Register of Pattern | Output current level data register-Color 2 | R/W | | 0000 0000 |
| 30h~3Bh | Color 3 Setting Register of Pattern | Output current level data register-Color 3 | R/W | | 0000 0000 |
| 40h~57h | PWM Register | Set PWM data | R/W | 16 | 0000 0000 |
| 60h/70h/80h/90h | Pattern TS &T1 Setting Register | Set the TS~T1 time | R/W | 18 | 0000 0000 |
| 61h/71h/81h/91h | Pattern T2 &T3 Setting Register | Set the T2~T3 time | R/W | 19 | 0000 0000 |
| 62h/72h/82h/92h | Pattern TP &T4 Setting Register | Set the TP~T4 time | R/W | 20 | 0000 0000 |
| 63h/73h/83h/93h | Pattern Color Enable Register | Set the color enable/disable | R/W | 21 | 0000 0001 |
| 64h/74h/84h/94h | Pattern Color Cycle Times Register | Set color repeat time | R/W | 22 | 0000 0000 |
| 65h/75h/85h/95h | Pattern Register | Set next step and Gamma of each pattern | R/W | 23 | 0000 0001 |
| 66h/76h/86h/96h | Pattern Loop Times Register | Set the loop time of Pattern | R/W | 24 | 0000 0000 |
| 99h | Color Update Register | Update color data | R/W | - | 0000 0000 |
| 9Ah | PWM Update Register | Update PWM data | R/W | - | 0000 0000 |
| 9Bh/9Ch/9D/9Eh | Pattern Update Register | Update the time data and start to run pattern | R/W | - | 0000 0000 |
| 9Fh | Reset Register | Reset the registers value to default | W | - | 0000 0000 |

**Table 3 01h Shutdown Control Register**

| Bit | D7 | D6 | D5 | D4 | D3:D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| Name | LCAI | IMAX | MS | SYNC | PFS | SLE | SSD |
| Default | 0 | 0 | 1 | 0 | 00 | 0 | 0 |

The Shutdown Control Register sets software shutdown and sleep modes of IS31FL3292.

When the SLE bit is set to "1", the IS31FL3292 enters Sleep Mode if all OUTx outputs are off for >40s. All OUTx are off without any bias. I_SLEEP = 1μA (Typ.). When the IS31FL3292 is in sleep mode, the SLE bit needs to be set to "0" so that the IS31FL3292 will wake up and disable the sleep mode.

The PFS bit sets the PWM resolution. PWM mode can operate at 220Hz (12-bit, 8+4-bit mode), 440Hz (12-bit, 8+4-bit mode) and 23kHz (8+4-bit mode).

MS and SYNC bit control the CLK pin status. When MS and SYNC are both set to “1”, the CLK pin will have a clock output to support cascade connection between 2 or more IS31FL3292.

**SSD Software Shutdown Enable**

0 Software shutdown mode

1 Normal operation

**SLE Sleep Mode Enable**

0 Sleep mode disable

1 Sleep mode enable (40s after no output current)

**PFS PWM Frequency Select**

00 220Hz (Force 220Hz in Pattern Mode or PWM mode)

01 440Hz (12-bit PWM mode)

1x 23kHz (8+4-bit PWM mode, 23kHz)

**SYNC Enable Synchronization Clock**

0 Disable, CLK pin is Hi-Z status

1 Enable, CLK is clock output.

**MS Master Slave**

0 Slave, CLK is input

1 Master, CLK is clock output or Hi-Z status

**IMAX Enable $I_{OUT(MAX)}$=40mA**

0 Default 30mA

1 $I_{OUT(MAX)}$=40mA

**LCAI Low Current Accuracy Improve**

0 Default maximum 30mA

1 1/3 output current, and improve low current accuracy

**Table 4 02h Output Enable Register 1**

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| Name | EN8 | EN7 | EN6 | EN5 | EN4 | EN3 | EN2 | EN1 |
| Default | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

**Table 5 03h Output Enable Register 2**

| Bit | D7:D6 | D5:D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|
| Name | - | RGMS | EN12 | EN11 | EN10 | EN9 |
| Default | 00 | 00 | 1 | 1 | 1 | 1 |

The Output Enable Register enables/disables the outputs independently. The ENx is only effective when SSD= “1”.

The RGMS bit is used to select RGB group mode. When the RGMS is not set to “00”, the MODx (x=1~12) bits in 04h/05h/06h are invalid, and three outputs in one RGB group run synchronously in pattern loop for color mixture. All 12 outputs can be divided into 4 RGB groups. OUT1, OUT2, OUT3 in RGB group 1. OUT4, OUT5, OUT6 in RGB group 2. OUT7, OUT8, OUT9 in RGB group 3. OUT10, OUT11, OUT12 in RGB group 4.

**ENx Output Enable Control**

0 Output disable

1 Output enable

**RGMS RGB Group Mode Select**

00 Mode 1, 12 Outputs running individual.

01 Mode 2, RGB Group 1/2/3/4 run in Pattern 1 to 4

10 Mode 3, RGB Group 1/2/3 run in Pattern 1 to 3, RGB Group 4 run in Pattern 4

11 Mode 4, RGB Group 1/2 run in Pattern 1 to 2, RGB Group 3/4 run in Pattern 3 to 4

**Table 6 04h Operating Configure Register 1**

| Bit | D7:D6 | D5:D4 | D3:D2 | D1:D0 |
|---|---|---|---|---|
| Name | MOD4 | MOD3 | MOD2 | MOD1 |
| Default | 00 | 00 | 00 | 00 |

**Table 7 05h Operating Configure Register 2**

| Bit | D7:D6 | D5:D4 | D3:D2 | D1:D0 |
|---|---|---|---|---|
| Name | MOD8 | MOD7 | MOD6 | MOD5 |
| Default | 00 | 00 | 00 | 00 |

**Table 8 06h Operating Configure Register 3**

| Bit | D7:D6 | D5:D4 | D3:D2 | D1:D0 |
|---|---|---|---|---|
| Name | MOD12 | MOD11 | MOD10 | MOD9 |
| Default | 00 | 00 | 00 | 00 |

The MODx (x=1~12) bits set output operation modes of IS31FL3292 when output not in RGB Group Mode.

**MODx OUT1~OUT12 LED Mode**

00 PWM Mode

01 Pattern Mode

10 Current Level Mode (No PWM)

When the OUTx works in PWM Mode, means the output current is controlled by PWM Registers (40h~57h).

When the OUTx works in Pattern Mode, it means the output current is controlled by Color Setting Registers (10h~1Bh, 20h~2Bh and 30h~3Bh).

When the OUTx works in Current Level Mode, it means the output current is controlled by Current Level Register (10h~1Bh).

**Table 9 07h Global Current Control Register**

| Bit | D7:D6 | D5:D0 |
|---|---|---|
| Name | - | GCC |
| Default | 00 | 11 1111 |

The Global Current Control Register modulates all OUTx (x=1~12). DC current which is noted as IOUT in 64 steps.

$I_{OUT}$ is computed by as shown in Formula (1).

If GCC=0x3F, CL=0xFF, $I_{OUT}=I_{OUT(MAX)}$

$$I_{OUT} = 30mA \times \frac{GCC}{64} \times \frac{CL}{256} \quad (1)$$

$$GCC = \sum_{n=0}^{7} D[n] \cdot 2^n \quad (2)$$

When IMAX="1", the 30mA will become 40mA.

**Table 10 08h Hold Function Register**

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| Name | HFE4 | HTS4 | HFE3 | HTS3 | HFE2 | HTS2 | HFE1 | HTS1 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

The Hold Function Register configures hold time for each output in Pattern Mode.

**HTS Hold Time Selection**

0 Hold at end of T4 when color loop done (always off)

1 Hold at end of T2 when color loop done (always on)

**HFE Hold Function Enable**

0 Hold function disable

1 Hold function enable

**Table 11 09h V_BM Function Register**

| Bit | D7 | D6 | D5:D4 | D3:D2 | D1:D0 |
|---|---|---|---|---|---|
| Name | VPE | BME | PAMF | CMF | TMP |
| Default | 0 | 0 | 00 | 00 | 00 |

The V_BM function register stores the V_BM pin function, PAMF selects the pattern and TMP selects the time point to have interrupt.

**Note 7:** When only one color is enabled in the Pattern Color Enable Register (63/h73h/83h/93h = 0x01, 0x02, or 0x04), the TMP bits can be set to "00" or "1x".

**VPE V_BM Pull High EN**

0 Disable, V_BM is open drain

1 Enable, V_BM is pull to VCC by 100kΩ

**BME Breath Mark function enable**

0 Disable, CLK/V_BM is clock function

1 Enable, CLK/V_BM is V_BM function

**CMF Color Mark Function**

00 Color 1

01 Color 2

10 Color 3

**PAMF Pattern Mark Function**

00 Pattern 1

01 Pattern 2

10 Pattern 3

11 Pattern 4

**TMP Time Point**

00 Start of T2

01 Start of TP

1x Start of T4

**0Ah PWM Frequency Adjust Unlock Register**

Write "0xA5" to 0Ah to unlock the PWM Frequency Adjust Register (0Bh).

**Table 12 0Bh PWM Frequency Adjust and Spread Spectrum Register**

| Bit | D7:D6 | D5:D4 | D3 | D2:D0 |
|---|---|---|---|---|
| Name | CLT | RNG | SSP | PFA |
| Default | 00 | 00 | 0 | 000 |

Before access to 0Bh, the 0Ah needs to be written with 0xA5 to unlock it.

The PFA bits adjust the PWM Frequency, for example, if PWM frequency is 23kHz at 8+4-bit PWM mode, if PFA is “000”, the PWM frequency is 23kHz, if PFA is “001”, the PWM frequency is 25.806kHz (+12.2%).

SSP bit enables the spread spectrum function, RNG bits adjust the range and CLT bits select the cycle time. The spread spectrum function only takes effect in 8+4-bit PWM mode (PFS bit is ‘1x’ in 01h).

**Note 8:** It is recommended to use SSP=1 only when PWM frequency is 23kHz.

| **PFA** | **PWM Frequency Adjust** |
|---|---|
| 000 | 0% |
| 001 | +12.2% |
| 010 | +29% |
| 011 | +52.7% |
| 100 | -53% |
| 101 | -39.8% |
| 110 | -31.8% |
| 111 | -21% |

| **SSP** | Spread Spectrum Enable |
|---|---|
| 0 | Disable |
| 1 | Enable |

| **CLT** | Spread Spectrum Cycle Time |
|---|---|
| 00 | 512ms |
| 01 | 256ms |
| 10 | 2ms |
| 11 | 1ms |

| **RNG** | Spread Spectrum Range |
|---|---|
| 00 | +3.2% |
| 01 | +7.2% |
| 10 | +12.2% |
| 11 | +27.2% |

**Table 13 0Ch~0Fh Pattern State Register (Read Only)**

| Bit | D7 | D6 | D5 | D4 | D3 | D2:D0 |
|---|---|---|---|---|---|---|
| Name | PS | CS3 | CS2 | CS1 | - | TS |
| Default | 0 | 0 | 0 | 0 | 0 | 000 |

The Pattern State Register stores the pattern status.

0Ch register is used for pattern 1, 0Dh for pattern 2, 0Eh for pattern 3, similarly 0Fh for pattern 4.

Below table shows the pattern running state.

**Note 9:** These reading results are only applicable for the condition: the color 1, color 2 and color 3 in one pattern are all enabled (63/h73h/83h/93h = 0x07).

| Read Result | D7:D0 | Pattern State | Color | Time |
|---|---|---|---|---|
| 0x90 | 1001 0000 | Running | - | TS |
| 0x91 | 1001 0001 | Running | Color1 | T1 |
| 0x92 | 1001 0010 | Running | Color1 | T2 |
| 0x93 | 1001 0011 | Running | Color1 | T3 |
| 0xA4 | 1010 0100 | Running | Color1 | TP |
| 0xA1 | 1010 0001 | Running | Color2 | T1 |
| 0xA2 | 1010 0010 | Running | Color2 | T2 |
| 0xA3 | 1010 0011 | Running | Color2 | T3 |
| 0xC4 | 1100 0100 | Running | Color2 | TP |
| 0xC1 | 1100 0001 | Running | Color3 | T1 |
| 0xC2 | 1100 0010 | Running | Color3 | T2 |
| 0xC3 | 1100 0011 | Running | Color3 | T3 |
| 0x94 | 1001 0100 | Running | Color3 | TP |
| 0x95 | 1001 0101 | Running | - | T4 |
| 0x00 | 0000 0000 | Not running | - | - |

**Table 14 10h~1Bh OUT1~OUT12 Current Level Register**

| Bit | D7:D0 |
|---|---|
| Name | CL |
| Default | 0000 0000 |

The output current may be computed using the Formula (1):

$$I_{OUT}=30mA\times\frac{GCC}{64}\times\frac{CL}{256} \quad (1)$$

$$CL=\sum_{n=0}^{7}D[n]\cdot 2^{n} \quad (3)$$

$$I_{LED}=30mA\times\frac{GCC}{64}\times\frac{CL}{256}\times\frac{PWM}{4096} \quad (4)$$

Where D[n] stands for the individual bit value, 1 or 0, in location n, PWM is the value in 40h~57h, $I_{OUT}$ is the peak current of the outputs. $I_{LED}$ is the average current of the outputs.

When IMAX= "1", the 30mA will become 40mA.

When IS31FL3292 operates in Current Level Mode, PWM = 4096 in the above equation.

For example: in Current Level node only, if D7:D0 = 10110101,

$I_{OUT}$ = 30mA × ($2^7$ +$2^5$ +$2^4$ +$2^2$ +$2^0$)/256

When IS31FL3292 operates in PWM & Current Level Mode, the value of CL and PWM will decide the output current together.

**Table 15-1 10h~1Bh Color 1 Setting Register of Pattern (OUT1~OUT12)**

| Bit | D7:D0 |
|---|---|
| Name | COL1_Oy |
| Default | 0000 0000 |

**Table 15-2 20h~2Bh Color 2 Setting Register of Pattern (OUT1~OUT12)**

| Bit | D7:D0 |
|---|---|
| Name | COL2_Oy |
| Default | 0000 0000 |

**Table 15-3 30h~3Bh Color 3 Setting Register of Pattern (OUT1~OUT12)**

| Bit | D7:D0 |
|---|---|
| Name | COL3_Oy |
| Default | 0000 0000 |

Color Setting Registers store the color setting for each output in Pattern Mode. Check Pattern Color Setting section for more information about the color setting registers.

When IS31FL3292 operates in Pattern Mode, the value of Color Registers will decide the output current of each output in 256 levels.

The output current may be computed using the Formula (4):

$$I_{OUT} = 30\,mA \times \frac{COLx\_Oy}{256} \qquad (5)$$

$$COLx\_Oy = \sum_{n=0}^{7} D[n] \cdot 2^n \qquad (6)$$

Where D[n] stands for the individual bit value, 1 or 0, in location n.

For example: if D7:D0 = 10110101,

$I_{OUT}$ = 30mA×($2^7$ +$2^5$ +$2^4$ +$2^2$ +$2^0$)/256

$I_{OUT}$ is the peak current of the outputs.

Need to write Color Update Register (99h) to update the data.

**Table 16 40h~57h PWM Register**

| Reg | 41h (43h, 45h…) | | 40h (42h, 44h…) |
|---|---|---|---|
| Bit | D7:D4 | D3:D0 | D7:D0 |
| Name | - | PWM_H | PWM_L |
| Defaul | 0000 | 0000 | 0000 0000 |

When IS31FL3292 operates in PWM Mode, each output has 2 bytes to modulate the PWM duty as below Table 17 in 4096 steps, in Pattern Mode, the PWM cannot be accessed.

The value of the PWM Registers decides the average current of each LED noted $I_{LED}$.

The value of the PWM Registers decides the average current of each LED noted $I_{LED}$.

$I_{LED}$ computed by Formula (1):

$$I_{LED} = 30mA \times \frac{GCC}{64} \times \frac{CL}{256} \times \frac{PWM}{4096} \qquad (7)$$

Where $I_{OUT}$ is the peak current of the outputs. $I_{LED}$ is the average current of the outputs.

$$PWM = \sum_{n=0}^{11} D[n] \cdot 2^n$$

Where D[n] stands for the individual bit value, 1 or 0, in location n.

For example: if PWM_H = 00001001, PWM_L = 10110101, N=4096, GCC=63, CL=255,

$I_{LED}$ = 30mA*($2^{11}$ +$2^8$ +$2^7$ +$2^5$ +$2^4$ +$2^2$ +$2^0$)/4096.

Need to write PWM Update Register (9Ah) to update the data.

**Table 17 Register of PWM Mode**

| Mode | Register | OUT1 | OUT2 | OUT3 |
|---|---|---|---|---|
| PWM | PWM_H | 41h | 43h | 45h |
| | PWM_L | 40h | 42h | 44h |
| | CL | 10h | 11h | 12h |
| | Register | OUT4 | OUT5 | OUT6 |
| | PWM_H | 47h | 49h | 4Bh |
| | PWM_L | 46h | 48h | 4Ah |
| | CL | 13h | 14h | 15h |
| | Register | OUT7 | OUT8 | OUT9 |
| | PWM_H | 4Dh | 4Fh | 51h |
| | PWM_L | 4Ch | 4Eh | 50h |
| | CL | 16h | 17h | 18h |
| | Register | OUT10 | OUT11 | OUT12 |
| | PWM_H | 53h | 55h | 57h |
| | PWM_L | 52h | 54h | 56h |
| | CL | 19h | 1Ah | 1Bh |

**Table 18 60/70/80/90h Pattern TS &T1 Setting Register**

| Bit | D7:D3 | D4:D0 |
|---|---|---|
| Name | T1 | TS |
| Default | 0000 | 0000 |

The TS & T1 Setting Registers set the TS and T1 time in Pattern Mode. 60h register is used for pattern 1, 70h for pattern 2, 80h for pattern 3, similarly 90h for pattern 4.

| TS | Pattern Start Time Selection |
|---|---|
| 0000 | 0.04s |
| 0001 | 0.16s |
| 0010 | 0.31s |
| 0011 | 0.46s |
| 0100 | 0.61s |
| 0101 | 0.92s |
| 0110 | 1.25s |
| 0111 | 1.92s |
| 1000 | 2.52s |
| 1001 | 3.12s |
| 1010 | 3.72s |
| 1011 | 5.04s |
| 1100 | 6.24s |
| 1101 | 7.44s |
| 1110 | 8.76s |
| 1111 | 9.96s |

| T1 | Rise Time Selection |
|---|---|
| 0000 | 0.04s |
| 0001 | 0.16s |
| 0010 | 0.31s |
| 0011 | 0.46s |
| 0100 | 0.61s |
| 0101 | 0.92s |
| 0110 | 1.25s |
| 0111 | 1.92s |
| 1000 | 2.52s |
| 1001 | 3.12s |
| 1010 | 3.72s |
| 1011 | 5.04s |
| 1100 | 6.24s |
| 1101 | 7.44s |
| 1110 | 8.76s |
| 1111 | 9.96s |

**Table 19 61/71/81/91h Pattern T2 &T3 Setting Register**

| Bit | D7:D3 | D4:D0 |
|---|---|---|
| Name | T3 | T2 |
| Default | 0000 | 0000 |

The T2 & T3 Setting Registers set the T2 and T3 time in Pattern Mode. 61h register is used for pattern 1, 71h for pattern 2, 81h for pattern 3, similarly 91h for pattern 4.

| T2 | Hold Time Selection |
|---|---|
| 0000 | 0.04s |
| 0001 | 0.16s |
| 0010 | 0.31s |
| 0011 | 0.46s |
| 0100 | 0.61s |
| 0101 | 0.92s |
| 0110 | 1.25s |
| 0111 | 1.92s |
| 1000 | 2.52s |
| 1001 | 3.12s |
| 1010 | 3.72s |
| 1011 | 5.04s |
| 1100 | 6.24s |
| 1101 | 7.44s |
| 1110 | 8.76s |
| 1111 | 9.96s |

| T3 | Fall Time Selection |
|---|---|
| 0000 | 0.04s |
| 0001 | 0.16s |
| 0010 | 0.31s |
| 0011 | 0.46s |
| 0100 | 0.61s |
| 0101 | 0.92s |
| 0110 | 1.25s |
| 0111 | 1.92s |
| 1000 | 2.52s |
| 1001 | 3.12s |
| 1010 | 3.72s |
| 1011 | 5.04s |
| 1100 | 6.24s |
| 1101 | 7.44s |
| 1110 | 8.76s |
| 1111 | 9.96s |

**Table 20 62/72/82/92h Pattern TP &T4 Setting Register**

| Bit | D7:D4 | D3:D0 |
|---|---|---|
| Name | T4 | TP |
| Default | 0000 | 0000 |

The TP & T4 Setting Registers set the TP and T4 time in Pattern Mode. 62h register is used for pattern 1, 72h for pattern 2, 82h for pattern 3, similarly 92h for pattern 4.

It should be noted that the sleep mode effective time is 40s, it starts at the end of T3. If T4+TP is too long, pattern loop will stop. When sleep mode is enabled, T4 & TP do not last longer than 4.20s.

| TP | Time between Pulses |
|---|---|
| 0000 | 0.04s |
| 0001 | 0.16s |
| 0010 | 0.31s |
| 0011 | 0.46s |
| 0100 | 0.61s |
| 0101 | 0.92s |
| 0110 | 1.25s |
| 0111 | 1.92s |
| 1000 | 2.52s |
| 1001 | 3.12s |
| 1010 | 3.72s |
| 1011 | 5.04s |
| 1100 | 6.24s |
| 1101 | 7.44s |
| 1110 | 8.76s |
| 1111 | 9.96s |

| T4 | Off Time Selection |
|---|---|
| 0000 | 0.04s |
| 0001 | 0.16s |
| 0010 | 0.31s |
| 0011 | 0.46s |
| 0100 | 0.61s |
| 0101 | 0.92s |
| 0110 | 1.25s |
| 0111 | 1.92s |
| 1000 | 2.52s |
| 1001 | 3.12s |
| 1010 | 3.72s |
| 1011 | 5.04s |
| 1100 | 6.24s |
| 1101 | 7.44s |
| 1110 | 8.76s |
| 1111 | 9.96s |

**Table 21 63/73/83/93h Pattern Color Enable Register**

| Bit | D7:D3 | D2 | D1 | D0 |
|---|---|---|---|---|
| Name | - | CE3 | CE2 | CE1 |
| Default | 00000 | 0 | 0 | 1 |

Pattern Color Enable Register enables/disable color function for each color in Pattern Mode. 63h register is used for pattern 1, 73h for pattern 2, 83h for pattern 3, similarly 93h for pattern 4.

Color Enable Register enables the color function for each color in Pattern Mode.

| CEx | Color Enable Selection |
|---|---|
| 0 | Color x disable |
| 1 | Color x enable |

**Table 22 64/74/84/94h Pattern Color Cycle Times Register**

| Bit | D7:D6 | D5:D4 | D3:D2 | D1:D0 |
|---|---|---|---|---|
| Name | - | CCT3 | CCT2 | CCT1 |
| Default | 00 | 00 | 00 | 00 |

Pattern Color Cycle Times Register Sets Color loop time for each color in pattern mode. 64h register is used for pattern 1, 74h for pattern 2, 84h for pattern 3, similarly 94h for pattern 4.

| CCTx | Color Cycle Times Selection |
|---|---|
| 00 | Endless |
| 01 | 1 time |
| 10 | 2 times |
| 11 | 3 times |

**Table 23-1 65h Pattern Register 1**

| Bit | D7:D4 | D3 | D2 | D1:D0 |
|---|---|---|---|---|
| Name | MTPLT1 | GAM1 | - | NXT1 |
| Default | 0000 | 0 | 0 | 01 |

GAM controls the gamma of pattern. MTPLT controls the loop of Pattern. NXT1 Only effective in RGB Group Mode.

| GAM1 | Gamma Selection |
|---|---|
| 0 | Gamma=2.4 |
| 1 | Linearity |

| MTPLT1 | Multi-Pulse Loop Time |
|---|---|
| 0000 | endless |
| 0001 | 1 time |
| 1111 | 15 times |

**NXT1 Pattern 1 Next**

01 Go to Pattern 2

00/10/11 Just stop

**Table 23-2 75h Pattern Register 2**

| Bit | D7:D4 | D3 | D2 | D1:D0 |
|---|---|---|---|---|
| Name | MTPLT2 | GAM2 | - | NXT2 |
| Default | 0000 | 0 | 0 | 01 |

GAM controls the gamma of pattern. MTPLT controls the loop of Pattern. NXT2 Only effective in RGB Group Mode.

**GAM2 Gamma Selection**

0 Gamma=2.4

1 Linearity

**MTPLT2 Multi-Pulse Loop Time**

0000 Endless

0001 1 time

…

1111 15 times

**NXT2 Pattern 2 Next**

01 Go to Pattern 1

10 Go to Pattern 3 (disable in RGB Group mode 4)

00/11 Just stop

**Table 23-3 85h Pattern Register 3**

| Bit | D7:D4 | D3 | D2 | D1:D0 |
|---|---|---|---|---|
| Name | MTPLT3 | GAM3 | - | NXT3 |
| Default | 0000 | 0 | 0 | 01 |

GAM controls the gamma of pattern. MTPLT controls the loop of Pattern. NXT3 Only effective in RGB Group Mode.

**GAM3 Gamma Selection**

0 Gamma=2.4

1 Linearity

**MTPLT3 Multi-Pulse Loop Time**

0000 endless

0001 1 time

…

1111 15 times

**NXT3 Pattern 3 Next**

01 Go to Pattern 1

10 Go to Pattern 2

11 Go to Pattern 4 (disable in RGB Group mode 3)

00 Just stop

**Table 23-4 95h Pattern Register 4**

| Bit | D7:D4 | D3 | D2 | D1:D0 |
|---|---|---|---|---|
| Name | MTPLT4 | GAM4 | - | NXT4 |
| Default | 0000 | 0 | 0 | 01 |

GAM controls the gamma of pattern. MTPLT controls the loop of Pattern. NXT4 Only effective in RGB Group Mode.

**GAM3 Gamma Selection**

0 Gamma=2.4

1 Linearity

**MTPLT3 Multi-Pulse Loop Time**

0000 endless

0001 1 time

…

1111 15 times

**NXT3 Pattern 4 Next**

01 Go to Pattern 1 (disable in RGB Group mode 3 and mode 4)

10 Go to Pattern 2 (disable in RGB Group mode 3 and mode 4)

11 Go to Pattern 3 (disable in RGB Group mode 3)

00 Just stop

**Table 24 66/76/86/96h Pattern Loop Times Register**

| Bit | D7 | D6:D0 |
|---|---|---|
| Name | PLTx_H | PLTx_L |
| Default | 0 | 000 0000 |

Pattern loop Times register sets the loop time of the pattern. 66h register is used for pattern 1, 76h for pattern 2, 86h for pattern 3, similarly 96h for pattern 4.

If PLT_H(D7)=0, PLT_L!=0

Pattern loop times:

$$Looptime = \sum_{n=0}^{6} D[n] \times 2^n \qquad (8)$$

If PLT_H(D7)=0, PLT_L=0, endless

If PLT_H(D7)=1, PLT_L!=0

Pattern loop times:

$$Looptime = 16 \times \sum_{n=0}^{6} D[n] \times 2^n \qquad (9)$$

If PLT_H(D7)=1, PLT_L=0, endless

**99h Color Update Register**

Write “0xC5” to 99h will update the data of 10h~1Bh/20h~2Bh/30h~3Bh.

**9Ah PWM Update Register**

Write “0xC5” to 9Ah will update the data of 40~57h.

**9B/9C/9D/9Eh Pattern time Update Register**

Write “0xC5” to 9B/9C/9D/9Eh will update the data of 60h~66h/70h~76h/80h~86h/90h~96h.

**9Fh Reset Register**

Once user writes “0xC5” to the Reset Register, IS31FL3292 will reset all registers to their default value. On initial power-up, the IS31FL3292 registers are reset to their default values for a blank display.

## TYPICAL APPLICATION INFORMATION

### GENERAL DESCRIPTION

IS31FL3292 is a 12-channel fun LED driver with auto breathing function. It has PWM Mode and Pattern Mode and Current Level Mode for RGB lighting effects.

### CURRENT SETTING

The maximum output current is 30mA. When IMAX="1", the 30mA will become 40mA. The Global Current Control register GCC can be used to set a lower current. The 8-bit CL registers (10h~18h) control the individual currents for each of the outputs.

For example, OUT1, OUT2 and OUT3 drive an RGB LED, OUT1 is Red LED, OUT2 is Green LED and OUT 3 is Blue LED. If GCC and CL bits are the same, then the RGB LED may appear slightly pink, or not so white. The CL bits can be used to adjust the IOUTx current so the RGB LED appears closer to a pure white color. We call this CL bit adjustment by another name: white balance register.

### PWM FREQUENCY SELECT

The IS31FL3292 output channels operate with a default 12-bit PWM resolution and the PWM frequency of 220Hz. Because all the OUTx channels are synchronized, the DC power supply will experience large instantaneous current surges when the OUTx channels turn ON. These current surges will generate an AC ripple on the power supply which cause stress to the decoupling capacitors. When the AC ripple is applied to a monolithic ceramic capacitor chip (MLCC) it will expand and contract causing the PCB to flex and generate audible hum in the range of between 20Hz to 20kHz, to avoid this hum, there are many countermeasures, such as selecting the capacitor type and value which will not cause the PCB to flex and contract.

An additional option for avoiding audible hum is to set the IS31FL3292's output PWM frequency above the audible frequency range. The Shutdown Control Register (01h) can be used to set the switching frequency to 220Hz/440Hz/23KHz. Combination settings of the PFS bits will result in different PWM frequency, select a value higher than 20kHz to avoid the audible frequency range.

### PWM CONTROL

The PWM Registers (40h~57h) can modulate LED brightness of each channels with 4096 steps. For example, if the data in PWM_H Register is "0000 0000" and in PWM_L Register is "0000 0100", then the PWM is 4/4096.

Writing new data continuously to the registers can modulate the brightness of the LEDs to achieve a breathing effect.

### CURRENT LEVEL MODE

The Current Level Registers (10h~1Bh) are active and can modulate LED peak current IOUT of each output with 256 steps independently. For example, if the data in Current Lever Register is "0000 0100", then the current level is the fourth step, with a current level of 4/256.

In Current Level Mode, a new value must be written to the Current Level registers to change the output current. Writing new data continuously to the registers can modulate the brightness of the LEDs to achieve breathing, blinking, or any other effects that the user defines.

In Current Level Mode, the output current (OUT1~OUT12) is configured by the Current Level Register (10h~1Bh).

### PWM MODE

PWM Mode is the combination of PWM and Current Level Mode. In this mode, the Current Level Registers (10h~1Bh) adjust the peak current ($I_{OUT}$) of the outputs, the PWM Registers (40h~57h) adjust the duty cycle of the output current, the final result is the output average current ILED.

**Table 17 Register of PWM Mode**

| Mode | Register | OUT1 | OUT2 | OUT3 |
|---|---|---|---|---|
| PWM | PWM_H | 41h | 43h | 45h |
| | PWM_L | 40h | 42h | 44h |
| | CL | 10h | 11h | 12h |
| | Register | OUT4 | OUT5 | OUT6 |
| | PWM_H | 47h | 49h | 4Bh |
| | PWM_L | 46h | 48h | 4Ah |
| | CL | 13h | 14h | 15h |
| | Register | OUT7 | OUT8 | OUT9 |
| | PWM_H | 4Dh | 4Fh | 51h |
| | PWM_L | 4Ch | 4Eh | 50h |
| | CL | 16h | 17h | 18h |
| | Register | OUT10 | OUT11 | OUT12 |
| | PWM_H | 53h | 55h | 57h |
| | PWM_L | 52h | 54h | 56h |
| | CL | 19h | 1Ah | 1Bh |

### RGB GROUP MODE

By setting the RGMS bits of the Operating Configure Register 3 (03h) to “01” “10” or “11”, the IS31FL3292 will operate in RGB Group Mode. In this mode 12 channels can be modulated breathing cycle independently by TS~TP (Figure 11). Setting different TS~T4 can achieve RGB breathing with auto color changing. All 12 outputs can be divided into 4 RGB groups. OUT1, OUT2, OUT3 in RGB group 1. OUT4, OUT5, OUT6 in RGB group 2. OUT7, OUT8, OUT9 in RGB group 3. OUT10, OUT11, OUT12 in RGB group 4. When RGMS bits is “01”, RGB Group 1/2/3/4 run in Pattern 1 to 4. When RGMS bits is “10”, RGB Group 1/2/3 run in Pattern 1 to 3, RGB Group 4 run in Pattern 4. When RGMS bits is “10”, RGB Group 1/2 run in Pattern 1 to 2, RGB Group 3/4 run in Pattern 3 to 4. The maximum intensity of each LED can be adjusted independently by the Color Setting Registers (10h~1Bh/20h~2Bh/30h~3Bh) (Table 28/29/30).

**Note 10:** If IS31FL3292 operates in the RGB Group Mode and then enters into sleep mode, the SLE bit needs to set as “0”, that the IS31FL3292 will wake up and disable the sleep mode.

### PATTERN MODE

By setting the MOD1~MOD12 bits of the Operating Configure Register (04h/05h/06h) to “01” and the RGMS bits of the Operating Configure Register 3 (03h) to “00”, the corresponding output will operate in Pattern Mode. In Pattern Mode, the timing characteristics for output current - current rising (T1), holding (T2), falling (T3) and off time (TS, TP, T4) (Figure 10), can be adjusted individually so that each output can independently maintain a pre-established pattern achieving mixing color breathing or a single-color breathing without requiring any additional interface activity, thus saving valuable system resources. OUT1~OUT3 running in Pattern 1, OUT4~OUT6 running in Pattern 2, OUT7~OUT9 running in Pattern 3, and OUT10~OUT12 running in Pattern 4.

### PATTERN COLOR SETTING

In Pattern Mode, the LED color is defined by COLx_Oy (x, y= 1, 2, 3) bits in Color Setting Registers (10h~1Bh/20h~2Bh/30h~3Bh). There are 4 RGB current combinations to generate 3 pre-defined colors for display. More than one of the 3 pre-defined colors can be chosen by setting CEx bits in Color Enable Register (63h/73h/83h/93h). When CEx is set, the color x is allowed to be displayed in current pattern.

In Pattern Mode, the output current (OUT1~OUT12) is configured by the Color Setting Register of Pattern as Table 25.

**Table 25 Color Register of Pattern Mode**

| Pattern Mode | Color Enable | OUT1 | OUT2 | OUT3 |
|---|---|---|---|---|
| Pattern 1 | CE1(63h) | 10h | 11h | 12h |
| | CE2(63h) | 20h | 21h | 22h |
| | CE3(63h) | 30h | 31h | 32h |
| Pattern Mode | Color Enable | OUT4 | OUT5 | OUT6 |
| Pattern 2 | CE1(73h) | 13h | 14h | 15h |
| | CE2(73h) | 23h | 24h | 25h |
| | CE3(73h) | 33h | 34h | 35h |
| Pattern Mode | Color Enable | OUT7 | OUT8 | OUT9 |
| Pattern 3 | CE1(83h) | 16h | 17h | 18h |
| | CE2(83h) | 26h | 27h | 28h |
| | CE3(83h) | 36h | 37h | 38h |
| Pattern Mode | Color Enable | OUT10 | OUT11 | OUT12 |
| Pattern 4 | CE1(93h) | 19h | 1Ah | 1Bh |
| | CE2(93h) | 29h | 2Ah | 2Bh |
| | CE3(93h) | 39h | 3Ah | 3Bh |

### PATTERN TIME SETTING

User should configure the related pattern time setting registers according to actual timing requirements via I2C interface before starting pattern. The pattern time is including TS, T1~T4 and TP. And the pattern has three continue lighting cycle as Color 1~Color 3. Please check the LED OPERATING MODE section for more about the time setting.

### GAMMA CORRECTION

In order to perform a better visual LED breathing effect, the device integrates gamma correction to the Pattern Mode. The gamma correction causes the change in intensity to appear more linear to the human eye.

Gamma correction, also known as gamma compression or encoding, is used to encode linear luminance to match the non-linear characteristics of display. Since the IS31FL3292 can modulate the brightness of the LEDs with 256 steps, a gamma correction function can be applied when computing each subsequent LED intensity setting such that the changes in brightness matches the human eye's brightness curve.

The IS31FL3292 provides three gamma corrections which can be set by GAM bits of Pattern Registers (65h/75h/85h/95h) for each pattern. The gamma correction is shown as below.

## BREATHING MARK FUNCTION

In RGB Group Mode or Pattern Mode, by setting the BME bit of the Breathing Mark Register (09h) to “1”, the breathing mark function is enabled. If the BME bit sets to “0”, the breathing mark function disabled. The CLK/V_BM pin is used as CLK. V_BM is an output pin. The breathing mark function is useful as a signal to notify the MCU when and where the pattern or color is running.

**Note 11:** When only one color is enabled in Pattern Color Enable Register (63/h73h/83h/93h = 0x01 or 0x02 or 0x04), the TMP bit can set as “00” and “1x”.

After selecting the PAMF (Pattern Mark Function) and CMF (Color Mark Function),

When you choose start of T2 (TMP=00): At the start time T2, V_BM will induce a falling edge and hold logic low, at the end of time period T2, V_BM will induce a rising edge.

When you choose start of TP(TMP=01): At the start time TP, V_BM will induce a falling edge and hold logic low, at the end of time period TP, V_BM will induce a rising edge.

When you choose start of T4(TMP=1x): At the start time T4, V_BM will induce a falling edge and hold logic low, at the end of time period T4, V_BM will induce a rising edge.

The VPE bit of 09h sets the pull up of the V_BM pin, when VPE= “0”, the V_BM is open drain and it needs external pull up resistor.

When VPE= “1”, the V_BM is pulled to internal VCC by 100kΩ.

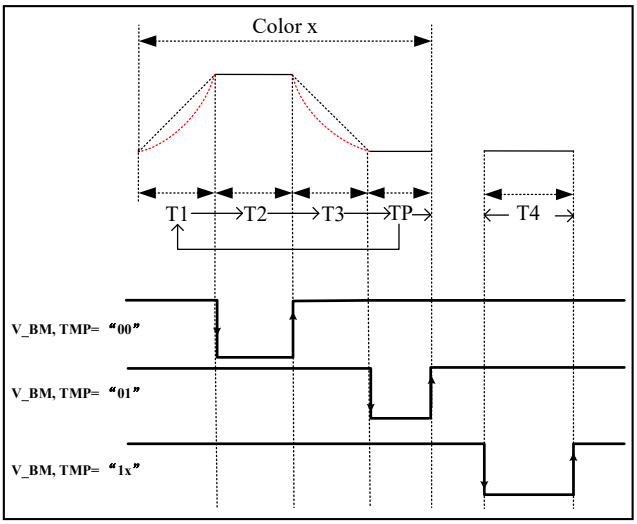



**Figure 8** V_BM Function

## SHUTDOWN MODE

Shutdown mode can either be used as a means of reducing power consumption or generating a flashing display (repeatedly entering and leaving shutdown mode). During shutdown mode all registers retain their data.

### Software Shutdown

By setting SSD bit of the Shutdown control Register (01h) to “0”, the IS31FL3292 will operate in software shutdown mode, wherein it will consume only 0.4μA (Typ.) current. When the IS31FL3292 is in software shutdown mode, all current sources are switched off.

### Hardware Shutdown

The chip enters hardware shutdown mode when the SDB pin is pulled low, wherein they consume only 0.4μA (Typ.) current. When set SDB high, the rising edge will reset the I2C module, but the register information retains.

## LED OPERATING MODE

When the RGMS = 00, 12 Outputs running individual. There have three operating modes which can be chosen by the MODx bits of Operating Configure Register (04h/05h/06h). When the RGMS = 01, 10 or 11, All 12 outputs can be divided into 4 RGB groups, and running in RGB Group mode.

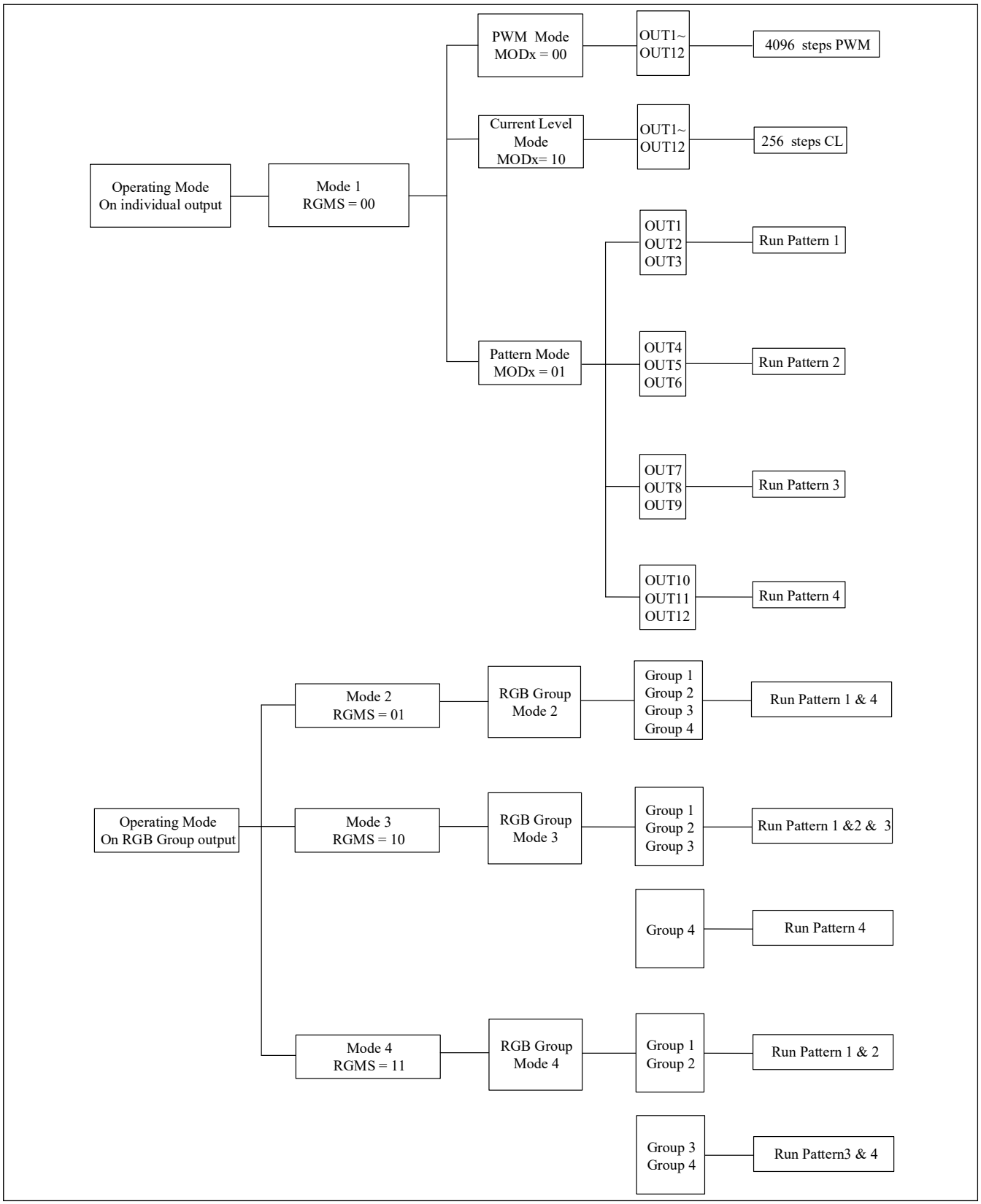



**Figure 9** Operating Mode Map

**Table 26 Pattern Select in RGB Group mode**

| | | | OUT1 | OUT2 | OUT3 | OUT4 | OUT5 | OUT6 | OUT7 | OUT8 | OUT9 | OUT10 | OUT11 | OUT12 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RGMS | RGB Group Mode | MODx | RGB Group 1 | | | RGB Group 2 | | | RGB Group 3 | | | RGB Group 4 | | |
| 00 | Mode 1 | 00 | Not run in Pattern | | | | | | | | | | | |
| | | 01 | Pattern 1 | | | Pattern 2 | | | Pattern 3 | | | Pattern 4 | | |
| | | 10 | Not run in Pattern | | | | | | | | | | | |
| 01 | Mode 2 | xx | Pattern 1 & Pattern 2 & Pattern 3 & Pattern 4 | | | | | | | | | | | |
| 10 | Mode 3 | xx | Pattern 1 & Pattern 2 & Pattern 3 | | | | | | | | | Pattern 4 | | |
| 11 | Mode 4 | xx | Pattern 1 & Pattern 2 | | | | | | Pattern 3 & Pattern 4 | | | | | |

### Pattern Mode

If MODx=10 (Pattern Mode), OUT1~OUT3 can operate in Pattern Mode only and run the pattern 1, OUT4~OUT6 run the pattern 2, OUT7~OUT9 run the pattern 3, OUT10~OUT12 run the pattern 4.

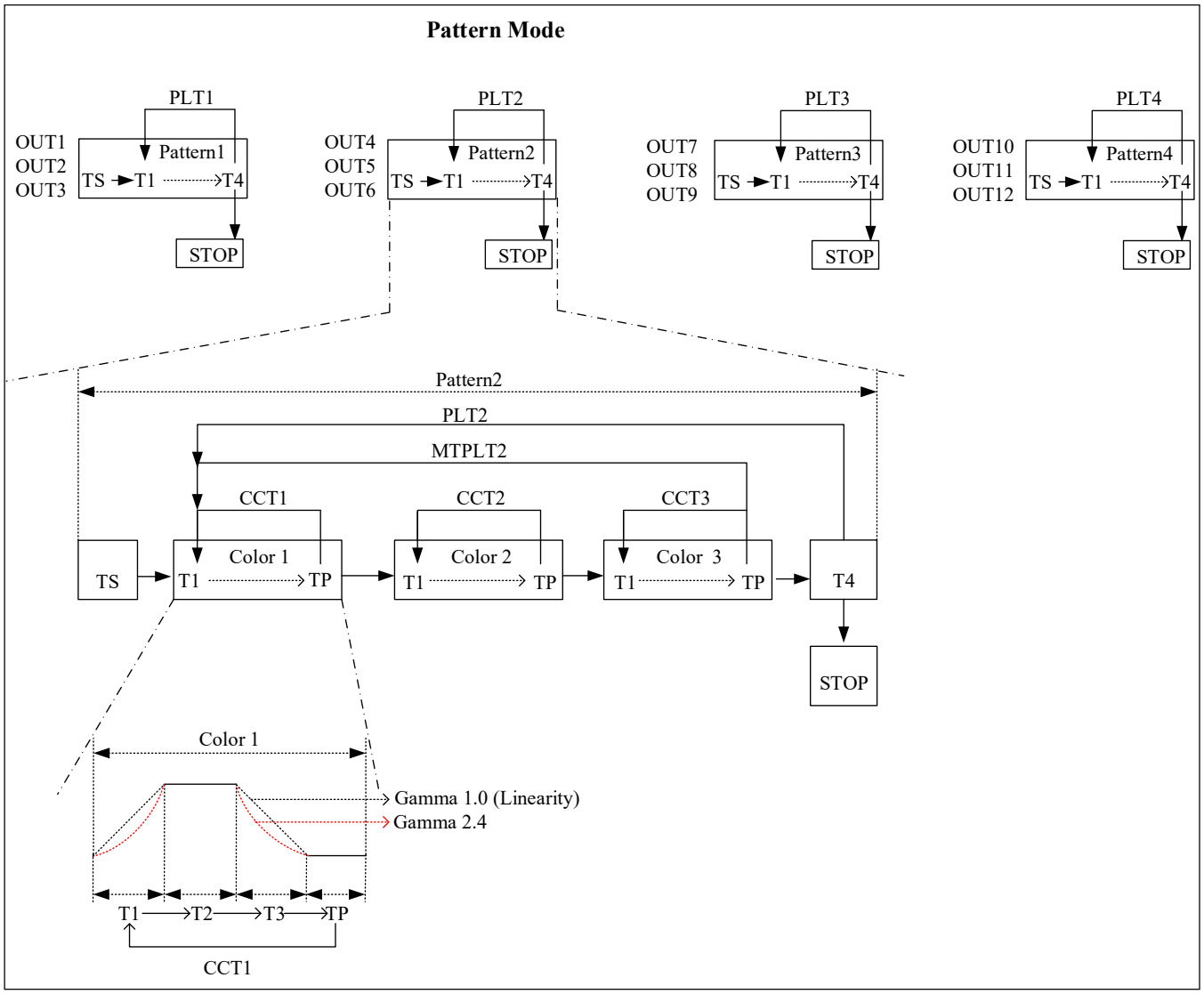



**Figure 10** Pattern Mode

**Table 27 Color Register of Pattern Mode**

| Pattern | Color Enable | OUT1 | OUT2 | OUT3 | OUT4 | OUT5 | OUT6 | OUT7 | OUT8 | OUT9 | OUT10 | OUT11 | OUT12 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Pattern 1 | CE1(63h) | 10h | 11h | 12h | | | | | | | | | |
| | CE2(63h) | 20h | 21h | 22h | | | | | | | | | |
| | CE3(63h) | 30h | 31h | 32h | | | | | | | | | |
| Pattern 2 | CE1(73h) | | | | 13h | 14h | 15h | | | | | | |
| | CE2(73h) | | | | 23h | 24h | 25h | | | | | | |
| | CE3(73h) | | | | 33h | 34h | 35h | | | | | | |
| Pattern 3 | CE1(83h) | | | | | | | 16h | 17h | 18h | | | |
| | CE2(83h) | | | | | | | 26h | 27h | 28h | | | |
| | CE3(83h) | | | | | | | 36h | 37h | 38h | | | |
| Pattern 4 | CE1(93h) | | | | | | | | | | 19h | 1Ah | 1Bh |
| | CE2(93h) | | | | | | | | | | 29h | 2Ah | 2Bh |
| | CE3(93h) | | | | | | | | | | 39h | 3Ah | 3Bh |

### RGB Group Mode

If RGMS="01 or 10 or 11", All 12 outputs can be divided into 4 RGB groups, and running in RGB Group mode.

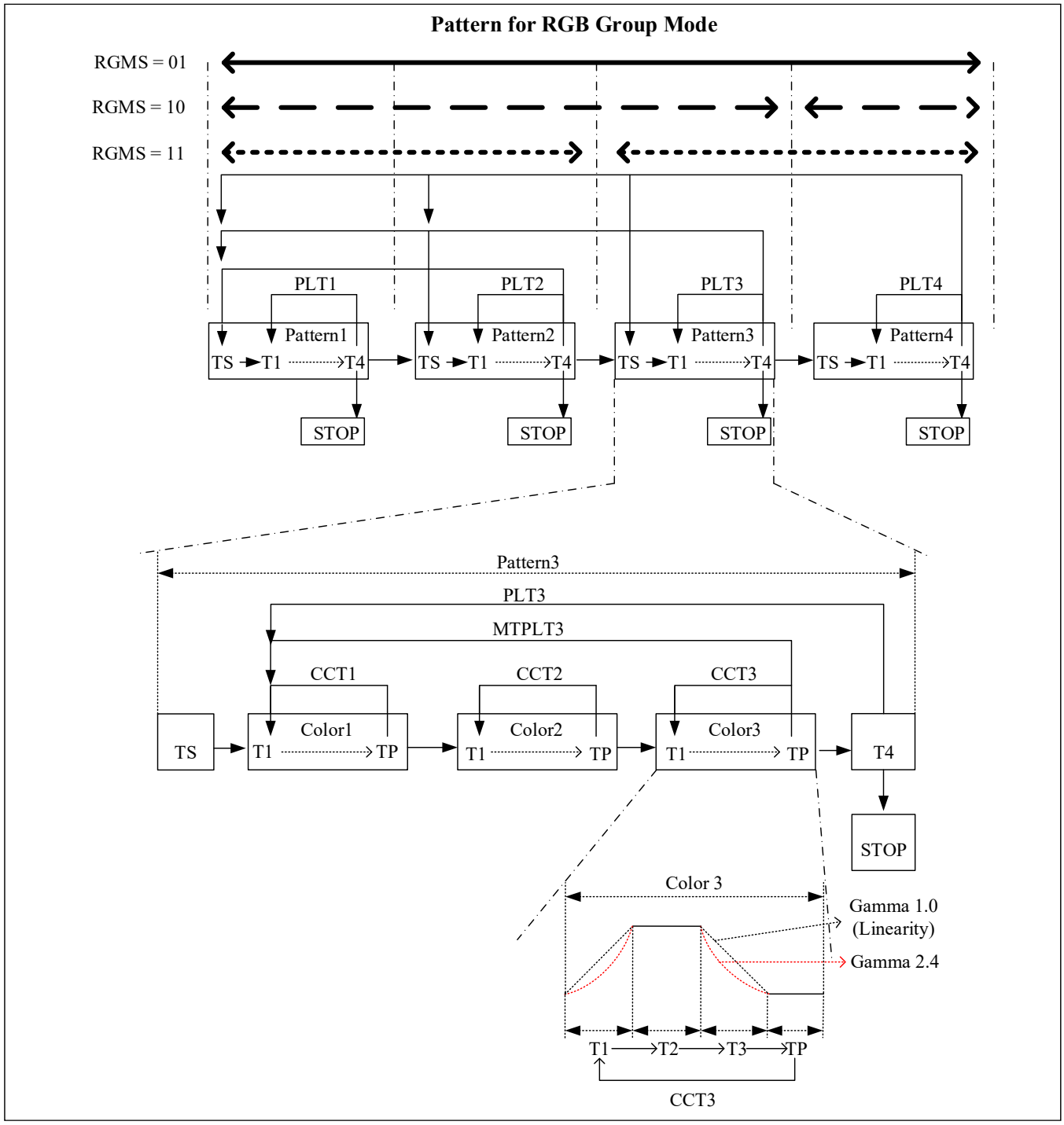



**Figure 11** RGB Group Mode

**Table 28 Color Register of RGB Group mode 2**

| Pattern | Color Enable | OUT1 | OUT2 | OUT3 | OUT4 | OUT5 | OUT6 | OUT7 | OUT8 | OUT9 | OUT10 | OUT11 | OUT12 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | RGB1 | | | RGB2 | | | RGB3 | | | RGB4 | | |
| Pattern 1 | CE1(63h) | 10h | 11h | 12h | 13h | 14h | 15h | 16h | 17h | 18h | 19h | 1Ah | 1Bh |
| | CE2(63h) | 20h | 21h | 22h | 23h | 24h | 25h | 26h | 27h | 28h | 29h | 2Ah | 2Bh |
| | CE3(63h) | 30h | 31h | 32h | 33h | 34h | 35h | 36h | 37h | 38h | 39h | 3Ah | 3Bh |
| Pattern 2 | CE1(73h) | 10h | 11h | 12h | 13h | 14h | 15h | 16h | 17h | 18h | 19h | 1Ah | 1Bh |
| | CE2(73h) | 20h | 21h | 22h | 23h | 24h | 25h | 26h | 27h | 28h | 29h | 2Ah | 2Bh |
| | CE3(73h) | 30h | 31h | 32h | 33h | 34h | 35h | 36h | 37h | 38h | 39h | 3Ah | 3Bh |
| Pattern 3 | CE1(83h) | 10h | 11h | 12h | 13h | 14h | 15h | 16h | 17h | 18h | 19h | 1Ah | 1Bh |
| | CE2(83h) | 20h | 21h | 22h | 23h | 24h | 25h | 26h | 27h | 28h | 29h | 2Ah | 2Bh |
| | CE3(83h) | 30h | 31h | 32h | 33h | 34h | 35h | 36h | 37h | 38h | 39h | 3Ah | 3Bh |
| Pattern 4 | CE1(93h) | 10h | 11h | 12h | 13h | 14h | 15h | 16h | 17h | 18h | 19h | 1Ah | 1Bh |
| | CE2(93h) | 20h | 21h | 22h | 23h | 24h | 25h | 26h | 27h | 28h | 29h | 2Ah | 2Bh |
| | CE3(93h) | 30h | 31h | 32h | 33h | 34h | 35h | 36h | 37h | 38h | 39h | 3Ah | 3Bh |

**Table 29 Color Register of RGB Group mode 3**

| Pattern | Color Enable | OUT1 | OUT2 | OUT3 | OUT4 | OUT5 | OUT6 | OUT7 | OUT8 | OUT9 | OUT10 | OUT11 | OUT12 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | RGB1 | | | RGB2 | | | RGB3 | | | RGB4 | | |
| Pattern 1 | CE1(63h) | 10h | 11h | 12h | 13h | 14h | 15h | 16h | 17h | 18h | | | |
| | CE2(63h) | 20h | 21h | 22h | 23h | 24h | 25h | 26h | 27h | 28h | | | |
| | CE3(63h) | 30h | 31h | 32h | 33h | 34h | 35h | 36h | 37h | 38h | | | |
| Pattern 2 | CE1(73h) | 10h | 11h | 12h | 13h | 14h | 15h | 16h | 17h | 18h | | | |
| | CE2(73h) | 20h | 21h | 22h | 23h | 24h | 25h | 26h | 27h | 28h | | | |
| | CE3(73h) | 30h | 31h | 32h | 33h | 34h | 35h | 36h | 37h | 38h | | | |
| Pattern 3 | CE1(83h) | 10h | 11h | 12h | 13h | 14h | 15h | 16h | 17h | 18h | | | |
| | CE2(83h) | 20h | 21h | 22h | 23h | 24h | 25h | 26h | 27h | 28h | | | |
| | CE3(83h) | 30h | 31h | 32h | 33h | 34h | 35h | 36h | 37h | 38h | | | |
| Pattern 4 | CE1(93h) | | | | | | | | | | 19h | 1Ah | 1Bh |
| | CE2(93h) | | | | | | | | | | 29h | 2Ah | 2Bh |
| | CE3(93h) | | | | | | | | | | 39h | 3Ah | 3Bh |

**Table 30 Color Register of RGB Group mode 4**

| Pattern | Color Enable | OUT1 | OUT2 | OUT3 | OUT4 | OUT5 | OUT6 | OUT7 | OUT8 | OUT9 | OUT10 | OUT11 | OUT12 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | RGB1 | | | RGB2 | | | RGB3 | | | RGB4 | | |
| Pattern 1 | CE1(63h) | 10h | 11h | 12h | 13h | 14h | 15h | | | | | | |
| | CE2(63h) | 20h | 21h | 22h | 23h | 24h | 25h | | | | | | |
| | CE3(63h) | 30h | 31h | 32h | 33h | 34h | 35h | | | | | | |
| Pattern 2 | CE1(73h) | 10h | 11h | 12h | 13h | 14h | 15h | | | | | | |
| | CE2(73h) | 20h | 21h | 22h | 23h | 24h | 25h | | | | | | |
| | CE3(73h) | 30h | 31h | 32h | 33h | 34h | 35h | | | | | | |
| Pattern 3 | CE1(83h) | | | | | | | 16h | 17h | 18h | 19h | 1Ah | 1Bh |
| | CE2(83h) | | | | | | | 26h | 27h | 28h | 29h | 2Ah | 2Bh |
| | CE3(83h) | | | | | | | 36h | 37h | 38h | 39h | 3Ah | 3Bh |
| Pattern 4 | CE1(93h) | | | | | | | 16h | 17h | 18h | 19h | 1Ah | 1Bh |
| | CE2(93h) | | | | | | | 26h | 27h | 28h | 29h | 2Ah | 2Bh |
| | CE3(93h) | | | | | | | 36h | 37h | 38h | 39h | 3Ah | 3Bh |

## CLASSIFICATION REFLOW PROFILES

| Profile Feature | Pb-Free Assembly |
|---|---|
| **Preheat & Soak**<br>Temperature min (Tsmin)<br>Temperature max (Tsmax)<br>Time (Tsmin to Tsmax) (ts) | 150°C<br>200°C<br>60-120 seconds |
| Average ramp-up rate (Tsmax to Tp) | 3°C/second max. |
| Liquidous temperature (TL)<br>Time at liquidous (tL) | 217°C<br>60-150 seconds |
| Peak package body temperature (Tp)* | Max 260°C |
| Time (tp)** within 5°C of the specified classification temperature (Tc) | Max 30 seconds |
| Average ramp-down rate (Tp to Tsmax) | 6°C/second max. |
| Time 25°C to peak temperature | 8 minutes max. |

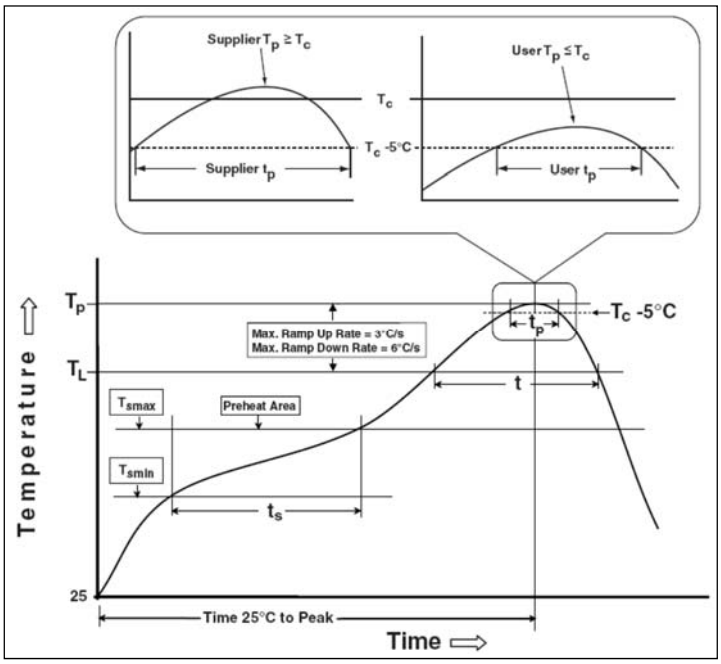
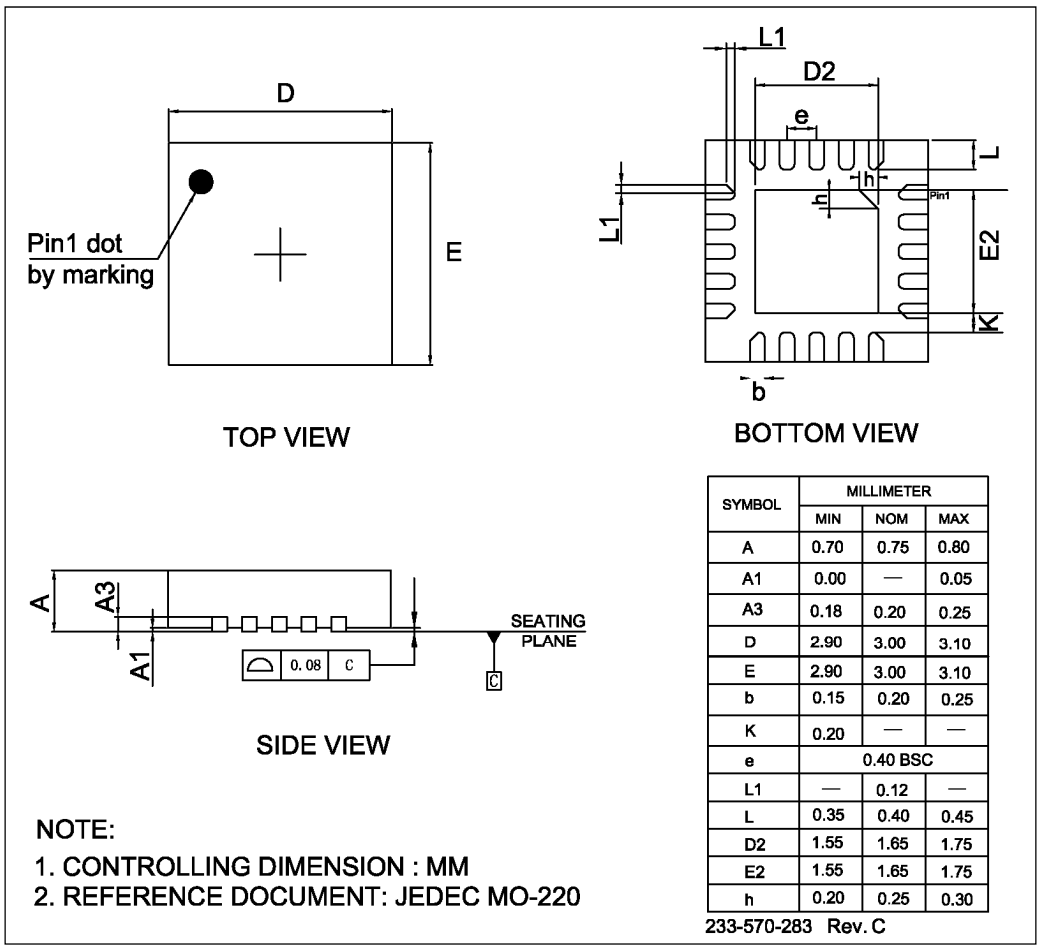



**Figure 12** Classification Profile

## PACKAGE INFORMATION

### QFN-20



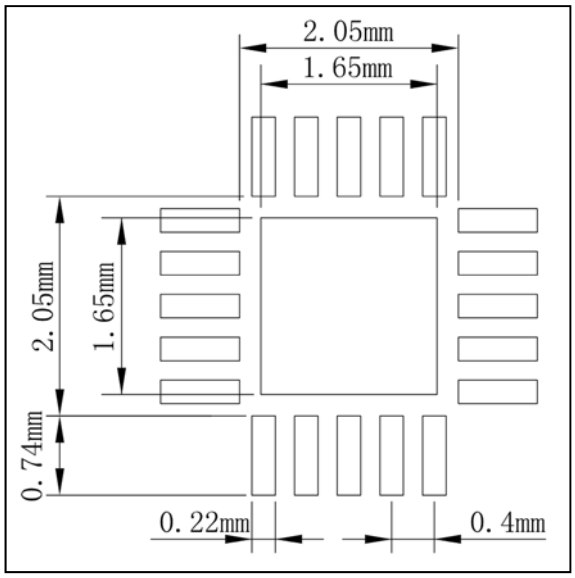

| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0.00 | — | 0.05 |
| A3 | 0.18 | 0.20 | 0.25 |
| D | 2.90 | 3.00 | 3.10 |
| E | 2.90 | 3.00 | 3.10 |
| b | 0.15 | 0.20 | 0.25 |
| K | 0.20 | — | — |
| e | 0.40 BSC | | |
| L1 | — | 0.12 | — |
| L | 0.35 | 0.40 | 0.45 |
| D2 | 1.55 | 1.65 | 1.75 |
| E2 | 1.55 | 1.65 | 1.75 |
| h | 0.20 | 0.25 | 0.30 |

NOTE:
1. CONTROLLING DIMENSION : MM
2. REFERENCE DOCUMENT: JEDEC MO-220

233-570-283 Rev. C

## RECOMMENDED LAND PATTERN

### QFN-20




**Note:**

1. Land pattern complies to IPC-7351.
2. All dimensions in MM.
3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (e.g. User's board manufacturing specs), user must determine suitability for use.

**REVISION HISTORY**

| Revision | Detail Information | Date |
|---|---|---|
| 0A | Initial Release | 2023.11.13 |
| A | 1. Updated Lumissil new Logo<br>2. Updated the EC table<br>3. Updated description of registers 01h and 03h<br>4. Added notes 7, 8, 9 ,10 and 11<br>5. Updated figures 9 and 11<br>6. Updated tables 27, 28, 29 and 30 | 2024.05.24 |