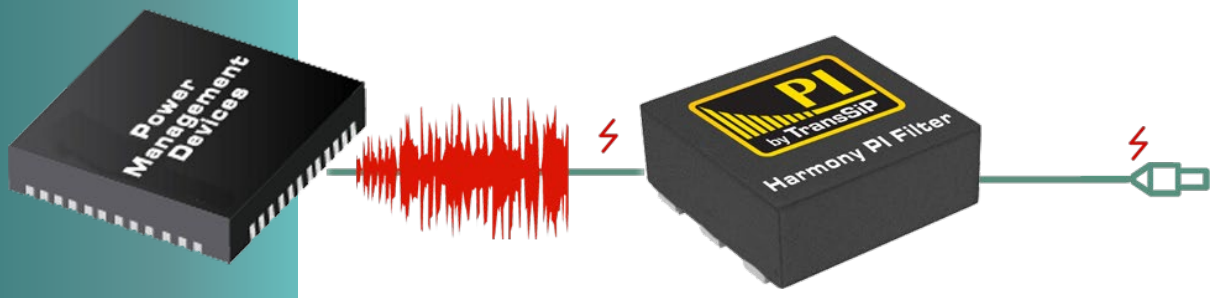
# Harmony PI Filter

## With SNJ Conditioning




## Applications:

- Power Source
- Wireless
- Computing
- Signal Processing
- Sensitive Devices

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## Revision History

| | | |
|---|---|---|
| 3/2019 | Revision 1.0 | Initial Release. |
| | Revision 2.0 | New ampacity options for 1A, 2A and 5A. |
| 3/2020 | Revision 3.0 | Updated application block diagram 1.3, and Wiki URL for SNJ. |
| 9/2020 | Revision 4.0 | Updated MSL handling to level 2a |
| 1/2021 | Revision 5.0 | Updated laser marking and PCB land pattern |
| 2/2022 | Revision 6.0 | Updated description, application circuits, and credentials |

## Design Resources

### Evaluation Kits

- Harmony Evaluation Board with SMA


### Reference Materials

- Harmony App Note

## Credentials





## Trademark Notice

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# 1.0 Introduction

Harmony PI filter is the world's first device-level and the most versatile solution for enhancing power integrity (PI) and signal integrity (SI). The patented switching noise jitter (SNJ) conditioning technology provides robust noise mitigation in two domains: Time and Frequency. The technology enables systems to achieve exciting levels of signal clarity, accuracy, and reliability. After all, Harmony is in a tiny package of 2.2 mm x 2.6 mm x 0.9 mm. It doesn't consume power, and there is no IR drop.

Harmony can be applied in the power chain and signal chain. When used in the power chain, the time-domain feature suppresses SNJ and chaotic noise at the output of a switching mode power supply. As a result, it makes high-speed current loops that are small to reduce radiated EMI, stabilize switching power supplies, and increase power conversion efficiency. At the same time, Harmony helps isolate noise generated from other parts of a circuit to affect the whole system, such as simultaneous switching noise (SSN), ground bounce, etc. In addition, Harmony eliminates problematic anti-resonance peaks, impedance violation, LC tank oscillations, voltage overshoot, and incorrect operation commonly caused by ferrite beads, capacitor banks, EMI, and RFI filters.

As a result, Harmony enables systems to run faster, more accurately, and reliably under real-world weak signal conditions. Furthermore, when a system runs algorithms more accurately, the processor run-time decreases because the repetition of iteration decreases; thus, extra energy saving is achievable.

For small signals produced by sensors below 1 kHz, such as Geophones, MEMS, LEDs, and photodetectors for biomedical monitors, applying Harmony to the signal chain provides a native 3dB cutoff at 700 Hz and eliminates all unwanted signals and noise after that. It helps simplify system architecture and cut costs by eliminating power-hungry and complex digital filtering, such as delta-sigma A/D converter.

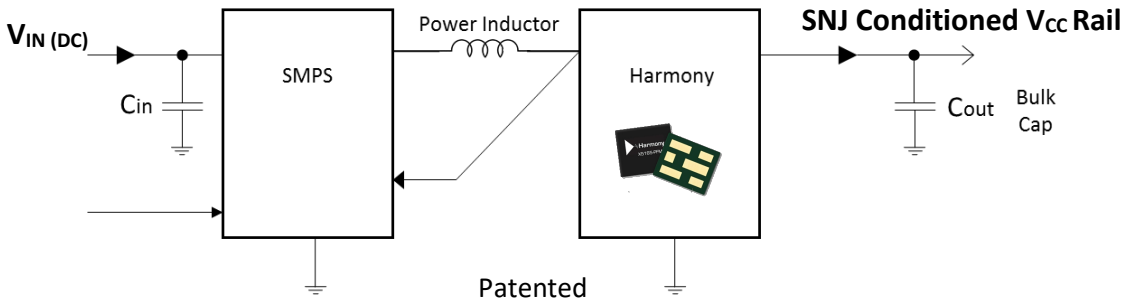
## 1.1 Applications

- **Power Source:** PMIC, SMPS, Energy Harvesting
- **Wireless:** GPS, LTE, CAT-M, NB-IOT, 5G, WLAN
- **Computing:** Solid State Disks, Memories, Graphic Cards, Motherboards
- **Signal Processing:** A/D, D/A, Audio, Video
- **Sensitive Devices:** High Precision Clocks, LEDs, Photodetectors, Geophones, MEMS, biomedical

**Key Features:**

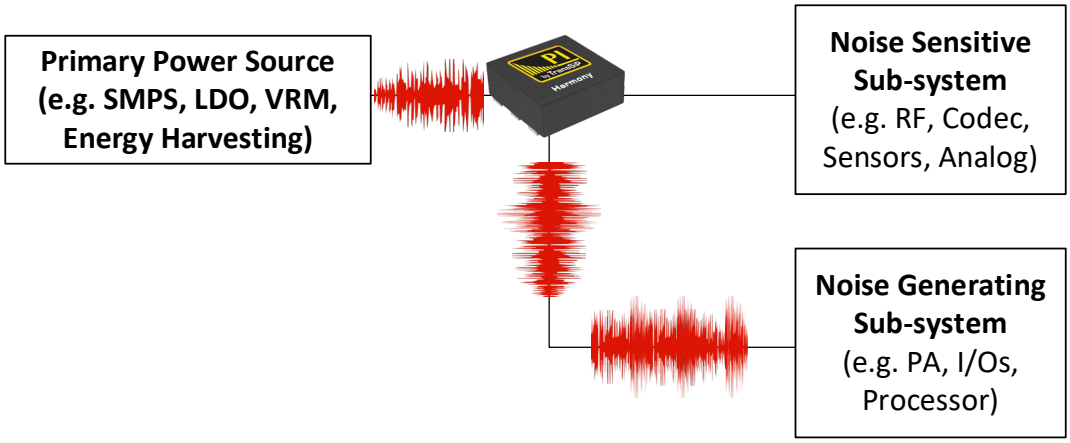
- Ampacity Options: 1A, 2A and 5A
- Voltage Rating: 6V DC
- Time Domain SNJ Conditioning
- Native 3dB Cutoff: 700 Hz
- Ultra-wideband Noise Suppression
- No IR Drop
- Operating Temperature: -55°C to +85°C
- RoHS
- 2.2 x 2.6 x 0.9 [mm]

## 1.2 TransSiP JC Circuit Topology in Power Chain (Simplified Schematic)

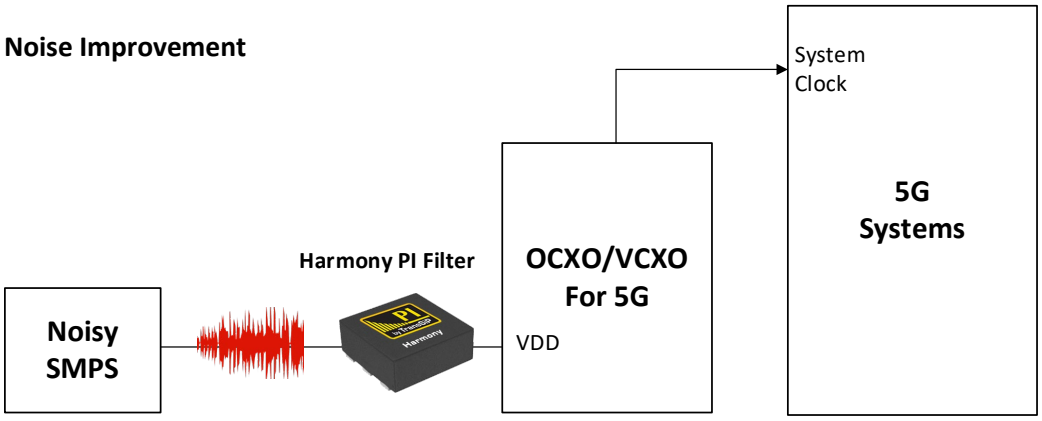


## 1.3 Application Examples

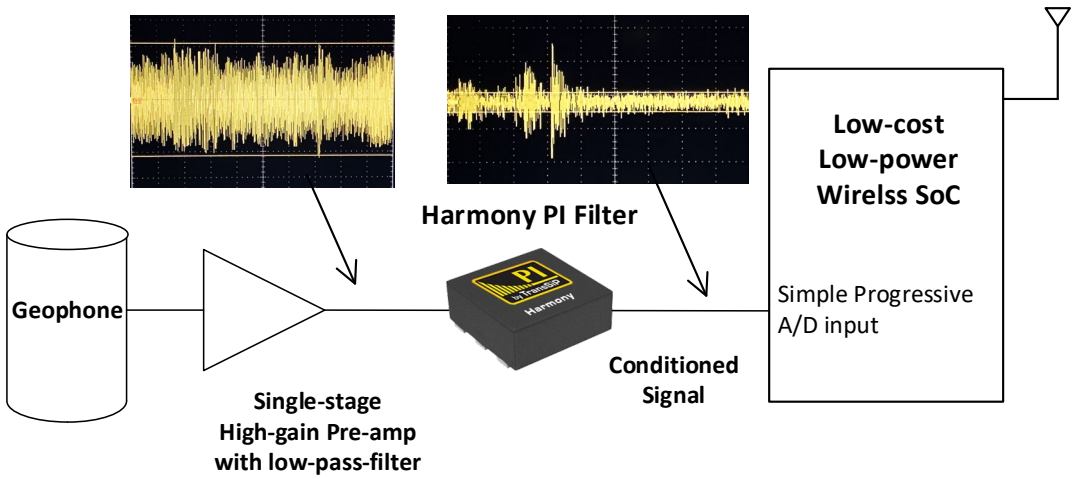
**Power Rails Isolation**



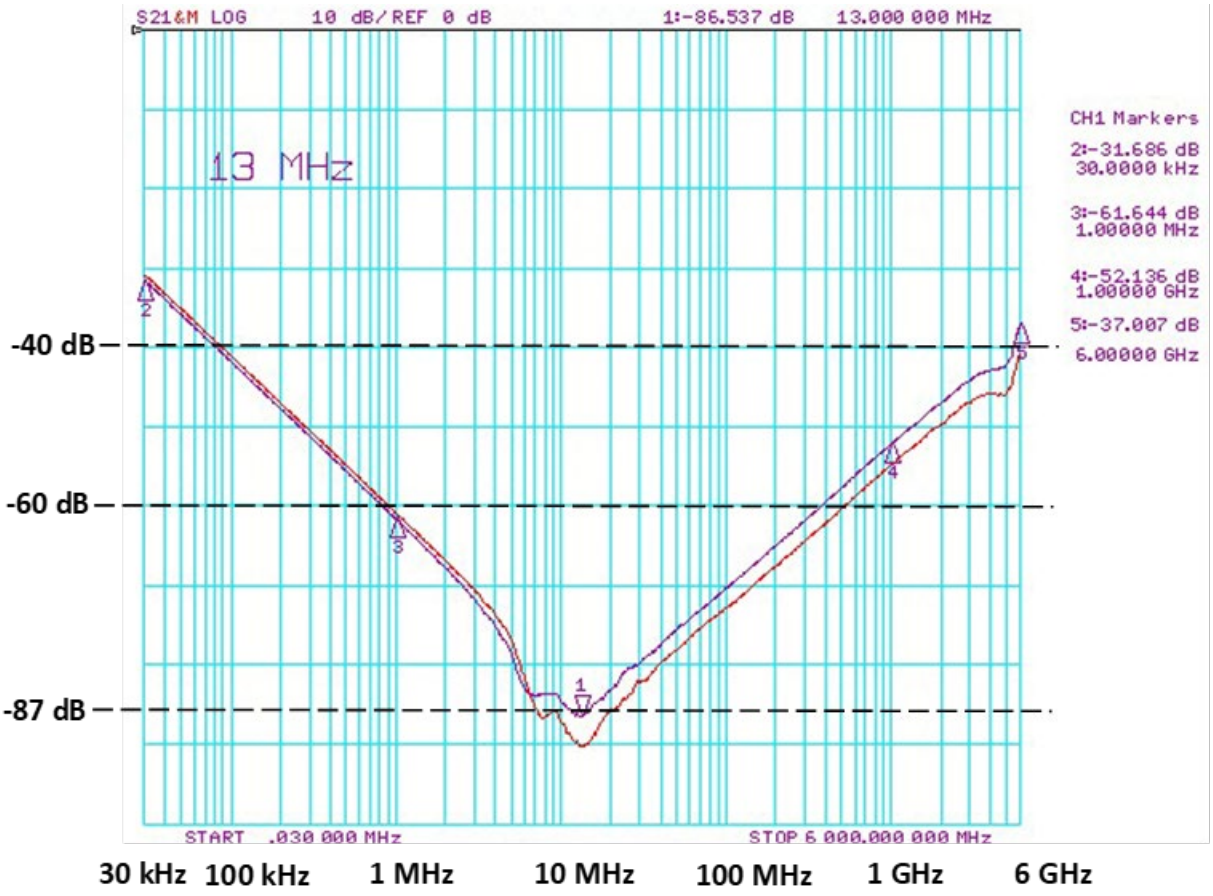

**Phase Noise Improvement**




**Simplify Signal Chain and Significantly Lower Energy Consumption**



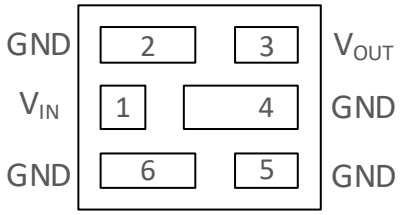
## 1.4 Insertion Loss Characteristics (Native)




# 2.0 Ordering Information

| Harmony PN TSNJ-①②③④ | Characteristics | SYMBOL | DESCRIPTION |
|---|---|---|---|
| ① | Rated Current | 1, 2 or 5 | Ampacity: 1 = 1A, 2 = 2A, 5 = 5A |
| ② | Reserved | A | Current Identifier |
| ③ | Rated Voltage | 6 | Rated voltage = 6 V DC |
| ④ | Package | L26 | LGA-2226 / 2.2 mm x 2.6mm x 0.9 mm |

## 2.1 Pin Assignment and Package Type

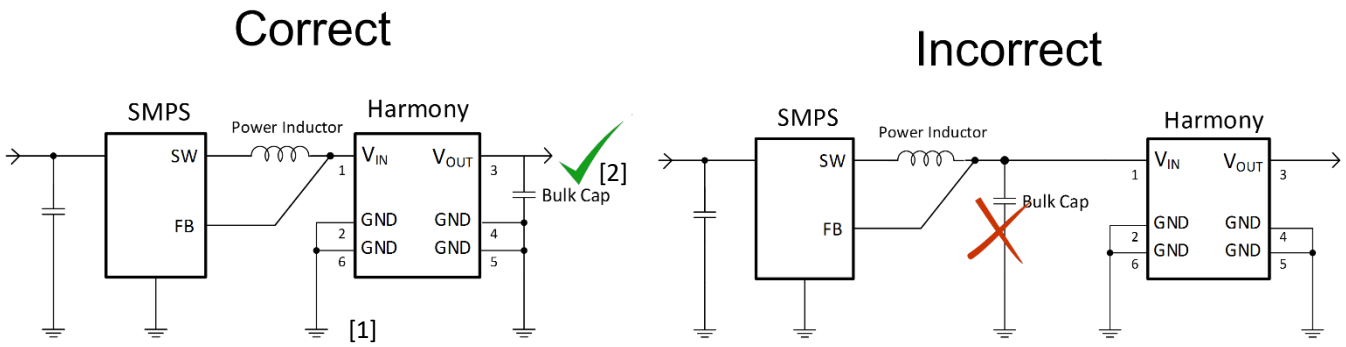



LGA-2226
(BOTTOM VIEW)

| Harmony LGA-2226 | Pin Name | Function |
|---|---|---|
| 1 | $V_{IN}$ | Voltage / Signal Input |
| 2 | GND | Ground |
| 3 | $V_{OUT}$ | Voltage / Signal Output |
| 4 | GND | Ground |
| 5 | GND | Ground |
| 6 | GND | Ground |

# 3.0 Application Information

## 3.1 Circuit Topology for SMPS

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Note [1]: Place the Harmony in close proximity to the power inductor and feedback (FB) node with traces as wide and as short as possible. Pay attention to the Grounding Guidelines in section 3.2.

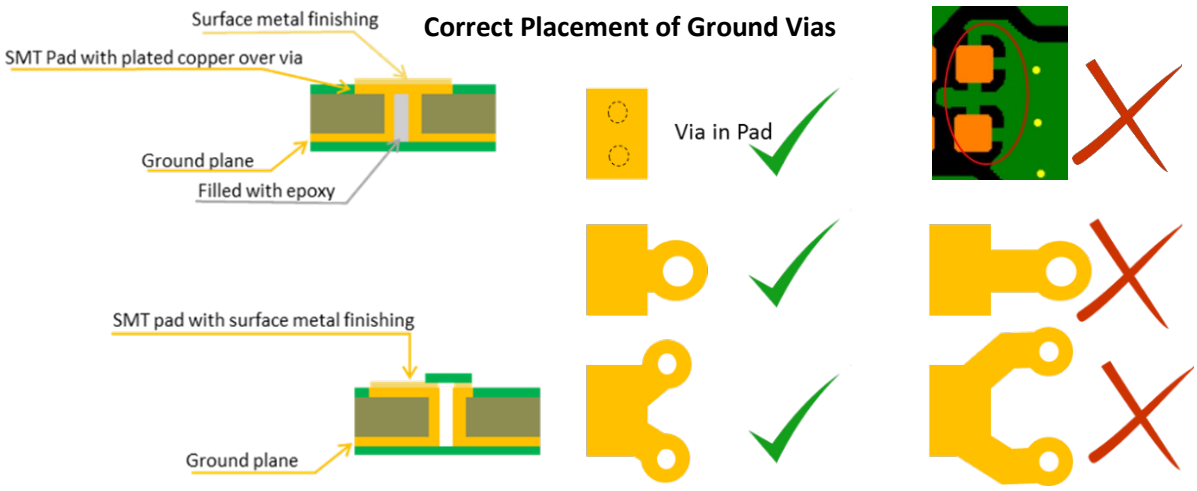
Note [2]: The bulk cap must be connected adjacent to the output of Harmony but NOT at the junction of the power inductor and FB node commonly used in conventional DC-DC topology. The bulk cap is typically with large capacitance or a bank of large capacitors. Small value capacitor is not required at the output of Harmony.

Glossary: SMPS stands for Switching Mode Power Supply

## 3.2 Harmony Grounding and SMPS Layout Guidelines

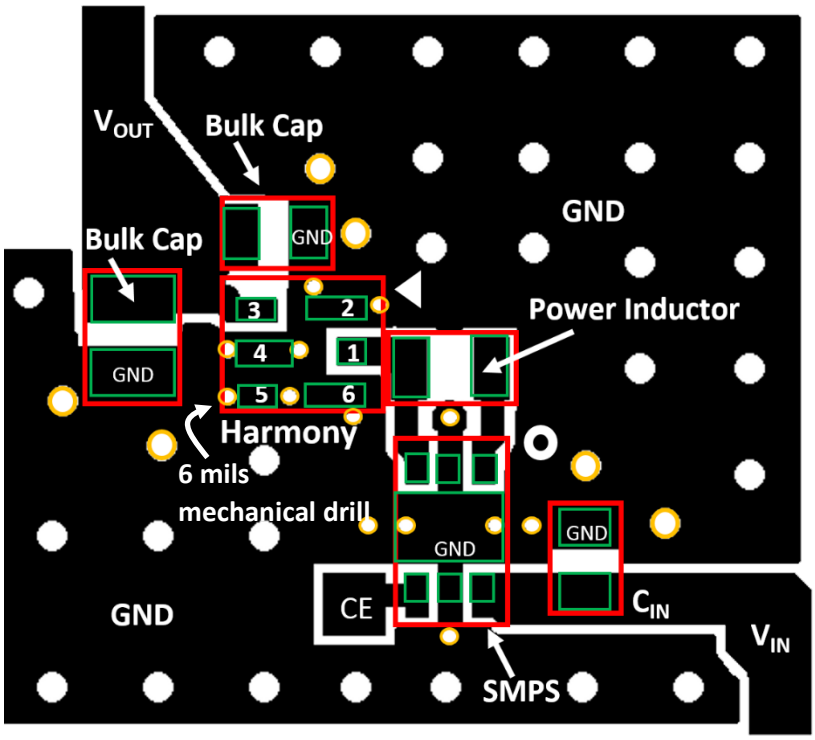
Grouding is of utmost importance to avoid potential performance, stability, and EMI problems. Key notes on layout are listed as follows:

1. **Ground Plane** – use a ground plane in the inner layer immediately below the Harmony. Connect each GND terminals directly to the ground plane by ground vias. 6 mil (152.4 µm) mechanical drill holes for the ground vias is adequate and must be placed immediately adjacent to the ground terminals as shown in the pictures above. At least one ground via at each end of the GND terminals should be used. Do not use long trace and thermal reliefs to connect the GND terminals. The ground plane should be directly connected to a battery or power source using as wide and as short a connection as possible.
2. **Via-in-Pad** – for compact design, using via-in-pad for connecting all the GND terminals of Harmony is highly recommended.
3. **Laser Drill** – because the typical diameter of a laser drill via is 50 µm or less, use multiple laser vias but not one in each of the ground terminals of the Harmony.
4. **Signal and Power Traces** – don't run signal and power traces under or in the inner layer below the Harmony without a ground plane inserted in between.
5. **SMPS** – when the Harmony is used with a SMPS, place the Harmony (Pin 1 - Vin) in close proximity to the power inductor and feedback node with traces as wide and as short as possible. Do not route traces under the power inductor.
6. **Stitching Vias** – ground planes between different layers should be interconnected with as many ground vias in close proximity as possible. Do not use a single via or vias with large separation to connect different layers of ground planes.



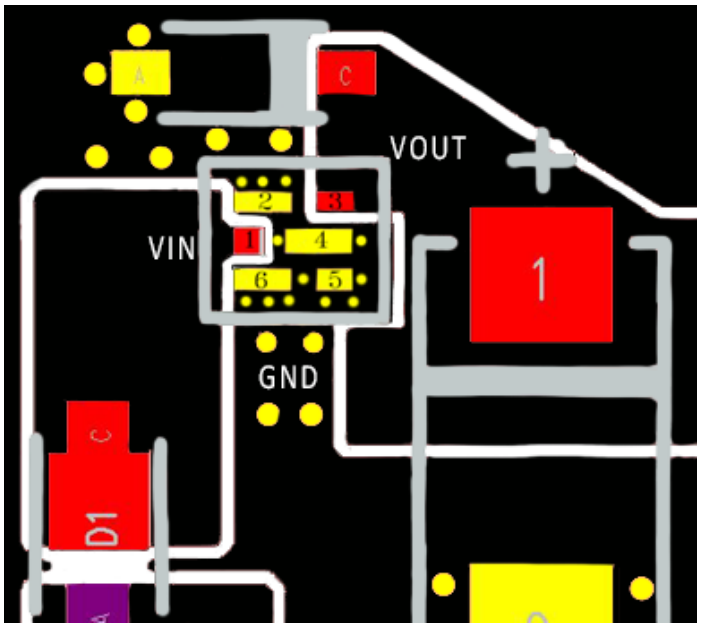
**Example Layout: Harmony for SMPS**

**(TOP LAYER PLACEMENT)**




**Example Layout: Harmony for Power Rail Isolation**

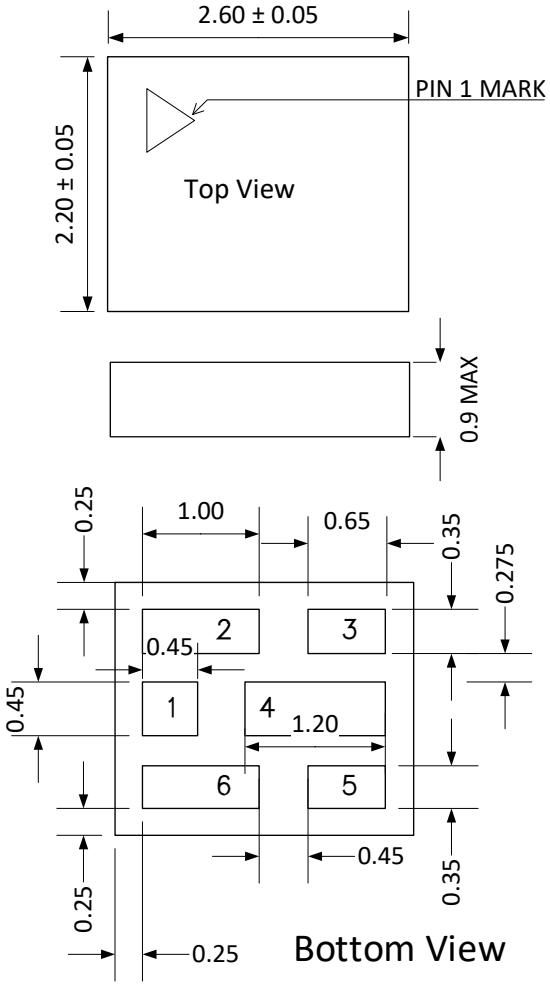
**(BOTTOM LAYER PLACEMENT)**



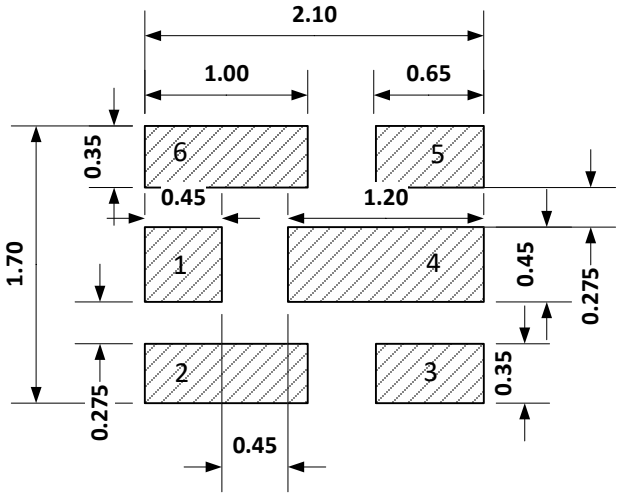
# 4.0 Package and PCB Land Pattern Information

**Unit: mm**

**Harmony LGA-2226**




**LGA-2226 PCB Land Pattern (Top View)**

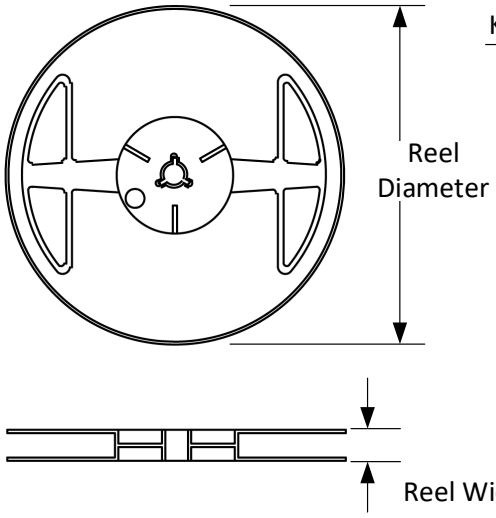



**Marking**

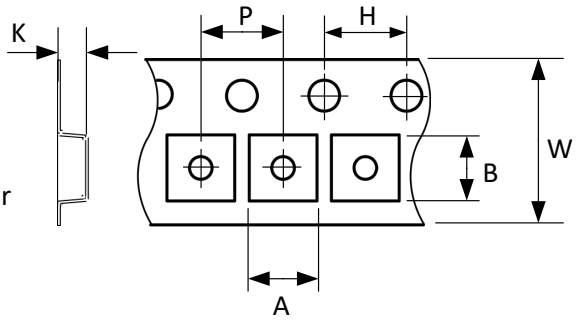

4-Digit Date Code Syntax: Week No. Year

## 5.0 Tape and Reel Information

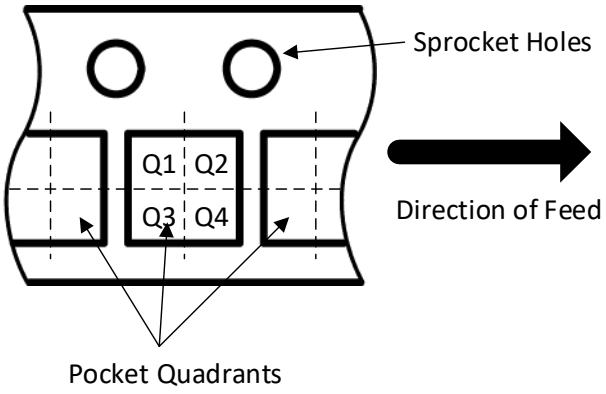
### Reel Dimensions




### Tape Dimensions




### Quadrant Assignments for Pin 1 Orientation in Tape




| Device | Package Type | Pins | Pin 1 Quadrant | Reel Diameter | Reel Width W1 | A | B | K | P | H | W | Qty/ Reel |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Harmony | LGA-2226 | 6 | Q2 | 180 | 14.0 | 2.4 | 2.8 | 1.05 | 4.0 | 4.0 | 12.0 | 3000 |

# 6.0 Handling and Soldering

## 6.1 Moisture Sensitivity Level 2a (MSL 2a) Handling at PCB Assembly

Harmony is moisture sensitive and needed to be handled with proper MSL 2a guidelines as outlined in J-STD-033D and J-STD-020E to avoid damage due to vaporization of absorbed moisture during reflow operations.

This device is also a new type of microSMT, therefore peak package temperature should not exceed 250°C and time at peak temperature should be < 5 sec.

MSL 2a devices are dry-packed prior to shipment from TransSiP. The packing uses a Moisture Barrier Bag (MBB) with desiccant and a Humidity Indicator Card (HIC). Shelf life of devices in a sealed bag is 12 months at <40°C and <90% room humidity (RH).

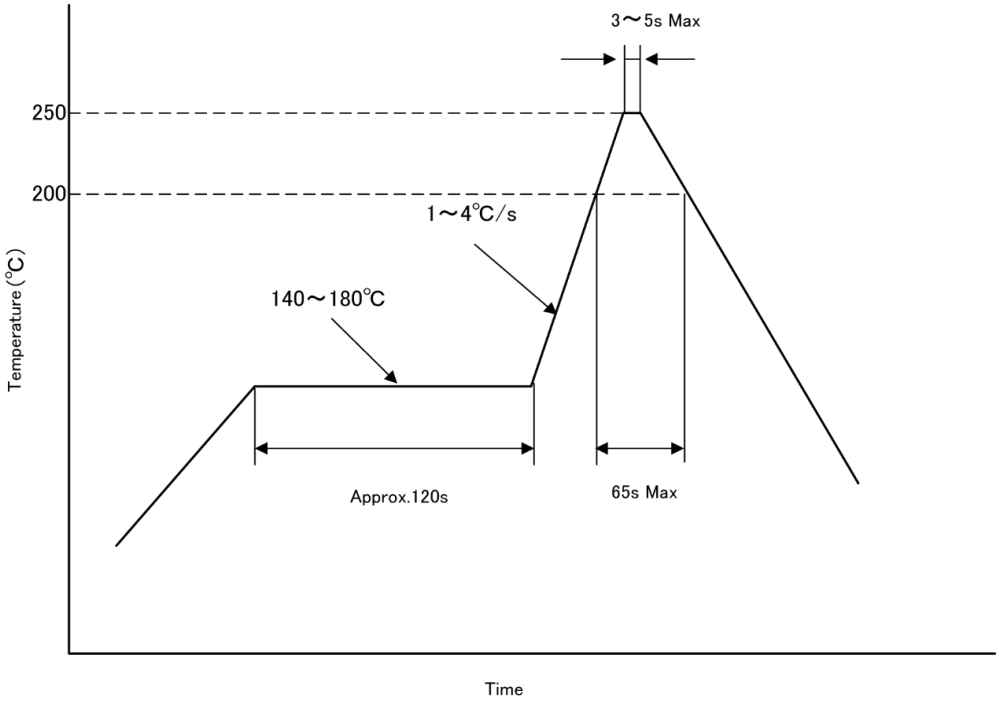
Upon opening of MBB, the HIC should be checked immediately; If the HIC is >10% when read at 23 ±5°C the parts will require dry baking prior to reflow.

After the MBB is opened, maximum floor life at factory ambient not to exceed 30°C/60% RH is 4 weeks. Parts which exceed this limit must be dry baked prior to reflow. Floor life is started to count and accumulate from the opening of the MBB that the counting of the 4 weeks period may be stopped if the parts are stored in dry cabinet at <10% RH.

When the accumulated floor life exceeds 4 weeks, dry baking is required before board mounting, please refer to J-STD-033D, Table 4-1 for required dry baking conditions- the MSL 2a devices will require a minimum of 9 days at 40°C, ≤5% RH. Further information may be found in Application Bulletin AP-0920 available through your TransSiP representative.

## 6.2 Reflow

The Symphony chipset is compatible with lead free soldering processes as defined in IPC/JEDEC J-STD-020. The reflow profile must not exceed the profile given IPC/JEDEC J-STD-020 Table 5-2, “Classification Reflow Profiles”.



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