TFT DISPLAY SPECIFICATION

WINSTAR Display Co.,Ltd.

華凌光電股份有限公司

Winstar Display Co., LTD
華凌光電股份有限公司
WEB: https://www.winstar.com.tw E-mail: sales@winstar.com.tw

SPECIFICATION

CUSTOMER : _____

MODULE NO.: WF0675ATYAB6MNG0#

APPROVED BY: **(FOR CUSTOMER USE ONLY)**	**PCB VERSION:** **DATA:**

SALES BY	APPROVED BY	CHECKED BY	PREPARED BY
			葉虹蘭
ISSUED DATE: 2024/03/05			

TFT Display Inspection Specification: https://www.winstar.com.tw/technology/download.html
Precaution in use of TFT module: https://www.winstar.com.tw/technology/download/declaration.html

Winstar Display Co., LTD 華凌光電股份有限公司	MODLE NO：
RECORDS OF REVISION	**DOC. FIRST ISSUE**

VERSION	DATE	REVISED PAGE NO.	**SUMMARY**
0	2023/12/04		First issue
A	2024/03/05		Modify General Specifications ,Table 1 and Power on/off Sequence

Contents

1.Module Classification Information

W	F	0675	A	T	Y	A	B6	M	N	G	0	#
①	②	③	④	⑤	⑥	⑦	⑧	⑨	⑩	⑪	⑫	⑬

①	Brand：WINSTAR DISPLAY CORPORATION		
②	Display Type：F→TFT Type, J→Custom TFT		
③	Display Size：067.5” TFT		
④	Model serials no.		
⑤	Backlight Type：	F→CCFL, White S→LED, High Light White	T→LED, White Z→Nichia LED, White
⑥	LCD Polarize Type/ Temperature range/ Gray Scale Inversion Direction	A→Transmissive, N.T, IPS TFT C→Transmissive, N. T, 6:00 ; F→Transmissive, N.T,12:00 ; I→Transmissive, W. T, 6:00 K→Transflective, W.T,12:00 L→Transmissive, W.T,12:00 N→Transmissive, Super W.T, 6:00	Q→Transmissive, Super W.T, 12:00 R→Transmissive, Super W.T, O-TFT V→Transmissive, Super W.T, VA TFT W→Transmissive, Super W.T, IPS TFT X→Transmissive, W.T, VA TFT Y→Transmissive, W.T, IPS TFT Z→Transmissive, W.T, O-TFT
⑦	A：TFT LCD B：TFT+SCREW HOLES+CONTROL BOARD C：TFT+ SCREW HOLES +A/D BOARD D：TFT+ SCREW HOLES +A/D BOARD+CONTROL BOARD E：TFT+ SCREW HOLES +POWER BOARD		F：TFT+CONTROL BOARD G：TFT+ SCREW HOLES H：TFT+D/V BOARD I：TFT+ SCREW HOLES +D/V BOARD J：TFT+POWER BD

⑧ Resolution:

M	1024768	N	128128	P	1280800	Q	480800	R	640320	S	480128
T	800320	U	8001280	**V**	176220	W	1280398	X	1024250	Y	1920720
A5	19201080	A6	480480	A7	10801920	A8	135240	A9	480640	B2	122250
B3	340800	B4	2801424	B5	12001920	B6	4801280	B7	800800	B8	40160

⑨	D: Digital	L:LVDS	M:MIPI	E:eDP

⑩ Interface:

N	Without control board	A	8Bit	B	16Bit	E	eDP	H	HDMI
I	I2C Interface	R	RS232	S	SPI Interface	U	USB		

⑪ TS:

N	Without TS	T	Resistive touch panel	C	Capacitive touch panel (G-F-F)
G	Capacitive touch panel (G-G)	C1	Capacitive touch panel (G-F-F)+OCA		
C2	Capacitive touch panel (G-F-F)+OCR	G1	Capacitive touch panel (G-G)+OCA		
G2	Capacitive touch panel (G-G)+OCR	B	CTP+GG+USB		

⑫	Version:	X:Raspberry pi	V: Raspberry pi 3B+

⑬	Special Code	#:Fit in with ROHS directive regulations

2.Summary

TFT 6.75” is a color active matrix a-Si LCD Q-Panel, using a-Si (amorphous silicon) TFTs (Thin Film Transistors) as an active switching devices. The module has a 6.75 inch diagonally measured active area with 480×1280 resolutions (480 horizontal by 1280 vertical pixel array). Each pixel is divided into RED, GREEN, BLUE dots which are arranged in vertical stripe and this module can display 16.7M colors.

3.General Specifications

Item	Dimension	Unit
Size	6.75	inch
Dot Matrix	480 x 3(RGB) x 1280	dots
Module dimension	74.4 x 188.1 x 6.6	mm
Active area	60.19 x 160.512	mm
Pixel pitch	0.1254 x 0.1254	mm
LCD type	TFT, Normally Black ,Transmissive	
View Angle	85/85/85/85	
TFT Driver IC	FL7703NI-G5-DP or Equivalent	
TFT Interface	4-Lanes MIPI	
CTP IC	GT911 or Equivalent	
CTP Interface	I2C	
CTP FW Version	0x70	
CTP Resolution	480*1280	
Backlight Type	LED,Normally White	
With /Without TP	With CTP	
Surface	Glare	

*Color tone slight changed by temperature and driving voltage.

4.Absolute Maximum Ratings

Item	Symbol	Min	Typ	Max	Unit
Operating Temperature	TOP	-20	—	+70	℃
Storage Temperature	TST	-30	—	+80	℃

Note: Device is subject to be damaged permanently if stresses beyond those absolute maximum ratings listed above

1. Temp. 60℃, 90% RH MAX. Temp.＞60℃, Absolute humidity shall be less than 90% RH at 60℃

5.Electrical Characteristics

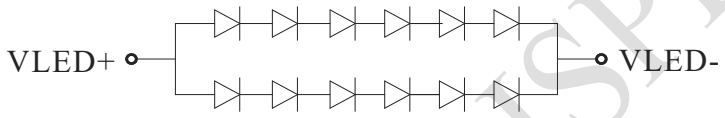
Operating conditions

Item	Symbol	Min	Typ	Max	Unit
Supply voltage for LCM	VCC	3.0	3.3	3.6	V
Supply LCM current	Icc	-	80	120	mA
Supply CTP	V_{CTP}	2.8	3.3	3.6	V
	I_{CTP}	-	13.0	20.0	mA

LED driving conditions

Parameter	Symbol	Min	Typ	Max	Unit	Remark
LED current	–	–	120	–	mA	–
LED voltage	VLED+	15.6	18.0	20.4	V	Note 1
LED Life Time	–	–	50,000	–	Hr	Note 2,3

Note 1 : There are 1 Groups LED
Note 2 : Ta = 25°C



Backlight LED Circuit

Note 2 : Ta = 25 ℃
Note 3 : Brightness to be decreased to 50% of the initial value
Note 4 : The single LED lamp case

6.DC Characteristics

6.1. DSI DC Characteristics

LP Mode

Parameter	Symbol	Conditions	Spec.			Unit
			Min.	Typ.	Max.	
Logic high level input voltage	V_{IHLPCD}	LP-CD	450	-	1350	mV
Logic low level input voltage	V_{ILLPCD}	LP-CD	0	-	200	mV
Logic high level input voltage	V_{IHLPRX}	LP-RX(CLK, D0)	880	-	1350	mV
Logic low level input voltage	V_{ILLPRX}	LP-RX(CLK, D0)	0	-	550	mV
Logic low level input voltage	$V_{ILLPRXULP}$	LP-RX(CLK ULP mode)	0	-	300	mV
Logic high level output voltage	V_{OHLPTX}	LP-TX(D0)	1.1	-	1.3	V
Logic low level output voltage	V_{OLLPTX}	LP-TX(D0)	-50	-	50	mV
Logic high level input current	V_{IH}	LP-CD, LP-RX	-	-	10	uA
Logic low level input current	V_{IL}	LP-CD, LP-RX	-10	-	-	uA
Input pulse rejection	SGD	DSI-CLK+/-, DSI-D0+/1	-	-	300	Vps

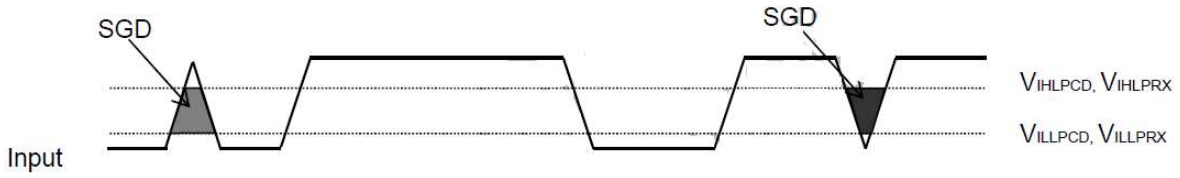


Figure 1: Input glitch rejections of low-power receivers

High Speed Mode

Parameter	Symbol	Conditions	Spec.			Unit
			Min.	Typ.	Max.	
Input common mode	V_{CMCLK} V_{CMDATA}	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	70	-	330	mV
Input common mode variation <450 MHZ	$V_{CMRCLKL}$ $V_{CMRDATAL}$	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-50	-	50	mV
Input common mode variation >450 MHZ	$V_{CMRCLKM}$ $V_{CMRDATAM}$	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-	-	100	mV
Low-level differential Input threshold	V_{THLCLK} $V_{THLDATA}$	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-70	-	-	mV
High-level differential Input threshold	V_{THHCLK} $V_{THHDATA}$	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-	-	70	mV
Single ended input low voltage	V_{ILHS}	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-40	-	-	mV
Single ended input high voltage	V_{IHHS}	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-	-	460	mV
Differential input termination resistor	R_{TERM}	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	80	100	125	Ω
Single-ended threshold voltage for termination enable	V_{TERMEN}	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-	-	450	mV
Termination capacitor	C_{TERM}	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-	-	-	pF

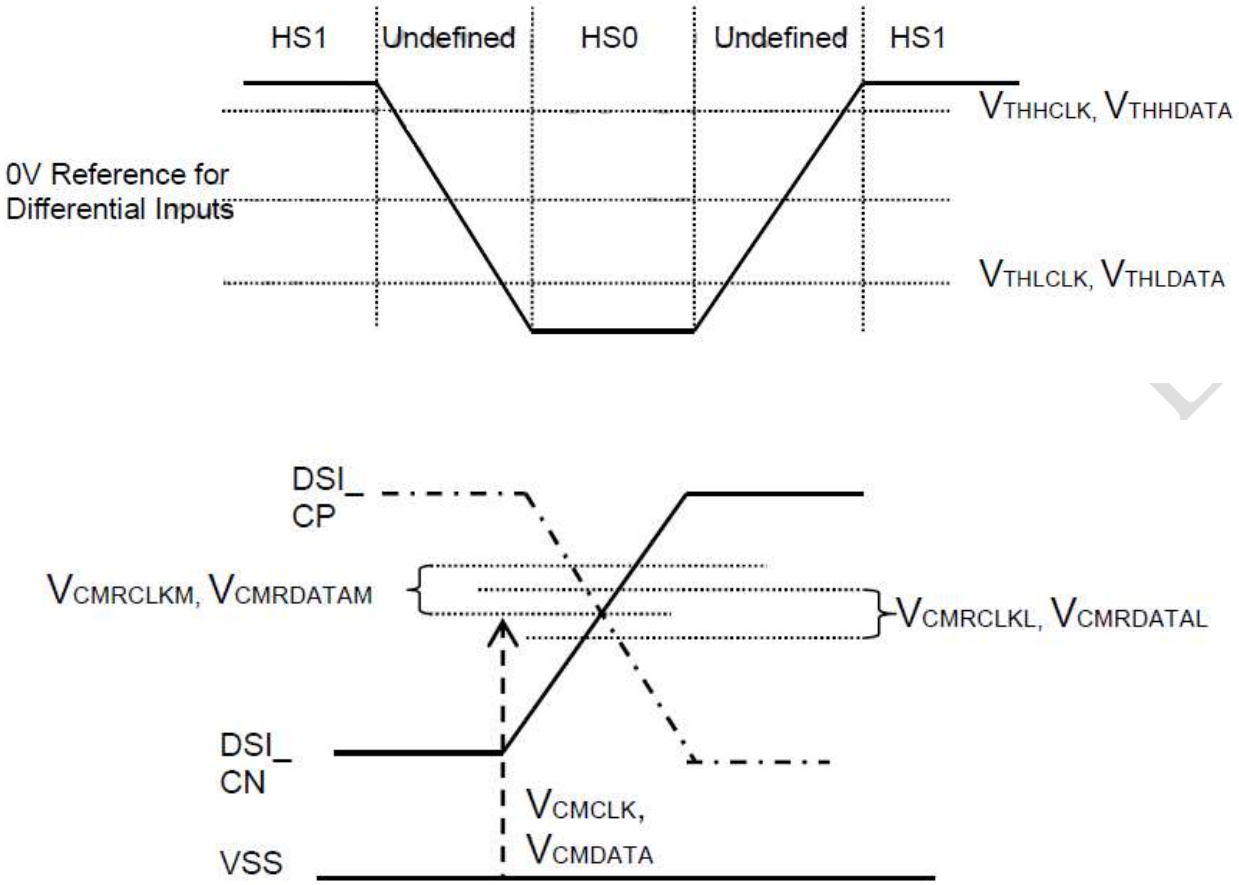


Figure 2: Differential voltage range and Command mode voltage

7.AC Characteristics

7.1. DSI Interface Timing Characteristics

High Speed Mode

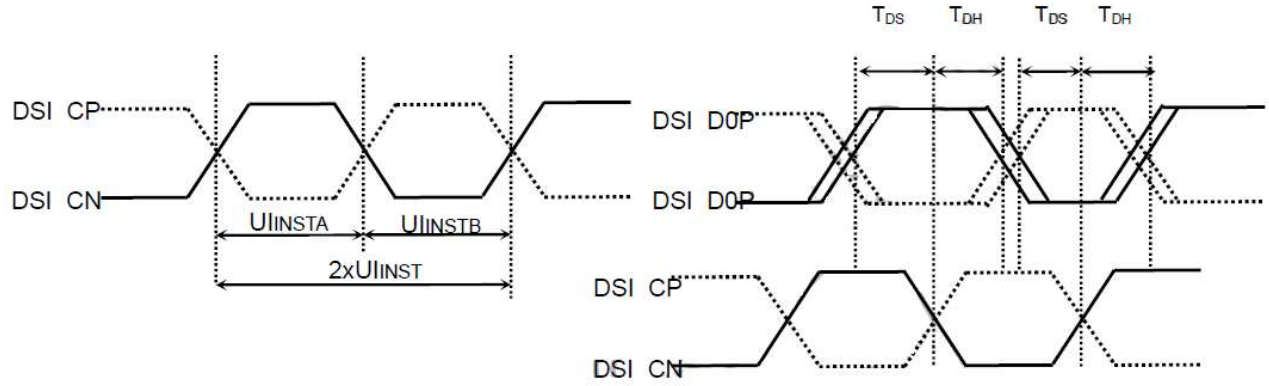


Figure 3: DSI clock timing Characteristics

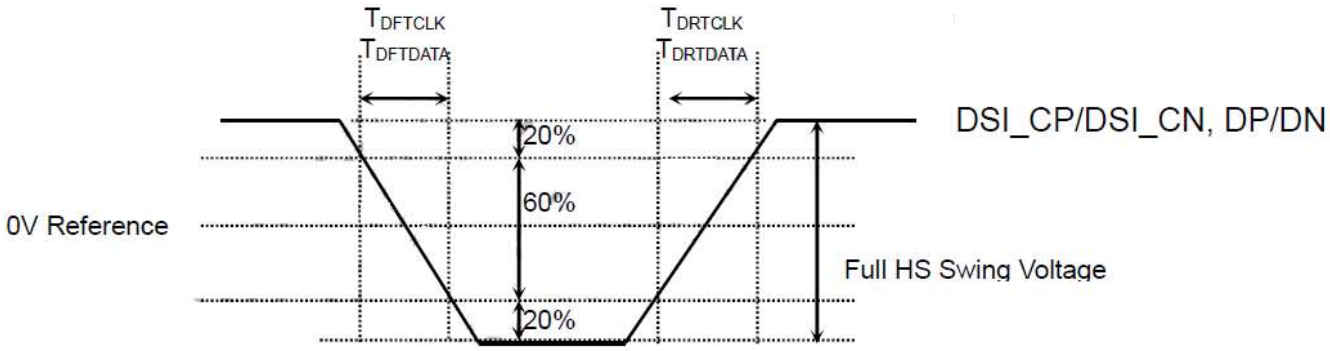


Figure 4: Rising and falling time on clock and data channel

Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_CP/ DSI_CN	Double UI instantaneous	2xUINST	4LANE：3.30	-	25	ns
	UI instantaneous	UINSTA UINSTB	4LANE：1.67	-	12.5	ns
DP/DN	Data to clock setup time	TDS	0.15xUI	-	-	ps
	Data to clock hold time	TDH	0.15xUI	-	-	ps
DSI_CP/ DSI_CN	Differential rise time for clock	TDRTCLK	150	-	0.3UI	ps
	Differential fall time for clock	TDFTCLK	150	-	0.3UI	ps
DP/DN	Differential rise time for data	TDRTDATA	150	-	0.3UI	ps
	Differential fall time for data	TDFTDATA	150	-	0.3UI	ps

Table 1: DSI High Speed Mode Characteristics

Low Power Mode

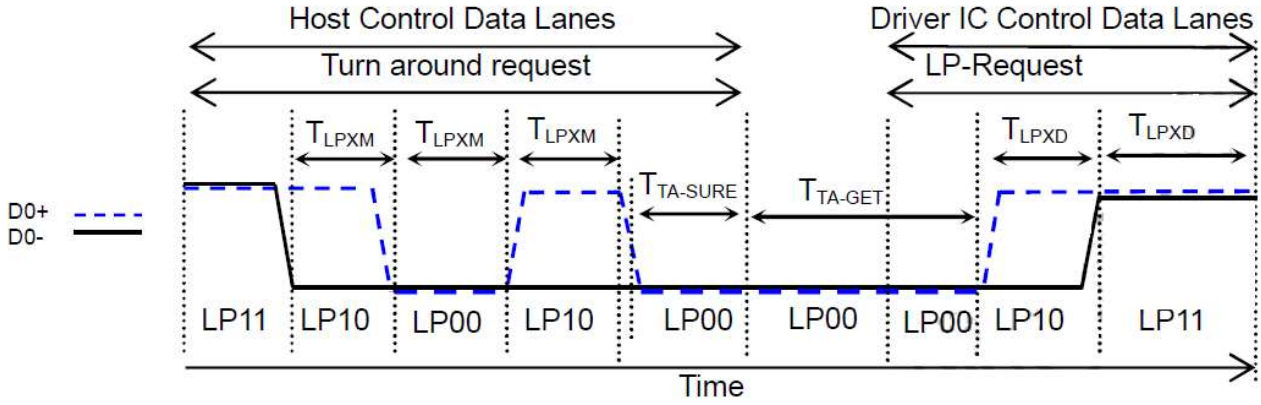


Figure 5: BTA from HOST to Display Module Timing

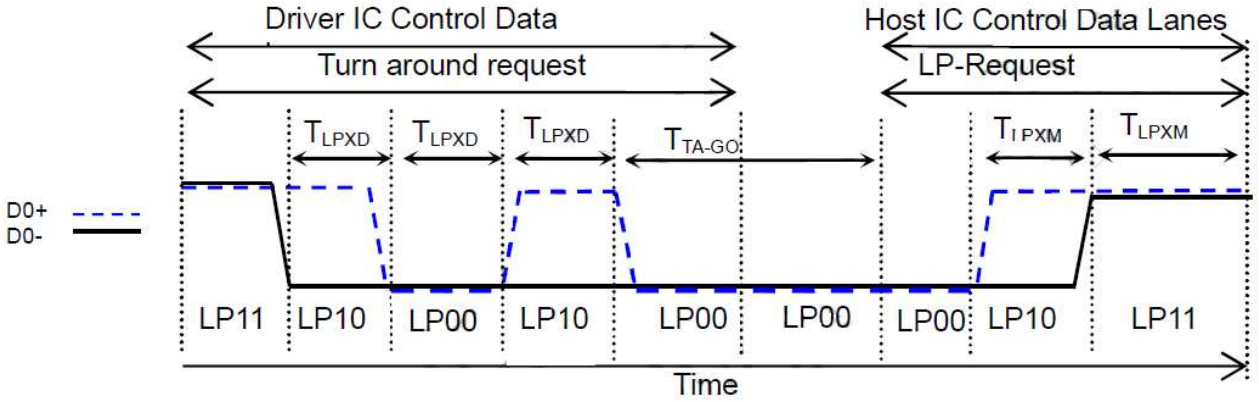
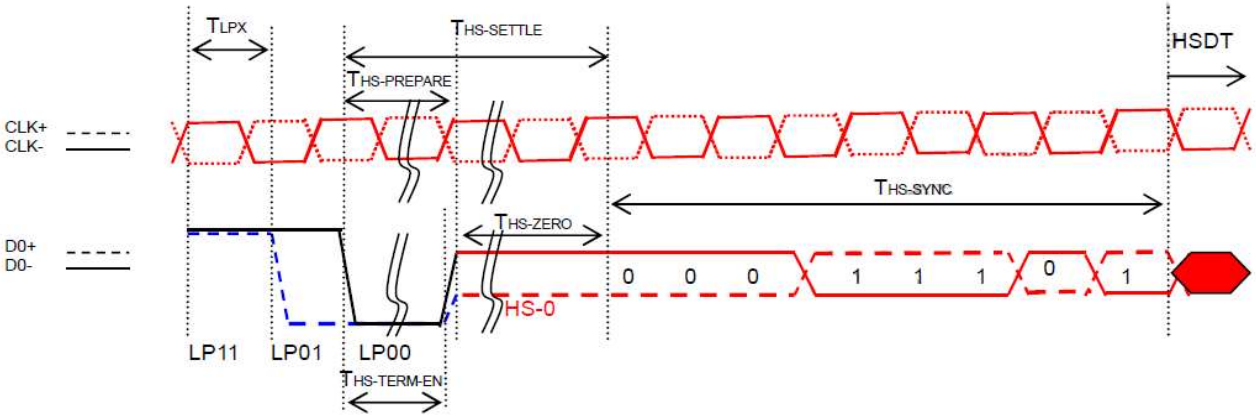


Figure 6: BTA from Display Module Timing to HOST

Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_D0P/ DSI_D0P	Length of LP-00/LP01/LP10/LP11 Host→ Display module	T_{LPXM}	50	-	-	ns
	Length of LP-00/LP01/LP10/LP11 Display module →Host	T_{LPXD}	50	-	-	ns
	Time-out before the MPU start driver	$T_{TA-SURE}$	T_{LPXD}	-	$2xT_{LPXD}$	ns
	Time to drive LP-00 by display module	T_{TA-GET}	$5xT_{LPXD}$	-	-	ns
	Time to drive LP-00 after turnaround request Host	T_{TAGO}	$4xT_{LPXD}$	-	-	ns

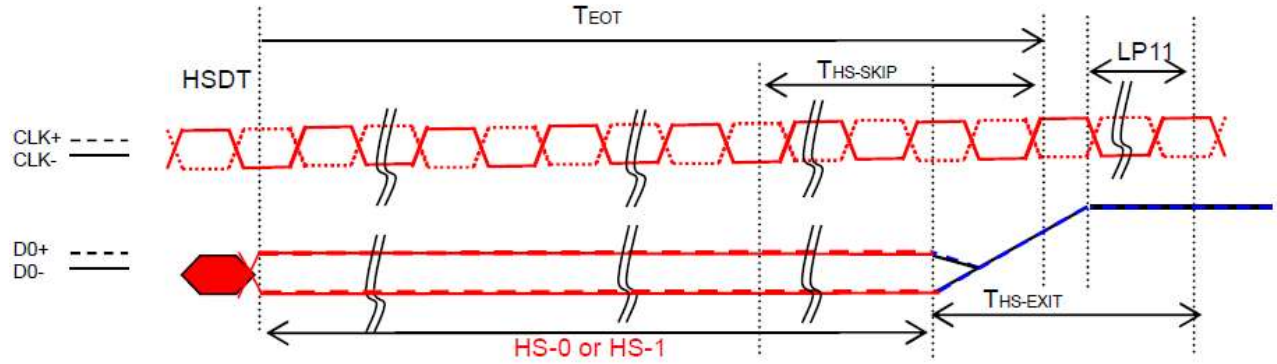
Table 2: DSI Low Power Mode Characteristics

DSI BURSTS



Signal	Item	Symbol	Spec.			
			Min.	Typ.	Max.	
DSI_D0P/ DSI_D0P	Length of LP-00/LP01/LP10/LP11	T_{LPX}	50	-	-	
	Time to Driver LP-00 to prepare for HS transmission	$T_{HS-PREPARE}$	40+4UI	-	85+6UI	
	Time to enable data receiver line termination	$T_{HS-TERM-EN}$	-	-	35+4xUI	
	Time to drive LP-00 by display module	T_{TA-GET}	5xT_{LPXD}	-	-	
	Time to drive LP-00 after turnaround request Host	T_{TAGO}	4xT_{LPXD}	-	-	

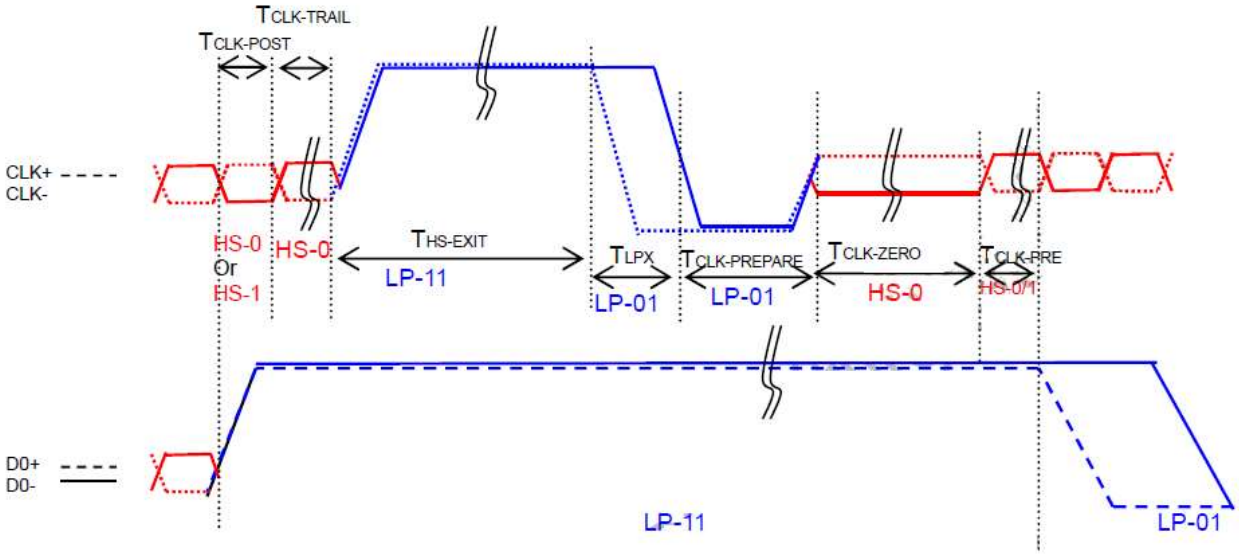
Table 3: DSI Low Power Mode to High Speed Mode Timing



NOTE:
If the last bit is HS-0, the transmitter changes from HS-0 to HS-1
If the last bit is HS-0, the transmitter changes from HS-1 to HS-0

Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_D0P/ DSI_D0P	Time-Out at Display Module to Ignore Transition Period of EoT	$T_{HS-SKIP}$	40	-	55+4xUI	ns
	Time to Driver LP-11 after HS Burst	$T_{HS-EXIT}$	100	-	-	ns

Table 4: DSI Low Power Mode to High Speed Mode Timing



Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_CP/ DSI_CN	Time that the MCU shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	$T_{CLK-POST}$	60+52xUI	-	-	ns
	Time to drive HS differential state after last payload clock bit of a HS transmission burst	$T_{CLK-TRAIL}$	60	-	-	ns
	Time to drive LP-11 after HS burst	$T_{HS-EXIT}$	100	-	-	ns
	Time to drive LP-00 to prepare for HS transmission	$T_{CLK-PREPARE}$	38	-	95	ns
	Time-out at Clock Lane Display Module to enable HS Termination	$T_{CLK-TERM-EN}$	-	-	38	ns
	Minimum lead HS-0 drive period before starting Clock	$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	300	-	-	ns
	Time that the HS clock shall be driven prior to any associated data Lane beginning the transition from LP to HS mode	$T_{CLK-PRE}$	8xUI			

Table 5: Clock Lanes High Speed Mode to/from Low Power Mode Timing

7.2. Reset input timing

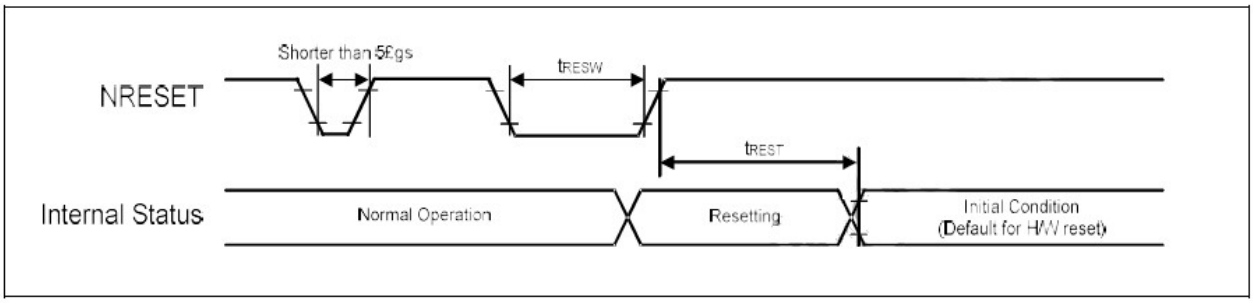


Figure 7: Reset input timing

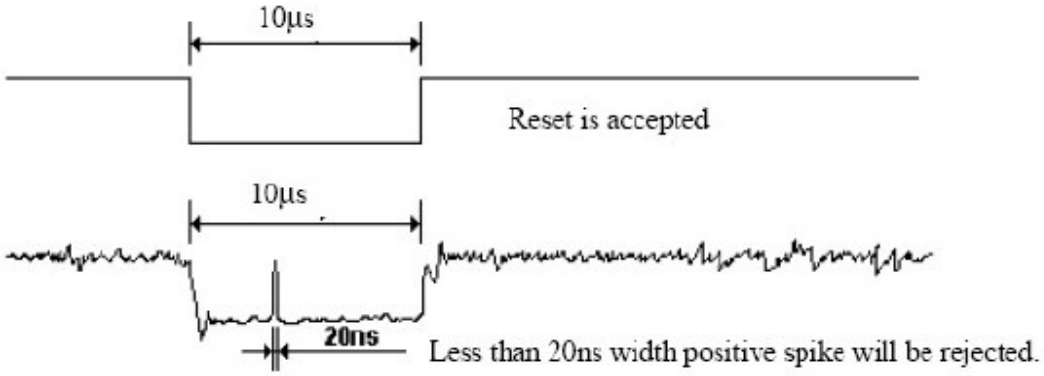
Symbol	Parameter	Related Pins	Spec.			Note	Unit
			Min.	Typ.	Max.		
tRESW	Reset low pulse width(1)	NRESET	10	-	-	-	µs
tREST	Reset complete time(2)	-	15	-	-	When reset applied during SLPIN mode	ms
		-	120	-	-	When reset applied during SLPOUT mode	ms

Table 6: Reset Input Timing

Note: (1) Spike due to an electrostatic discharge on NRESET line does not cause irregular system reset according to the following table.

NRESET Pulse	Action
Shorter than 5 µs	Reset Rejected
Longer than 10 µs	Reset
Between 5 µs and 10 µs	Reset Start

(2) During the resetting period, the display will be blanked (The display is entering blanking sequence, which Maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then return to Default condition for H/W reset.
(3) During Reset Complete Time, ID and VCOM value in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 15ms after a rising edge of NRESET.
(4) Spike Rejection also applies during a valid reset pulse as shown as below:



(5) It is necessary to wait 15msec after releasing NRESET before sending commands. Also Sleep Out command cannot be sent for 120msec.

7.3. Tearing Effect (TEE)

The driver IC can inform to the HOST when a tearing effect event (New V-synch) has been happen on the driver IC by Tearing Effect (TEE). The Tearing Effect (TEE) is using a following sequence:

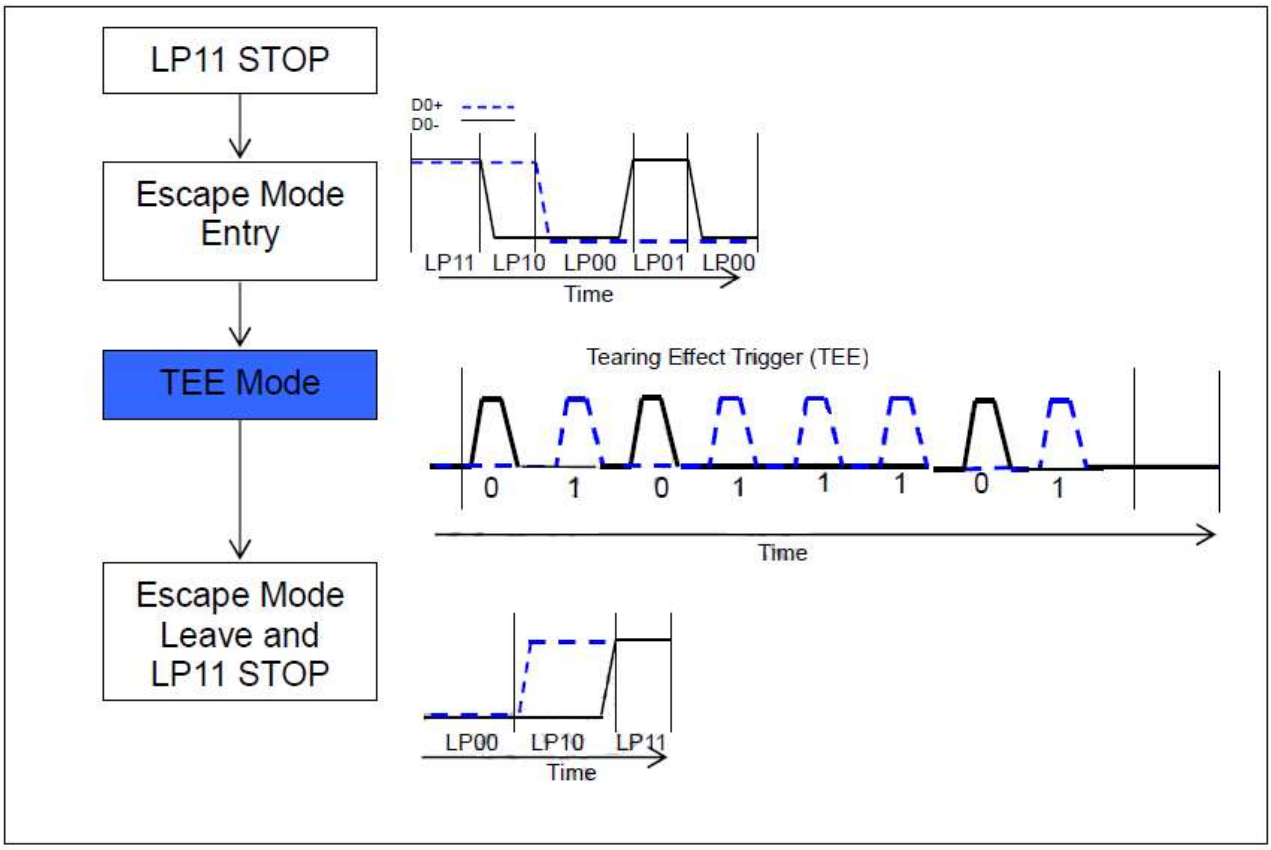


Figure 8: DSI Data Lane D0 TEE sequence

7.4. MIPI Timing Table

Parameter	Symbol	Min.	Typ.	Max.	Unit
PCLK	fPcLk	50	66	72	MHZ
H Total Time	THP	672	840	880	Clocks
H Active Time	HACT	600	600	600	Clocks
H Front Porch	THFP	32	100	120	Clocks
HSync Pulse Width	HSPW	8	50	60	Clocks
H Back Porch	THBP	32	90	100	Clocks
HS+HFP+HBP	-	72	240	280	Clocks
V Total Time	TVP	1290	1314	1326	Lines
V Active Time	VACT	1280	1280	1280	Lines
V Front Porch	TVFP	4	16	20	Lines
VSync Pulse Width	VSPW	2	4	4	Lines
V Back Porch	TVBP	4	14	22	Lines
VS+VFP+VBP	-	10	34	46	Lines
V Frequency	Fps	58	60	62	Hz
MIPI lane number		4	4	4	
Bit rate	BRbps	302	397	434	Mbps/lane

8.Power on/off Sequence

Power source VCC can be applied and powered down in any order. VCC can be powered down in any order.
During power off, if LCD is in the Sleep Out mode, VCC must be powered down minimum 120msec after NRESET has been released.
During power off, if LCD is in the Sleep In mode, VCC can be powered down minimum 0msec after NRESET has been released.
NCS can be applied at any timing or can be permanently grounded. NRESET has priority over NCS.

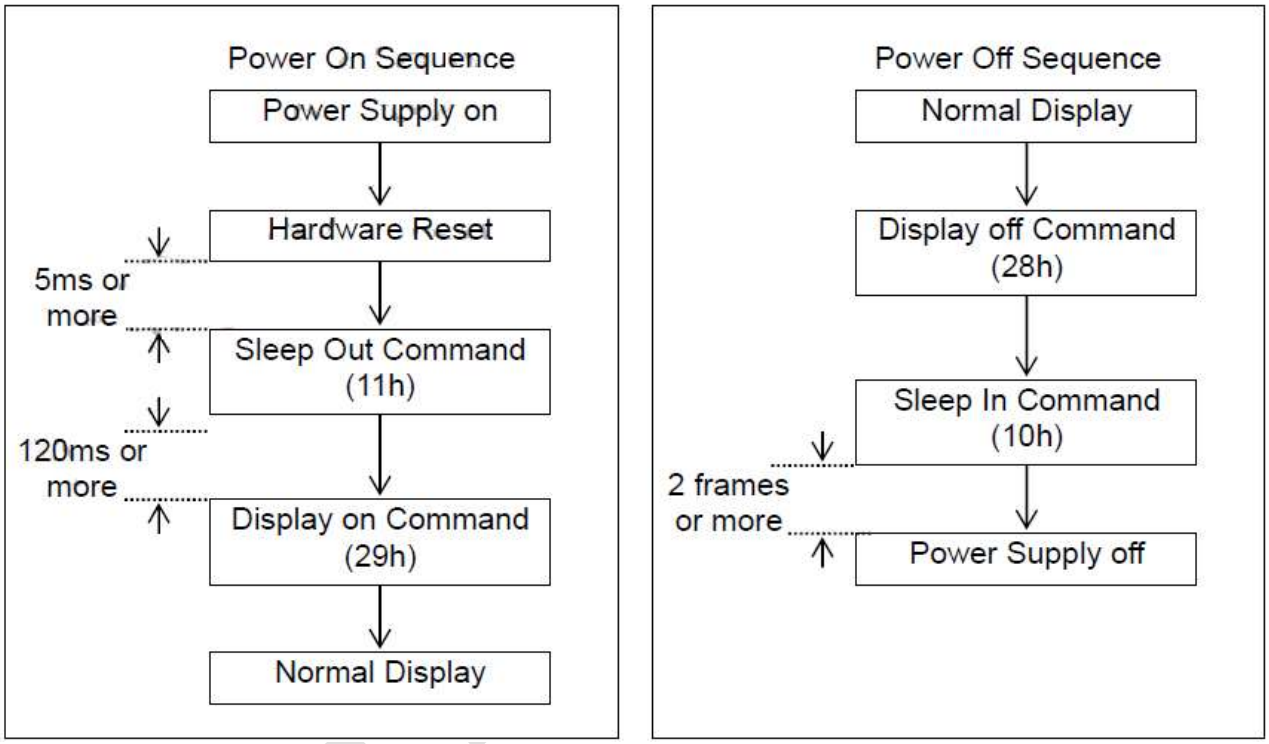


Figure 9 The power supply ON/OFF setting for Display ON/OFF and Sleep In/out

9.Optical Characteristics

Item		Symbol	Condition.	Min	Typ.	Max.	Unit	Remark
Response time		Tr	θ=0°、Φ=0°	-	16	21	.ms	Note 3
		Tf		-	14	19	.ms	
Contrast ratio		CR	At optimized viewing angle	1000	1500	-	-	Note 4
Color Chromaticity	White	Wx	θ=0°、Φ=0	0.243	0.293	0.343	-	Note 2,6,7
		Wy		0.272	0.322	0.372	-	
Viewing angle	Hor.	ΘR	CR≧10	75	85	-	Deg.	Note 1
		ΘL		75	85	-		
	Ver.	ΦT		75	85	-		
		ΦB		75	85	-		
Brightness		-	-	300	400	-	cd/m2	Center of display
Uniformity		(U)	-	75	-	-	%	Note 5

Ta=25±2℃

Note 1: Definition of viewing angle range

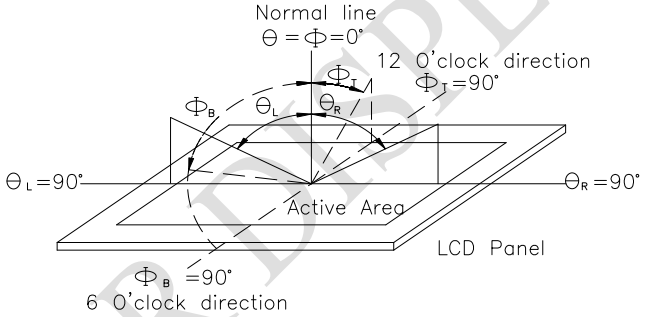


Fig 9.1. Definition of viewing angle

Note 2: Test equipment setup:

After stabilizing and leaving the panel alone at a driven temperature for 10 minutes, the measurement should be executed. Measurement should be executed in a stable, windless, and dark room. Optical specifications are measured by Topcon BM-7orBM-5 luminance meter 1.0° field of view at a distance of 50cm and normal direction.

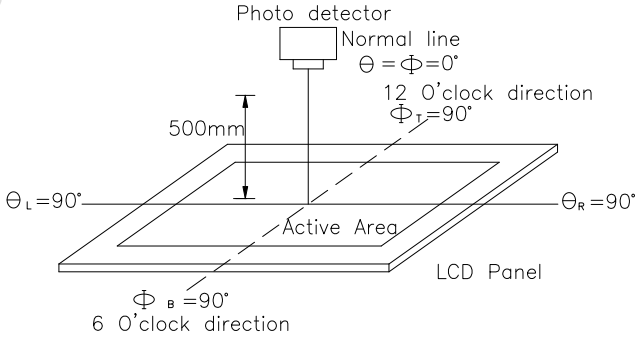
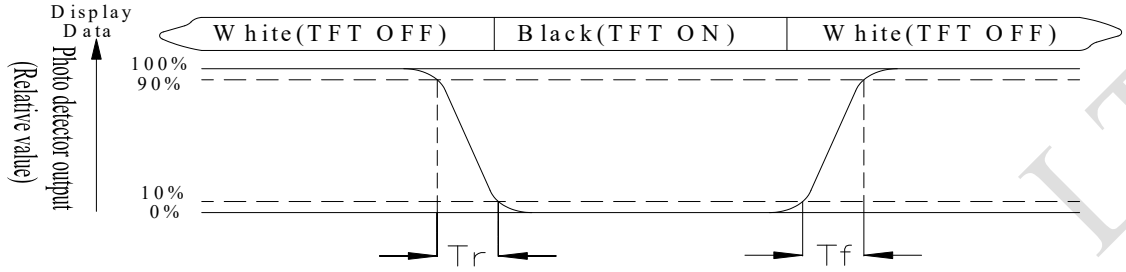


Fig9.2. Optical measurement system setup

Note 3: Definition of Response time:
The response time is defined as the LCD optical switching time interval between “White” state and “Black” state. Rise time, Tr, is the time between photo detector output intensity changed from 90%to 10%. And fall time, Tf, is the time between photo detector output intensity changed from 10%to 90%



Note 4: Definition of contrast ratio:
The contrast ratio is defined as the following expression.

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD on the "White" state}}{\text{Luminance measured when LCD on the "Black" state}}$$

Note 5: Definition of Luminance Uniformity
Active area is divided into 9 measuring areas (reference the picture in below). Every measuring point is placed at the center of each measuring area.
Luminance Uniformity (U) = Lmin/Lmax x100%
L = Active area length
W = Active area width

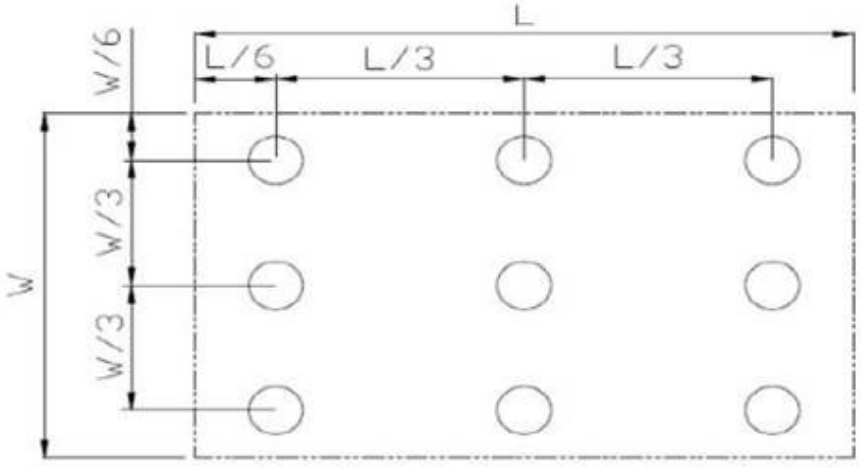


Fig 9.3. Definition of uniformity

Note 6: Definition of color chromaticity (CIE 1931)
Color coordinates measured at the center point of LCD

Note 7: Measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.

10.Interface

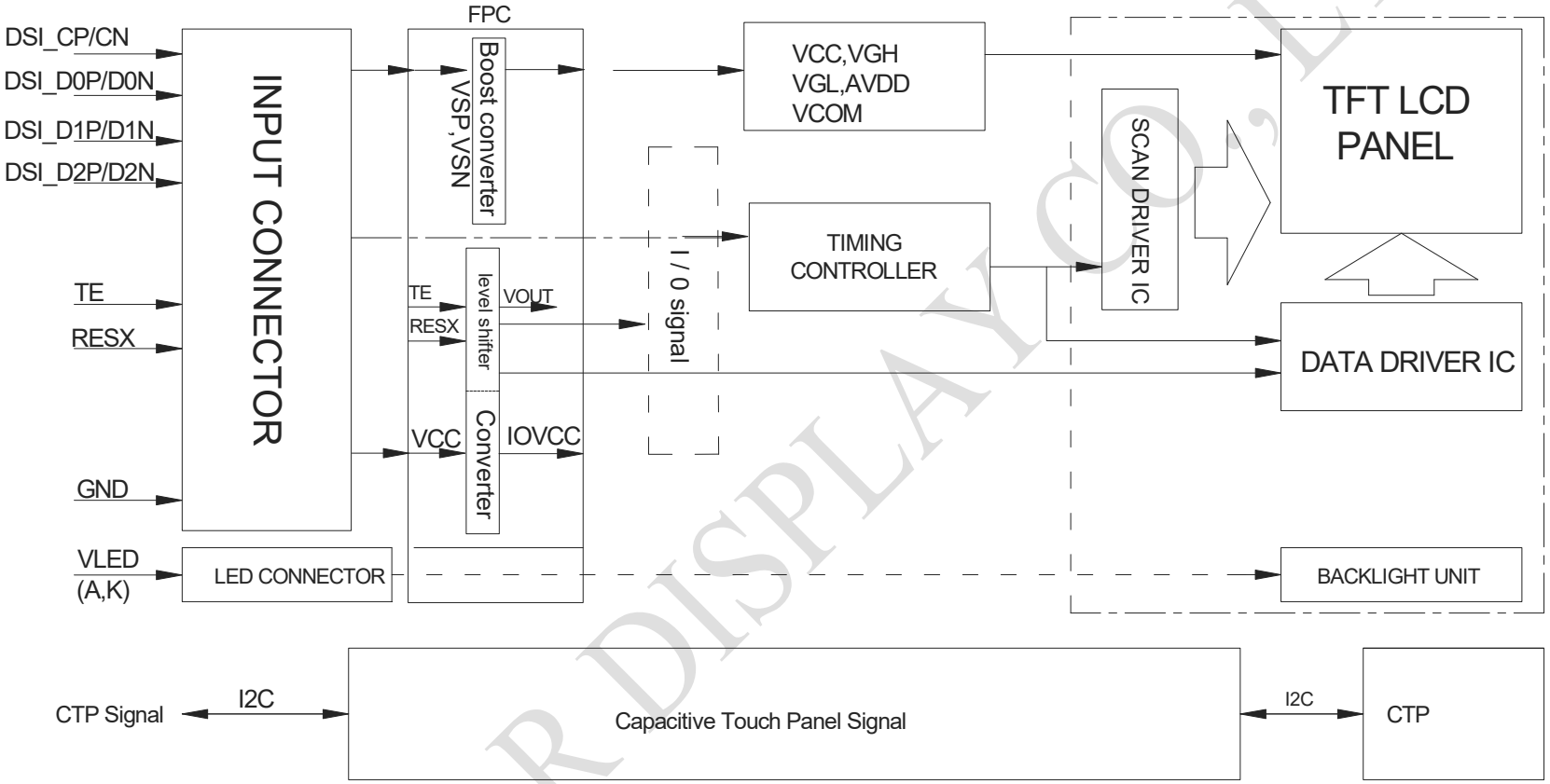
10.1. LCM PIN Definition

Pin No.	Symbol	Pin Description
1	GND	Ground
2	D3N	High speed interface data differential signal input pins.
3	D3P	
4	GND	Ground
5	D2N	High speed interface data differential signal input pins.
6	D2P	
7	GND	Ground
8	CLKN	High speed interface clock differential signal input pins. OPEN
9	CLKP	
10	GND	Ground
11	D1N	High speed interface data differential signal input pins.
12	D1P	
13	GND	Ground
14	D0N	High speed interface data differential signal input/output pins.
15	D0P	
16	GND	Ground
17	GND	Ground
18	TE	Serve as a TE (Tearing Effect) output signal Leave the pin open when not in use.
19	RESET	Reset pin. This signal will reset the device and must be applied to properly initialize the chip.
20	GND	Ground
21-23	VCC	Power supply
24	GND	Ground
25-28	NC	No connection
29	VLED-	Power for LED backlight cathode
30	VLED+	Power for LED backlight anode

10.2. CTP PIN Definition

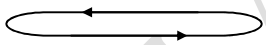
Pin	Symbol	Function	Remark
1	VSS	Ground for analog circuit	
2	VDDT	Power Supply : +3.3V	
3	SCL	I2C clock input	
4	NC	No connection	
5	SDA	I2C data input and output	
6	NC	No connection	
7	/RST	External Reset, Low is active	
8	NC	No connection	
9	/INT	External interrupt to the host	
10	VSS	Ground for analog circuit	

11.Block Diagram



12.Reliability

Content of Reliability Test (Wide temperature, -20℃~70℃)

Environmental Test			
Test Item	**Content of Test**	**Test Condition**	**Note**
High Temperature storage	Endurance test applying the high storage temperature for a long time.	80℃ 200hrs	2
Low Temperature storage	Endurance test applying the low storage temperature for a long time.	-30℃ 200hrs	1,2
High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	70℃ 200hrs	——
Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	-20℃ 200hrs	1
High Temperature/ Humidity Operation	The module should be allowed to stand at 60℃,90%RH max	60℃,90%RH 96hrs	1,2
Thermal shock resistance	The sample should be allowed stand the following 10 cycles of operation -20℃ 25℃ 70℃  30min 5min 30min 1 cycle	-20℃/70℃ 10 cycles	——
Vibration test	Endurance test applying the vibration during transportation and using.	Total fixed amplitude : 1.5mm Vibration Frequency : 10~55Hz One cycle 60 seconds to 3 directions of X,Y,Z for Each 15 minutes	3
Static electricity test	Endurance test applying the electric stress to the terminal.	VS=±600V(contact), ±800v(air), RS=330Ω CS=150pF 10 times	——

Note1: No dew condensation to be observed.

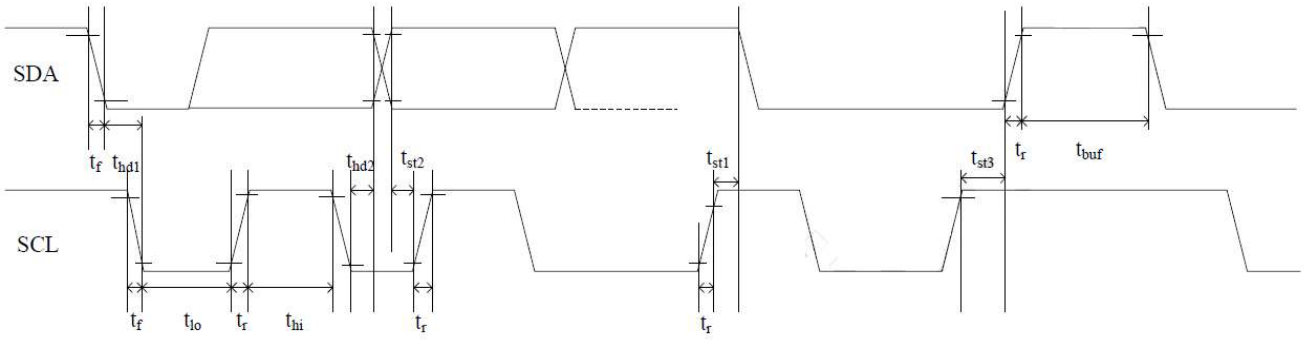
Note2: The function test shall be conducted after 4 hours storage at the normal Temperature and humidity after remove from the test chamber.

Note3: The packing have to including into the vibration testing.

13.Touch Panel Information

I²C Timing

The provides a standard I²C interface for SCL and SDA to communicate with host.
The always serves as slave device in the system with all communication being initialized by the host. It is strongly recommended that transmission rate be kept at or below 400Kbps.
The I²C timing is shown below:

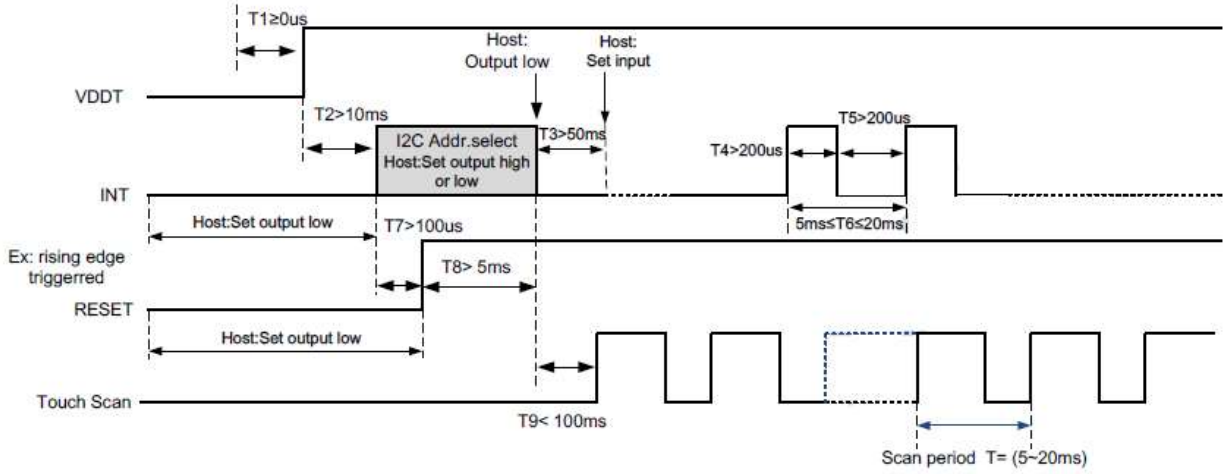


Test condition: 3.3V host interface voltage, 400Kbps transmission rate, 2KΩpull-up resistor

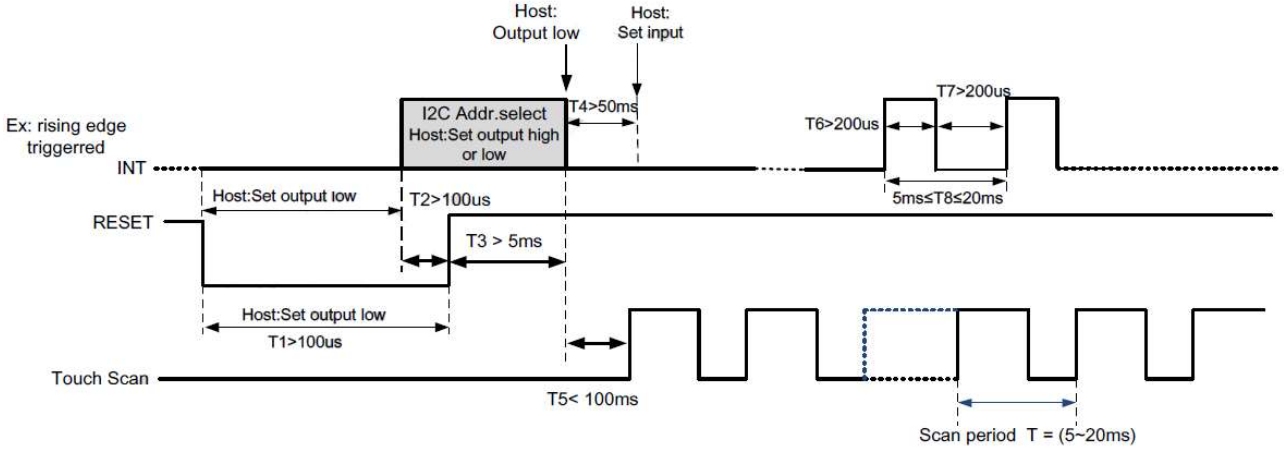
Parameter	Symbol	Min.	Max.	Unit
SCL low period	t_{lo}	1.3	-	us
SCL high period	t_{hi}	0.6	-	us
SCL setup time for Start condition	t_{st1}	0.6	-	us
SCL setup time for Stop condition	t_{st3}	0.6	-	us
SCL hold time for Start condition	t_{hd1}	0.6	-	us
SDA setup time	t_{st2}	0.1	-	us
SDA hold time	t_{hd2}	0	-	us

Supports I²C slave addresses:0x28/0x29. The host can select the addresses by changing the status of Reset and INT pins during the power-on initialization phase. See the diagram below for configuration methods and timing:

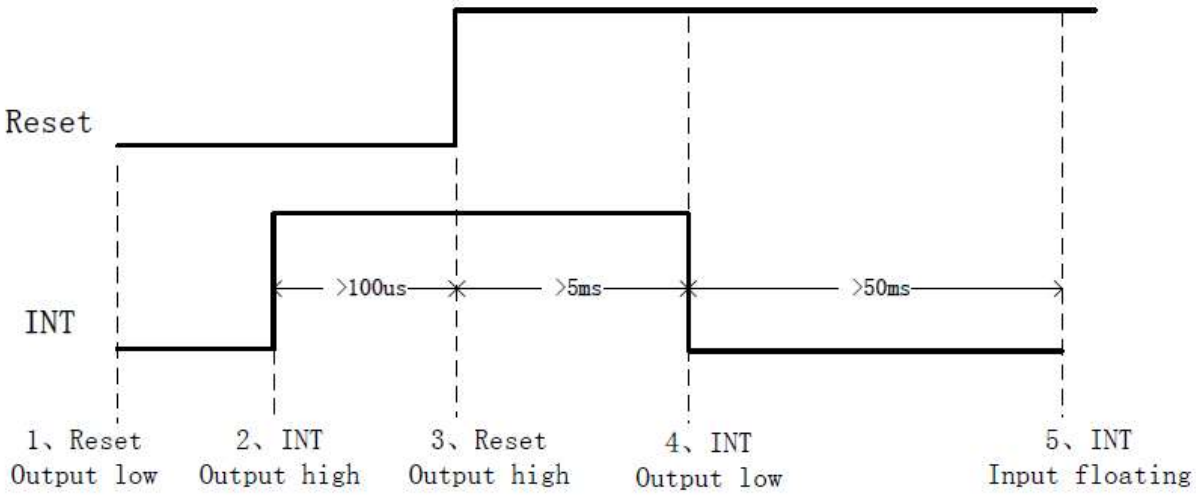
Power-on Timing:



Timing for host resetting:



Timing for setting slave address to 0x28/0x29:



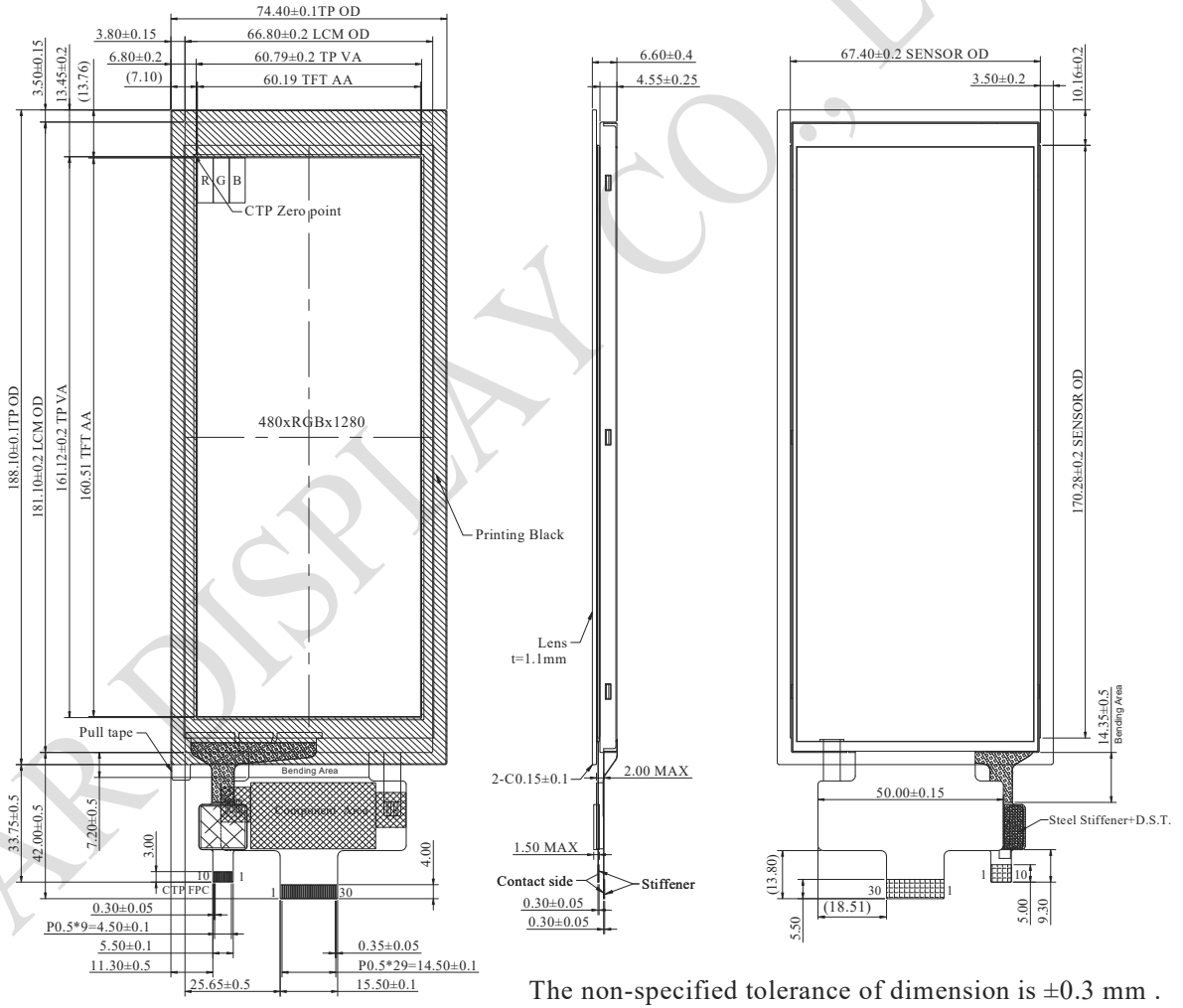
14.Contour Drawing

TFT FPC

PIN No.	SYMBOL	PIN No.	SYMBOL
1	GND	16	GND
2	D3N	17	GND
3	D3P	18	TE
4	GND	19	RESET
5	D2N	20	GND
6	D2P	21	VCC
7	GND	22	VCC
8	CLKN	23	VCC
9	CLKP	24	GND
10	GND	25	NC
11	D1N	26	NC
12	D1P	27	NC
13	GND	28	NC
14	D0N	29	VLED-
15	D0P	30	VLED+

CTP FPC

PIN No.	SYMBOL
1	VSS
2	VDDT
3	SCL
4	NC
5	SDA
6	NC
7	/RST
8	NC
9	/INT
10	VSS



The non-specified tolerance of dimension is ±0.3 mm .

15.Initial Code For Reference

```
#define Width 600
#define Height 1280


#define VFP 16
#define VBP 16
#define VSA 4


#define HFP 110
#define HBP 110
#define HSA 92

============================

DSI_CMD(0x04,0xB9);
DSI_PA(0xF1);     //1
DSI_PA(0x12);     //2
DSI_PA(0x87);     //3

DSI_CMD(0x04,0xB2);
DSI_PA(0x40);     //1
DSI_PA(0x05);     //2
DSI_PA(0x78);     //3

DSI_CMD(0x0B,0xB3); /// SET RGB
DSI_PA(0x10);     //1 VBP_RGB_GEN
DSI_PA(0x10);     //2 VFP_RGB_GEN
DSI_PA(0x28);     //3 DE_BP_RGB_GEN
DSI_PA(0x28);     //4 DE_FP_RGB_GEN
DSI_PA(0x03);     //5
DSI_PA(0xFF);     //6
DSI_PA(0x00);     //7
DSI_PA(0x00);     //8
DSI_PA(0x00);     //9
DSI_PA(0x00);     //10

DSI_CMD(0x02,0xB4); /// Set Panel Inversion
DSI_PA(0x80);     //1

DSI_CMD(0x03,0xB5); /// Set BGP
DSI_PA(0x0A);     //1 vref
DSI_PA(0x0A);     //2 nvref

DSI_CMD(0x03,0xB6); /// Set VCOM
DSI_PA(0x91);     //1 F_VCOM
DSI_PA(0x91);     //2 B_VCOM
```

```
DSI_CMD(0x05,0xB8); ///Set ECP
DSI_PA(0x26);
DSI_PA(0x22);
DSI_PA(0xF0);
DSI_PA(0x13);


DSI_CMD(0x1C,0xBA); /// Set DSI
DSI_PA(0x33);     //1    // 33 4 lane 32 3 lane
DSI_PA(0x81);     //2
DSI_PA(0x05);     //3
DSI_PA(0xF9);     //4
DSI_PA(0x0E);     //5
DSI_PA(0x0E);     //6
DSI_PA(0x20);     //7
DSI_PA(0x00);     //8
DSI_PA(0x00);     //9
DSI_PA(0x00);     //10
DSI_PA(0x00);     //11
DSI_PA(0x00);     //12
DSI_PA(0x00);     //13
DSI_PA(0x00);     //14
DSI_PA(0x44);     //15
DSI_PA(0x25);     //16
DSI_PA(0x00);     //17
DSI_PA(0x91);     //18 0x90->0x91 for ESD
DSI_PA(0x0A);     //19
DSI_PA(0x00);     //20
DSI_PA(0x00);     //21
DSI_PA(0x01);     //22
DSI_PA(0x4F);     //23
DSI_PA(0x01);     //24
DSI_PA(0x00);     //25
DSI_PA(0x00);     //26
DSI_PA(0x37);     //27

DSI_CMD(0x02,0xBC); /// Set VDC
DSI_PA(0x47);     //1

DSI_CMD(0x06,0xBF); ///Set PCR
DSI_PA(0x02);
DSI_PA(0x10);
DSI_PA(0x00);
DSI_PA(0x80);
DSI_PA(0x04);

DSI_CMD(0x0A,0xC0); /// Set SCR
DSI_PA(0x73);     //1
DSI_PA(0x73);     //2
```

```
DSI_PA(0x50);     //3
DSI_PA(0x50);     //4
DSI_PA(0x00);     //5
DSI_PA(0x00);     //6
DSI_PA(0x12);     //7
DSI_PA(0x73);     //8    D1:D0?????????????0
DSI_PA(0x00);    //9

DSI_CMD(0x12,0xC1); /// Set POWER VGH VGL????????
DSI_PA(0x57);     //1 VBTHS VBTLS
DSI_PA(0x00);     //2 E3
DSI_PA(0x32);     //3 VSPR
DSI_PA(0x32);     //4 VSNR
DSI_PA(0x77);     //5 VSP VSN
DSI_PA(0xF4);     //6 APS
DSI_PA(0x77);
DSI_PA(0x77);
DSI_PA(0xCC);
DSI_PA(0xCC);
DSI_PA(0xFF);
DSI_PA(0xFF);
DSI_PA(0x11);
DSI_PA(0x11);
DSI_PA(0x00);
DSI_PA(0x00);
DSI_PA(0x32);

DSI_CMD(0x0D,0xC7); //
DSI_PA(0x10);     //1     enable VOUT output
DSI_PA(0x00);     //2
DSI_PA(0x0A);     //3
DSI_PA(0x00);     //4
DSI_PA(0x00);     //5
DSI_PA(0x00);     //6     setting VOUT at 3.3V
DSI_PA(0x00);     //7     HOUT SEL    D6:D5       VOUT SEL D1:D0
DSI_PA(0x00);     //8        PWM SEL D1:D0
DSI_PA(0xED);     //9              D7:MIPI ERR DIS TE/    D6:VGL DET DIS TE/    D5:VGH DET
DIS TE/   D4:DBV ZERO DIS TE/    D3:LVPUR DIS TE/    D2:TE ONLY AT NORMAL/
D1:CRC MATC/    D0:REF_CRC DIS TE
DSI_PA(0xC5);     //10
DSI_PA(0x00);     //11
DSI_PA(0xA5);     //12

DSI_CMD(0x05,0xC8); //
DSI_PA(0x10);     //1     enable VOUT output
DSI_PA(0x40);     //2
DSI_PA(0x1E);     //3
DSI_PA(0x03);     //4

DSI_CMD(0x02,0xCC); /// Set Panel
```

```
DSI_PA(0x0B);     //1 Forward:0x0B , Backward:0x07

DSI_CMD(0x23,0xE0); /// Set Gamma2.2
DSI_PA(0x00);    //1
DSI_PA(0x01);    //2
DSI_PA(0x01);    //3
DSI_PA(0x1E);    //4
DSI_PA(0x38);    //5
DSI_PA(0x3F);    //6
DSI_PA(0x27);    //7
DSI_PA(0x1F);    //8
DSI_PA(0x04);    //9
DSI_PA(0x08);    //10
DSI_PA(0x0C);    //11
DSI_PA(0x0E);    //12
DSI_PA(0x11);    //13
DSI_PA(0x0E);    //14
DSI_PA(0x10);    //15
DSI_PA(0x11);    //16
DSI_PA(0x19);    //17
DSI_PA(0x00);    //1
DSI_PA(0x01);    //2
DSI_PA(0x01);    //3
DSI_PA(0x1E);    //4
DSI_PA(0x38);    //5
DSI_PA(0x3F);    //6
DSI_PA(0x27);    //7
DSI_PA(0x1F);    //8
DSI_PA(0x04);    //9
DSI_PA(0x08);    //10
DSI_PA(0x0C);    //11
DSI_PA(0x0E);    //12
DSI_PA(0x11);    //13
DSI_PA(0x0E);    //14
DSI_PA(0x10);    //15
DSI_PA(0x11);    //16
DSI_PA(0x19);    //17

DSI_CMD(0x08,0xE1);
DSI_PA(0x11);     //1
DSI_PA(0x11);     //2
DSI_PA(0x91);     //3
DSI_PA(0x00);     //4 D7:D5:VGH DET SEL/    D4:D0:VGL DET SEL
DSI_PA(0x00);     //5 D5:D0:VSN DET SE
DSI_PA(0x00);     //6 D5:D0:VSP DET SE
DSI_PA(0x00);     //7 D7:PUREN_IOVCC/    D6:D4:IOVCC PUR_SEL/    D3:D2:DCHG1/
D1:D0:DCHG2

DSI_CMD(0x0F,0xE3); /// Set EQ
DSI_PA(0x07);     //1
```

```
DSI_PA(0x07);     //2
DSI_PA(0x0B);     //3
DSI_PA(0x0B);     //4
DSI_PA(0x0B);     //5
DSI_PA(0x0B);     //6
DSI_PA(0x00);     //7   PEQVCI1
DSI_PA(0x00);     //8   NEQVCI1
DSI_PA(0x00);     //9   VCOM_PULLGND_OFF
DSI_PA(0x00);     //10 VCOM_PULLGND_OFF
DSI_PA(0xFF);     //11 VCOM_IDLE_ON
DSI_PA(0x04);     //12
DSI_PA(0xC0);     //13 defaut C0 ESD detect function
DSI_PA(0x10);     //14 SLPOTP

DSI_CMD(0x40,0xE9); /// Set GIP
DSI_PA(0xC8);   //1   PANSEL          //04,C4
DSI_PA(0x10);   //2   SHR_0[11:8] //00,10
DSI_PA(0x07);   //3   SHR_0[7:0]    //04,0F
DSI_PA(0x00);   //4   SHR_1[11:8]
DSI_PA(0x00);   //5   SHR_1[7:0]
DSI_PA(0x80);   //6   SPON[7:0]     B2
DSI_PA(0x81);   //7   SPOFF[7:0]    B8
DSI_PA(0x12);   //8   SHR0_1[3:0], SHR0_2[3:0]
DSI_PA(0x31);   //9   SHR0_3[3:0], SHR1_1[3:0]
DSI_PA(0x23);   //10   SHR1_2[3:0], SHR1_3[3:0]
DSI_PA(0x4F);   //11   SHP[3:0], SCP[3:0]   48
DSI_PA(0x86);   //12   CHR[7:0]    //08,8B
DSI_PA(0x80);   //13   CON[7:0]
DSI_PA(0x28);   //14   COFF[7:0]
DSI_PA(0x47);   //15   CHP[3:0], CCP[3:0]
DSI_PA(0x08);   //16   USER_GIP_GATE[7:0]
DSI_PA(0x00);   //17   CGTS_L[21:16]
DSI_PA(0x00);   //18   CGTS_L[15:8]
DSI_PA(0x04);   //19   CGTS_L[7:0]
DSI_PA(0x00);   //20   CGTS_INV_L[21:16]
DSI_PA(0x00);   //21   CGTS_INV_L[15:8]
DSI_PA(0x00);   //22   CGTS_INV_L[7:0]
DSI_PA(0x00);   //23   CGTS_R[21:16]
DSI_PA(0x00);   //24   CGTS_R[15:8]
DSI_PA(0x04);   //25   CGTS_R[7:0]
DSI_PA(0x00);   //26   CGTS_INV_R[21:16]
DSI_PA(0x00);   //27   CGTS_INV_R[15:8]
DSI_PA(0x00);   //28   CGTS_INV_R[7:0]
DSI_PA(0x98);   //29   COS1_L[3:0] ,COS2_L[3:0] ,//     STV0 VSD
DSI_PA(0x18);   //30   COS3_L[3:0] ,COS4_L[3:0] ,//     STV2 VGL
DSI_PA(0xFA);   //31    COS5_L[3:0] ,COS6_L[3:0] ,//     VDS    VDDE
DSI_PA(0xB3);   //32    COS7_L[3:0] ,COS8_L[3:0] ,//     VDDO CLK8
DSI_PA(0x17);   //33   COS9_L[3:0] ,COS10_L[3:0],//     CLK6 CLK4
DSI_PA(0x58);   //34   COS11_L[3:0],COS12_L[3:0],//     CLK2
DSI_PA(0x88);   //35   COS13_L[3:0],COS14_L[3:0],//
```

```
DSI_PA(0x88);   //36   COS15_L[3:0],COS16_L[3:0],//
DSI_PA(0x88);   //37   COS17_L[3:0],COS18_L[3:0],//
DSI_PA(0x88);   //38   COS19_L[3:0],COS20_L[3:0],//
DSI_PA(0x88);   //39   COS21_L[3:0],COS22_L[3:0],//
DSI_PA(0x98);   //40   COS1_R[3:0] ,COS2_R[3:0] ,//     STV0 VSD
DSI_PA(0x08);   //41   COS3_R[3:0] ,COS4_R[3:0] ,//     STV1 VGL
DSI_PA(0xFA);   //42   COS5_R[3:0] ,COS6_R[3:0] ,//     VDS   VDDE
DSI_PA(0xB2);   //43   COS7_R[3:0] ,COS8_R[3:0] ,//     VDDO CLK7
DSI_PA(0x06);   //44   COS9_R[3:0] ,COS10_R[3:0],//     CLK5 CLK3
DSI_PA(0x48);   //45   COS11_R[3:0],COS12_R[3:0],//     CLK1
DSI_PA(0x88);   //46   COS13_R[3:0],COS14_R[3:0],//
DSI_PA(0x88);   //47   COS15_R[3:0],COS16_R[3:0],//
DSI_PA(0x88);   //48   COS17_R[3:0],COS18_R[3:0],//
DSI_PA(0x88);   //49   COS19_R[3:0],COS20_R[3:0],//
DSI_PA(0x88);   //50   COS21_R[3:0],COS22_R[3:0],//
DSI_PA(0x00);   //51   TCONOPTION
DSI_PA(0x00);   //52   OPTION
DSI_PA(0x00);   //53   OTPION
DSI_PA(0x01);   //54   OPTION
DSI_PA(0x00);   //55   CHR2
DSI_PA(0x80);   //56   CON2
DSI_PA(0x28);   //57   COFF2
DSI_PA(0x47);   //58   CHP2,CCP2
DSI_PA(0x00);   //59   CKS 21 20 19 18 17 16
DSI_PA(0x00);   //60   CKS 15 14 13 12 11 10 9 8
DSI_PA(0x00);   //61   CKS 7~0
DSI_PA(0x00);   //62   COFF[7:6]    CON[5:4]     SPOFF[3:2]      SPON[1:0]
DSI_PA(0x00);   //63   COFF2[7:6]     CON2[5:4]     - - - -

DSI_CMD(0x3E,0xEA); /// Set GIP2
DSI_PA(0x97); //1    ys
DSI_PA(0x0C); //2    user_gip_gate1[7:0]
DSI_PA(0x07); //3    ck_all_on_width1[5:0]
DSI_PA(0x07); //4    ck_all_on_width2[5:0]
DSI_PA(0x08); //5    ck_all_on_width3[5:0]
DSI_PA(0xB4); //6    ys_flag_period[7:0]
DSI_PA(0x00);   //7    ys_2
DSI_PA(0x00);   //8    user_gip_gate1_2[7:0]
DSI_PA(0x00);   //9    ck_all_on_width1_2[5:0]
DSI_PA(0x00);   //10 ck_all_on_width2_2[5:0]
DSI_PA(0x00);   //11 ck_all_on_width3_2[5:0]
DSI_PA(0x00);   //12 ys_flag_period_2[7:0]
DSI_PA(0x9F);   //13   COS1_L[3:0] ,COS2_L[3:0] ,//     STV0    ,   VSD
DSI_PA(0x08);   //14   COS3_L[3:0] ,COS4_L[3:0] ,//     STV2    ,   VGL
DSI_PA(0x8A);   //15   COS5_L[3:0] ,COS6_L[3:0] ,//     VDS     ,   VDDE
DSI_PA(0xB4);   //16   COS7_L[3:0] ,COS8_L[3:0] ,//     VDDO    ,   CLK8
DSI_PA(0x60);   //17   COS9_L[3:0] ,COS10_L[3:0],//     CLK6    ,    CLK4
DSI_PA(0x28);   //18   COS11_L[3:0],COS12_L[3:0],//     CLK2
DSI_PA(0x88);   //19   COS13_L[3:0],COS14_L[3:0],//
DSI_PA(0x88);   //20   COS15_L[3:0],COS16_L[3:0],//
```

```
DSI_PA(0x88);   //21   COS17_L[3:0],COS18_L[3:0],//
DSI_PA(0x88);   //22   COS19_L[3:0],COS20_L[3:0],//
DSI_PA(0x88);   //23   COS21_L[3:0],COS22_L[3:0],//
DSI_PA(0x9F);   //24   COS1_R[3:0] ,COS2_R[3:0] ,//    STV0   ,   VSD
DSI_PA(0x18);   //25   COS3_R[3:0] ,COS4_R[3:0] ,//    STV1   ,   VGL
DSI_PA(0x8A);   //26   COS5_R[3:0] ,COS6_R[3:0] ,//    VDS    ,   VDDE
DSI_PA(0xB5);   //27   COS7_R[3:0] ,COS8_R[3:0] ,//    VDDO   ,   CLK7
DSI_PA(0x71);   //28   COS9_R[3:0] ,COS10_R[3:0],//    CLK5   ,   CLK3
DSI_PA(0x38);   //29   COS11_R[3:0],COS12_R[3:0],//    CLK1
DSI_PA(0x88);   //30   COS13_R[3:0],COS14_R[3:0],//
DSI_PA(0x88);   //31   COS15_R[3:0],COS16_R[3:0],//
DSI_PA(0x88);   //32   COS17_R[3:0],COS18_R[3:0],//
DSI_PA(0x88);   //33   COS19_R[3:0],COS20_R[3:0],//
DSI_PA(0x88);   //34   COS21_R[3:0],COS22_R[3:0],//
DSI_PA(0x23);   //35 EQOPT , EQ_SEL
DSI_PA(0x10);   //36 EQ_DELAY[7:0]
DSI_PA(0x00);   //37 EQ_DELAY_HSYNC [3:0]
DSI_PA(0x01);   //38
DSI_PA(0x1B);   //39 HSYNC_TO_CL1_CNT9[8]
DSI_PA(0x00);   //40 HSYNC_TO_CL1_CNT9[7:0]
DSI_PA(0x00);   //41 HIZ_R HIZ_L
DSI_PA(0x00);   //42 CKS_GS[21:16]
DSI_PA(0x00);   //43 CKS_GS[15:8]
DSI_PA(0x00);   //44 CKS_GS[7:0]
DSI_PA(0x00);   //45 CK_MSB_EN[21:16]
DSI_PA(0x00);   //46 CK_MSB_EN[15:8]
DSI_PA(0x00);   //47 CK_MSB_EN[7:0]
DSI_PA(0x00);   //48 CK_MSB_EN_GS[21:16]
DSI_PA(0x00);   //49 CK_MSB_EN_GS[15:8]
DSI_PA(0x00);   //50 CK_MSB_EN_GS[7:0]
DSI_PA(0x00);   //51 SHR2[11:8]
DSI_PA(0x00);   //52 SHR2[7:0]
DSI_PA(0x00);   //53 SHR2_1[3:0] SHR2_2
DSI_PA(0x00);   //54 SHR2_3[3:0]
DSI_PA(0x44);   //55 SHP1[3:0], SHP2[3:0]
DSI_PA(0x80);   //56 SPON1[7:0]
DSI_PA(0x81);   //57 SPOFF1[7:0]
DSI_PA(0x80);   //58 SPON2[7:0]
DSI_PA(0x81);   //59 SPOFF2[7:0]
DSI_PA(0x00);   //60 SPOFF2[9:8]/SPON2[9:8]/SPOFF1[9:8]/SPON1[9:8]
DSI_PA(0x00);   //61


DSI_CMD(0x04,0xEF);
DSI_PA(0xFF);    //1
DSI_PA(0xFF);    //2
DSI_PA(0x01);    //3


DSI_CMD(0x01,0x11); ////Sleep Out
```

```
DelayX1ms(250);

DSI_CMD(0x01,0x29); ///Display On
DelayX1ms(50);
```

winstar **LCM Sample Estimate Feedback Sheet**

Module Number： _____ **Page: 1**

1、Panel Specification：

1.	Panel Type：	□ Pass	□ NG , _____
2.	View Direction：	□ Pass	□ NG , _____
3.	Numbers of Dots：	□ Pass	□ NG , _____
4.	View Area：	□ Pass	□ NG , _____
5.	Active Area：	□ Pass	□ NG , _____
6.	Operating Temperature：	□ Pass	□ NG , _____
7.	Storage Temperature：	□ Pass	□ NG , _____
8.	Others： _____		

2、Mechanical

1.	PCB Size：	□ Pass	□ NG , _____
2.	Frame Size：	□ Pass	□ NG , _____
3.	Material of Frame：	□ Pass	□ NG , _____
4.	Connector Position：	□ Pass	□ NG , _____
5.	Fix Hole Position：	□ Pass	□ NG , _____
6.	Backlight Position：	□ Pass	□ NG , _____
7.	Thickness of PCB：	□ Pass	□ NG , _____
8.	Height of Frame to PCB：	□ Pass	□ NG , _____
9.	Height of Module：	□ Pass	□ NG , _____
10.	Others：	□ Pass	□ NG , _____

3、Relative Hole Size：

1.	Pitch of Connector：	□ Pass	□ NG , _____
2.	Hole size of Connector：	□ Pass	□ NG , _____
3.	Mounting Hole size：	□ Pass	□ NG , _____
4.	Mounting Hole Type：	□ Pass	□ NG , _____
5.	Others：	□ Pass	□ NG , _____

4、Backlight Specification：

1.	B/L Type：	□ Pass	□ NG , _____
2.	B/L Color：	□ Pass	□ NG , _____
3.	B/L Driving Voltage (Reference for LED Type)：	□ Pass	□ NG , _____
4.	B/L Driving Current：	□ Pass	□ NG , _____
5.	Brightness of B/L：	□ Pass	□ NG , _____
6.	B/L Solder Method：	□ Pass	□ NG , _____
7.	Others：	□ Pass	□ NG , _____

>> Go to page 2 <<

5、Electronic Characteristics of Module：

1.	Input Voltage：	□ Pass	□ NG ,_____
2.	Supply Current：	□ Pass	□ NG ,_____
3.	Driving Voltage for LCD：	□ Pass	□ NG ,_____
4.	Contrast for LCD：	□ Pass	□ NG ,_____
5.	B/L Driving Method：	□ Pass	□ NG ,_____
6.	Negative Voltage Output：	□ Pass	□ NG ,_____
7.	Interface Function：	□ Pass	□ NG ,_____
8.	LCD Uniformity：	□ Pass	□ NG ,_____
9.	ESD test：	□ Pass	□ NG ,_____
10.	Others：	□ Pass	□ NG ,_____

6、Summary：

Sales signature：_____

Customer Signature：_____ **Date：** / /

winstar

LCM Sample Estimate Feedback Sheet

Module Number： _____ **Page: 1**

1、Panel Specification：

1.	Panel Type：	□ Pass	□ NG , _____
2.	View Direction：	□ Pass	□ NG , _____
3.	Numbers of Dots：	□ Pass	□ NG , _____
4.	View Area：	□ Pass	□ NG , _____
5.	Active Area：	□ Pass	□ NG , _____
6.	Operating Temperature：	□ Pass	□ NG , _____
7.	Storage Temperature：	□ Pass	□ NG , _____
8.	Others： _____		

2、Mechanical

1.	PCB Size：	□ Pass	□ NG , _____
2.	Frame Size：	□ Pass	□ NG , _____
3.	Material of Frame：	□ Pass	□ NG , _____
4.	Connector Position：	□ Pass	□ NG , _____
5.	Fix Hole Position：	□ Pass	□ NG , _____
6.	Backlight Position：	□ Pass	□ NG , _____
7.	Thickness of PCB：	□ Pass	□ NG , _____
8.	Height of Frame to PCB：	□ Pass	□ NG , _____
9.	Height of Module：	□ Pass	□ NG , _____
10.	Others：	□ Pass	□ NG , _____

3、Relative Hole Size：

1.	Pitch of Connector：	□ Pass	□ NG , _____
2.	Hole size of Connector：	□ Pass	□ NG , _____
3.	Mounting Hole size：	□ Pass	□ NG , _____
4.	Mounting Hole Type：	□ Pass	□ NG , _____
5.	Others：	□ Pass	□ NG , _____

4、Backlight Specification：

1.	B/L Type：	□ Pass	□ NG , _____
2.	B/L Color：	□ Pass	□ NG , _____
3.	B/L Driving Voltage (Reference for LED Type)：	□ Pass	□ NG , _____
4.	B/L Driving Current：	□ Pass	□ NG , _____
5.	Brightness of B/L：	□ Pass	□ NG , _____
6.	B/L Solder Method：	□ Pass	□ NG , _____
7.	Others：	□ Pass	□ NG , _____

>> Go to page 2 <<

5、Electronic Characteristics of Module：

1.	Input Voltage：	□ Pass	□ NG ,_____
2.	Supply Current：	□ Pass	□ NG ,_____
3.	Driving Voltage for LCD：	□ Pass	□ NG ,_____
4.	Contrast for LCD：	□ Pass	□ NG ,_____
5.	B/L Driving Method：	□ Pass	□ NG ,_____
6.	Negative Voltage Output：	□ Pass	□ NG ,_____
7.	Interface Function：	□ Pass	□ NG ,_____
8.	LCD Uniformity：	□ Pass	□ NG ,_____
9.	ESD test：	□ Pass	□ NG ,_____
10.	Others：	□ Pass	□ NG ,_____

6、Summary：

Sales signature：_____

Customer Signature：_____ **Date**：____/____/____