NV34C02WF

EEPROM SPD 2-kb I²C for DDR2 DIMM

Description

The NV34C02WF is a EEPROM Serial 2−kb, internally organized as 16 pages of 16 bytes each, for a total of 256 bytes of 8 bits each.

It features a 16−byte page write buffer and supports both the Standard (100 kHz) as well as Fast (400 kHz) I²C protocol.

Write operations can be inhibited by taking the WP pin High (this protects the entire memory) or by setting an internal Write Protect flag via Software command (this protects the lower half of the memory).

In addition to Permanent Software Write Protection, the NV34C02WF also features JEDEC compatible Reversible Software Write Protection for DDR2 Serial Presence Detect (SPD) applications operating over the 1.7 V to 3.6 V supply voltage range.

The NV34C02WF is fully backwards compatible with earlier DDR1 SPD applications operating over the 1.7 V to 5.5 V supply voltage range.

Features

- Supports Standard and Fast I²C Protocol
- 1.7 V to 5.5 V Supply Voltage Range
- 16−Byte Page Write Buffer
- Hardware Write Protection for Entire Memory
- Software Write Protection for Lower 128 Bytes
- Schmitt Triggers and Noise Suppression Filters on I²C Bus Inputs (SCL and SDA)
- Low power CMOS Technology
- 1,000,000 Program/Erase Cycles
- 100 Year Data Retention
- Automotive Grade 1 Temperature Range
- This Device is Pb−Free, Halogen Free/BFR Free and RoHS Compliant*

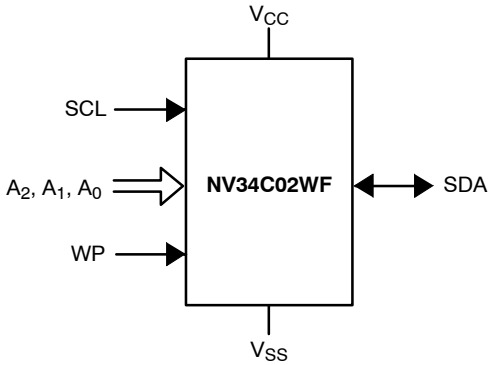


Figure 1. Functional Symbol

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

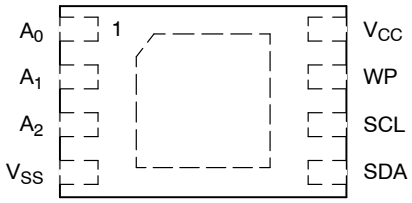
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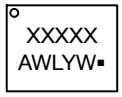
UDFN8
U SUFFIX
CASE 517DH

PIN CONFIGURATION



US8 (U)

PART MARKING



XXXXX	= Specific Device Code
A	= Assembly Location
WL	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

PIN FUNCTION

Pin Name	Function
A_0, A_1, A_2	Device Address Input
SDA	Serial Data Input/Output
SCL	Serial Clock Input
WP	Write Protect Input
V_{CC}	Power Supply
V_{SS}	Ground

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 3 of this data sheet.

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Table 1. ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Unit
Operating Temperature	−45 to +130	°C
Storage Temperature	−65 to +150	°C
Voltage on Any Pin with Respect to Ground (Note 1)	−0.5 to +6.5	V
Voltage on Pin A_0 with Respect to Ground	−0.5 to +10.5	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The DC input voltage on any pin should not be lower than −0.5 V or higher than V_{CC} + 0.5 V. During transitions, the voltage on any pin may undershoot to no less than −1.5 V or overshoot to no more than V_{CC} + 1.5 V, for periods of less than 20 ns.

Table 2. RELIABILITY CHARACTERISTICS (Note 2)

Symbol	Parameter	Min	Units
N_{END} (Note 3)	Endurance	1,000,000	Program/ Erase Cycles
T_{DR}	Data Retention	100	Years

2. These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC−Q100 and JEDEC test methods.
3. Page Mode, V_{CC} = 5 V, 25°C

Table 3. D.C. OPERATING CHARACTERISTICS (V_{CC} = 1.7 V to 5.5 V, T_A = −40°C to +125°C, unless otherwise specified.)

Symbol	Parameter	Test Conditions		Min	Max	Units
I_{CC}	Supply Current	V_{CC} < 3.6 V, f_{SCL} = 100 kHz			1	mA
		V_{CC} > 3.6 V, f_{SCL} = 400 kHz			2	
I_{SB}	Standby Current	All I/O Pins at GND or V_{CC}	T_A = −40°C to +125°C $V_{CC} \le$ 3.3 V		1	μA
			T_A = −40°C to +125°C V_{CC} > 3.3 V		3	
I_L	I/O Pin Leakage	Pin at GND or V_{CC}			2	μA
V_{IL}	Input Low Voltage			−0.5	0.3 x V_{CC}	V
V_{IH}	Input High Voltage			0.7 x V_{CC}	V_{CC} + 0.5	
V_{OL}	Output Low Voltage	V_{CC} > 2.5 V, I_{OL} = 3 mA			0.4	
		V_{CC} < 2.5 V, I_{OL} = 1 mA			0.2	

Table 4. PIN IMPEDANCE CHARACTERISTICS (V_{CC} = 1.7 V to 5.5 V, T_A = −40°C to +125°C, unless otherwise specified.)

Symbol	Parameter	Conditions	Max	Units
C_{IN} (Note 4)	SDA I/O Pin Capacitance	V_{IN} = 0 V, f = 1.0 MHz, V_{CC} = 5.0 V	8	pF
	Other Input Pins		6	
I_{WP} (Note 5)	WP Input Current	V_{IN} < V_{IH}, V_{CC} = 5.5 V	130	μA
		V_{IN} < V_{IH}, V_{CC} = 3.6 V	120	
		V_{IN} < V_{IH}, V_{CC} = 1.7 V	80	
		V_{IN} > V_{IH}	2	
I_A (Note 5)	Address Input Current (A0, A1, A2) Product Rev H	V_{IN} < V_{IH}, V_{CC} = 5.5 V	50	μA
		V_{IN} < V_{IH}, V_{CC} = 3.6 V	35	
		V_{IN} < V_{IH}, V_{CC} = 1.7 V	25	
		V_{IN} > V_{IH}	2	

4. These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC−Q100 and JEDEC test methods.
5. When not driven, the WP, A0, A1 and A2 pins are pulled down to GND internally. For improved noise immunity, the internal pull-down is relatively strong; therefore the external driver must be able to supply the pull-down current when attempting to drive the input HIGH. To conserve power, as the input level exceeds the trip point of the CMOS input buffer (~ 0.5 x V_{CC}), the strong pull-down reverts to a weak current source.

Table 5. A.C. CHARACTERISTICS (V_{CC} = 1.7 V to 5.5 V, T_A = −40°C to +125°C) (Note 6)

Symbol	Parameter	Standard		Fast		Units
		Min	Max	Min	Max	
F_{SCL}	Clock Frequency		100		400	kHz
$t_{HD:STA}$	START Condition Hold Time	4		0.6		μs
t_{LOW}	Low Period of SCL Clock	4.7		1.3		μs
t_{HIGH}	High Period of SCL Clock	4		0.6		μs
$t_{SU:STA}$	START Condition Setup Time	4.7		0.6		μs
$t_{HD:DAT}$	Data Hold Time	0		0		μs
$t_{SU:DAT}$	Data Setup Time	250		100		ns
t_R (Note 7)	SDA and SCL Rise Time		1000		300	ns
t_F (Note 7)	SDA and SCL Fall Time		300		300	ns
$t_{SU:STO}$	STOP Condition Setup Time	4		0.6		μs
t_{BUF}	Bus Free Time Between STOP and START	4.7		1.3		μs
t_{AA}	SCL Low to SDA Data Out		3.5		0.9	μs
t_{DH}	Data Out Hold Time	100		100		ns
T_i (Note 7)	Noise Pulse Filtered at SCL and SDA Inputs		100		100	ns
$t_{SU:WP}$	WP Setup Time	0		0		μs
$t_{HD:WP}$	WP Hold Time	2.5		2.5		μs
t_{WR}	Write Cycle Time		5		5	ms
t_{PU} (Notes 7 & 8)	Power−up to Ready Mode		1		1	ms

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. Test conditions according to “A.C. Test Conditions” table.
7. Tested initially and after a design or process change that affects this parameter.
8. t_{PU} is the delay between the time V_{CC} is stable and the device is ready to accept commands.

Table 6. A.C. TEST CONDITIONS

Input Levels	0.2 V_{CC} to 0.8 V_{CC}
Input Rise and Fall Times	≤ 50 ns
Input Reference Levels	0.3 V_{CC}, 0.7 V_{CC}
Output Reference Levels	0.5 V_{CC}
Output Load	Current Source: I_{OL} = 3 mA (V_{CC} ≥ 2.5 V); I_{OL} = 1 mA (V_{CC} < 2.5 V); C_L = 100 pF

ORDERING INFORMATION

Device	Marking	Package	Shipping†
NV34C02WF	TBD	UDFN8 (Pb−Free)	3000 / Tape & Reel

9. All packages are RoHS−compliant (Lead−free, Halogen−free)

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Power−On Reset (POR)

The NV34C02WF incorporates Power−On Reset (POR) circuitry which protects the internal logic against powering up in the wrong state.

The NV34C02WF will power up into Standby mode after V_{CC} exceeds the POR trigger level and will power down into Reset mode when V_{CC} drops below the POR trigger level. This bi−directional POR feature protects the device against 'brown−out' failure following a temporary loss of power.

Pin Description

SCL: The Serial Clock input pin accepts the Serial Clock generated by the Master.

SDA: The Serial Data I/O pin receives input data and transmits data stored in EEPROM. In transmit mode, this pin is open drain. Data is acquired on the positive edge, and is delivered on the negative edge of SCL.

A_0, A_1 and A_2: The Address pins accept the device address. These pins have on−chip pull−down resistors.

WP: The Write Protect input pin inhibits all write operations, when pulled HIGH. This pin has an on−chip pull−down resistor.

Functional Description

The NV34C02WF supports the Inter−Integrated Circuit (I^2C) Bus data transmission protocol, which defines a device that sends data to the bus as a transmitter and a device receiving data as a receiver. Data flow is controlled by a Master device, which generates the serial clock and all START and STOP conditions. The NV34C02WF acts as a Slave device. Master and Slave alternate as either transmitter or receiver. Up to 8 devices may be connected to the bus as determined by the device address inputs A_0, A_1, and A_2.

I^2C Bus Protocol

The I^2C bus consists of two 'wires', SCL and SDA. The two wires are connected to the V_{CC} supply via pull−up resistors. Master and Slave devices connect to the 2−wire bus via their respective SCL and SDA pins. The transmitting device pulls down the SDA line to 'transmit' a '0' and releases it to 'transmit' a '1'.

Data transfer may be initiated only when the bus is not busy (see A.C. Characteristics).

During data transfer, the SDA line must remain stable while the SCL line is HIGH. An SDA transition while SCL is HIGH will be interpreted as a START or STOP condition (Figure 2).

Start

The START condition precedes all commands. It consists of a HIGH to LOW transition on SDA while SCL is HIGH. The START acts as a 'wake−up' call to all receivers. Absent a START, a Slave will not respond to commands.

Stop

The STOP condition completes all commands. It consists of a LOW to HIGH transition on SDA while SCL is HIGH. The STOP starts the internal Write cycle (when following a Write command) or sends the Slave into standby mode (when following a Read command).

Device Addressing

The Master initiates data transfer by creating a START condition on the bus. The Master then broadcasts an 8−bit serial Slave address. The first 4 bits of the Slave address are set to 1010, for normal Read/Write operations (Figure 3). The next 3 bits, A_2, A_1 and A_0, select one of 8 possible Slave devices. The last bit, R/$\overline{W}$, specifies whether a Read (1) or Write (0) operation is to be performed.

Acknowledge

After processing the Slave address, the Slave responds with an acknowledge (ACK) by pulling down the SDA line during the 9^{th} clock cycle (Figure 4). The Slave will also acknowledge the byte address and every data byte presented in Write mode. In Read mode the Slave shifts out a data byte, and then releases the SDA line during the 9^{th} clock cycle. If the Master acknowledges the data, then the Slave continues transmitting. The Master terminates the session by not acknowledging the last data byte (NoACK) and by sending a STOP to the Slave. Bus timing is illustrated in Figure 5.

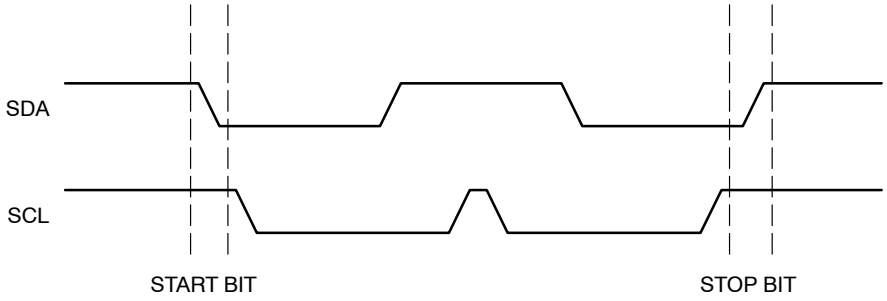


Figure 2. Start/Stop Timing

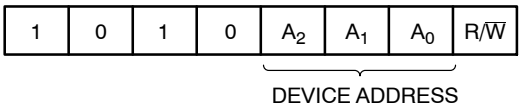


Figure 3. Slave Address Bits

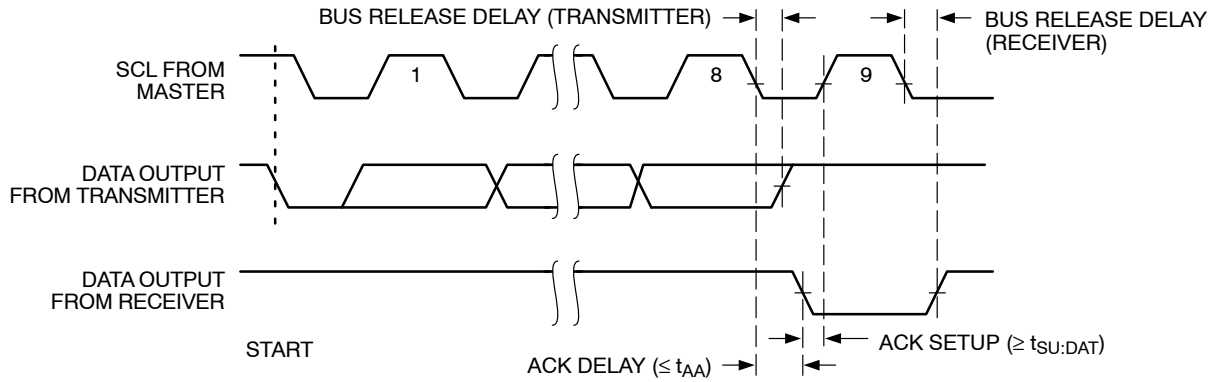


Figure 4. Acknowledge Timing

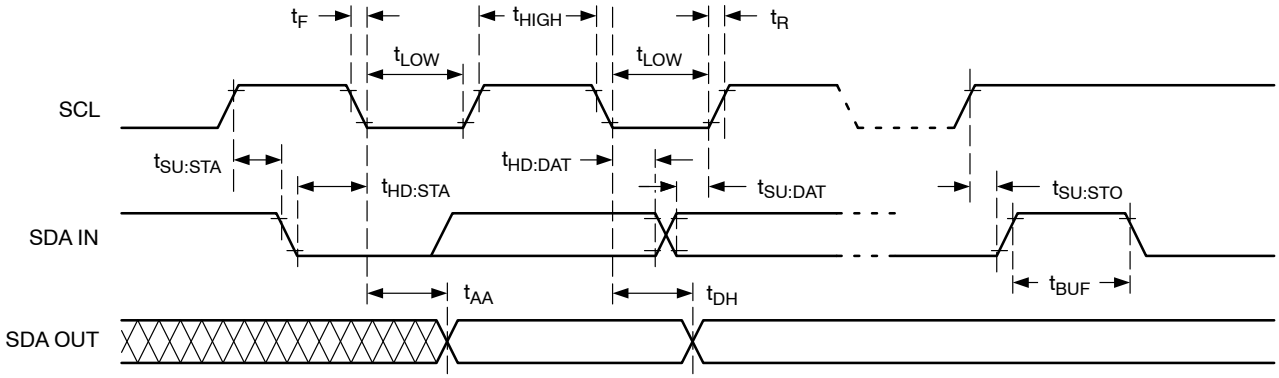


Figure 5. Bus Timing

Write Operations

Byte Write

In Byte Write mode the Master sends a START, followed by Slave address, byte address and data to be written (Figure 6). The Slave acknowledges all 3 bytes, and the Master then follows up with a STOP, which in turn starts the internal Write operation (Figure 7). During internal Write, the Slave will not acknowledge any Read or Write request from the Master.

Page Write

The NV34C02WF contains 256 bytes of data, arranged in 16 pages of 16 bytes each. A page is selected by the 4 most significant bits of the address byte following the Slave address, while the 4 least significant bits point to the byte within the page. Up to 16 bytes can be written in one Write cycle (Figure 8).

The internal byte address counter is automatically incremented after each data byte is loaded. If the Master transmits more than 16 data bytes, then earlier bytes will be overwritten by later bytes in a ‘wrap−around’ fashion (within the selected page). The internal Write cycle starts immediately following the STOP.

Acknowledge Polling

Acknowledge polling can be used to determine if the NV34C02WF is busy writing or is ready to accept commands. Polling is implemented by interrogating the device with a ‘Selective Read’ command (see READ OPERATIONS).

The NV34C02WF will not acknowledge the Slave address, as long as internal Write is in progress.

Delivery State

The NV34C02WF is shipped ‘unprotected’, i.e. neither SWP flag is set. The entire 2 kb memory is erased, i.e. all bytes are FFh.

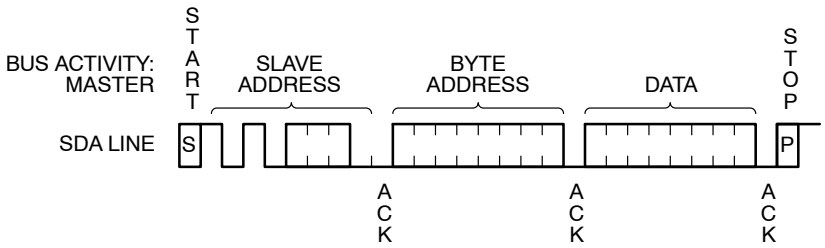


Figure 6. Byte Write Timing

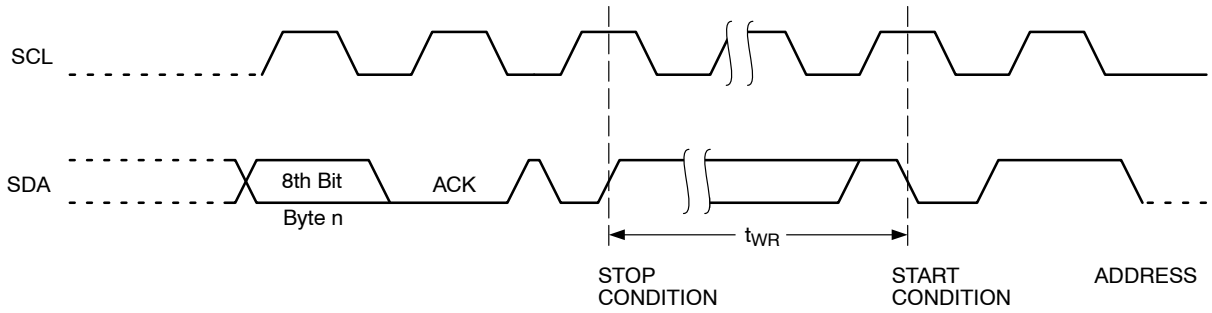
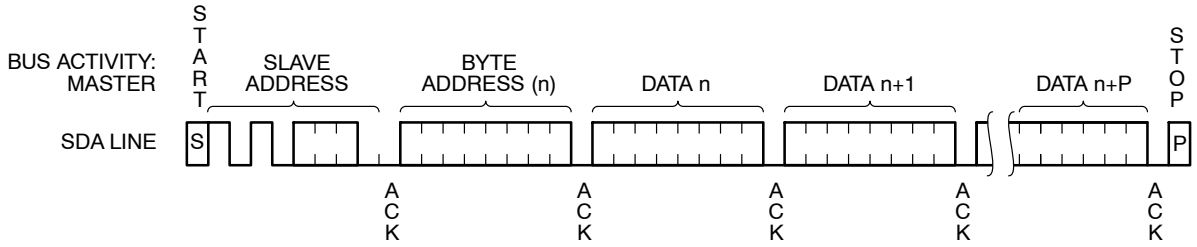


Figure 7. Write Cycle Timing



NOTE: IN THIS EXAMPLE n = XXXX 0000(B); X = 1 or 0

Figure 8. Page Write Timing

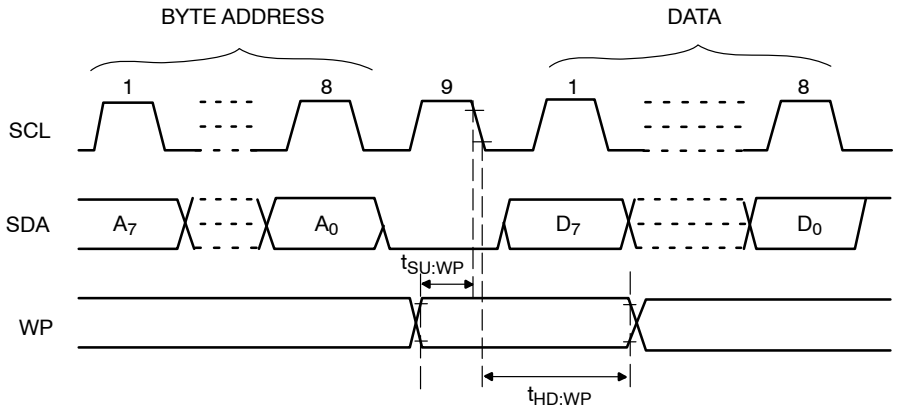


Figure 9. WP Timing

Read Operations

Immediate Address Read

In standby mode, the NV34C02WF internal address counter points to the data byte immediately following the last byte accessed by a previous operation. If that 'previous' byte was the last byte in memory, then the address counter will point to the 1st memory byte, etc.

When, following a START, the NV34C02WF is presented with a Slave address containing a '1' in the R/$\overline{W}$ bit position (Figure 10), it will acknowledge (ACK) in the 9th clock cycle, and will then transmit data being pointed at by the internal address counter. The Master can stop further transmission by issuing a NoACK, followed by a STOP condition.

Selective Read

The Read operation can also be started at an address different from the one stored in the internal address counter. The address counter can be initialized by performing a 'dummy' Write operation (Figure 11). Here the START is followed by the Slave address (with the R/$\overline{W}$ bit set to '0') and the desired byte address. Instead of following up with data, the Master then issues a 2nd START, followed by the 'Immediate Address Read' sequence, as described earlier.

Sequential Read

If the Master acknowledges the 1st data byte transmitted by the NV34C02WF, then the device will continue transmitting as long as each data byte is acknowledged by the Master (Figure 12). If the end of memory is reached during sequential Read, then the address counter will 'wrap−around' to the beginning of memory, etc. Sequential Read works with either 'Immediate Address Read' or 'Selective Read', the only difference being the starting byte address.

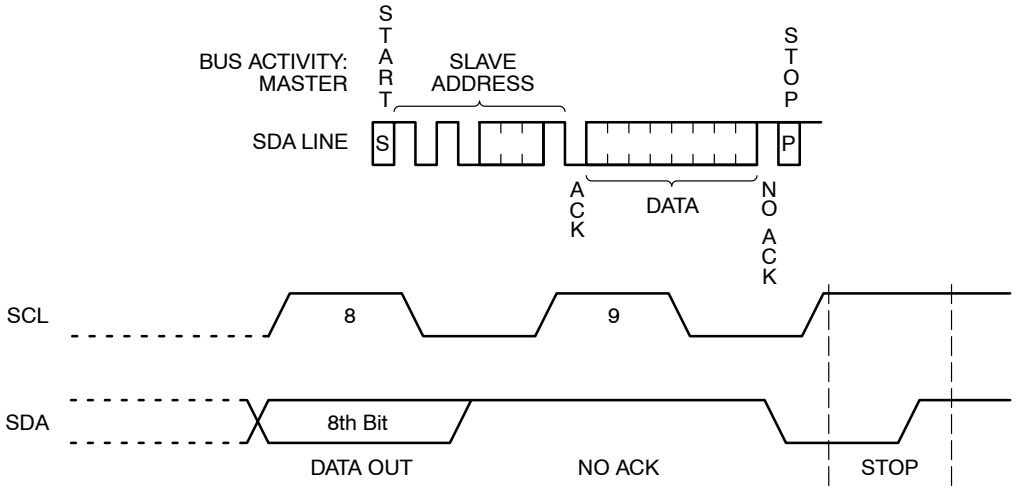


Figure 10. Immediate Address Read Timing

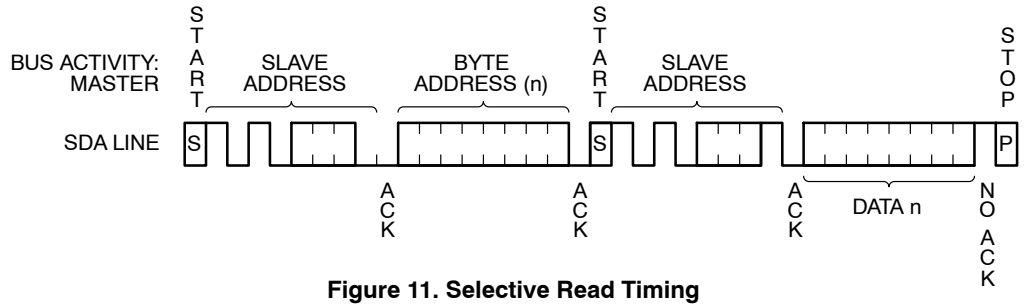


Figure 11. Selective Read Timing

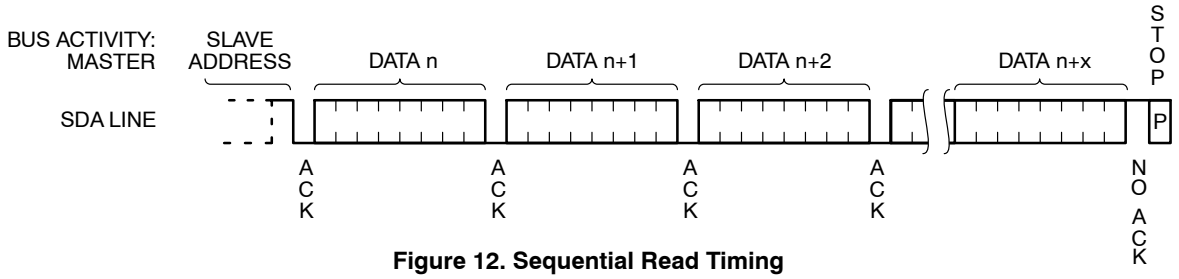


Figure 12. Sequential Read Timing

Software Write Protection

The lower half of memory (first 128 bytes) can be protected against Write requests by setting one of two Software Write Protection (SWP) flags.

The Permanent Software Write Protection (PSWP) flag can be set or read while all address pins are at regular CMOS levels (GND or V_{CC}), whereas the very high voltage V_{HV} must be present on address pin A_0 to set, clear or read the Reversible Software Write Protection (**RSWP**) flag. The D.C. OPERATING CONDITIONS for RSWP operations are shown in Table 7.

The SWP commands are listed in Table 8. All commands are preceded by a START and terminated with a STOP, following the ACK or NoACK from the NV34C02WF. All SWP related Slave addresses use the pre−amble: 0110 (6h), instead of the regular 1010 (Ah) used for memory access. For **PSWP** commands, the three address pins can be at any logic level, whereas for **RSWP** commands the address pins must be at pre−assigned logic levels. V_{HV} is interpreted as logic '1'. The V_{HV} condition must be established on pin A_0 before the START and maintained just beyond the STOP. Otherwise an RSWP request could be interpreted by the NV34C02WF as a PSWP request.

The SWP Slave addresses follow the standard I^2C convention, i.e. to read the state of the SWP flag, the LSB of the Slave address must be '1', and to set or clear a flag, it must be '0'. For Write commands a dummy byte address and dummy data byte must be provided (Figure 14). In contrast to a regular memory Read, a SWP Read does not return Data. Instead the NV34C02WF will respond with NoACK if the flag is set and with ACK if the flag is not set. Therefore, the Master can immediately follow up with a STOP, as there is no meaningful data following the ACK interval (Figure 15).

Hardware Write Protection

With the WP pin held HIGH, the entire memory, as well as the SWP flags are protected against Write operations, see Memory Protection Map below. If the WP pin is left floating or is grounded, it has no impact on the operation of the NV34C02WF.

The state of the WP pin is strobed on the last falling edge of SCL immediately preceding the first data byte (Figure 9). If the WP pin is HIGH during the strobe interval, the NV34C02WF will not acknowledge the data byte and the Write request will be rejected.

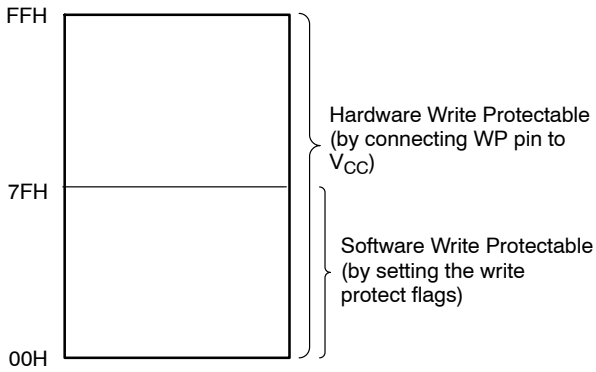


Figure 13. Memory Protection Map

Table 7. RSWP D.C. OPERATING CONDITIONS (Note 10)

Symbol	Parameter	Test Conditions	Min	Max	Units
ΔV_{HV}	A_0 Overdrive ($V_{HV} - V_{CC}$)	1.7 V < V_{CC} < 3.6 V	4.8		V
I_{HVD}	A_0 High Voltage Detector Current			0.1	mA
V_{HV}	A_0 Very High Voltage		7	10	V
I_{HV}	A_0 Input Current @ V_{HV}			1	mA

10. To prevent damaging the NV34C02WF while applying V_{HV}, it is strongly recommended to limit the power delivered to pin A_0, by inserting a series resistor (> 1.5 kΩ) between the supply and the input pin. The resistance is only limited by the combination of V_{HV} and maximum I_{HVD}. While the resistor can be omitted if V_{HV} is clamped well below 10 V, it nevertheless provides simple protection against EOS events.

    As an example: V_{CC} = 1.7 V, V_{HV} = 8 V, 1.5 kΩ < R_S < 15 kΩ.

Table 8. SWP COMMANDS

Action	Control Pin Levels (Note 11)				Flag State (Note 12)		Slave Address					ACK ?	Address Byte	ACK ?	Data Byte	ACK ?	Write Cycle
	WP	A_2	A_1	A_0	PSWP	RSWP	b_7 to b_4	b_3	b_2	b_1	b_0						
Set PSWP	X	A_2	A_1	A_0	1	X	0110	A_2	A_1	A_0	X	No					
	GND	A_2	A_1	A_0	0	X		A_2	A_1	A_0	0	Yes	X	Yes	X	Yes	Yes
	V_{CC}	A_2	A_1	A_0	0	X		A_2	A_1	A_0	0	Yes	X	Yes	X	No	No
	X	A_2	A_1	A_0	0	X		A_2	A_1	A_0	1	Yes					
Set RSWP	X	GND	GND	V_{HV}	1	X		0	0	1	X	No					
	X	GND	GND	V_{HV}	0	1		0	0	1	X	No					
	GND	GND	GND	V_{HV}	0	0		0	0	1	0	Yes	X	Yes	X	Yes	Yes
	V_{CC}	GND	GND	V_{HV}	0	0		0	0	1	0	Yes	X	Yes	X	No	No
	X	GND	GND	V_{HV}	0	0		0	0	1	1	Yes					
Clear RSWP	X	GND	V_{CC}	V_{HV}	1	X		0	1	1	X	No					
	GND	GND	V_{CC}	V_{HV}	0	X		0	1	1	0	Yes	X	Yes	X	Yes	Yes
	V_{CC}	GND	V_{CC}	V_{HV}	0	X		0	1	1	0	Yes	X	Yes	X	No	No
	X	GND	V_{CC}	V_{HV}	0	X		0	1	1	1	Yes					

11. Here A_2, A_1 and A_0 are either at V_{CC} or GND.
12. 1 stands for ‘Set’, 0 stands for ‘Not Set’, X stands for ‘don’t care’.

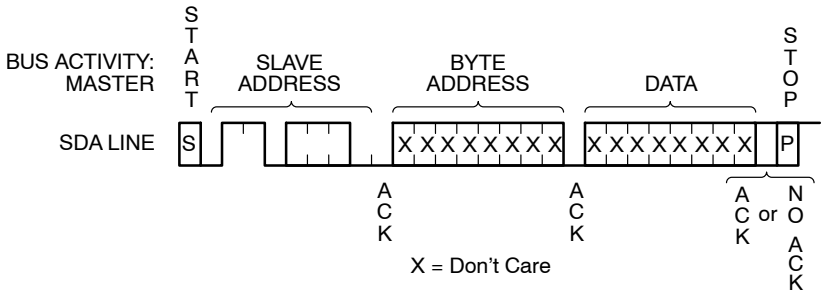


Figure 14. Software Write Protect (Write)

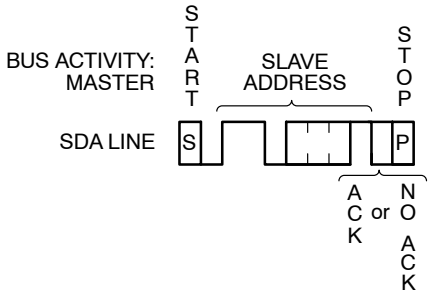


Figure 15. Software Write Protect (Read)

ON Semiconductor is licensed by Philips Corporation to carry the I^2C Bus Protocol.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

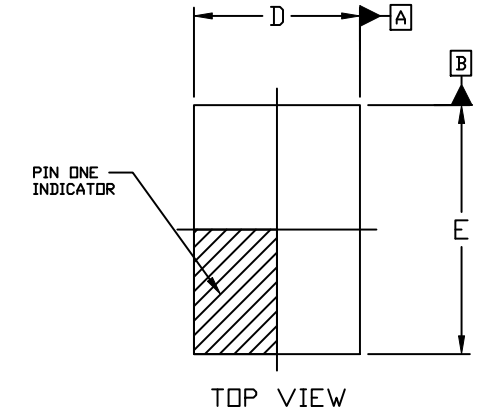
ON Semiconductor®

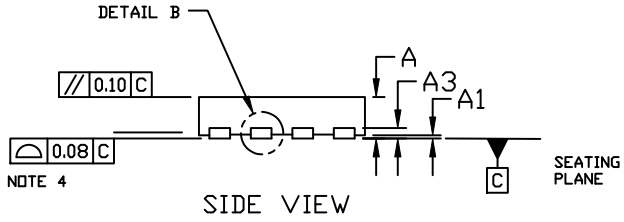


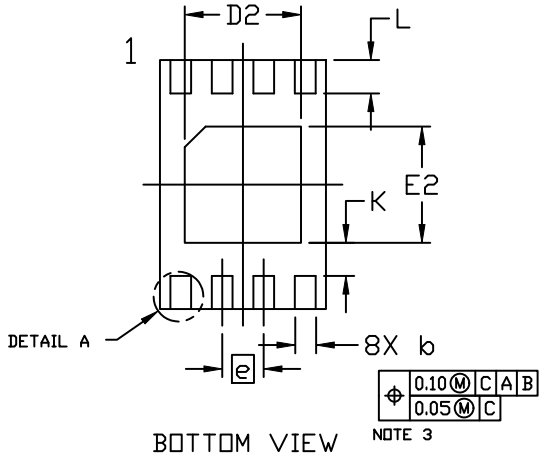
SCALE 2:1

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CASE 517DH
ISSUE A

DATE 10 DEC 2020

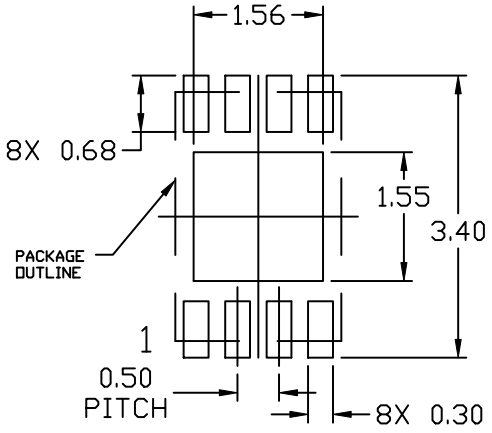






NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M,1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.25MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

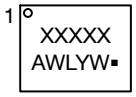
	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	0.45	0.50	0.55
A1	0.00	---	0.05
A3	0.13 REF		
b	0.20	0.25	0.30
D	1.90	2.00	2.10
D2	1.30	1.40	1.50
E	2.90	3.00	3.10
E2	1.30	1.40	1.50
e	0.50 BSC		
K	0.40 REF		
L	0.30	0.40	0.50



RECOMMENDED MOUNTING FOOTPRINT*

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX	= Specific Device Code
A	= Assembly Location
WL	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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