General Description

BDE-MP2674R10 is a high performance multiprotocol 2.4-GHz wireless module series based on Texas Instrument (TI)'s multiprotocol wireless microcontroller (MCU) CC2674R106T0RGZ. In order to fulfil different integration scenarios, we provide different variants for this module series. They are listed and described in Table 1.

BDE-MP2674R10 module series integrates an powerful 48-MHz Arm® Cortex®-M33 MCU and a dedicated software controlled radio controller (Arm® Cortex®-M0) providing flexible low-power RF transceiver capability to support multiple physical layers and RF standards. It supports Thread, Zigbee®, Matter, Bluetooth® 5.3 Low Energy, IEEE 802.15.4g, IPv6-enabled smart objects (6LoWPAN), proprietary systems including TI 15.4-Stack (2.4-GHz), and concurrent multiprotocol through a Dynamic Multiprotocol Manager (DMM) driver. The device is optimized for low-power wireless communication and advanced sensing in building security systems, HVAC, medical, wired networking, portable electronics, and home theater & entertainment markets.

BDE-MP2674R10 module series can support +5 dBm output power and a receive sensitivity of -104 dBm for 125-kbps Bluetooth® Low Energy Coded PHY. It is with low standby current of 0.92 µA with full 256 KB RAM retention that enables longer battery life wireless applications. The module series supports for ARM® TrustZone® based secure key storage, device ID and trusted functions; Low SER (Soft Error Rate) FIT (Failure-in-time) for long operational lifetime with no disruption for industrial markets with always-on SRAM parity against corruption due to potential radiation events. The device also has an autonomous ultra-low power Sensor Controller CPU with fast wake-up capability. As an example, the sensor controller is capable of 1-Hz ADC sampling at 1-µA system current.

BDE-MP2674R10 module series integrates all required system-level hardware components including clocks, balun filter, other passives, and PCB trace antenna or U.FL connector into a small PCB form factor. It is for easy assembly and low-cost PCB design. It can work standalone with integrated powerful Arm® Cortex®-M33 for a wide range of applications without the need of external MCU. With its best-in-class radio performance, ultra-low power, small form factor and low cost, the BDE-MP2674R10 module series is the best choice for the applications that are sensitive to power consumption, size and cost.

Table 1. Module Variants

Orderable Part Number	Antenna Option	Integrated On-board SPI Flash	Operating Temperature
BDE-MP2674R10A32	PCB trace antenna	32-Mbit	-40℃ to +85℃
BDE- MP2674R10U32	U.FL connector	32-Mbit	-40℃ to +85℃
BDE- MP2674R10N32	ANT pin	32-Mbit	-40℃ to +85℃
BDE- MP2674R10A0	PCB trace antenna	Not included	-40℃ to +85℃
BDE- MP2674R10U0	U.FL connector	Not included	-40℃ to +85℃
BDE- MP2674R10N0	ANT pin	Not included	-40℃ to +85℃

Key Features

- **Wireless microcontroller**
  - Powerful 48-MHz Arm® Cortex®- M33 processor with TrustZone®
  - FPU and DSP extension
  - 1024 KB flash program memory
  - 8 KB of cache SRAM
  - 256 KB of ultra-low leakage SRAM with parity for high-reliability operation
    - 32 kB of additional SRAM is available if parity is disabled
  - Integrated 32-Mbit SPI flash
    - BDE-MP2674R10A32
    - BDE- MP2674R10U32
    - BDE- MP2674R10N32
  - Dynamic multiprotocol manager (DMM) driver
  - Programmable radio includes support for 2-(G)FSK, 4-(G)FSK, MSK, Bluetooth® 5.3 Low Energy, IEEE 802.15.4 PHY and MAC
  - Supports over-the-air upgrade (OTA)
- **Ultra-low power sensor controller**
  - Autonomous MCU with 4 KB of SRAM
  - Sample, store, and process sensor data
  - Fast wake-up for low-power operation
  - Software defined peripherals, capacitive touch, flow meter, LCD
- **Low power consumption**
  - MCU consumption:
    - 4.0 mA active mode, CoreMark®
    - 83 µA/MHz running CoreMark®
    - 1.19 µA standby mode, RTC, 256 KB RAM
    - 0.13 µA shutdown mode, wake-up on pin
  - Ultra low-power sensor controller consumption:
    - 30 µA in 2 MHz mode
    - 809 µA in 24 MHz mode
  - Radio Consumption:
    - 6.4 mA RX
    - 7.3 mA TX at 0 dBm
    - 9.8 mA TX at +5 dBm
- **Wireless protocol support**
  - Thread, Zigbee®, Matter
  - Bluetooth® 5.3 Low Energy
  - SimpleLink™ TI 15.4-stack
  - 6LoWPAN
  - Proprietary systems
- **High performance radio**
  - -104 dBm for Bluetooth® Low Energy 125-kbps
  - – 105 dBm for IEEE 802.15.4-2006 2.4 GHz OQPSK (coherent modem)
- **Qualification and Regulatory**
  - Bluetooth SIG
  - FCC
  - IC
  - CE-RED
- **MCU peripherals**
  - Most digital peripherals can be routed to any GPIO
  - Four 32-bit or eight 16-bit general-purpose timers
  - 12-bit SAR ADC, 200 kSamples/s, 8 channels
  - 8-bit DAC
  - Two comparators
  - Programmable current source
  - Four UART, four SPI, two I^2C, I^2S
  - Real-time clock (RTC)
  - Integrated temperature and battery monitor
  - 31 GPIOs – none SPI flash versions
  - 27 GPIOs – SPI flash versions
- **Security enablers**
  - Supports secure boot
  - Supports secure key storage and device ID
  - Arm TrustZone for trusted execution environment
  - AES 128- and 256-bit cryptographic accelerator
  - ECC and RSA public key hardware accelerator
  - SHA2 Accelerator (full suite up to SHA-512)
  - True random number generator (TRNG)
  - Secure debug lock
  - Software anti-rollback protection
- **Operating range**
  - On-chip buck DC/DC converter

- 1.8 V to 3.8 V single supply voltage – None SPI flash variants
- 2.3V to 3.8V single supply voltage- SPI flash variants
- -40 to +85°C

- **Package**
  - Dimension: 21.5 mm x 15 mm x 2.15 mm
  - LCC-36 – BDE-MP2674R10A
  - LCC-39 – BDE-MP2674R10U and BDE-MP2674R10N
  - RoHS-compliant package
- **Antenna**
  - Integrated ceramic chip antenna: BDE-MP2674R10A32/BDE- MP2674R10A0
  - Integrated U.FL connector for connecting external antenna： BDE- MP2674R10U32/BDE-MP2674R10U0
  - ANT pin out for connecting external antenna - BDE- MP2674R10N32/BDE- MP2674R10N0:
- **Additional integrated components**
  - 48.0-MHz HFXT
  - 32.768-kHz LFXT
  - 32-Mbit SPI flash
    - BDE- MP2674R10A32
    - BDE- MP2674R10U32
    - BDE- MP2674R10N32
  - RF filter and passive components

Applications

- 2400 to 2480 MHz ISM and SRD systems with down to 4 kHz of receive bandwidth
- Building automation
  - Building security systems – motion detector, electronic smart lock, door and window sensor, garage door system, gateway
  - HVAC – thermostat, wireless environmental sensor, HVAC system controller, gateway
  - Fire safety system – smoke and heat detector, fire alarm control panel (FACP)
  - Video surveillance – IP network camera
  - Elevators and escalators – elevator main control panel for elevators and escalators
- Industrial transport – asset tracking
- Factory automation and control
- Medical
  - Personal care & fitness
  - Patient monitoring & diagnostics – medical sensor patches, multiparameter patient monitor
  - Medical equipment
  - Home healthcare – blood glucose monitor, pulse oximeter
- Electronic point of sale (EPOS) – Electronic Shelf Label (ESL)
- Communication equipment
- Wired networking – wireless LAN or Wi-Fi access points, edge router
- Personal electronics
  - Portable electronics – RF smart remote control
  - Home theater & entertainment – smart speakers, smart display, set-top box
  - Connected peripherals – consumer wireless keypads
  - Gaming – electronic and robotic toys
  - Wearables (non-medical) – smart trackers, smart clothing

Reference

[1] CC2674R10 resources: https://www.ti.com/product/CC2674R10

Contents

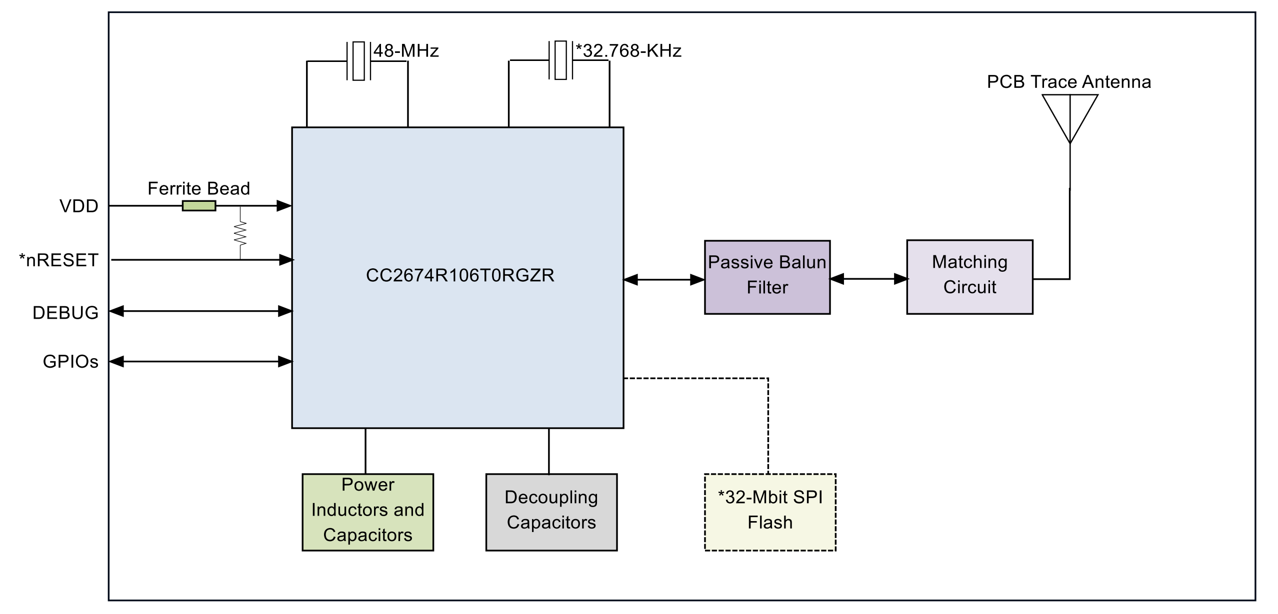
1. System Overview

1.1. Block Diagram

BDE-MP2674R10 module series is based on the Taxes Instruments' CC2674R10 single chip wireless MCU. With clocks, other required passives and antenna/connector (optional) integrated, it allows faster time to market at reduced development cost.

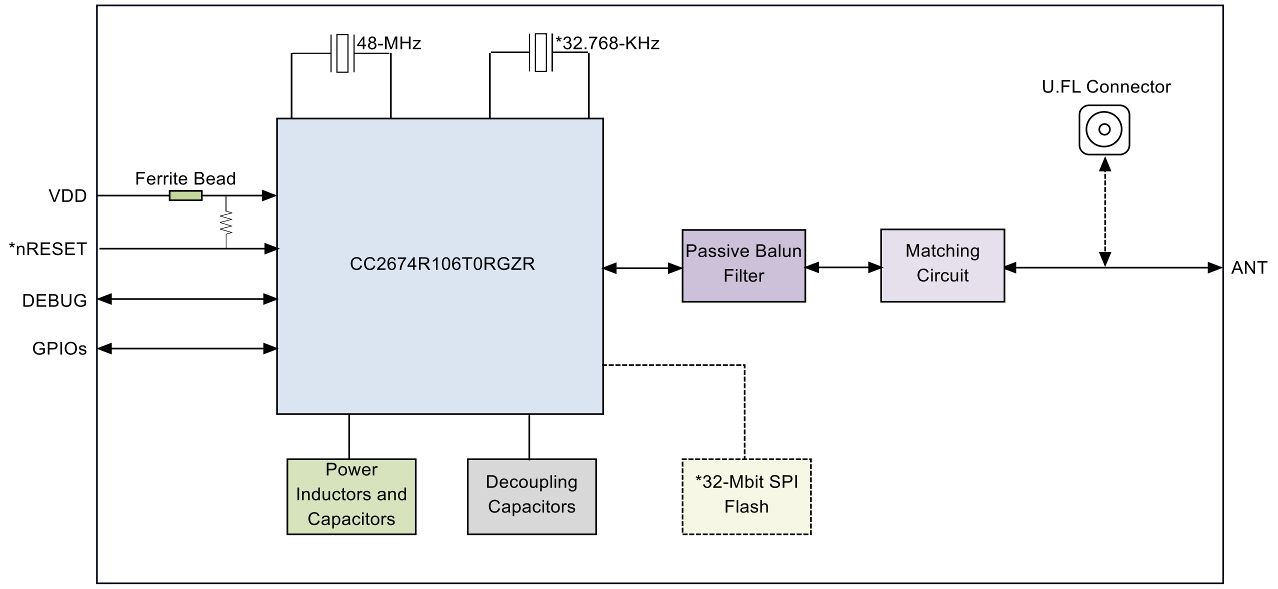
The block diagram of the module series can be seen in Figure 1 and Figure 2, comprises of:

- 48-MHz HFXT
- 32.768-kHz LFXT
- 32-Mbit SPI flash (SPI flash variants)
- Power inductors and capacitors
- Pull-up resistor
- Passive balun filter
- Decoupling capacitors
- Matching circuit
- PCB trace antenna / U.FL connector for external antenna / ANT pin out for external antenna



Note:
(1) This block diagram is for BDE-MP2674R10A;
(2) The 32-Mbit SPI flash is only for SPI flash variants;
(3) Reset pin has an internal pull-up resistor and a decoupling capacitor.

Figure 1. The block diagram of BDE-MP2674R10A



Note:
1. This block diagram is for BDE-MP2674R10U and BDE-MP2674R10N;
2. The 32-Mbit SPI flash is only for SPI flash variants;
3. The U.FL connector is only included in module BDE-MP2674R10U;
4. Reset pin has an internal pull-up resistor and a decoupling capacitor.

Figure 2. The block diagram of BDE-MP2674R10U and BDE-MP2674R10N

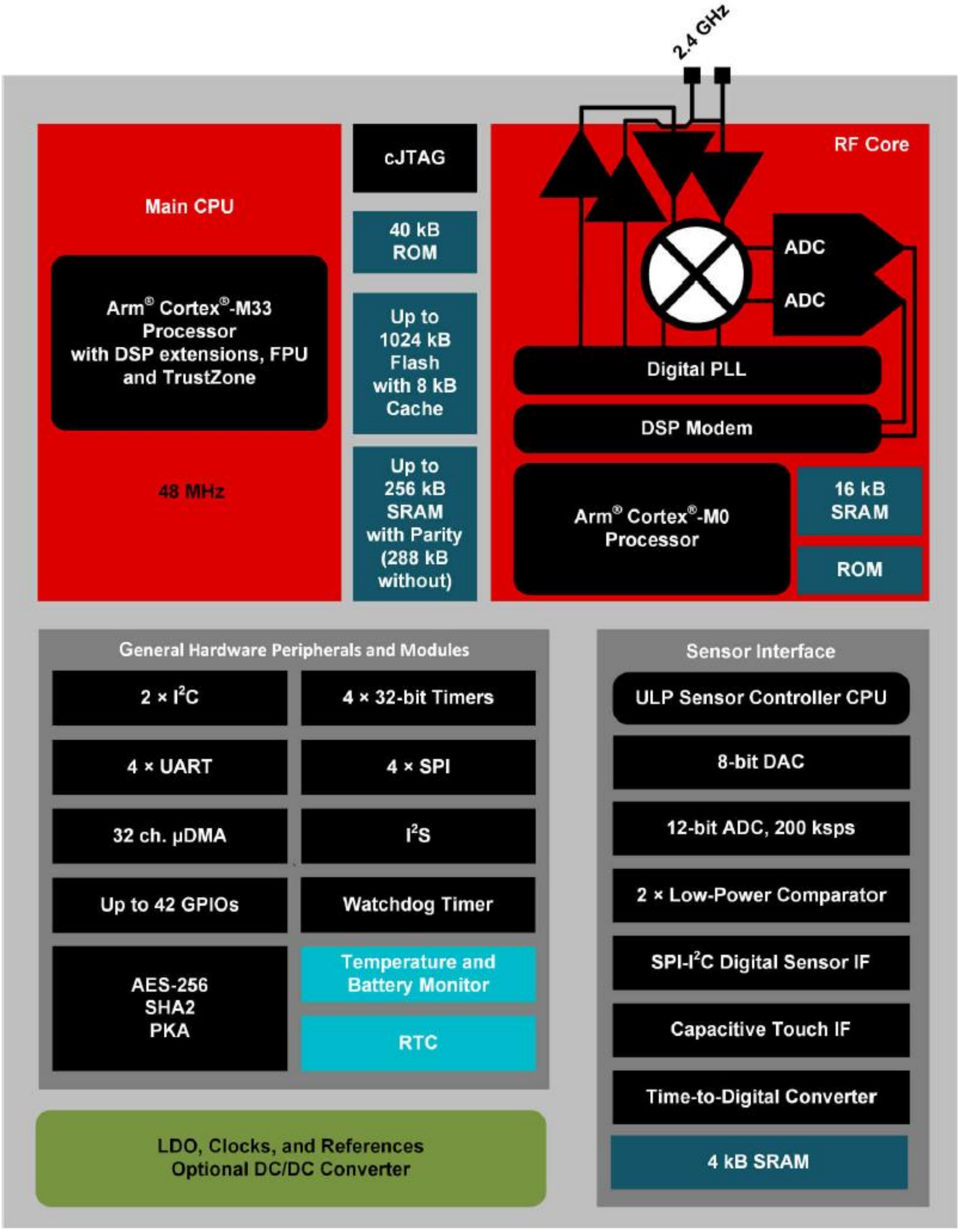


Figure 3. The block diagram of CC2674R10 (Adopted from CC2674R10 Datasheet)

1.2. System CPU

The BDE-MP2674R10 module series utilizes CC2674R10 SimpleLink™ Wireless MCU. The MCU contains an Arm® Cortex®-M33 system CPU with TrustZone®, which runs the application and the higher layers of radio protocol stacks. The system CPU is the foundation of a high-performance, low-cost platform that meets the system requirements of minimal memory implementation, and low-power consumption, while delivering outstanding computational performance and exceptional system response to interrupts.

Its features include the following:

- ARMv8-M architecture with TrustZone® security extension optimized for small-footprint embedded applications
- Arm Thumb®-2 mixed 16- and 32-bit instruction set delivers the high performance expected of a 32-bit Arm core in a compact memory size
- 8 regions of non-secure memory protected regions
- 8 regions of secure memory protected regions
- 4 regions of Security Attribute Unit (SAU)
- Single-cycle multiply instruction and hardware divide
- Digital-signal-processing (DSP) extension
- IEEE 754-compliant single-precision Floating Point Unit (FPU)
- Fast code execution permits increased sleep mode time
- Deterministic, high-performance interrupt handling for time-critical applications
- Full debug with data matching for watchpoint generation
  - Data Watchpoint and Trace Unit (DWT)
  - JTAG Debug Access Port (DAP)
  - Flash Patch and Breakpoint Unit (FPB)
- Trace support reduces the number of pins required for debugging and tracing
  - Instrumentation Trace Macrocell Unit (ITM)
  - Trace Port Interface Unit (TPIU) with asynchronous serial wire output (SWO)
- Optimized for single-cycle flash memory access
- Tightly connected to 8 kB 4-way random replacement cache for minimal active power consumption and wait states
- Ultra-low-power consumption with integrated sleep modes
- 48 MHz operation

1.3. Radio (RF Core)

The RF Core is a highly flexible and future proof radio module which contains an Arm Cortex-M0 processor that interfaces the analog RF and base-band circuitry, handles data to and from the system CPU side, and assembles the information bits in a given packet structure. The RF core offers a high level, command-based API to the main CPU that configurations and data are passed through. The Arm Cortex-M0 processor is not programmable by customers and is interfaced through the TI-provided RF driver that is included with the SimpleLink Software Development Kit (SDK).

The RF core can autonomously handle the time-critical aspects of the radio protocols, thus offloading the main CPU, which reduces power and leaves more resources for the user application. Several signals are also available to control external circuitry such as RF switches or range extenders autonomously.

The various physical layer radio formats are partly built as a software defined radio where the radio behavior is either defined by radio ROM contents or by non-ROM radio formats delivered in form of firmware patches with the SimpleLink SDKs. This allows the radio platform to be updated for support of future versions of standards even with over-the-air (OTA) updates while still using the same silicon.

1.3.1. Bluetooth 5.3 Low Energy

The RF Core offers full support for Bluetooth 5.3 Low Energy, including the high-speed 2 Mbps physical layer and the 500 kbps and 125 kbps long range PHYs (Coded PHY) through the TI provided Bluetooth 5.3 stack or through a high-level Bluetooth API. The Bluetooth 5.3 PHY and part of the controller are in radio and system ROM, providing significant savings in memory usage and more space available for applications.

The new high-speed mode allows data transfers up to 2 Mbps, twice the speed of Bluetooth 4.2 and five times the speed of Bluetooth 4.0, without increasing power consumption. In addition to faster speeds, this mode offers significant improvements for energy efficiency and wireless coexistence with reduced radio communication time.

Bluetooth 5.3 also enables unparalleled flexibility for adjustment of speed and range based on application needs, which capitalizes on the high-speed or long-range modes respectively. Data transfers are now possible at 2 Mbps, enabling development of applications using voice, audio, imaging, and data logging that were not previously an option using Bluetooth low energy. With high-speed mode, existing applications deliver faster responses, richer engagement, and longer battery life. Bluetooth 5.3 enables fast, reliable firmware updates.

1.3.2. 802.15.4 Thread, Zigbee, and 6LoWPAN

Through a dedicated IEEE radio API, the RF Core supports the 2.4-GHz IEEE 802.15.4-2011 physical layer (2 Mchips per second Offset-QPSK with DSSS 1:8), used in Thread, Zigbee, and 6LoWPAN protocols. The 802.15.4 PHY and MAC are in radio and system ROM. TI also provides royalty-free protocol stacks for Thread and Zigbee as part of the SimpleLink SDK, enabling a robust end-to-end solution.

1.4. Memory

The up to 1024 KB nonvolatile (Flash) memory provides storage for code and data. The flash memory is in-system programmable and erasable. The last flash memory sector must contain a Customer Configuration section (CCFG) that is used by boot ROM and TI provided drivers to configure the device. This configuration is done through the ccfg.c source file that is included in all TI provided examples.

The ultra-low leakage system static RAM (SRAM) is split into up to eight 32 kB blocks and can be used for both storage of data and execution of code. Retention of SRAM contents in Standby power mode is enabled by default and included in Standby mode power consumption numbers. Parity checking for detection of bit errors in memory is built-in, which reduces chip-level soft errors and thereby increases reliability. Parity can be disabled for an additional 32 kB which can be allocated for general purpose SRAM. System SRAM is always initialized to zeroes upon code execution from boot.

To improve code execution speed and lower power when executing code from nonvolatile memory, a 4-way nonassociative 8 kB cache is enabled by default to cache and prefetch instructions read by the system CPU. The cache can be used as a general-purpose RAM by enabling this feature in the Customer Configuration Area (CCFG).

There is a 4 kB ultra-low leakage SRAM available for use with the Sensor Controller Engine which is typically used for storing Sensor Controller programs, data and configuration parameters. This RAM is also accessible by the system CPU. The Sensor

Controller RAM is not cleared to zeroes between system resets.

The ROM includes a TI-RTOS kernel and low-level drivers, as well as significant parts of selected radio stacks, which frees up flash memory for the application. The ROM also contains a serial (SPI and UART) bootloader that can be used for initial programming of the device.

The module also provides an option with integrated an on-board 32-Mbit SPI flash for the applications that need to store big application data.

1.5. Sensor Controller

The Sensor Controller contains circuitry that can be selectively enabled in both Standby and Active power modes. The peripherals in this domain can be controlled by the Sensor Controller Engine, which is a proprietary power-optimized CPU. This CPU can read and monitor sensors or perform other tasks autonomously; thereby significantly reducing power consumption and offloading the system CPU.

The Sensor Controller Engine is user programmable with a simple programming language that has syntax similar to C. This programmability allows for sensor polling and other tasks to be specified as sequential algorithms rather than static configuration of complex peripheral modules, timers, DMA, register programmable state machines, or event routing.

The main advantages are:

- Flexibility - data can be read and processed in unlimited manners while still ensuring ultra-low power.
- 2 MHz low-power mode enables lowest possible handling of digital sensors
- Dynamic reuse of hardware resources
- 40-bit accumulator supporting multiplication, addition and shift
- Observability and debugging options

Typical use cases may be (but are not limited to) the following:

- Read analog sensors using integrated ADC or comparators
- Interface digital sensors using GPIOs, SPI, UART, or I2C (UART and I2C are bit-banged)
- Capacitive sensing
- Waveform generation
- Very low-power pulse counting (flow metering)
- Key scan

The peripherals in the Sensor Controller include the following:

- The low-power clocked comparator can be used to wake the system CPU from any state in which the comparator is active. A configurable internal reference DAC can be used in conjunction with the comparator. The output of the comparator can also be used to trigger an interrupt or the ADC.
- Capacitive sensing functionality is implemented through the use of a constant current source, a time-to-digital converter, and a comparator. The continuous time comparator in this block can also be used as a higher accuracy alternative to the low-power clocked comparator. The Sensor Controller takes care of baseline tracking, hysteresis, filtering, and other related functions when these modules are used for capacitive sensing.

- The ADC is a 12-bit 200 ksps ADC with eight inputs and a built-in voltage reference. The ADC can be triggered by many different sources including timers, I/O pins, software, and comparators.
- The analog modules can connect to up to eight different GPIOs.
- Dedicated SPI master with up to 6 MHz clock speed.

The peripherals in the Sensor Controller can also be controlled from the main application processor.

1.6. Cryptography

The device comes with a wide set of modern cryptography-related hardware accelerator, drastically reducing code footprint and execution time for cryptographic operations. It also has the benefit of being lower power and improves availability and responsiveness of the system because the cryptography operations run in a background hardware thread.

Together with a large selection of open-source cryptography libraries provided with the Software Development Kit (SDK), this allows for secure and future proof IoT applications to be easily built on top of the platform. The hardware accelerator modules are:

- **True Random Number Generator (TRNG)** module provides a true, nondeterministic noise source for the purpose of generating keys, initialization vectors (IVs), and other random number requirements. The TRNG is built on 24 ring oscillators that create unpredictable output to feed a complex nonlinear-combinatorial circuit.
- **Secure Hash Algorithm 2 (SHA-2)** with support for SHA224, SHA256, SHA384, and SHA512.
- **Advanced Encryption Standard (AES)** with 128, 192 and 256 bit key lengths.
- **Public Key Accelerator** - Hardware accelerator supporting mathematical operations needed for elliptic curves up to 512 bits.

Through use of these modules and the TI provided cryptography drivers, the following capabilities are available for application or stack:

- Key Agreement Schemes
- Signature Processing
- Curve Support
- Message Authentication Codes
- Block cipher mode of operation
- Hash Algorithm
- True random number generation

Other capabilities, such as RSA encryption and signatures (using keys as large as 2048 bits) as well as other ECC curves such as Curve1174, can be implemented using the provided public key accelerator but are not part of the TI SimpleLink SDK for the device.

1.7. Timers

A large selection of timers are available as part of the device. These timers are:

- Real-Time Clock (RTC)
- General Purpose Timers (GPTIMER)

- Sensor Controller Timers
- Radio Timer
- Watchdog timer
- Always On Watchdog timer (AON_WDT)

1.8. Serial Peripherals and I/O

The SPI interface provides a standardized synchronous serial interface to communicate with devices compatible with SPI (3 and 4 wire), MICROWIRE and TI Synchronous Serial Format. The SPIs support master/slave operation up to 12 MHz, programmable clock bit rate with prescaler, as well as configurable phase and polarity.

The UART interface implements universal asynchronous receiver and transmitter functions. The UART supports flexible baud-rate generation up to a maximum of 3 Mbps with FIFO, multiple data sizes, stop and parity bits as well as hardware handshake.

The I^2S interface provides a standardized interface to exchange digital audio with devices compatible with this standard, including ADCs, DACs and CODECs. The I^2S can also receive pulse-density modulation (PDM) data from devices such as digital microphones and perform conversion to PCM data.

The I^2C interface enables low speed serial communications with devices compatible with the I^2C standard. The I^2C interface can handle both standard (100 kHz) and fast (400 kHz) speeds, as well as four modes of operation: master transmit/receive and slave transmit/receive.

The I/O controller (IOC) controls the digital I/O pins and contains multiplexer circuitry to allow a set of peripherals to be assigned to I/O pins in a flexible manner. All digital I/Os are interrupt and wake-up capable, have a programmable pullup and pulldown function, and can generate an interrupt on a negative or positive edge (configurable). When configured as an output, pins can function as either push-pull or open-drain. Five GPIOs have high-drive capabilities, which are marked in bold in Section 2.1. All digital peripherals can be connected to any digital pin on the device.

1.9. Battery and Temperature Monitor

A combined temperature and battery voltage monitor is available in the device. The battery and temperature monitor allows an application to continuously monitor on-chip temperature and supply voltage and respond to changes in environmental conditions as needed. The module contains window comparators to interrupt the system CPU when temperature or supply voltage go outside defined windows. These events can also be used to wake up the device from Standby mode through the Always-On (AON) event fabric.

1.10. µDMA

The device includes a direct memory access (µDMA) controller. The µDMA controller provides a way to offload data-transfer tasks from the system CPU, thus allowing for more efficient use of the processor and the available bus bandwidth. The µDMA controller can perform a transfer between memory and peripherals. The µDMA controller has dedicated channels for each supported on-chip module and can be programmed to automatically perform transfers between peripherals and memory when the peripheral is ready to transfer more data.

1.11. Debug

The debug subsystem implements two IEEE standards for debug and test purposes:

IEEE 1149.7 Class 4: Reduced-pin and Enhanced-functionality Test Access Port and Boundary-scan Architecture. This is known by the acronym cJTAG (compact JTAG) and this device uses only two pins to communicate to the target: TMS (JTAG_TMSC) and TCK (JTAG_TCKC). This is the default mode of operation.

IEEE standard 1149.1: Test Access Port and Boundary Scan Architecture Test Access Port (TAP). This standard is known by the acronym JTAG and this device uses four pins to communicate to the target: TMS (JTAG_TMSC), TCK (JTAG_TCKC), TDI (JTAG_TDI) and TDO (JTAG_TDO).

The debug subsystem also implements a user-configurable firewall to control unauthorized access to debug/test ports.

1.12. Clock

The module has the following internal system clocks.

SCLK_MF is an internal 2 MHz clock that is used by the Sensor Controller in low-power mode and also for internal power management circuitry. The SCLK_MF clock is always driven by the internal 2 MHz RC Oscillator (RCOSC_MF).

SCLK_LF is the 32.768 kHz internal low-frequency system clock. It can be used by the Sensor Controller for ultra-low-power operation and is also used for the RTC and to synchronize the radio timer before or after Standby power mode. SCLK_LF can be driven by the internal 32.8 kHz RC Oscillator (RCOSC_LF), a 32.768 kHz watch-type crystal, or a clock input on any digital IO.

When using a crystal or the internal RC oscillator, the device can output the 32 kHz SCLK_LF signal to other devices, thereby reducing the overall system cost.

The module includes two crystals on board, a high frequency crystal (HFXT) with 48-MHz and a low frequency crystal (LFXT) with 32.768-KHz. The characteristics for two crystals can be found in Section 3.

1.13. Network Processor

Depending on the product configuration, the module device can function as a wireless network processor (WNP - a device running the wireless protocol stack with the application running on a separate host MCU), or as a system-on-chip (SoC) with the application and protocol stack running on the system CPU inside the device. In the first case, the external host MCU communicates with the device using SPI or UART. In the second case, the application must be written according to the application framework supplied with the wireless protocol stack.

1.14. Power Management

To minimize power consumption, the CC2674R10 supports a number of power modes and power management features (see Table 2).

Table 2. Power Mode

Mode	Software Configurable Power Modes (1)				Reset Pin Held
	Active	Idle	Standby	Shutdown	
CPU	Active	Off	Off	Off	Off
Flash	On	Available	Off	Off	Off
SRAM	On	On	Retention	Off	Off
Supply System	On	On	Duty Cycled	Off	Off
Register and CPU retention	Full	Full	Partial	No	No
SRAM retention	Full	Full	Full	Off	Off
48 MHz high-speed clock (SCLK_HF)	or RCOSC_HF	or RCOSC_HF	Off	Off	Off
2 MHz medium-speed clock (SCLK_MF)	RCOSC_MF	RCOSC_MF	Available	Off	Off
32 kHz low-speed clock (SCLK_LF)	XOSC_LF or RCOSC_LF	XOSC_LF or RCOSC_LF	XOSC_LF or RCOSC_LF	Off	Off
Peripherals	Available	Available	Off	Off	Off
Sensor Controller	Available	Available	Available	Off	Off
Wake-up on RTC	Available	Available	Available	Off	Off
Wake-up on pin edge	Available	Available	Available	Available	Off
Wake-up on reset pin	On	On	On	On	On
Brownout detector (BOD)	On	On	Duty Cycled	Off	Off
Power-on reset (POR)	On	On	On	Off	Off
Watchdog timer (WDT)	Available	Available	Paused	Off	Off
Always-on Watchdog timer (AON_WDT)	Available	Available	Available	Off	Off

In the Active mode, the application system CPU is actively executing code. Active mode provides normal operation of the processor and all of the peripherals that are currently enabled. The system clock can be any available clock source (see Table 2).

In Idle mode, all active peripherals can be clocked, but the Application CPU core and memory are not clocked and no code is executed. Any interrupt event brings the processor back into active mode.

In Standby mode, only the always-on (AON) domain is active. An external wake-up event, RTC event, or Sensor Controller event is required to bring the device back to active mode. MCU peripherals with retention do not need to be reconfigured when waking up again, and the CPU continues execution from where it went into standby mode. All GPIOs are latched in standby mode.

In Shutdown mode, the device is entirely turned off (including the AON domain and Sensor Controller), and the I/Os are latched with the value they had before entering shutdown mode. A change of state on any I/O pin defined as a wake from shutdown pin wakes up the device and functions as a reset trigger. The CPU can differentiate between reset in this way and reset-by-reset pin or power-on reset by reading the reset status register. The only state retained in this mode is the latched I/O state and the flash memory contents.

The Sensor Controller is an autonomous processor that control the peripherals in the Sensor Controller indepently of the system CPU. This means that the system CPU does not have to wake up, for example to perform an ADC sampling or poll a digital sensor over SPI, thus saving both current and wake-up time that would otherwise be wasted. The Sensor Controller Studio tool enables the user to program the Sensor Controller, control its peripherals, and wake up the system CPU as needed. All Sensor Controller peripherals can also be controlled by the system CPU.

The power, RF and clock management for the CC2674R10 device require specific configuration and handling by software for optimized performance. This configuration and handling is implemented in the TI-provided drivers that are part of the CC2674R10 software development kit (SDK). Therefore, BDE highly recommends using this software framework for all application development on the device. The complete SDK with TI-RTOS (optional), device drivers, and examples are offered free of charge in source code.

1.15. Antenna

The module series provides three different types of antenna integration, integrated PCB trace antenna, U.FL connector and ANT pin for connecting external antenna. Detail characteristics for the antennas can be found in Section 3.

Note: For more details, refer to the CC2674R10 SimpleLink™ Arm® Cortex®-M33 multiprotocol 2.4-GHz wireless MCU with 1-MB flash;

2. Pinout Functions

The module series is with LGA-36 package, 36 pas are exposed for user. This section describes pinout functions of the module in details.

2.1. Pinout Diagram

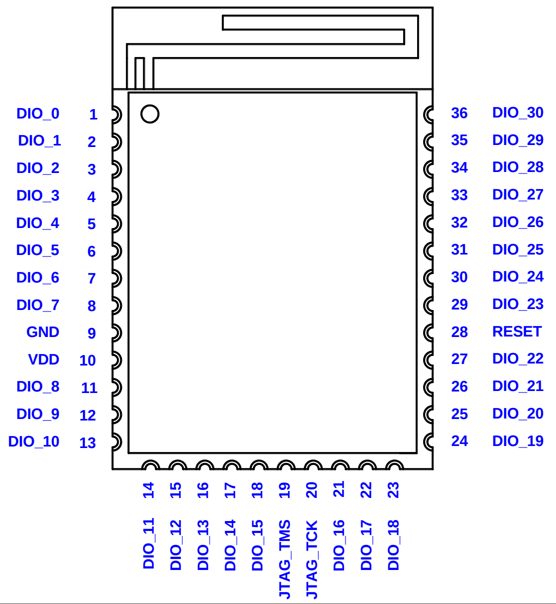


Figure 4. Pinout Diagram of BDE-MP2674R10A Top View

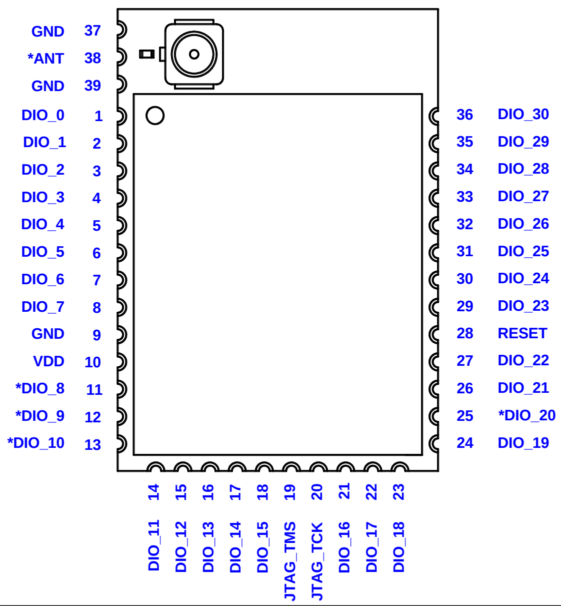


Figure 5. Pinout Diagram of BDE-MP2674R10U and BDE-MP2674R10N Top View

The following I/O pins marked in Figure 4 in **bold** have high-drive capabilities:
- Pin 6, DIO5
- Pin 7, DIO6
- Pin 8, DIO7
- Pin 19, JTAG_TMS
- Pin 21, DIO16
- Pin 22, DIO17

The following I/O pins marked in Figure 5 in *italics* have analog capabilities:
- Pin 29, DIO23
- Pin 30, DIO24
- Pin 31, DIO25
- Pin 32, DIO26
- Pin 33, DIO27
- Pin 34, DIO28
- Pin 35, DIO29
- Pin 36, DIO30

The following four I/O pins are assigned to on-board 32-Mbit SPI flash for SPI flash variants series:
- Pin 11, SFL_MISO_DIO8
- Pin 12, SFL_MOSI_DIO9
- Pin 13, SFL_CLK_DIO10
- Pin 25, SFL_CS_DIO20

Notes on the pin diagram:
1. Pin 38 is for connecting external antenna for BDE-MP2674R10N, if U.FL versions BDE-MP2674R10U are selected, leave this pin NC.

2.2. Pinout Descriptions

Table 3 describes the definitions of the pins of the module. Pin number of CC2674R10 chip is also stated here, because the chip pin is referred to in the software design kit (SDK).

Table 3. Pin Description (1)

Module Pin #	Pin Name	Type	CC2674R106T0RGZR Pin #	Description
1	DIO_0	I/O	5	GPIO
2	DIO_1	I/O	6	GPIO
3	DIO_2	I/O	7	GPIO
4	DIO_3	I/O	8	GPIO
5	DIO_4	I/O	9	GPIO
6	DIO_5	I/O	10	GPIO, high-drive capability
7	DIO_6	I/O	11	GPIO, high-drive capability
8	DIO_7	I/O	12	GPIO, high-drive capability
9	GND	Ground	-	Power ground

Module Pin #	Pin Name	Type	CC2674R106T0RGZR Pin #	Description
10	VDD	Power	-	Power supply
11	DIO_8	I/O	14	SFL_MISO(2), GPIO
12	DIO_9	I/O	15	SFL_MOSI(2), GPIO
13	DIO_10	I/O	16	SFL_SCLK(2), GPIO
14	DIO_11	I/O	17	GPIO
15	DIO_12	I/O	18	GPIO
16	DIO_13	I/O	19	GPIO
17	DIO_14	I/O	20	GPIO
18	DIO_15	I/O	21	GPIO
19	JTAG_TMS	I/O	24	JTAG TMSC, high-drive capability
20	JTAG_TCK	I	25	JTAG TCKC
21	DIO_16	I/O	26	GPIO, JTAG_TDO, high-drive capability
22	DIO_17	I/O	27	GPIO, JTAG_TDI, high-drive capability
23	DIO_18	I/O	28	GPIO
24	DIO_19	I/O	29	GPIO
25	DIO_20	I/O	30	SFL_CS(2), GPIO
26	DIO_21	I/O	31	GPIO
27	DIO_22	I/O	32	GPIO
28	RESET	I	35	Reset, active-low, 100K ohm internal pull-up resistor
29	DIO_23	I/O	36	GPIO, analog capability
30	DIO_24	I/O	37	GPIO, analog capability
31	DIO_25	I/O	38	GPIO, analog capability
32	DIO_26	I/O	39	GPIO, analog capability
33	DIO_27	I/O	40	GPIO, analog capability
34	DIO_28	I/O	41	GPIO, analog capability
35	DIO_29	I/O	42	GPIO, analog capability
36	DIO_30	I/O	43	GPIO, analog capability
37(3)	GND	Ground	-	Power ground
38(3)	ANT	RF	-	Antenna port
39(3)	GND	Ground	-	Power ground

Note (1): For pin multiplexing details, refer to CC2674R10 SimpleLink™ Arm® Cortex®-M33 multiprotocol 2.4-GHz wireless MCU with 1-MB flash;
Note (2): These four pins can be used as GPIOs in none SPI flash variants modules BDE-MP2674R10A0, BDE- MP2674R10U0 and BDE - MP2674R10N0; these four pins are used as SPI for on-board 32-Mbit flash in SPI flash variants modules BDE- MP2674R10A32, BDE- MP2674R10U32 and BDE- MP2674R10N32;
Note (3): Pin 37, Pin 38 and Pin 39 are only included in BDE-MP2674R10U and BDE-MP2674R10N.

2.3. Connections for Unused Pins

Table 4. Connections for Unused Pins

Function	Signal Name	Acceptable Practice	Proffered Practice
GPIO (Digital or analog)	DIOn	NC or GND	NC

3. Specifications

3.1. Electrical Characteristics

3.1.1. Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Over operating free-air temperature range (unless otherwise noted).

Table 5. Absolute Maximum Ratings

Parameter	MIN	MAX	Unit	Note
VDD, Supply voltage	-0.3	4.1	V	
Voltage on any digital pins	-0.3	VDDS+0.3≤4.1	V	Including DIOs with analog capability
Voltage on ADC input	-0.3	VDDS	V	Voltage scaling enabled
	-0.3	1.49	V	Voltage scaling disabled, internal reference
	-0.3	VDD/2.9	V	Voltage scaling disabled, VDD as reference
Input level, for ANT pin (Pin38)		5	dBm	For –N variants
T_{STG}, Storage temperature	-40	125	°C	

3.1.2. ESD Ratings

Table 3. ESD Ratings

Parameter	Description	Value	Unit	Note
Electrostatic discharge	Contact discharge	4000	V	As per EN 301-489
	Air discharge	8000	V	As per EN 301-489

3.1.3. Recommended Operating Conditions

Operation at or near maximum operating temperature for extended durations will result in a reduction in lifetime.

Over operating free-air temperature range (unless otherwise noted).

Table 4. Recommended Operating Conditions

Parameter	MIN	TYP	MAX	Unit	Note
VDD, Supply voltage	1.8	3.3	3.8	V	
	2.3	3.3	3.8	V	For SPI flash variants
T_A, Operating Temperature	-40	25	85	°C	

Rising supply voltage slew rate	0		100	mV/µs	
Falling supply voltage slew rate	0		20	mV/µs	

3.1.4. Power Consumption

The measurement is made with the evaluation module (EM board) for BDE-MP2674R10 with T_A = 25 °C, VDD = 3.0 V, DCDC enabled, GLDO disabled, unless otherwise noted.

Table 5. Power Consumption – Power Modes

Power Mode	Test Condition	TYP	Unit
Reset	Reset. RESET pin asserted or VDD below power-on-reset threshold	150	nA
Shutdown	Shutdown. No clocks running, no retention	128.6	nA
Standby without cache retention	RTC running, CPU, 256 kB RAM and (partial) register retention. RCOSC_LF	1.06	uA
	RTC running, CPU, 128 kB RAM and (partial) register retention. RCOSC_LF	0.96	uA
	RTC running, CPU, 256 kB RAM and (partial) register retention. XOSC_LF	1.19	uA
	RTC running, CPU, 128 kB RAM and (partial) register retention. XOSC_LF	1.09	uA
Standby with cache retention	RTC running, CPU, 256 kB RAM and (partial) register retention. RCOSC_LF	2.55	uA
	RTC running, CPU, 128 kB RAM and (partial) register retention. RCOSC_LF	2.45	uA
	RTC running, CPU, 256 kB RAM and (partial) register retention. XOSC_LF	2.66	uA
	RTC running, CPU, 128 kB RAM and (partial) register retention. XOSC_LF	2.57	uA
Idle	Supply Systems and RAM powered RCOSC_HF	720.9	uA
Active	MCU running CoreMark at 48 MHz with parity enabled RCOSC_HF	4.13	mA
	MCU running CoreMark at 48 MHz with parity disabled RCOSC_HF	3.97	mA
Peripheral, power domain	Delta current with domain enabled	74.0	uA
Peripheral, Serial power domain	Delta current with domain enabled	6.89	uA
Peripheral, RF Core	Delta current with power domain enabled, clock enabled, RF core idle	120.4	uA
Peripheral, µDMA	Delta current with clock enabled, module is idle	68.2	uA
Peripheral, Timers	Delta current with clock enabled, module is idle	115.4	uA
Peripheral, I2C	Delta current with clock enabled, module is idle	11.5	uA
Peripheral, I2S	Delta current with clock enabled, module is idle	26.1	uA
Peripheral, SPI	Delta current with clock enabled, module is idle	65.9	uA
Peripheral, UART	Delta current with clock enabled, module is idle	135.1	uA
Peripheral, CRYPTO (AES)	Delta current with clock enabled, module is idle	18.6	uA
Peripheral, PKA	Delta current with clock enabled, module is idle	79.3	uA
Peripheral, TRNG	Delta current with clock enabled, module is idle	24.69	uA
Sensor Controller Engine, Active	24 MHz, infinite loop	808.5	uA
Sensor Controller Engine, Low-power	2 MHz, infinite loop	30.1	uA

Table 6. Power Consumption – Radio Modes

Power Mode	Test Condition	TYP	Unit
Radio receive current	2440 MHz, Bluetooth Low Energy	6.4	mA
Radio transmit current	0 dBm output power setting 2440 MHz, Bluetooth Low Energy	7.3	mA
	+5 dBm output power setting 2440 MHz, Bluetooth Low Energy	9.8	mA

3.1.5. Clock Characteristics

Table 7. 48-MHz Crystal Oscillator (XOSC_HF) Characteristics

Parameter	Test Condition	MIN	TYP	MAX	Unit
Crystal frequency			48		MHz
ESR, Equivalent series resistance					Ω
Frequency tolerance	T_A: 25°C	-10		+10	ppm
Frequency stability	T_A: -40°C ~ 85°C	-30		+30	ppm
C_L, Crystal load capacitance			7		pF

Table 8. 32.768-KHz Crystal Oscillator (XOSC_LF) Characteristics

Parameter	Test Condition	MIN	TYP	MAX	Unit
Crystal frequency			32.768		KHz
ESR, Equivalent series resistance					Ω
Frequency tolerance	T_A: 25°C	-20		+20	ppm
Frequency stability	T_A: -40°C ~ 85°C	-30		+30	ppm
C_L, Crystal load capacitance			12.5		pF

3.1.6. Reset Timing

Table 9. Reset Timing

Parameter	MIN	TYP	MAX	Unit
nRESET low duration	1			us

3.1.7. UART Characteristics

Measured over operating free-air temperature range (unless otherwise noted)

Table 10. UART Characteristics

Parameter	MIN	TYP	MAX	Unit
UART baud rate			3	MBaud

3.1.8. SPI Characteristics

Measured over operating free-air temperature range (unless otherwise noted)

Table 11. SPI Characteristics

Parameter	Test Condition	MIN	TYP	MAX	Unit
SPI clock frequency	Primary Mode 1.71 < VDD < 3.8			12	MHz

	Secondary Mode 2.7 < VDD < 3.8			8	
	Secondary Mode VDD < 2.7			7	
SPI duty cycle		45	50	55	%

For timing characteristics or other details, please refer to CC2674R10 datasheet: CC2674R10 SimpleLink™ Arm® Cortex®-M33 multiprotocol 2.4-GHz wireless MCU with 1-MB flash.

3.1.9. GPIO DC Characteristics

Table 12. GPIO DC Characteristics

Parameter	Test Condition	MIN	TYP	MAX	Unit
TA = 25 °C, VDDS = 1.8 V					
GPIO VOH at 8 mA load	IOCURR = 2, high-drive GPIOs only		1.56		V
GPIO VOL at 8 mA load	IOCURR = 2, high-drive GPIOs only		0.24		V
GPIO VOH at 4 mA load	IOCURR = 1		1.59		V
GPIO VOL at 4 mA load	IOCURR = 1		0.21		V
GPIO pullup current	Input mode, pullup enabled, Vpad = 0 V		73		µA
GPIO pulldown current	Input mode, pulldown enabled, Vpad = VDDS		19		µA
GPIO low-to-high input transition, with hysteresis	IH = 1, transition voltage for input read as 0 → 1		1.08		V
GPIO high-to-low input transition, with hysteresis	IH = 1, transition voltage for input read as 1 → 0		0.73		V
GPIO input hysteresis	IH = 1, difference between 0 → 1 and 1 → 0 points		0.35		V
TA = 25 °C, VDDS = 3.0 V					
GPIO VOH at 8 mA load	IOCURR = 2, high-drive GPIOs only		2.59		V
GPIO VOL at 8 mA load	IOCURR = 2, high-drive GPIOs only		0.42		V
GPIO VOH at 4 mA load	IOCURR = 1		2.63		V
GPIO VOL at 4 mA load	IOCURR = 1		0.40		V
TA = 25 °C, VDDS = 3.8 V					
GPIO pullup current	Input mode, pullup enabled, Vpad = 0 V		282		µA
GPIO pulldown current	Input mode, pulldown enabled, Vpad = VDDS		110		µA
GPIO low-to-high input transition, with hysteresis	IH = 1, transition voltage for input read as 0 → 1		1.97		V
GPIO high-to-low input transition, with hysteresis	IH = 1, transition voltage for input read as 1 → 0		1.55		V
GPIO input hysteresis	IH = 1, difference between 0 → 1 and 1 → 0 points		0.42		V
TA = 25 °C					
VIH	Lowest GPIO input voltage reliably interpreted as a High	0.8*VDDS			V
VIL	Highest GPIO input voltage reliably interpreted as a Low			0.2*VDDS	V

3.1.10. ADC Characteristics

Table 12. ADC Characteristics

Parameter	Test Condition	MIN	TYP	MAX	Unit
Resolution			12		bit

Parameter	Test Condition	MIN	TYP	MAX	Unit
Input voltage range		0		VDD	V
Reference voltage	Equivalent fixed internal reference (input voltage scaling enabled). For best accuracy, the ADC conversion should be initiated through the TI-RTOS API in order to include the gain/offset compensation factors stored in FCFG1		4.3		V
Reference voltage	Fixed internal reference (input voltage scaling disabled). For best accuracy, the ADC conversion should be initiated through the TI-RTOS API in order to include the gain/offset compensation factors stored in FCFG1. This value is derived from the scaled value (4.3 V) as follows: Vref = 4.3 V × 1408 / 4095		1.48		V
Reference voltage	VDD as reference, input voltage scaling enabled		VDD		V
	VDD as reference, input voltage scaling disabled		VDD/2.82		V
Sampling rate				200	ksps

For more details on the ADC characteristic, please refer to CC2674R10 datasheet: CC2674R10 SimpleLink™ Arm® Cortex®-M33 multiprotocol 2.4-GHz wireless MCU with 1-MB flash.

3.1.11. DAC Characteristics

Table 12. DAC Characteristics

Parameter	Test Condition	MIN	TYP	MAX	Unit
Resolution			8		bit
Supply voltage	Any load, any VREF, pre-charge OFF, DAC charge-pump ON	1.8		3.8	V
	External Load, any VREF, pre-charge OFF, DAC charge-pump OFF	2.0		3.8	V
	Any load, VREF = DCOUPL, pre-charge ON	2.6		3.8	V

Parameter	Test Condition	MIN	TYP	MAX	Unit
Clock frequency	Buffer ON (recommended for external load)	16		250	kHz
	Buffer OFF (internal load)	16		1000	kHz

For more details on the ADC characteristic, please refer to CC2674R10 datasheet: CC2674R10 SimpleLink™ Arm® Cortex®-M33 multiprotocol 2.4-GHz wireless MCU with 1-MB flash.

3.1.12. Comparator Characteristics

T_C = 25 °C, V_{DDS} = 3.0 V, unless otherwise noted.

Parameter	Test Condition	MIN	TYP	MAX	Unit
Input voltage range		0		VDD	V
Clock frequency			32		KHz
Internal reference voltage	Using internal DAC with VDDS as reference voltage, DAC code = 0 - 255	0.024		2.865	V
Offset	Measured at VDDS / 2, includes error from internal DAC		±5		mV
Decision time	Step from –50 mV to 50 mV		1		Clock Cycle

3.2. RF Characteristics

The measurement is made with the evaluation module (EM board) for BDE-MP2674R10 with T_A = 25 °C, VDD = 3.0 V, DCDC enabled, GLDO disabled, unless otherwise noted.

3.2.1. Receive (RX) Characteristics – Bluetooth Low Energy 125 Kbps (LE Coded)

Table 13. Receive (RX) Characteristics – Bluetooth Low Energy 125 Kbps (LE Coded)

Parameter	Test Condition	TYP	Unit
Receiver sensitivity	BER = 10^{-3}	-102	dBm
Receiver situation	BER = 10^{-3}	5	dBm
Co-channel rejection (1)	Wanted signal at –67 dBm, modulated interferer in channel, BER = 10^{-3}	-6	dB
Selectivity, ±1 MHz (1)	Wanted signal at –67 dBm, modulated interferer at ±1 MHz, BER = 10^{-3}	9 / 5	dB
Selectivity, ±2 MHz (1)	Wanted signal at –67 dBm, modulated interferer at ±2 MHz, BER = 10^{-3}	44 / 31	dB
Selectivity, ±3 MHz (1)	Wanted signal at –67 dBm, modulated interferer at ±3 MHz, BER = 10^{-3}	47 / 42	dB
Selectivity, ±4 MHz (1)	Wanted signal at –67 dBm, modulated interferer at ±4 MHz, BER = 10^{-3}	49 / 45	dB
Selectivity, image frequency	Wanted signal at –67 dBm, modulated interferer at image frequency, BER = 10^{-3}	31	dB
Selectivity, image frequency ±1 MHz	Note that Image frequency + 1 MHz is the Co- channel –1 MHz. Wanted signal at –67 dBm, modulated interferer at ±1 MHz from image frequency, BER = 10^{-3}	5 / 38	dB

Note [(1)]: For pin

3.2.2. Receive (RX) Characteristics – Bluetooth Low Energy 500 Kbps (LE Coded)

Table 14. Receive (RX) Characteristics – Bluetooth Low Energy 500 Kbps (LE Coded)

Parameter	Test Condition	TYP	Unit
Receiver sensitivity	BER = 10^{-3}	-99	dBm
Receiver situation	BER = 10^{-3}	5	dBm
Co-channel rejection	Wanted signal at –67 dBm, modulated interferer in channel, BER = 10^{-3}	-4.5	dB
Selectivity, ±1 MHz	Wanted signal at –67 dBm, modulated interferer at ±1 MHz, BER = 10^{-3}	9 / 5	dB
Selectivity, ±2 MHz	Wanted signal at –67 dBm, modulated interferer at ±2 MHz, BER = 10^{-3}	42 / 31	dB
Selectivity, ±3 MHz	Wanted signal at –67 dBm, modulated interferer at ±3 MHz, BER = 10^{-3}	45 / 41	dB
Selectivity, ±4 MHz	Wanted signal at –67 dBm, modulated interferer at ±4 MHz, BER = 10^{-3}	46 / 42	dB
Selectivity, image frequency	Wanted signal at –67 dBm, modulated interferer at image frequency, BER = 10^{-3}	31	dB
Selectivity, image frequency ±1 MHz	Note that Image frequency + 1 MHz is the Co- channel –1 MHz. Wanted signal at –67 dBm, modulated interferer at ±1 MHz from image frequency, BER = 10^{-3}	5 / 41	dB

3.2.3. Receive (RX) Characteristics – Bluetooth Low Energy 1 Mbps (LE 1M)

Table 15. Receive (RX) Characteristics – Bluetooth Low Energy 1 Mbps (LE 1M)

Parameter	Test Condition	TYP	Unit
Receiver sensitivity	BER = 10^{-3}	-96.5	dBm
Receiver situation	BER = 10^{-3}	5	dBm
Co-channel rejection	Wanted signal at –67 dBm, modulated interferer in channel, BER = 10^{-3}	-6	dB
Selectivity, ±1 MHz	Wanted signal at –67 dBm, modulated interferer at ±1 MHz, BER = 10^{-3}	7 / 5	dB
Selectivity, ±2 MHz	Wanted signal at –67 dBm, modulated interferer at ±2 MHz, BER = 10^{-3}	39 / 28	dB
Selectivity, ±3 MHz	Wanted signal at –67 dBm, modulated interferer at ±3 MHz, BER = 10^{-3}	44 / 38	dB
Selectivity, ±4 MHz	Wanted signal at –67 dBm, modulated interferer at ±4 MHz, BER = 10^{-3}	47 / 35	dB
Selectivity, image frequency	Wanted signal at –67 dBm, modulated interferer at image frequency, BER = 10^{-3}	28	dB
Selectivity, image frequency ±1 MHz	Note that Image frequency + 1 MHz is the Co- channel –1 MHz. Wanted signal at –67 dBm, modulated interferer at ±1 MHz from image frequency, BER = 10^{-3}	5 / 38	dB
Out-of-band blocking	30 MHz to 2000 MHz	-10	dBm
Out-of-band blocking	2003 MHz to 2399 MHz	-10	dBm
Out-of-band blocking	2484 MHz to 2997 MHz	-10	dBm
Out-of-band blocking	3000 MHz to 12.75 GHz (excluding VCO frequency)	-2	dBm
Intermodulation	Wanted signal at 2402 MHz, –64 dBm. Two interferers at 2405 and 2408 MHz respectively, at the given power level	-37	dBm

3.2.4. Receive (RX) Characteristics – Bluetooth Low Energy 2 Mbps (LE 2M)

Table 16. Receive (RX) Characteristics – Bluetooth Low Energy 2 Mbps (LE 2M)

Parameter	Test Condition	TYP	Unit
Receiver sensitivity	BER = 10^{-3}	-92	dBm
Receiver situation	BER = 10^{-3}	2	dBm
Co-channel rejection	Wanted signal at –67 dBm, modulated interferer in channel, BER = 10^{-3}	-8	dB
Selectivity, ±2 MHz	Wanted signal at –67 dBm, modulated interferer at ±2 MHz, BER = 10^{-3}	9 / 5	dB
Selectivity, ±4 MHz	Wanted signal at –67 dBm, modulated interferer at ±4 MHz, BER = 10^{-3}	40 / 32	dB
Selectivity, ±6 MHz	Wanted signal at –67 dBm, modulated interferer at ±6 MHz, BER = 10^{-3}	46 / 40	dB
Selectivity, image frequency	Wanted signal at –67 dBm, modulated interferer at image frequency, BER = 10^{-3}	5	dB
Selectivity, image frequency ±1 MHz	Note that Image frequency + 1 MHz is the Co- channel –1 MHz. Wanted signal at –67 dBm, modulated interferer at ±1 MHz from image frequency, BER = 10^{-3}	-8 / 32	dB
Out-of-band blocking	30 MHz to 2000 MHz	-10	dBm
Out-of-band blocking	2003 MHz to 2399 MHz	-10	dBm
Out-of-band blocking	2484 MHz to 2997 MHz	-12	dBm
Out-of-band blocking	3000 MHz to 12.75 GHz (excluding VCO frequency)	-10	dBm
Intermodulation	Wanted signal at 2402 MHz, –64 dBm. Two interferers at 2405 and 2408 MHz respectively, at the given power level	-38	dBm

3.2.5. Transmit (TX) Characteristics – Bluetooth Low Energy

The measurement is made with the evaluation module (EM board) for BDE-MP2674R10 with TA = 25 °C, VDD = 3.0 V, fRF = 2440 MHz, DCDC enabled, GLDO disabled, unless otherwise noted.

Table 17. Transmit (TX) Characteristics

Parameter	Test Condition	TYP	Unit
Max output power	Conducted output from ANT pin of the module	8	dBm
Output power programmable range	Conducted output from ANT pin of the module	28	dB
Spurious emissions and harmonics			
			dBm

4. Mechanical Specifications

5. Dimensions

The following pages include mechanical, footprint drawings, and marking information. This information is the most current data available for the designated devices.

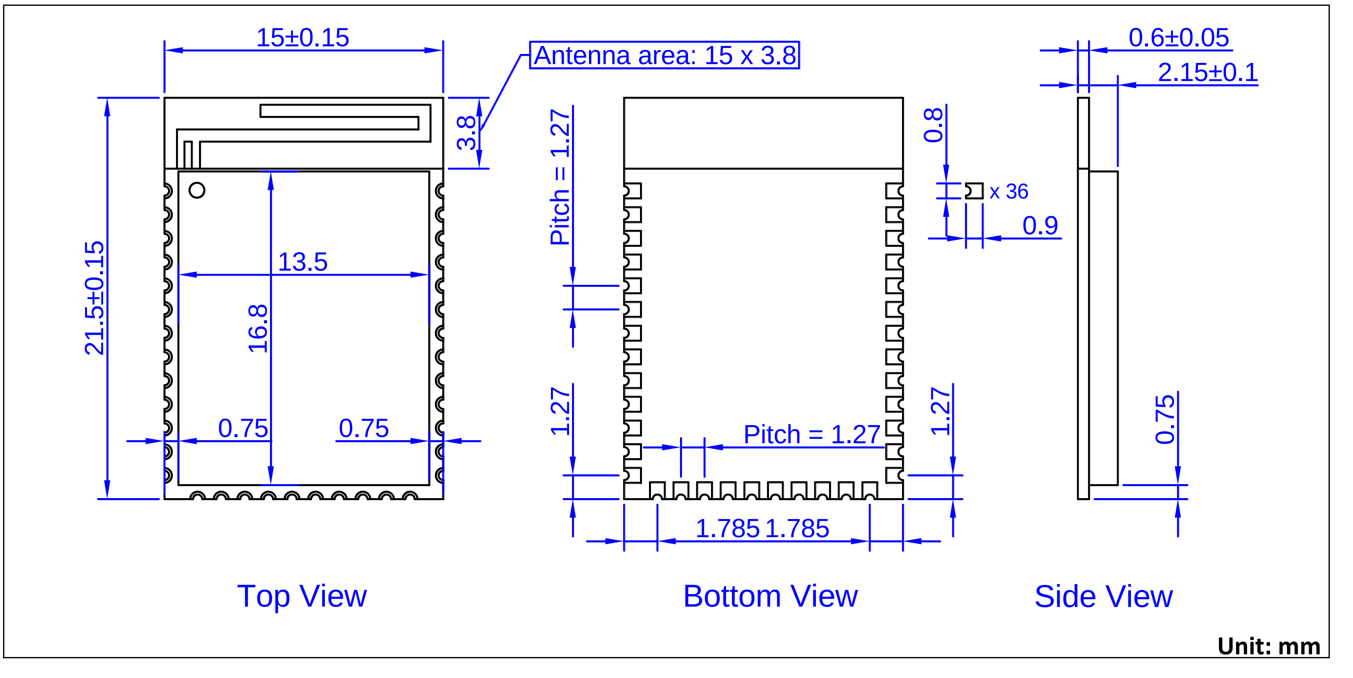


Figure 5. Mechanical Drawing of BDE-MP2674R10A

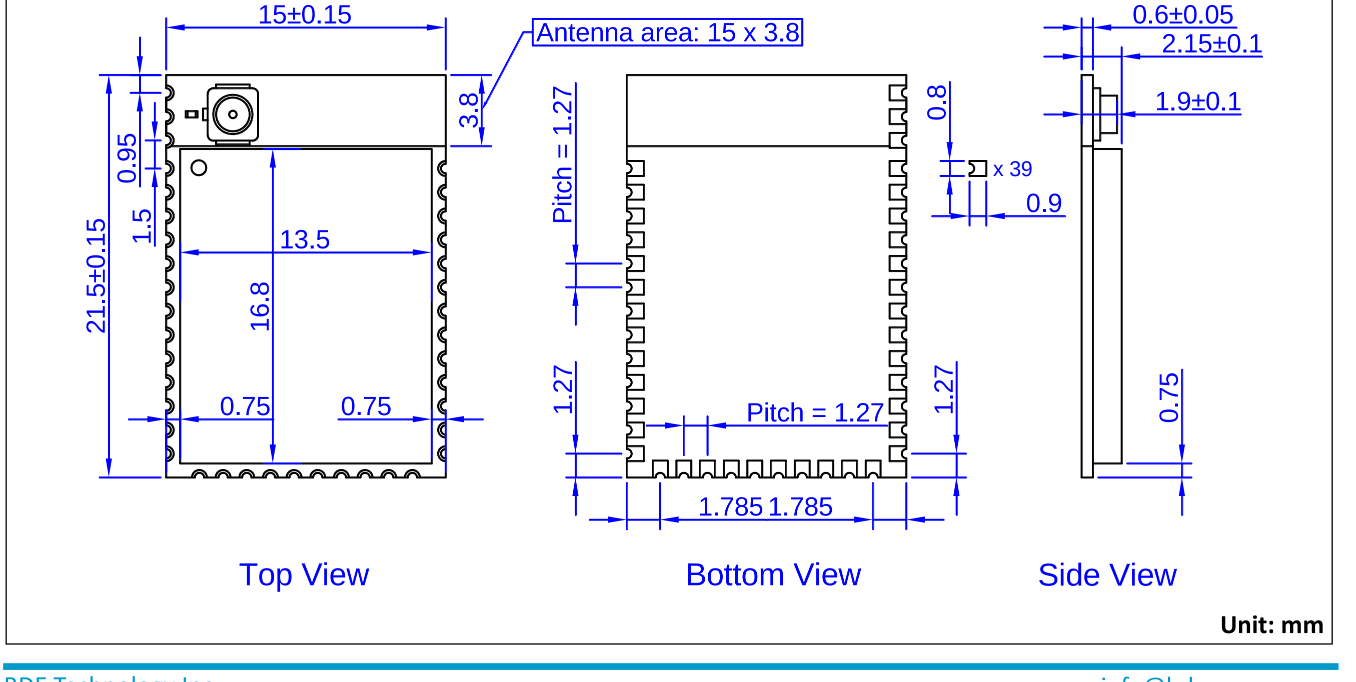
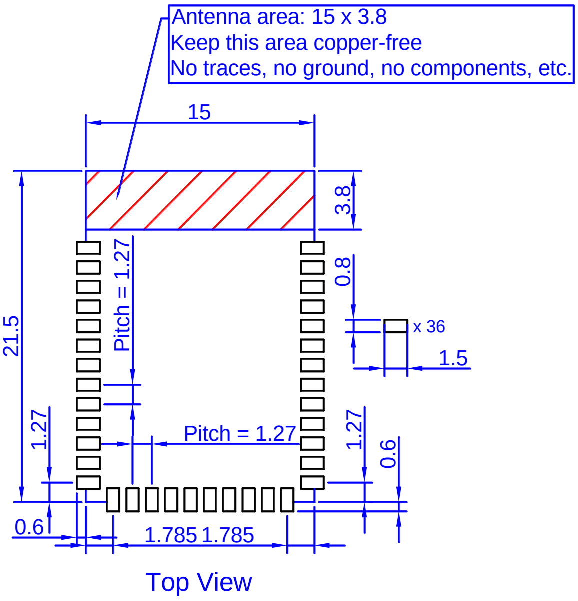


Figure 6. Mechanical Drawing of BDE-MP2674R10U and BDE-MP2674R10N

6. PCB Footprint

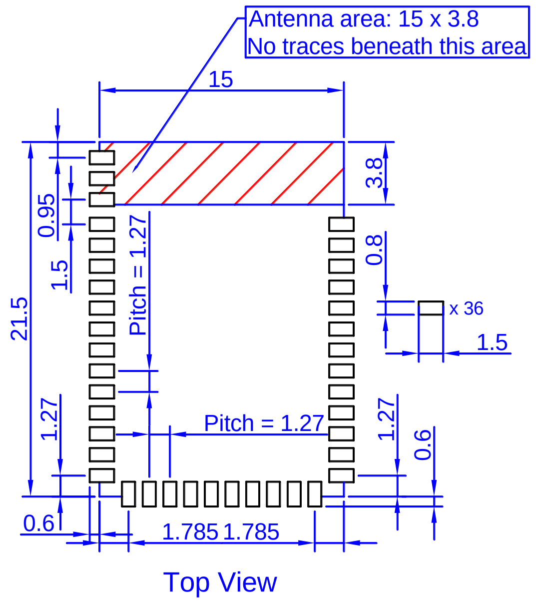


Note:

1. Solder mask should be the same or 5% larger than the dimension of the pad;
2. Solder paste must be the same as the pin for all peripheral pads.

Unit: mm

Figure 7. Recommended Module Footprint of BDE-MP2674R10A



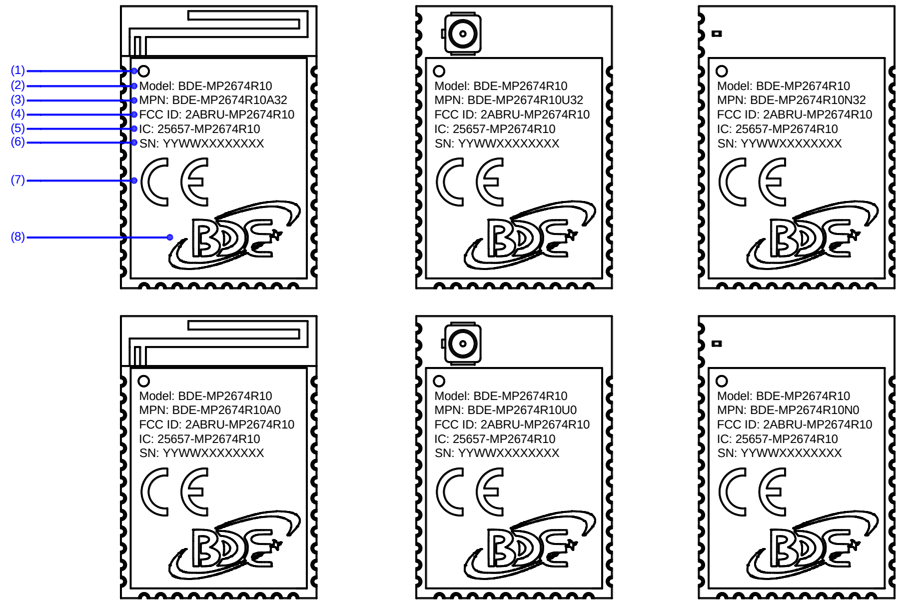
Note:

1. Solder mask should be the same or 5% larger than the dimension of the pad;
2. Solder paste must be the same as the pin for all peripheral pads.

Unit: mm

Figure 8. Recommended Module Footprint of BDE-MP2674R10U and BDE-MP2674R10N

7. Marking

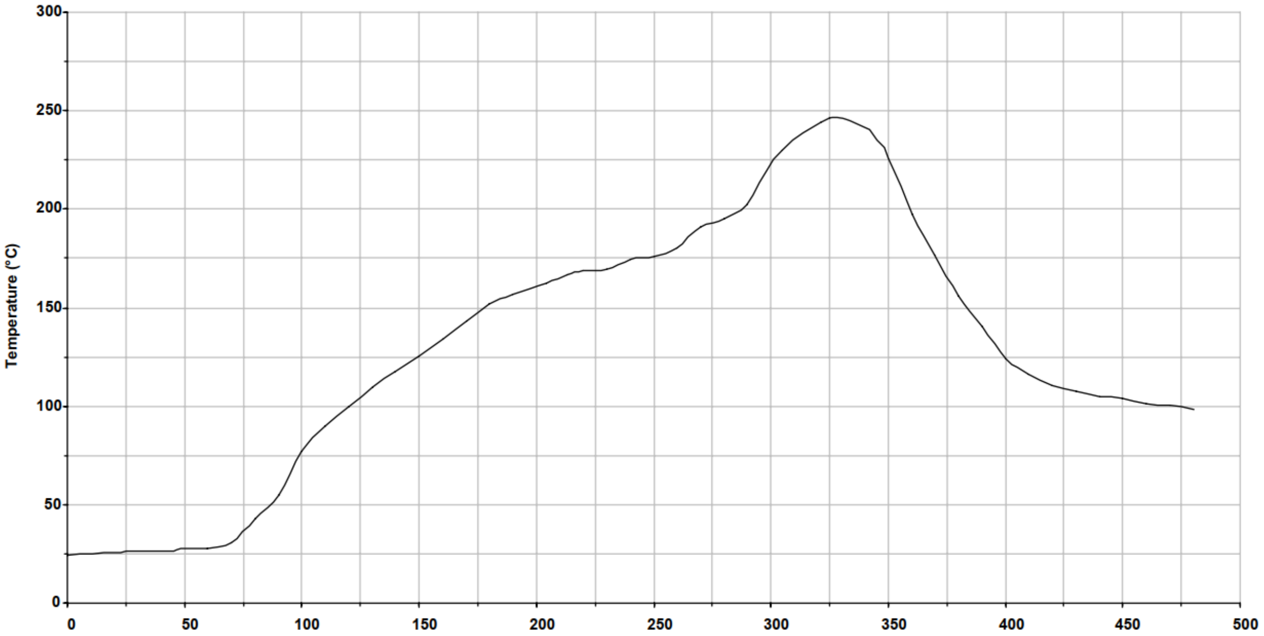


(1) Pin one index;

(2) Model series;
(3) Orderable manufacturer part number;
(4) FCC ID;
(5) IC ID;
(6) Serial number;
(7) CE marking;
(8) BDE logo

Figure 9. Module Marking

8. Typical Reflow Profile



Key features of the profile:

- Initial ramp = 1-2.5°C/sec to 175°C ±25°C equilibrium;
- Equilibrium time = 60 to 180 seconds;
- Ramp to maximum temperature (245°C) = 3°C/sec max;
- Time above liquidus temperature (217°C): 45-90 seconds;
- Device absolute maximum reflow temperature: 260°C.

Figure 10. Typical Reflow Profile

9. Ordering Information

Part Number	Size (mm)	Core Chip	Shipping Form	MOQ
BDE-MP2674R10A0	21.5 × 15 × 2.15	CC2674R10	Tape & Reel	1K
BDE-MP2674R10A32	21.5 × 15 × 2.15	CC2674R10	Tape & Reel	1K
BDE-MP2674R10U0	21.5 × 15 × 2.15	CC2674R10	Tape & Reel	1K
BDE-MP2674R10U32	21.5 × 15 × 2.15	CC2674R10	Tape & Reel	1K
BDE-MP2674R10N0	21.5 × 15 × 2.15	CC2674R10	Tape & Reel	1K
BDE-MP2674R10N32	21.5 × 15 × 2.15	CC2674R10	Tape & Reel	1K

10. Revision History

Revision	Date	Description
V0.1	25-September-2022	Preliminary, draft

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