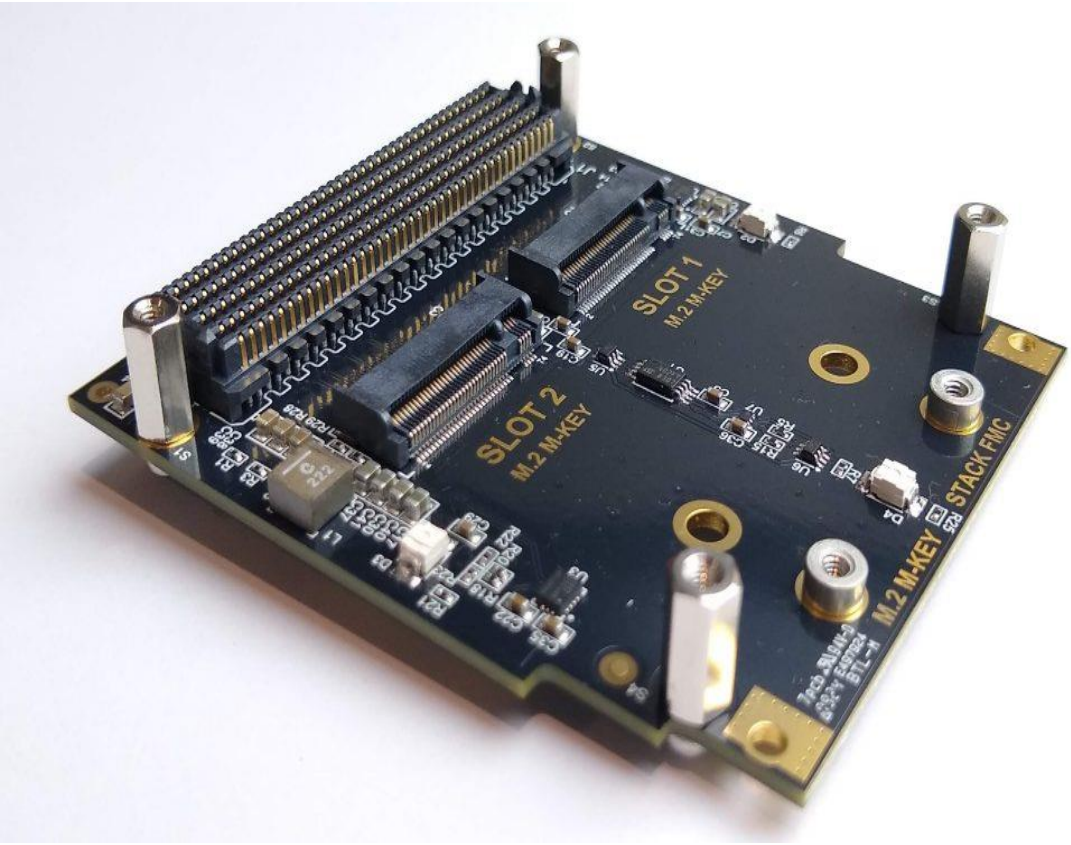
M.2 M-key Stack FMC

Overview

Description

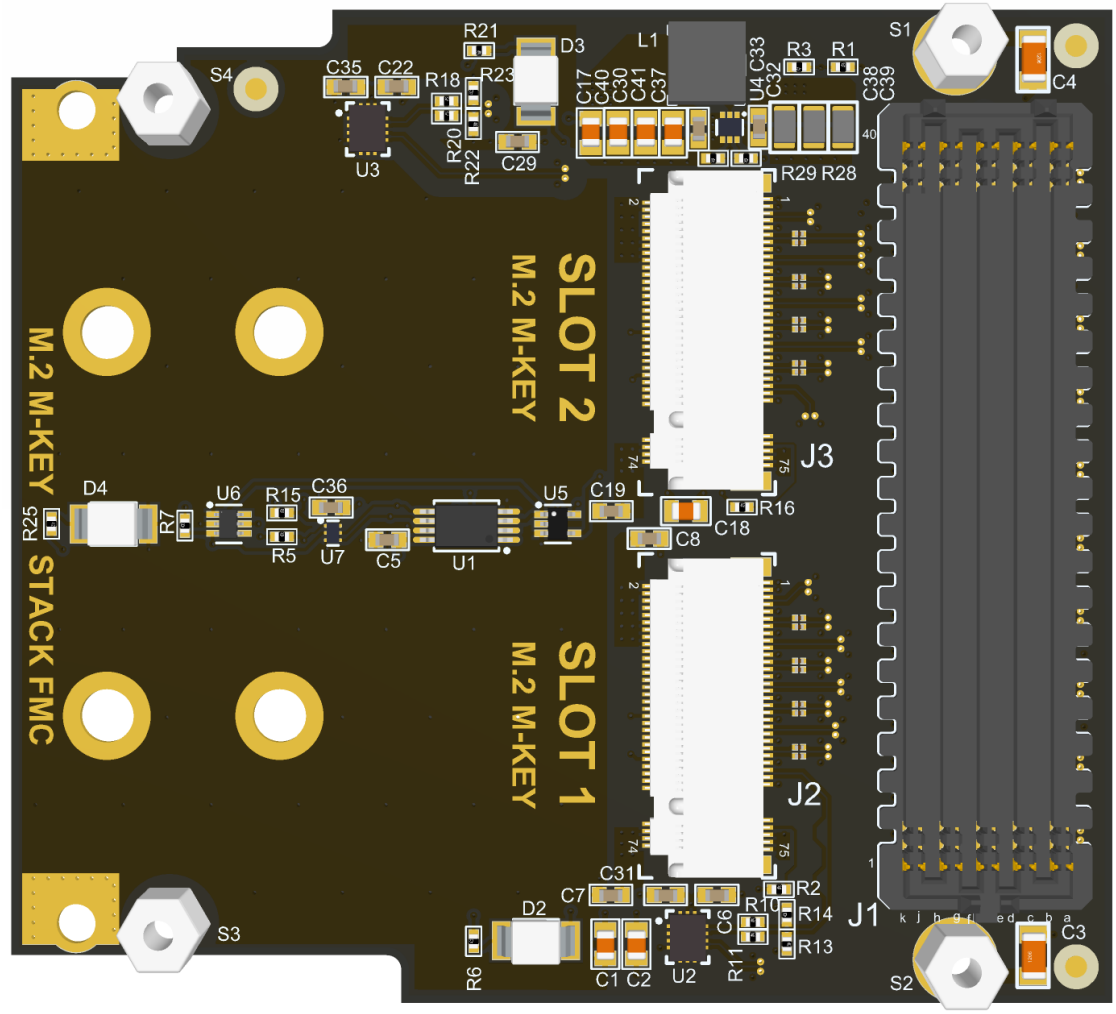
M.2 M-key Stack FMC is an adapter that allows 2x M.2 M-key PCIe modules to be connected to FPGA and MPSoC based development boards. The adapter uses the FPGA Mezzanine Card (FMC) form factor for connection with FPGA and MPSoC development boards via the FMC connector. It has 2x M-key M.2 sockets and can carry M.2 M-key PCIe modules of length 30mm and 42mm without extension, and 60mm, 80mm or 110mm with extension. Each M.2 slot has its own independent connection to the FPGA for maximum throughput and can support a 4-lane PCIe connection up to Gen4.



M.2 M-key Stack FMC

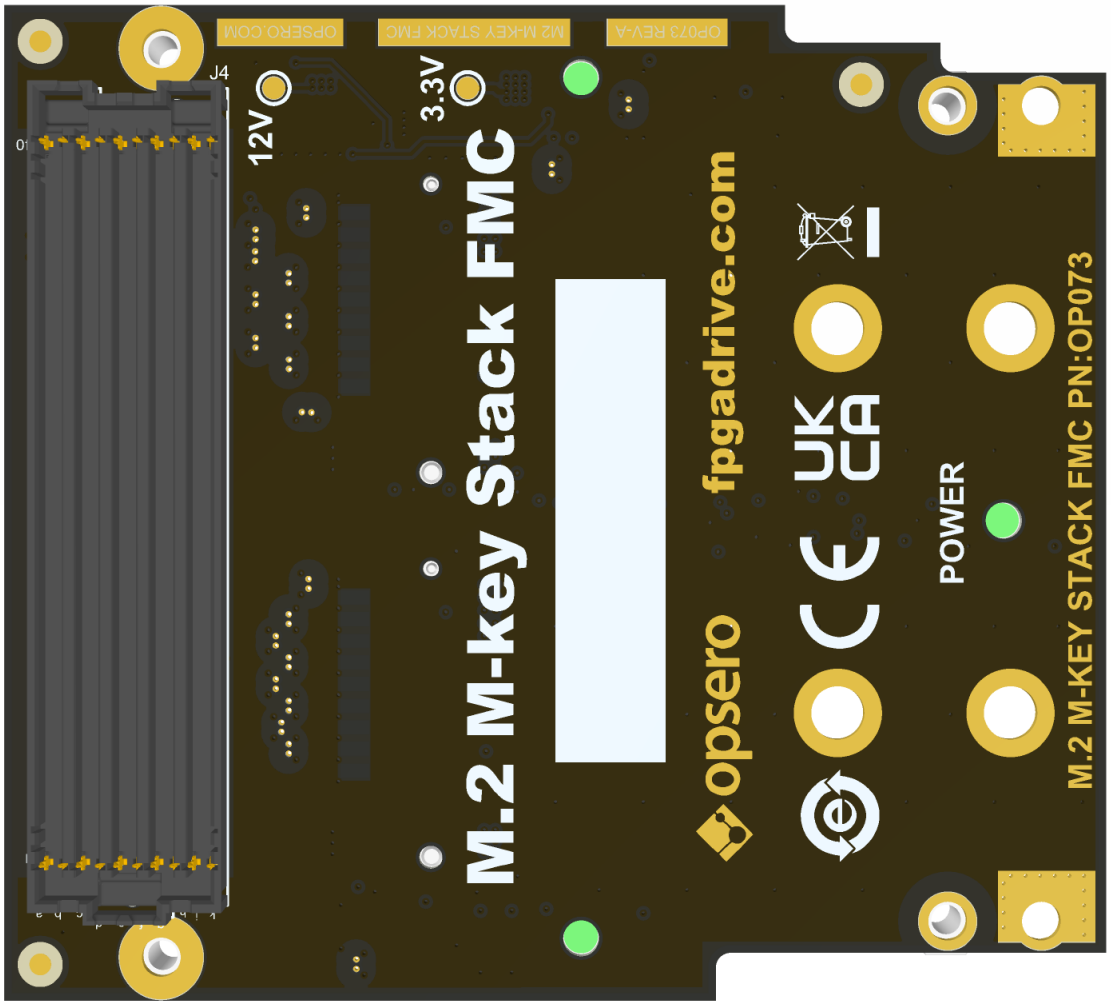
A key feature of the mezzanine card is it's Carrier-side FMC connector located on the side opposite to the M.2 module connectors (see bottom view below). This connector is a High Pin Count (HPC) FMC connector that is designed to mate with a second mezzanine (FMC) card. The FMC connectors are routed such that the second mezzanine card is provided all of the power and I/O signals from the FPGA/MPSoC development board, with the exception of the multi-gigabit transceiver (MGT) lanes and clocks. The M.2 M-key Stack FMC is able to drive the reset (PERST_N) signals of the attached M.2 modules via an I2C I/O expander. Read more about the Opsero Stack FMC concept in the detailed description section.

Top view



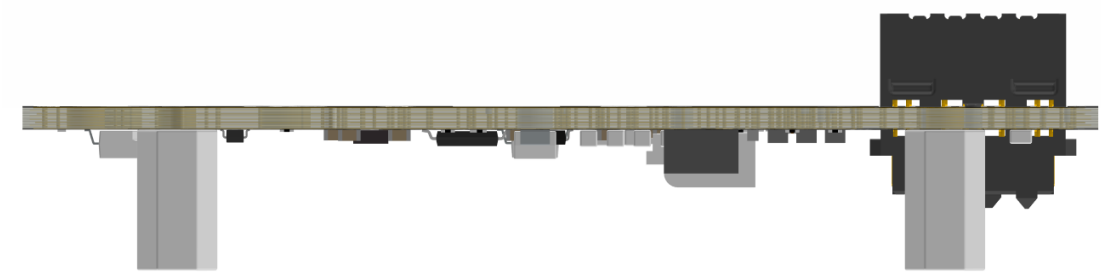
M.2 M-key Stack FMC top

Bottom view



M.2 M-key Stack FMC bottom

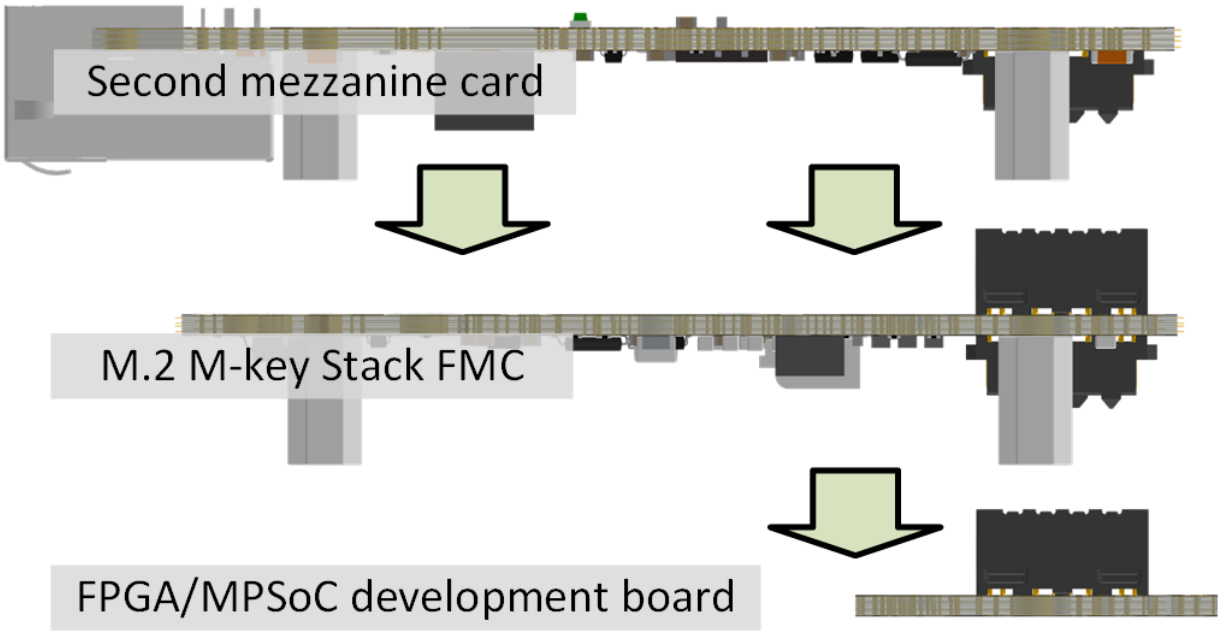
Profile view



M.2 M-key Stack FMC profile

Stacked view

The image below illustrates the Stack FMC concept, where the M.2 M-key Stack FMC is used with a second mezzanine card stacked on top. In this example, the second mezzanine card is the Robust Ethernet FMC.



M.2 M-key Stack FMC profile stacked

Features

- 2x M-key M.2 connectors for M.2 PCIe modules
- HPC Carrier-side FMC connector for “stacking” a second mezzanine card
- Support and example designs for multiple development boards
- Supports up to PCIe Gen4 speeds
- FMC pinout conforms to VITA 57.1 FMC Standard
- Standalone example designs
- PetaLinux example designs

Supported development boards

For a list of all the FPGA and MPSoC development boards that are compatible with the M.2 M-key Stack FMC, please refer to the list of compatible boards. For a list of boards for which we currently have a reference design, please refer to the list of supported boards in the reference design documentation.

Supported M.2 modules

The M.2 M-key Stack FMC has been designed to support all standard M-key M.2 modules for PCIe Gen1 to Gen4. However, support for any particular module is also dependent on the availability of the required software drivers, the version of PetaLinux used, the transceiver settings in the Vivado design, and other factors.

Ordering

The M.2 M-key Stack FMC can be purchased from the vendors listed below. The links under the part number column will take you to the corresponding order page.

Vendor	Part name	Part number
Opsero	M.2 M-key Stack FMC	OP073
Digi-Key	M.2 M-key Stack FMC	OP073

Included with the M.2 M-key Stack FMC are:

- 2x machine screws for fixing the M.2 modules to the mezzanine card
- 2x machine screws for fixing the mezzanine card to the carrier card
- 4x stand-offs for fixing a second FMC to the mezzanine card

Note that the M.2 M-key Stack FMC does NOT come with M.2 modules.

Pin Configuration

Pinout table

The M.2 M-key Stack FMC has a high pin count FPGA Mezzanine Card (FMC) connector, providing the connections to the FPGA on the development board. The following table defines the pinout of the FMC connector and describes each pin's purpose on this mezzanine card.

To avoid confusion, we have chosen not to label the PCIe lanes as being TX or RX; instead we have labelled them with the direction in which the signal flows (eg. FPGA-to-SSD1 means that the FPGA transmits this signal and the SSD1 receives).

The last column of the table identifies all of the pins that are routed through to the Carrier-side FMC connector for use by the second mezzanine card. A cross (x) mark in this column indicates that the second mezzanine card can consider this pin floating (not connected).

Pin	Pin name	Net	Description	Passed through
A1	GND	GND	Ground	YES
A2	DP1_M2C_P	SSDA2FPGA_1_P	PCIe lane 1 positive (SSD1-to-FPGA)	NO
A3	DP1_M2C_N	SSDA2FPGA_1_N	PCIe lane 1 negative (SSD1-to-FPGA)	NO
A4	GND	GND	Ground	YES
A5	GND	GND	Ground	YES
A6	DP2_M2C_P	SSDA2FPGA_2_P	PCIe lane 2 positive (SSD1-to-FPGA)	NO
A7	DP2_M2C_N	SSDA2FPGA_2_N	PCIe lane 2 negative (SSD1-to-FPGA)	NO
A8	GND	GND	Ground	YES
A9	GND	GND	Ground	YES
A10	DP3_M2C_P	SSDA2FPGA_3_P	PCIe lane 3 positive (SSD1-to-FPGA)	NO

A11	DP3_M2C_N	SSDA2FPGA_3_N	PCIe lane 3 negative (SSD1-to-FPGA)	NO
A12	GND	GND	Ground	YES
A13	GND	GND	Ground	YES
A14	DP4_M2C_P	SSDB2FPGA_0_P	PCIe lane 0 positive (SSD2-to-FPGA)	NO
A15	DP4_M2C_N	SSDB2FPGA_0_N	PCIe lane 0 negative (SSD2-to-FPGA)	NO
A16	GND	GND	Ground	YES
A17	GND	GND	Ground	YES
A18	DP5_M2C_P	SSDB2FPGA_1_P	PCIe lane 1 positive (SSD2-to-FPGA)	NO
A19	DP5_M2C_N	SSDB2FPGA_1_N	PCIe lane 1 negative (SSD2-to-FPGA)	NO
A20	GND	GND	Ground	YES
A21	GND	GND	Ground	YES
A22	DP1_C2M_P	FPGA2SSDA_1_P	PCIe lane 1 positive (FPGA-to-SSD1)	NO
A23	DP1_C2M_N	FPGA2SSDA_1_N	PCIe lane 1 negative (FPGA-to-SSD1)	NO
A24	GND	GND	Ground	YES
A25	GND	GND	Ground	YES
A26	DP2_C2M_P	FPGA2SSDA_2_P	PCIe lane 2 positive (FPGA-to-SSD1)	NO
A27	DP2_C2M_N	FPGA2SSDA_2_N	PCIe lane 2 negative (FPGA-to-SSD1)	NO
A28	GND	GND	Ground	YES
A29	GND	GND	Ground	YES

A30	DP3_C2M_P	FPGA2SSDA_3_P	PCIe lane 3 positive (FPGA-to-SSD1)	NO
A31	DP3_C2M_N	FPGA2SSDA_3_N	PCIe lane 3 negative (FPGA-to-SSD1)	NO
A32	GND	GND	Ground	YES
A33	GND	GND	Ground	YES
A34	DP4_C2M_P	FPGA2SSDB_0_P	PCIe lane 0 positive (FPGA-to-SSD2)	NO
A35	DP4_C2M_N	FPGA2SSDB_0_N	PCIe lane 0 negative (FPGA-to-SSD2)	NO
A36	GND	GND	Ground	YES
A37	GND	GND	Ground	YES
A38	DP5_C2M_P	FPGA2SSDB_1_P	PCIe lane 1 positive (FPGA-to-SSD2)	NO
A39	DP5_C2M_N	FPGA2SSDB_1_N	PCIe lane 1 negative (FPGA-to-SSD2)	NO
A40	GND	GND	Ground	YES
B1	CLK_DIR	N/C	Passed through	YES
B2	GND	GND	Ground	YES
B3	GND	GND	Ground	YES
B4	DP9_M2C_P	N/C	Not connected	NO
B5	DP9_M2C_N	N/C	Not connected	NO
B6	GND	GND	Ground	YES
B7	GND	GND	Ground	YES
B8	DP8_M2C_P	N/C	Not connected	NO
B9	DP8_M2C_N	N/C	Not connected	NO
B10	GND	GND	Ground	YES

B11	GND	GND	Ground	YES
B12	DP7_M2C_P	SSDB2FPGA_3_P	PCIe lane 3 positive (SSD2-to-FPGA)	NO
B13	DP7_M2C_N	SSDB2FPGA_3_N	PCIe lane 3 negative (SSD2-to-FPGA)	NO
B14	GND	GND	Ground	YES
B15	GND	GND	Ground	YES
B16	DP6_M2C_P	SSDB2FPGA_2_P	PCIe lane 2 positive (SSD2-to-FPGA)	NO
B17	DP6_M2C_N	SSDB2FPGA_2_N	PCIe lane 2 negative (SSD2-to-FPGA)	NO
B18	GND	GND	Ground	YES
B19	GND	GND	Ground	YES
B20	GBTCLK1_M2C_P	REFCLKB_FPGA_P	100MHz PCIe reference clock for the FPGA	NO
B21	GBTCLK1_M2C_N	REFCLKB_FPGA_N	100MHz PCIe reference clock for the FPGA	NO
B22	GND	GND	Ground	YES
B23	GND	GND	Ground	YES
B24	DP9_C2M_P	N/C	Not connected	NO
B25	DP9_C2M_N	N/C	Not connected	NO
B26	GND	GND	Ground	YES
B27	GND	GND	Ground	YES
B28	DP8_C2M_P	N/C	Not connected	NO
B29	DP8_C2M_N	N/C	Not connected	NO
B30	GND	GND	Ground	YES

B31	GND	GND	Ground	YES
B32	DP7_C2M_P	FPGA2SSDB_3_P	PCIe lane 3 positive (FPGA-to-SSD2)	NO
B33	DP7_C2M_N	FPGA2SSDB_3_N	PCIe lane 3 negative (FPGA-to-SSD2)	NO
B34	GND	GND	Ground	YES
B35	GND	GND	Ground	YES
B36	DP6_C2M_P	FPGA2SSDB_2_P	PCIe lane 2 positive (FPGA-to-SSD2)	NO
B37	DP6_C2M_N	FPGA2SSDB_2_N	PCIe lane 2 negative (FPGA-to-SSD2)	NO
B38	GND	GND	Ground	YES
B39	GND	GND	Ground	YES
B40	RES0	N/C	Passed through	YES
C1	GND	GND	Ground	YES
C2	DP0_C2M_P	FPGA2SSDA_0_P	PCIe lane 0 positive (FPGA-to-SSD1)	NO
C3	DP0_C2M_N	FPGA2SSDA_0_N	PCIe lane 0 negative (FPGA-to-SSD1)	NO
C4	GND	GND	Ground	YES
C5	GND	GND	Ground	YES
C6	DP0_M2C_P	SSDA2FPGA_0_P	PCIe lane 0 positive (SSD1-to-FPGA)	NO
C7	DP0_M2C_N	SSDA2FPGA_0_N	PCIe lane 0 negative (SSD1-to-FPGA)	NO
C8	GND	GND	Ground	YES
C9	GND	GND	Ground	YES
C10	LA06_P	N/C	Passed through	YES

C11	LA06_N	N/C	Passed through	YES
C12	GND	GND	Ground	YES
C13	GND	GND	Ground	YES
C14	LA10_P	N/C	Passed through	YES
C15	LA10_N	N/C	Passed through	YES
C16	GND	GND	Ground	YES
C17	GND	GND	Ground	YES
C18	LA14_P	N/C	Passed through	YES
C19	LA14_N	N/C	Passed through	YES
C20	GND	GND	Ground	YES
C21	GND	GND	Ground	YES
C22	LA18_P_CC	N/C	Passed through	YES
C23	LA18_N_CC	N/C	Passed through	YES
C24	GND	GND	Ground	YES
C25	GND	GND	Ground	YES
C26	LA27_P	N/C	Passed through	YES
C27	LA27_N	N/C	Passed through	YES
C28	GND	GND	Ground	YES
C29	GND	GND	Ground	YES
C30	SCL	I2C_SCL	I2C Clock	YES
C31	SDA	I2C_SDA	I2C Data (bidirectional)	YES
C32	GND	GND	Ground	YES
C33	GND	GND	Ground	YES

C34	GA0	GA0	EEPROM Address Bit 1 (A1)	YES
C35	12P0V_1	12V0	12VDC	YES
C36	GND	GND	Ground	YES
C37	12P0V_2	12V0	12VDC	YES
C38	GND	GND	Ground	YES
C39	3P3V_1	3V3	Passed through	YES
C40	GND	GND	Ground	YES
D1	PG_C2M	PG	Power Good (Driven by carrier)	YES
D2	GND	GND	Ground	YES
D3	GND	GND	Ground	YES
D4	GBTCLK0_M2C_P	REFCLKA_FPGA_P	100MHz PCIe reference clock for the FPGA	NO
D5	GBTCLK0_M2C_N	REFCLKA_FPGA_P	100MHz PCIe reference clock for the FPGA	NO
D6	GND	GND	Ground	YES
D7	GND	GND	Ground	YES
D8	LA01_P_CC	N/C	Passed through	YES
D9	LA01_N_CC	N/C	Passed through	YES
D10	GND	GND	Ground	YES
D11	LA05_P	N/C	Passed through	YES
D12	LA05_N	N/C	Passed through	YES
D13	GND	GND	Ground	YES
D14	LA09_P	N/C	Passed through	YES

D15	LA09_N	N/C	Passed through	YES
D16	GND	GND	Ground	YES
D17	LA13_P	N/C	Passed through	YES
D18	LA13_N	N/C	Passed through	YES
D19	GND	GND	Ground	YES
D20	LA17_P_CC	N/C	Passed through	YES
D21	LA17_N_CC	N/C	Passed through	YES
D22	GND	GND	Ground	YES
D23	LA23_P	N/C	Passed through	YES
D24	LA23_N	N/C	Passed through	YES
D25	GND	GND	Ground	YES
D26	LA26_P	N/C	Passed through	YES
D27	LA26_N	N/C	Passed through	YES
D28	GND	GND	Ground	YES
D29	TCK	N/C	Passed through	YES
D30	TDI	TDI-TDO	Passed through	YES
D31	TDO	TDI-TDO	Passed through	YES
D32	3P3VAUX	3V3AUX	3.3VDC Power supply for EEPROM	YES
D33	TMS	N/C	Passed through	YES
D34	TRST_L	N/C	Passed through	YES
D35	GA1	GA1	EEPROM Address Bit 0 (A0)	YES
D36	3P3V_2	3V3	Passed through	YES
D37	GND	GND	Ground	YES

D38	3P3V_3	3V3	Passed through	YES
D39	GND	GND	Ground	YES
D40	3P3V_4	3V3	Passed through	YES
E1	GND	GND	Ground	YES
E2	HA01_P_CC	N/C	Passed through	YES
E3	HA01_N_CC	N/C	Passed through	YES
E4	GND	GND	Ground	YES
E5	GND	GND	Ground	YES
E6	HA05_P	N/C	Passed through	YES
E7	HA05_P	N/C	Passed through	YES
E8	GND	GND	Ground	YES
E9	HA09_P	N/C	Passed through	YES
E10	HA09_P	N/C	Passed through	YES
E11	GND	GND	Ground	YES
E12	HA13_P	N/C	Passed through	YES
E13	HA13_P	N/C	Passed through	YES
E14	GND	GND	Ground	YES
E15	HA16_P	N/C	Passed through	YES
E16	HA16_P	N/C	Passed through	YES
E17	GND	GND	Ground	YES
E18	HA20_P	N/C	Passed through	YES
E19	HA20_P	N/C	Passed through	YES
E20	GND	GND	Ground	YES
E21	HB03_P	N/C	Passed through	YES

E22	HB03_P	N/C	Passed through	YES
E23	GND	GND	Ground	YES
E24	HB05_P	N/C	Passed through	YES
E25	HB05_P	N/C	Passed through	YES
E26	GND	GND	Ground	YES
E27	HB09_P	N/C	Passed through	YES
E28	HB09_P	N/C	Passed through	YES
E29	GND	GND	Ground	YES
E30	HB13_P	N/C	Passed through	YES
E31	HB13_P	N/C	Passed through	YES
E32	GND	GND	Ground	YES
E33	HB19_P	N/C	Passed through	YES
E34	HB19_P	N/C	Passed through	YES
E35	GND	GND	Ground	YES
E36	HB21_P	N/C	Passed through	YES
E37	HB21_P	N/C	Passed through	YES
E38	GND	GND	Ground	YES
E39	VADJ_1	N/C	Passed through	YES
E40	GND	GND	Ground	YES
F1	PG_M2C	N/C	Passed through	YES
F2	GND	GND	Ground	YES
F3	GND	GND	Ground	YES
F4	HA00_P_CC	N/C	Passed through	YES
F5	HA00_P_CC	N/C	Passed through	YES

F6	GND	GND	Ground	YES
F7	HA04_P	N/C	Passed through	YES
F8	HA04_P	N/C	Passed through	YES
F9	GND	GND	Ground	YES
F10	HA08_P	N/C	Passed through	YES
F11	HA08_P	N/C	Passed through	YES
F12	GND	GND	Ground	YES
F13	HA12_P	N/C	Passed through	YES
F14	HA12_P	N/C	Passed through	YES
F15	GND	GND	Ground	YES
F16	HA15_P	N/C	Passed through	YES
F17	HA15_P	N/C	Passed through	YES
F18	GND	GND	Ground	YES
F19	HA19_P	N/C	Passed through	YES
F20	HA19_P	N/C	Passed through	YES
F21	GND	GND	Ground	YES
F22	HB02_P	N/C	Passed through	YES
F23	HB02_P	N/C	Passed through	YES
F24	GND	GND	Ground	YES
F25	HB04_P	N/C	Passed through	YES
F26	HB04_P	N/C	Passed through	YES
F27	GND	GND	Ground	YES
F28	HB08_P	N/C	Passed through	YES
F29	HB08_P	N/C	Passed through	YES

F30	GND	GND	Ground	YES
F31	HB12_P	N/C	Passed through	YES
F32	HB12_P	N/C	Passed through	YES
F33	GND	GND	Ground	YES
F34	HB16_P	N/C	Passed through	YES
F35	HB16_P	N/C	Passed through	YES
F36	GND	GND	Ground	YES
F37	HB20_P	N/C	Passed through	YES
F38	HB20_P	N/C	Passed through	YES
F39	GND	GND	Ground	YES
F40	VADJ_2	N/C	Passed through	YES
J1	GND	GND	Ground	YES
J2	CLK3_BIDIR_P	N/C	Passed through	YES
J3	CLK3_BIDIR_P	N/C	Passed through	YES
J4	GND	GND	Ground	YES
J5	GND	GND	Ground	YES
J6	HA03_P	N/C	Passed through	YES
J7	HA03_P	N/C	Passed through	YES
J8	GND	GND	Ground	YES
J9	HA07_P	N/C	Passed through	YES
J10	HA07_P	N/C	Passed through	YES
J11	GND	GND	Ground	YES
J12	HA11_P	N/C	Passed through	YES
J13	HA11_P	N/C	Passed through	YES

J14	GND	GND	Ground	YES
J15	HA14_P	N/C	Passed through	YES
J16	HA14_P	N/C	Passed through	YES
J17	GND	GND	Ground	YES
J18	HA18_P	N/C	Passed through	YES
J19	HA18_P	N/C	Passed through	YES
J20	GND	GND	Ground	YES
J21	HA22_P	N/C	Passed through	YES
J22	HA22_P	N/C	Passed through	YES
J23	GND	GND	Ground	YES
J24	HB01_P	N/C	Passed through	YES
J25	HB01_P	N/C	Passed through	YES
J26	GND	GND	Ground	YES
J27	HB07_P	N/C	Passed through	YES
J28	HB07_P	N/C	Passed through	YES
J29	GND	GND	Ground	YES
J30	HB11_P	N/C	Passed through	YES
J31	HB11_P	N/C	Passed through	YES
J32	GND	GND	Ground	YES
J33	HB15_P	N/C	Passed through	YES
J34	HB15_P	N/C	Passed through	YES
J35	GND	GND	Ground	YES
J36	HB18_P	N/C	Passed through	YES
J37	HB18_P	N/C	Passed through	YES

J38	GND	GND	Ground	YES
J39	VIO_B_M2C_1	N/C	Passed through	YES
J40	GND	GND	Ground	YES
K1	VREF_B_M2C	N/C	Passed through	YES
K2	GND	GND	Ground	YES
K3	GND	GND	Ground	YES
K4	CLK2_BIDIR_P	N/C	Passed through	YES
K5	CLK2_BIDIR_P	N/C	Passed through	YES
K6	GND	GND	Ground	YES
K7	HA02_P	N/C	Passed through	YES
K8	HA02_P	N/C	Passed through	YES
K9	GND	GND	Ground	YES
K10	HA06_P	N/C	Passed through	YES
K11	HA06_P	N/C	Passed through	YES
K12	GND	GND	Ground	YES
K13	HA10_P	N/C	Passed through	YES
K14	HA10_P	N/C	Passed through	YES
K15	GND	GND	Ground	YES
K16	HA17_P_CC	N/C	Passed through	YES
K17	HA17_P_CC	N/C	Passed through	YES
K18	GND	GND	Ground	YES
K19	HA21_P	N/C	Passed through	YES
K20	HA21_P	N/C	Passed through	YES
K21	GND	GND	Ground	YES

K22	HA23_P	N/C	Passed through	YES
K23	HA23_P	N/C	Passed through	YES
K24	GND	GND	Ground	YES
K25	HB00_P_CC	N/C	Passed through	YES
K26	HB00_P_CC	N/C	Passed through	YES
K27	GND	GND	Ground	YES
K28	HB06_P_CC	N/C	Passed through	YES
K29	HB06_P_CC	N/C	Passed through	YES
K30	GND	GND	Ground	YES
K31	HB10_P	N/C	Passed through	YES
K32	HB10_P	N/C	Passed through	YES
K33	GND	GND	Ground	YES
K34	HB14_P	N/C	Passed through	YES
K35	HB14_P	N/C	Passed through	YES
K36	GND	GND	Ground	YES
K37	HB17_P_CC	N/C	Passed through	YES
K38	HB17_P_CC	N/C	Passed through	YES
K39	GND	GND	Ground	YES
K40	VIO_B_M2C_2	N/C	Passed through	YES
G1	GND	GND	Ground	YES
G2	CLK1_M2C_P	N/C	Passed through	YES
G3	CLK1_M2C_N	N/C	Passed through	YES
G4	GND	GND	Ground	YES
G5	GND	GND	Ground	YES

G6	LA00_P_CC	N/C	Passed through	YES
G7	LA00_N_CC	N/C	Passed through	YES
G8	GND	GND	Ground	YES
G9	LA03_P	N/C	Passed through	YES
G10	LA03_N	N/C	Passed through	YES
G11	GND	GND	Ground	YES
G12	LA08_P	N/C	Passed through	YES
G13	LA08_N	N/C	Passed through	YES
G14	GND	GND	Ground	YES
G15	LA12_P	N/C	Passed through	YES
G16	LA12_N	N/C	Passed through	YES
G17	GND	GND	Ground	YES
G18	LA16_P	N/C	Passed through	YES
G19	LA16_N	N/C	Passed through	YES
G20	GND	GND	Ground	YES
G21	LA20_P	N/C	Passed through	YES
G22	LA20_N	N/C	Passed through	YES
G23	GND	GND	Ground	YES
G24	LA22_P	N/C	Passed through	YES
G25	LA22_N	N/C	Passed through	YES
G26	GND	GND	Ground	YES
G27	LA25_P	N/C	Passed through	YES
G28	LA25_N	N/C	Passed through	YES
G29	GND	GND	Ground	YES

G30	LA29_P	N/C	Passed through	YES
G31	LA29_N	N/C	Passed through	YES
G32	GND	GND	Ground	YES
G33	LA31_P	N/C	Passed through	YES
G34	LA31_N	N/C	Passed through	YES
G35	GND	GND	Ground	YES
G36	LA33_P	N/C	Passed through	YES
G37	LA33_N	N/C	Passed through	YES
G38	GND	GND	Ground	YES
G39	VADJ_3	VADJ	Passed through	YES
G40	GND	GND	Ground	YES
H1	VREF_A_M2C	N/C	Passed through	YES
H2	PRSNT_M2C_L	GND	Ground	YES
H3	GND	GND	Ground	YES
H4	CLK0_M2C_P	N/C	Passed through	YES
H5	CLK0_M2C_N	N/C	Passed through	YES
H6	GND	GND	Ground	YES
H7	LA02_P	N/C	Passed through	YES
H8	LA02_N	N/C	Passed through	YES
H9	GND	GND	Ground	YES
H10	LA04_P	PERST_B	Passed through	YES
H11	LA04_N	PEDET_B	Passed through	YES
H12	GND	GND	Ground	YES
H13	LA07_P	N/C	Passed through	YES

H14	LA07_N	N/C	Passed through	YES
H15	GND	GND	Ground	YES
H16	LA11_P	N/C	Passed through	YES
H17	LA11_N	N/C	Passed through	YES
H18	GND	GND	Ground	YES
H19	LA15_P	N/C	Passed through	YES
H20	LA15_N	N/C	Passed through	YES
H21	GND	GND	Ground	YES
H22	LA19_P	N/C	Passed through	YES
H23	LA19_N	N/C	Passed through	YES
H24	GND	GND	Ground	YES
H25	LA21_P	N/C	Passed through	YES
H26	LA21_N	N/C	Passed through	YES
H27	GND	GND	Ground	YES
H28	LA24_P	N/C	Passed through	YES
H29	LA24_N	N/C	Passed through	YES
H30	GND	GND	Ground	YES
H31	LA28_P	N/C	Passed through	YES
H32	LA28_N	N/C	Passed through	YES
H33	GND	GND	Ground	YES
H34	LA30_P	N/C	Passed through	YES
H35	LA30_N	N/C	Passed through	YES
H36	GND	GND	Ground	YES
H37	LA32_P	N/C	Passed through	YES

H38	LA32_N	N/C	Passed through	YES
H39	GND	GND	Ground	YES
H40	VADJ_4	VADJ	Passed through	YES

Specifications

Recommended Operating Conditions

SUPPLY VOLTAGE	MIN	TYP	MAX	UNIT
12 VDC	+11.4	+12	+12.6	V
3.3 VDC	+3.14	+3.3	+3.46	V
VADJ (1.2VDC)	+1.14	+1.2	+1.26	V
VADJ (1.5VDC)	+1.425	+1.5	+1.575	V
VADJ (1.8VDC)	+1.71	+1.8	+1.89	V
VADJ (2.5VDC)	+2.375	+2.5	+2.625	V
VADJ (3.3VDC)	+3.135	+3.3	+3.465	V

Notes:

- All VADJ pins must be supplied with the same voltage chosen from one of the following levels: +1.2VDC, +1.5VDC, +1.8VDC, +2.5VDC, +3.3VDC. Note that many carriers have a system controller that will make this choice for you.

Power Consumption

The power consumption of the M.2 M-key Stack FMC will depend heavily on the M.2 modules being used and the load they are being put under. Power consumption measurements for some typical M.2 modules will be added to this section in the near future.

Thermal Information

We have not performed comprehensive thermal testing on the M.2 M-key Stack FMC, however we recommend that it be operated under ambient temperatures between 0 and 70 degrees C. This advice is based on the recommended ambient operating temperatures of a basket of NVMe SSDs currently on the market. The active devices on the mezzanine card itself have operating ranges that exceed those of the typical SSD and are listed in the table below.

Component Ambient Operating Temperatures

DEVICE	MIN	MAX	UNIT
TI, 3-16V 5A Buck Converter, TPS565247DRLR	-40	150	C
TI, IO Expander, TCA9536DTMR	-40	125	C
TI, Dual Inverter, SN74LVC2G14DCKR	-40	125	C
TI, Bus Switch, SN74CBTLV1G125DCKR	-40	85	C
MicroChip, 2x Output PCIe Clock Generator, DSC557-0334FI1	-40	85	C
ST, 2K EEPROM, M24C02-FDW6TP	-40	85	C
Amphenol, PCIe M.2 connector, MDT420M02003	-40	80	C

Components that are not listed in the table above (such as resistors, capacitors) are selected to have minimum operating temperature that is lower than -20 degrees C, and maximum operating temperature that is greater than 70 degrees C.

I2C (EEPROM) Timing

The serial EEPROM (part number ST, 2K EEPROM, M24C02-FDW6TP) has a maximum operating clock frequency of 400 kHz.

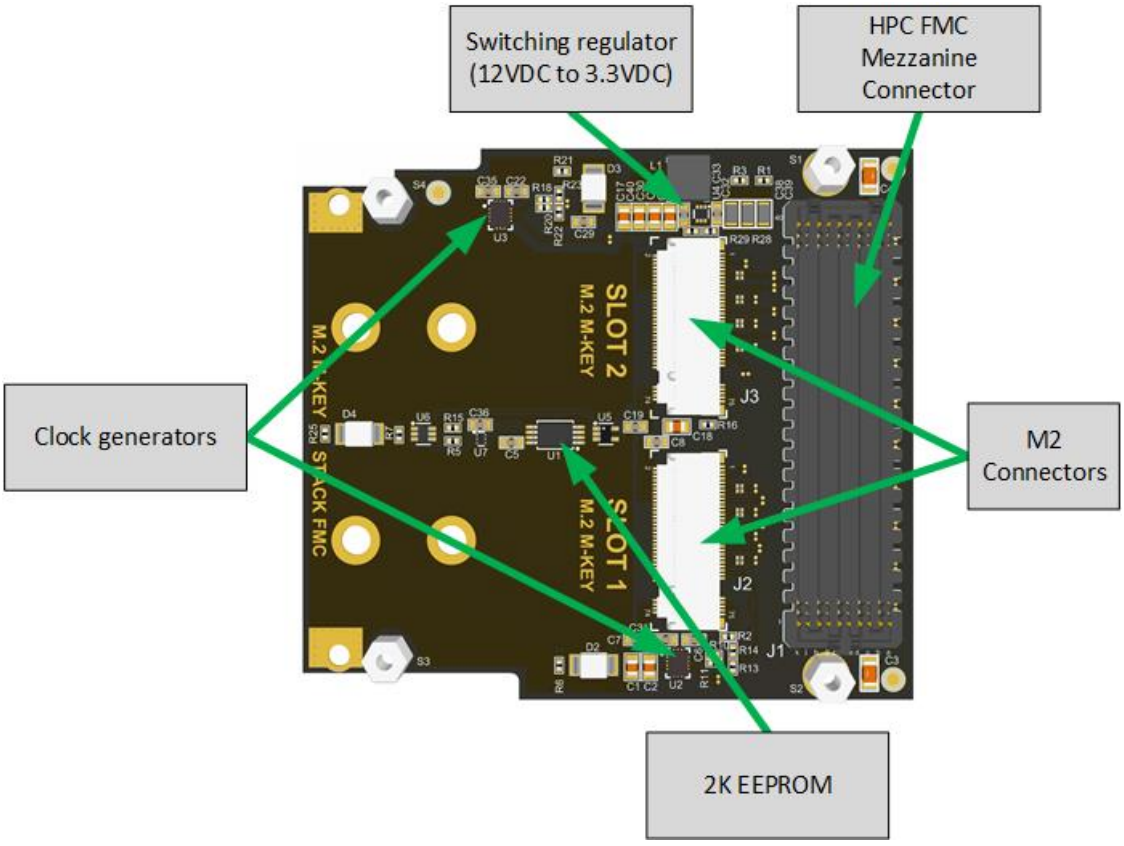
Certifications

- RoHS
- CE
- UKCA

Detailed Description

Hardware Overview

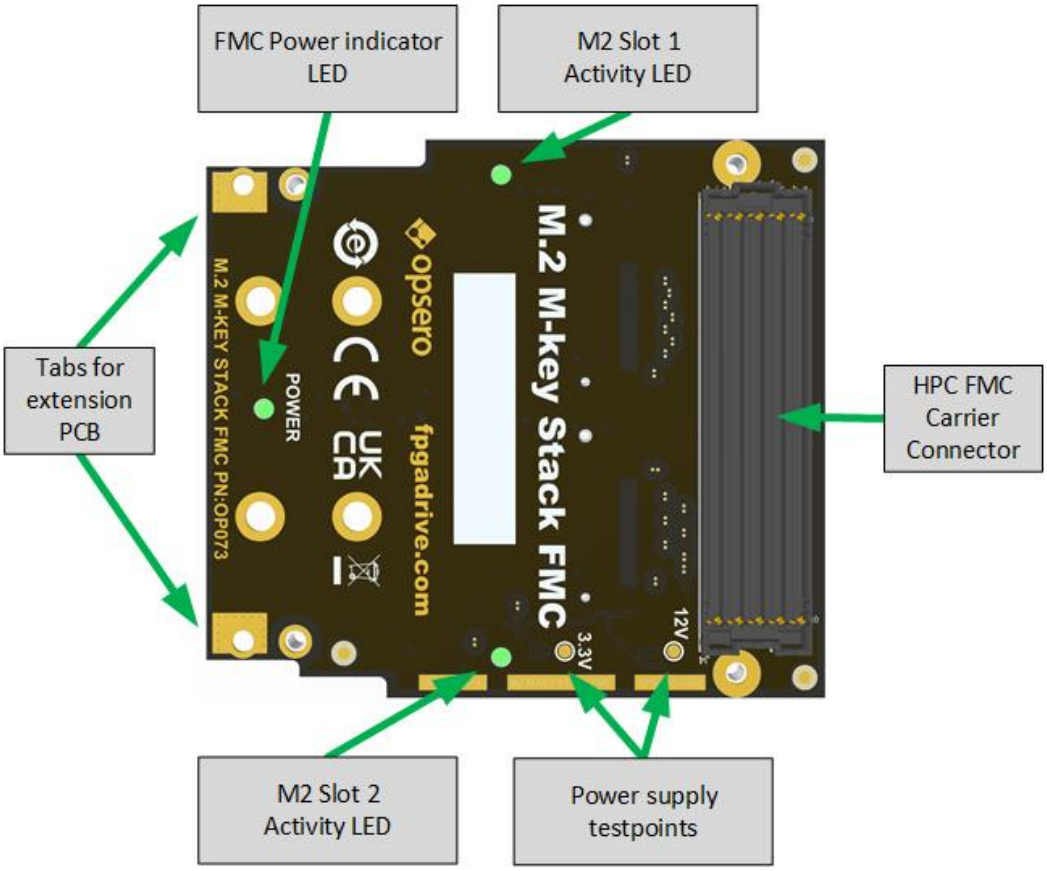
The figure below illustrates the various hardware components that are located on the top-side of the M.2 M-key Stack FMC.



The main components on the top-side of the mezzanine card are:

- 2x M-key M.2 socket connectors (for the SSDs)
- High Pin Count FMC *Mezzanine* Connector
- 2K EEPROM
- 2x PCIe Clock oscillators (100MHz)
- Switching regulator

The figure below illustrates the various hardware components that are located on the bottom-side of the mezzanine card.



The main components on the bottom-side of the mezzanine card are:

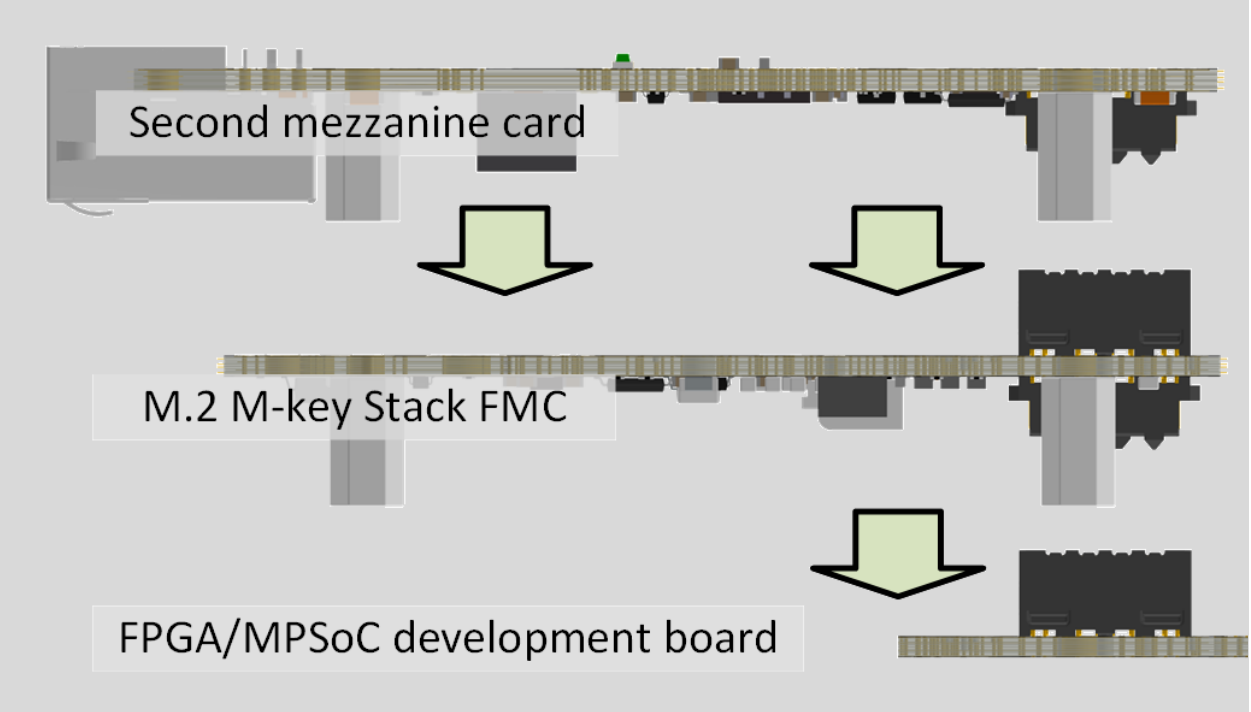
- High Pin Count FMC *Carrier* connector
- FMC Power indicator LED
- M.2 module activity LEDs
- Test points for power supplies

Stack FMC concept

With the M.2 M-key Stack FMC, Opsero introduces the Stack FMC concept whereby a single FMC slot of the FPGA/MPSoC development board can be shared by two mezzanine cards. Many FMC cards do not make use of all of the I/O that is provided by the FMC carrier board. Normally, when using such FMC cards, the unused I/Os are not accessible and this removes from the potential applications of the FPGA/MPSoC device. Opsero's new range of Stack FMCs offer a solution to this problem, by proposing a standard method for partitioning the FMC I/Os and power supplies between two mezzanine cards.

Opsero Stack FMCs are mezzanine cards that have a *carrier-side* FMC connector on the side of the board that is opposite the *mezzanine-side* FMC connector. The carrier-

side FMC connector mates with a second mezzanine card. A complete stack (see image below) consists of the FPGA/MPSoC development board at the bottom, followed by the first level mezzanine card (the Stack FMC) with the second level mezzanine card on the top.



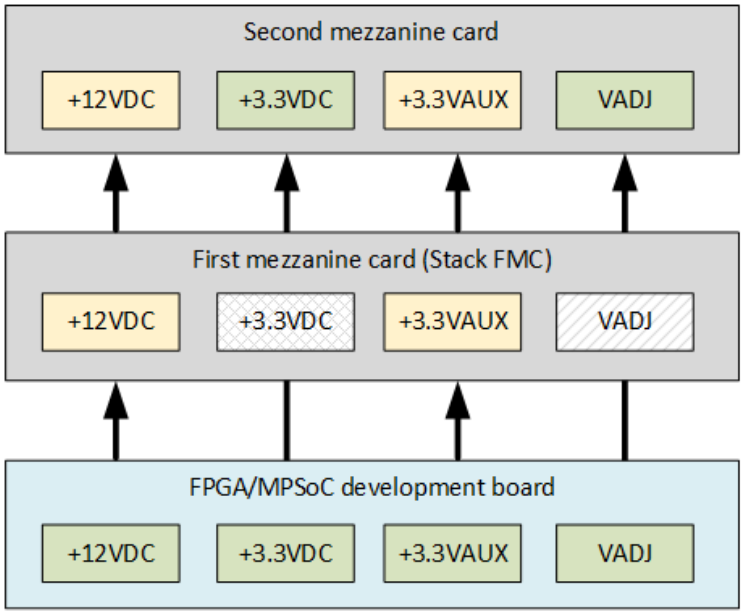
M.2 M-key Stack FMC stackup

Power and I/O partitioning

The partitioning of power and I/O between a Stack FMC and a second mezzanine card was designed with the objective of achieving compatibility with the greatest number of existing FMC cards, while respecting the limits of the VITA 57.1 standard as much as possible.

Power

It cannot be expected that the power capacity of a single FMC slot be able to supply two FMC cards if there is no intelligent partitioning of the power supplies. A Stack FMC satisfies the majority of it's power needs from the +12VDC power supply, and passes the main power supplies +3.3VDC and VADJ up for exclusive use by the second mezzanine card. A Stack FMC also uses the +3.3VAUX supply, however only ever drawing a few milliamps from it. The +12VDC and +3.3VAUX supplies are also passed up to the second mezzanine card. The diagram below illustrates the power partitioning in a complete stack.

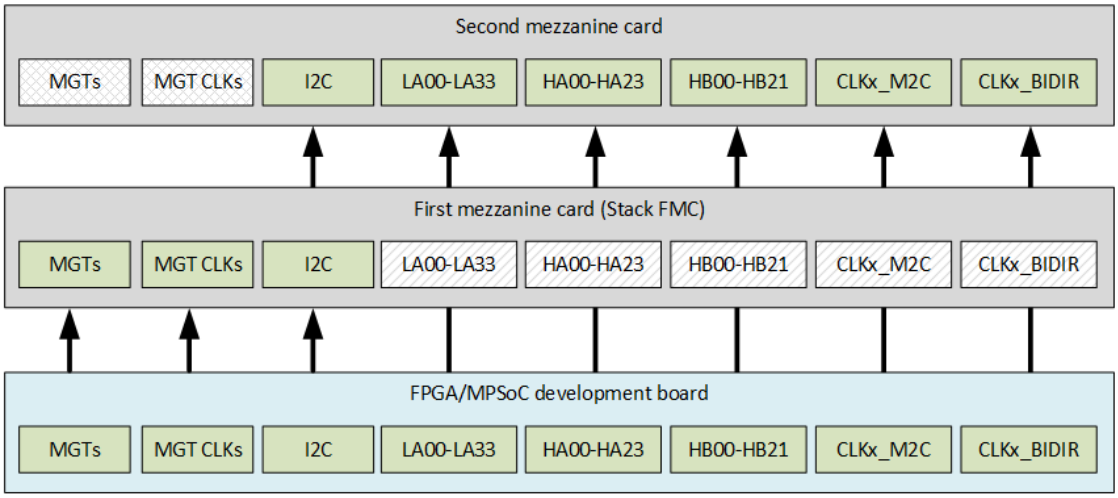


M.2 M-key Stack FMC power partition

- A grey shaded box indicates that the supply is not available on that level
- A yellow box indicates that the supply is shared by both levels
- A green box indicates that the supply is exclusively available to that level

I/O

The I/O partitioning was designed with the objective that the Stack FMC could accomodate the greatest number of existing FMC cards as second mezzanine. As such, *all of the I/O signals* are passed through to the second mezzanine, with the exception of the gigabit transceivers and their associated clocks. This choice comes with the limitation that the second mezzanine does not have access to any gigabit transceivers, and that the Stack FMC requires an on-board I2C I/O expander to satisfy all of it's low-speed I/O needs (if any). Naturally, the I2C bus is shared between the two mezzanine cards. The diagram below illustrates the partitioning of the I/O signals in a complete stack.



M.2 M-key Stack FMC IO partition

- A grey shaded box indicates that the I/Os are not available on that level
- A green box indicates that the I/Os are exclusively available to that level

M.2 connectors

The M.2 M-key modules connect to the mezzanine card through 2x M-key M.2 connectors (Amphenol, PCIe M.2 connector, MDT420M02003).

The pinout of the M.2 connector is shown in the table below:

Pin #	Pin name	Connection	Pin #	Pin name	Connection
1	GND	GND	2	3.3V	3V3
3	GND	GND	4	3.3V	3V3
5	PER-N3	SSD2FPGA_3_N	6	N/C	NC
7	PER-P3	SSD2FPGA_3_P	8	N/C	NC
9	GND	GND	10	DAS/DSS#/LED1#	DAS/DSS#
11	PET-N3	FPGA2SSD_3_N	12	3.3V	3V3
13	PET-P3	FPGA2SSD_3_P	14	3.3V	3V3
15	GND	GND	16	3.3V	3V3
17	PER-N2	SSD2FPGA_2_N	18	3.3V	3V3

19	PER-P2	SSD2FPGA_2_P	20	N/C	NC
21	GND	GND	22	N/C	NC
23	PET-N2	FPGA2SSD_2_N	24	N/C	NC
25	PET-P2	FPGA2SSD_2_P	26	N/C	NC
27	GND	GND	28	N/C	NC
29	PER-N1	SSD2FPGA_1_N	30	N/C	NC
31	PER-P1	SSD2FPGA_1_P	32	N/C	NC
33	GND	GND	34	N/C	NC
35	PET-N1	FPGA2SSD_1_N	36	N/C	NC
37	PET-P1	FPGA2SSD_1_P	38	DEVSLP	GND
39	GND	GND	40	SMB_CLK	NC
41	PER-N0	SSD2FPGA_0_N	42	SMB_DATA	NC
43	PER-P0	SSD2FPGA_0_P	44	ALERT#	NC
45	GND	GND	46	N/C	NC
47	PET-N0	FPGA2SSD_0_N	48	N/C	NC
49	PET-P0	FPGA2SSD_0_P	50	PERST#	PERST#
51	GND	GND	52	CLKREQ#	NC
53	REFCLK-N	REFCLK_SSD_N	54	PEWAKE#	NC
55	REFCLK-P	REFCLK_SSD_P	56	RSVD	NC
57	GND	GND	58	RSVD	NC
67	N/C	NC	68	SUSCLK	NC
69	PEDET	PEDET	70	3.3V	3V3
71	GND	GND	72	3.3V	3V3
73	GND	GND	74	3.3V	3V3

75	GND	GND

HPC FMC Mezzanine Connector

The M.2 M-key Stack FMC has a high pin count (HPC) FMC (FPGA Mezzanine Card) connector for interfacing with an FPGA or SoC development board. The part number of this connector is Samtec, High pin count FMC connector, Module side, ASP-134488-01 . This HPC FMC connector can be mated with LPC, HPC or FMC+ carrier connectors.

Note: When mated with an LPC FMC connector, only one M.2 module is connected, and only with a single lane PCIe interface. To get full functionality from the mezzanine card, it is recommended to use it with fully connected HPC or FMC+ connectors.

The pinout of this connector conforms to the VITA 57.1 FPGA Mezzanine Card Standard (for more information, see Pin configuration. For more information on the FMC connector and the VITA 57.1 standard, see the Samtec page on VITA 57.1 .

HPC FMC Carrier Connector

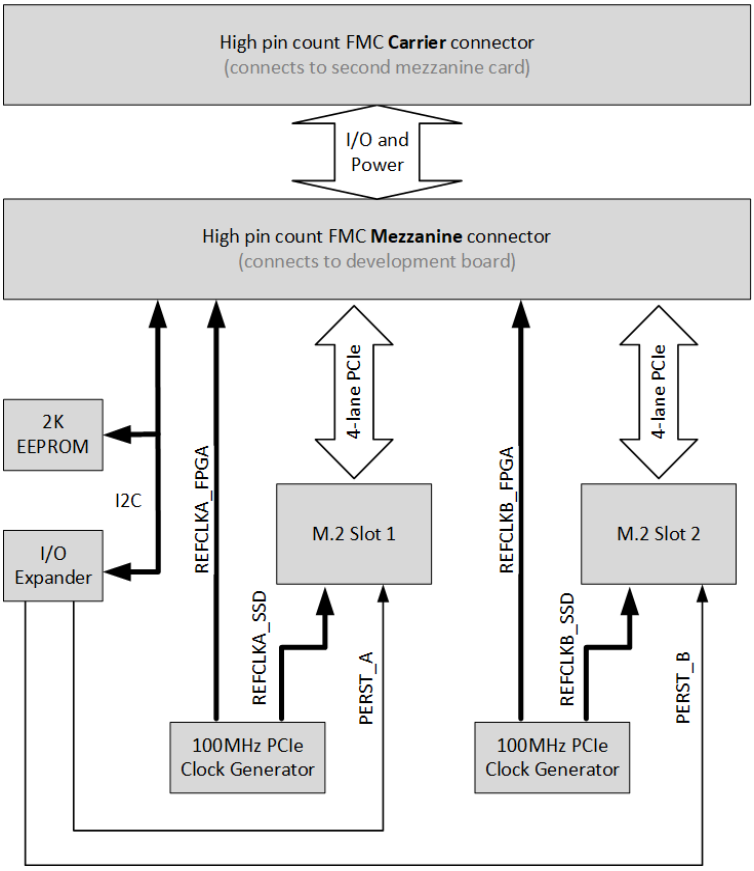
The mezzanine card has a HPC FMC *Carrier-side* connector on the side opposite to the M.2 modules. This second FMC connector is used to mate with an FMC mezzanine card, allowing the second FMC card to use all of the power and I/O signals that are not used by the M.2 M-key Stack FMC.

I/O Interfaces

The M.2 M-key Stack FMC uses the 12VDC power input from the carrier board and also the following I/O signals:

- 2x 4-lane PCIe interfaces for the M.2 modules
- 2x LVDS 100MHz PCIe reference clocks
- I2C bus

The 2x 4-lane PCIe interfaces are routed to independent gigabit transceivers on the FMC connector for maximum throughput. The figure below illustrates the main connections to the FMC connector.



The following I/O signals are passed through to the FMC *Carrier* connector for use by a second mezzanine card.

Signals common to all FMC cards (LPC, HPC and FMC+):

- LA00-LA33
- CLK0_M2C_P/N, CLK1_M2C_P/N
- VREF_A_M2C
- PG
- JTAG signals: TCK, TDI, TDO, TMS, TRST_L
- GA0, GA1
- I2C_SCL, I2C_SDA

Signals used by HPC and FMC+ cards:

- HA00-HA23
- HB00-HB21
- PG_M2C
- CLK_DIR
- RES0

- VIO_B_M2C_1, VIO_B_M2C_2
- CLK2_BIDIR_P/N, CLK3_BIDIR_P/N
- VREF_B_M2C

None of the gigabit transceiver pins nor their associated clock pins are passed through to the FMC *Carrier* connector, as they are used by the M.2 M-key Stack FMC.

PCIe interfaces

The 4-lane PCIe interfaces are routed to FMC pins that are dedicated to gigabit transceivers. The connections are shown in the tables below. Note that in this documentation, the label for the first M.2 module is M.2 Slot 1 while the second is M.2 Slot 2.

M.2 Slot 1

Direction	PCIe lane	FMC Pin	FMC name	Net name
SSD-to-FPGA	0	C6/C7	DP0_M2C_P/N	SSDA2FPGA_0_P/N
	1	A2/A3	DP1_M2C_P/N	SSDA2FPGA_1_P/N
	2	A6/A7	DP2_M2C_P/N	SSDA2FPGA_2_P/N
	3	A10/A11	DP3_M2C_P/N	SSDA2FPGA_3_P/N
FPGA-to-SSD	0	C2/C3	DP0_C2M_P/N	FPGA2SSDA_0_P/N
	1	A22/A23	DP1_C2M_P/N	FPGA2SSDA_1_P/N
	2	A26/A27	DP2_C2M_P/N	FPGA2SSDA_2_P/N
	3	A30/A31	DP3_C2M_P/N	FPGA2SSDA_3_P/N

M.2 Slot 2

Direction	PCIe lane	FMC Pin	FMC name	Net name
SSD-to-FPGA	0	A14/A15	DP4_M2C_P/N	SSDB2FPGA_0_P/N
	1	A18/A19	DP5_M2C_P/N	SSDB2FPGA_1_P/N
	2	B16/B17	DP6_M2C_P/N	SSDB2FPGA_2_P/N
	3	B12/B13	DP7_M2C_P/N	SSDB2FPGA_3_P/N
FPGA-to-SSD	0	A34/A35	DP4_C2M_P/N	FPGA2SSDB_0_P/N
	1	A38/A39	DP5_C2M_P/N	FPGA2SSDB_1_P/N

	2	B36/B37	DP6_C2M_P/N	FPGA2SSDB_2_P/N
	3	B32/B33	DP7_C2M_P/N	FPGA2SSDB_3_P/N

Reference clocks

The mezzanine card has two clock oscillators (MicroChip, 2x Output PCIe Clock Generator, DSC557-0334FI1), one for each M.2 slot. Each clock oscillator generates two synchronous 100MHz clocks; one LVDS and the other HCSL. The LVDS clocks are fed to the FMC connector, while the HCSL clocks are fed directly to the M.2 slots.

Synchronous to	FMC Pin	FMC name	Net name
M.2 Slot 1	D4/D5	GBTCLK0_M2C_P/N	REFCLKA_FPGA_P/N
M.2 Slot 2	B20/B21	GBTCLK1_M2C_P/N	REFCLKB_FPGA_P/N

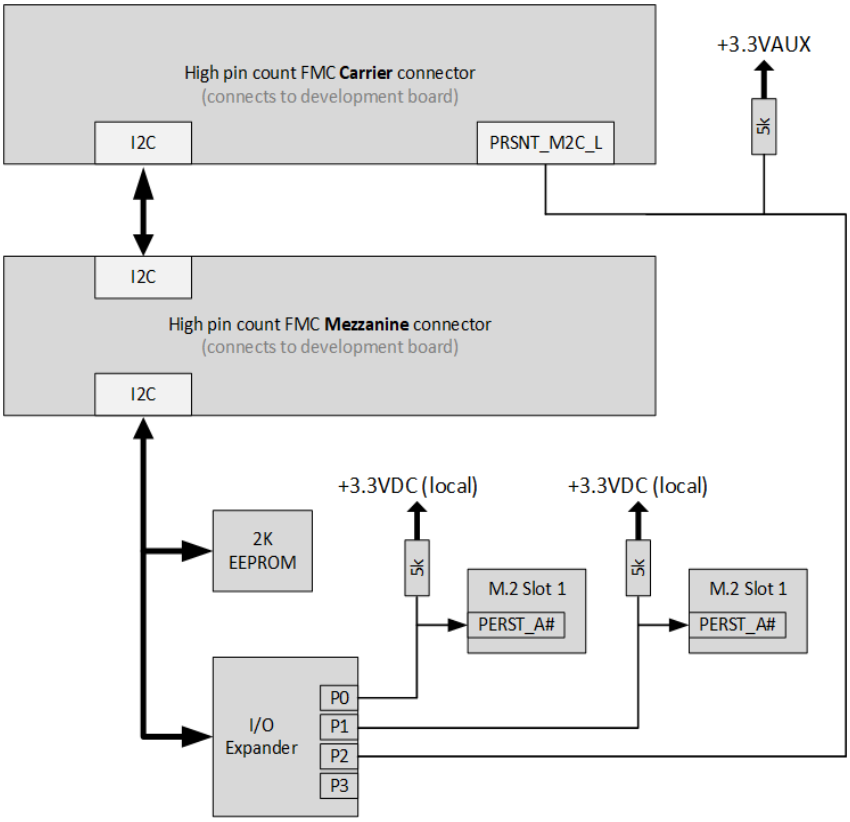
I2C bus

A 2K EEPROM and I/O expander sit on the FMC card's dedicated I2C bus. The FMC pins of the I2C bus are shown below, and it is up to the user to determine their corresponding connections to the FPGA/MPSoC on the carrier board being used.

I2C bus signal	FMC pin name	FMC pin number
SCL (clock)	SCL	C30
SDA (data)	SDA	C31

Be aware that on some carrier boards, the FMC I2C bus passes through an I2C MUX. On some boards it connects to FPGA pins whereas on others it connects to PS pins. If you wish to communicate with the EEPROM or I/O expander, it is necessary to check the schematic drawing of your carrier board to determine the structure of the I2C bus and to which pins it connects.

The diagram below illustrates the I2C bus connections and provides more detail of the I/O expander connections.



I2C bus

EEPROM

The EEPROM (ST, 2K EEPROM, M24C02-FDW6TP) stores IPMI FRU data that can be read by the carrier board and contains the following information:

- Manufacturer name (Opsero Electronic Design Inc.)
- Product name
- Product part number
- Serial number
- Power supply requirements

The FRU data is read by some carrier boards to determine the correct VADJ voltage to apply to the mezzanine card. All Opsero FMC products have their EEPROMs programmed with valid FRU data to allow these carrier boards to correctly power them.

Erasing or writing over the contents of the EEPROM can corrupt the IPMI FRU data making the mezzanine card unusable with carrier boards that require the information. We recommend that you do not use the mezzanine card's EEPROM for non-volatile storage but instead use the storage options provided by the carrier board. If you mistakenly erase or corrupt the contents of the EEPROM, you can reprogram it using

the Opsero FMC EEPROM Tool. Read more about the FMC EEPROM tool in the User Guide.

I/O Expander

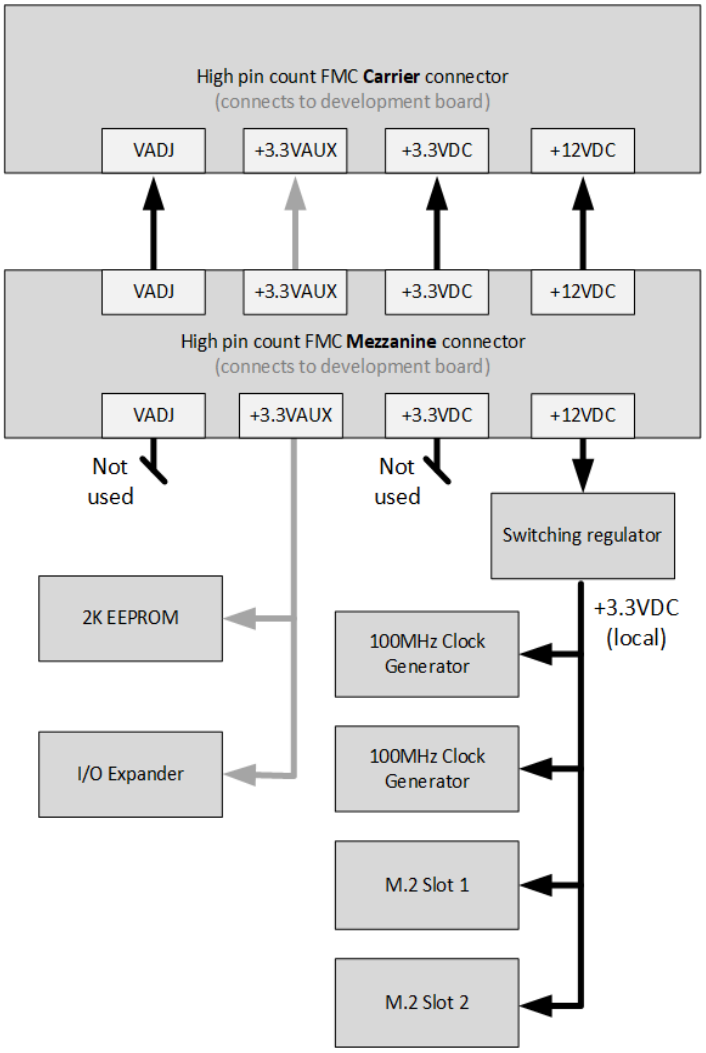
The M.2 M-key Stack FMC passes through all of the FMC I/O signals to the second mezzanine card, with the exception of the gigabit transceivers and their associated clocks. The I2C I/O expander (TI, IO Expander, TCA9536DTMR) is provided as a means to drive each M.2 module's reset signal (PERST#), for applications that require this level of control. The PERST# signals are also connected to pull up resistors so that the M.2 modules are released from reset on power up. The I/O expander's GPIOs all default to inputs on power-up, so most applications will not need to deal with the I/O expander at all.

PERST_A#/B#	Function
0 (LOW)	M.2 module in reset
1 (HIGH)	M.2 module operational

Power Supplies

All power required by the M.2 M-key Stack FMC is supplied by the FPGA/MPSoC board through the FMC connector:

- +12VDC
- +3.3VAUX



Power supplies

The FPGA/MPSoC carrier board also supplies a 3.3VDC and adjustable (VADJ) power supply, however these are not used by the M.2 M-key Stack FMC. All of the supplies are passed through to the FMC *Carrier* connector for use by a second mezzanine card.

12VDC Supply

The 12VDC supply is used to power both M.2 modules via a buck switching regulator (TI, 3-16V 5A Buck Converter, TPS565247DRLR). The switching regulator converts the 12VDC supply to a 3.3VDC supply which powers both M.2 modules and their corresponding 100MHz clock oscillators.

An LED indicates when power from the switching regulator is active, and it can be seen in the labelled bottom view of the board above.

3.3VAUX Supply

The 3.3VAUX supply is used by the M.2 M-key Stack FMC to power the following devices:

- 2K EEPROM
- I/O Expander
- Inverter
- Bus switch

3.3VDC Supply (FMC)

The 3.3VDC supply from the FPGA/MPSoC board is not used by the M.2 M-key Stack FMC and is passed through to the FMC *Carrier* connector for use by a second mezzanine card.

3.3VDC Supply (local)

The local 3.3VDC supply that is generated by the buck switching regulator is used to power the two M.2 modules and their respective 100MHz clock oscillators. This 3.3VDC supply is not connected to the FMC provided 3.3VDC, and it is not passed through to the second mezzanine card.

VADJ Supply

The adjustable voltage supply (VADJ), is the I/O voltage that is supplied by all standard FMC carriers. When used without a second mezzanine card, the M.2 M-key Stack FMC can accept any VADJ voltage in the range of 1.2V to 3.3V. The mezzanine card has an onboard FRU EEPROM that specifies acceptance of any VADJ voltage within the range 1.2V to 3.3V. All carriers with a power management system will read this EEPROM on power-up and apply a voltage in the range specified by the EEPROM. Note that some development boards require the VADJ voltage to be configured by a DIP switch or jumper placement, in which case we suggest that it be set to 1.8V.

When the M.2 M-key Stack FMC is used with a second mezzanine card, the address of it's FRU EEPROM is changed so that the power management system instead reads the FRU EEPROM of the second mezzanine. In this way, the second mezzanine determines the adjustable voltage supply (VADJ) according to it's needs.

The adjustable voltage supply (VADJ) is not used by the M.2 M-key Stack FMC and is passed through to the FMC *Carrier* connector for use by a second mezzanine card.

Power LED and testpoints

A single green LED on the mezzanine card is used to indicate when the required power supplies are active. The location of this LEDs can be seen in the labelled bottom view of the board above.

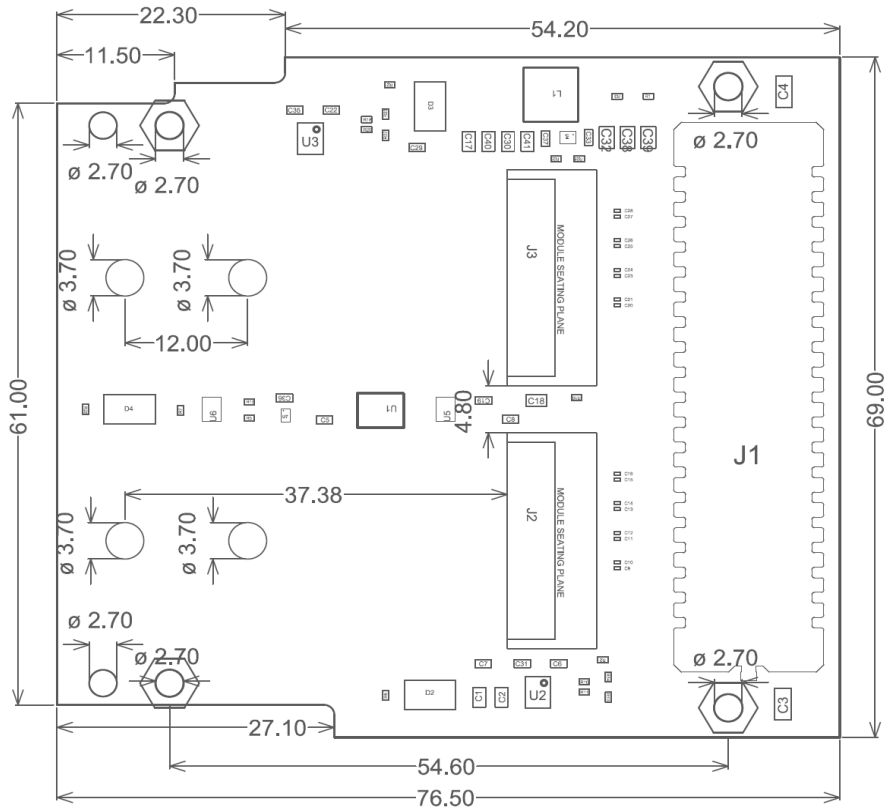
To aid hardware debug, test points are accessible on the bottom side of the mezzanine card for each of the power supplies of the M.2 M-key Stack FMC.

Mechanical Information

Dimensions

The mechanical dimensions of the M.2 M-key Stack FMC are illustrated in the figures below. All dimensions are in millimeters (mm).

The assembly drawings are also available as PDF files that you can download at the provided links.



M.2 M-key Stack FMC mechanical drawing

- M.2 M-key Stack FMC Rev-A Assembly Drawing PDF

3D Model

The 3D model of the board is available as a STEP file at the link below:

- M.2 M-key Stack FMC Rev-A 3D STEP model

Mezzanine fastening hardware

For mechanical fastening of the mezzanine card to the carrier board, the M.2 M-key Stack FMC comes pre-assembled with 4x hex standoffs and 4x machine screws. The M.2 M-key Stack FMC also comes with 2x machine screws for fixing the FMC to the carrier board. We **highly recommend** using these machine screws to fix the mezzanine card to the carrier board.

The hex standoff and machine screw part numbers are listed below:

- Hex standoff, Thread M2.5 x 0.45, Brass, Board-to-board length 10mm
  Part number: V6516C
  Manufacturer: Assmann
- Machine screw, Thread M2.5 x 0.45, Length (below head) 4mm, Stainless steel, Phillips head
  Part number: 90116A105
  Supplier: McMaster-Carr

Screws and standoffs for the FMC

M.2 module fastening hardware

For mechanical fastening of the M.2 modules to the FMC card, the M.2 M-key Stack FMC comes pre-assembled with 2x M.2 standoffs that can be moved to suit the length of the M.2 modules being used. Also provided are 2x machine screws for fixing the M.2 modules to the FMC, the part number is listed below:

- Machine screw, Thread M2.5 x 0.45, Length (below head) 3mm, Stainless steel, Phillips head

Part number: 90116A104
Supplier: McMaster-Carr

Screws for M.2 modules

Note that these screws are 1mm shorter than those used to secure the FMC card.

Fastening hardware for second FMC

For mechanical fastening of the second FMC to the M.2 M-key Stack FMC, 4x hex standoffs are provided and the part number is listed below:

- Hex standoff, Thread M2.5 x 0.45, Brass, Board-to-board length 10mm
  Part number: V6622C
  Manufacturer: Assmann

We **highly recommend** using the provided mounting hardware when using a second FMC with the M.2 M-key Stack FMC, as it ensures a stable and reliable connection between the boards.

Standoffs for securing the second FMC

Instructions for attaching a second FMC to the M.2 M-key Stack FMC can be found in the getting started guide.

Getting Started

Minimum setup

To start developing with the M.2 M-key Stack FMC, we recommend that you get setup with the minimum hardware and software requirements:

1. An FPGA or MPSoC development board from our list of supported boards.
2. One M.2 M-key Stack FMC.
3. At least one M.2 NVMe SSD (see our list of tested SSDs).
4. Build and run one of our example designs.

Hardware setup

For instructions on attaching the SSDs and connecting the M.2 M-key Stack FMC into the carrier board, we have put together the following video:

https://www.youtube.com/watch?v=A-80u63AjiM

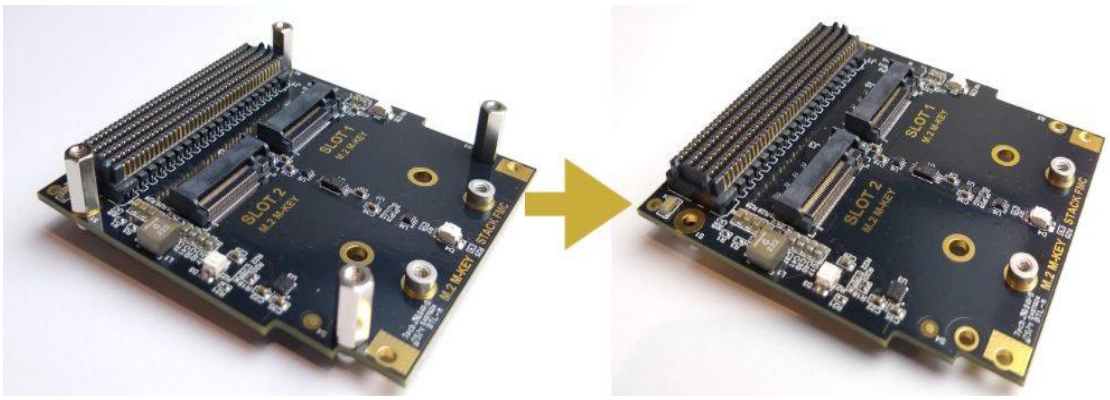
Fastening the mezzanine

FMC mezzanine cards are **not** hot-pluggable; to prevent the mezzanine card from detaching from the carrier while active, we recommend using the provided machine screws to fix the mezzanine card to the carrier board. The screws should be screwed into the mezzanine's hex standoffs from the underside of the carrier board. The details on these screws can be found in the mechanical information section.

Attaching a second FMC

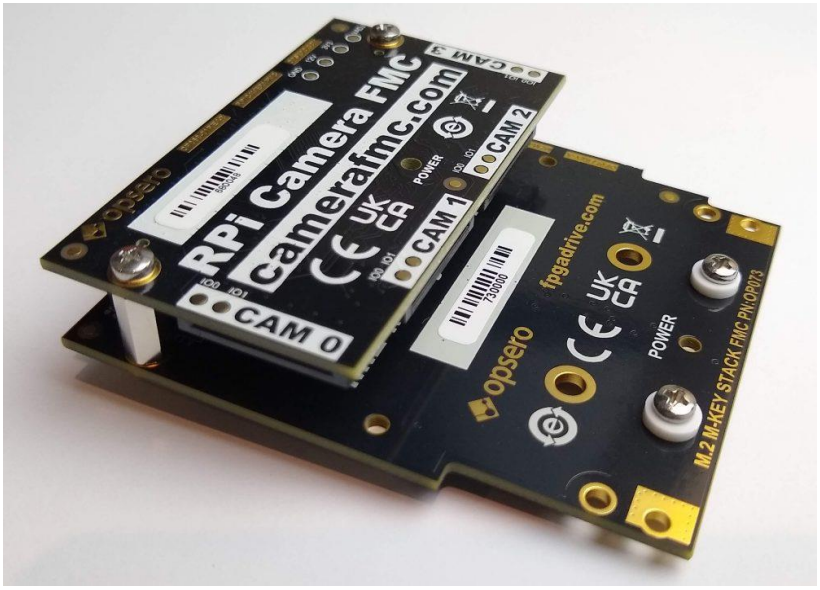
To attach a second FMC to the M.2 M-key Stack FMC:

1. Remove the pre-assembled hex standoffs and screws from the M.2 M-key Stack FMC



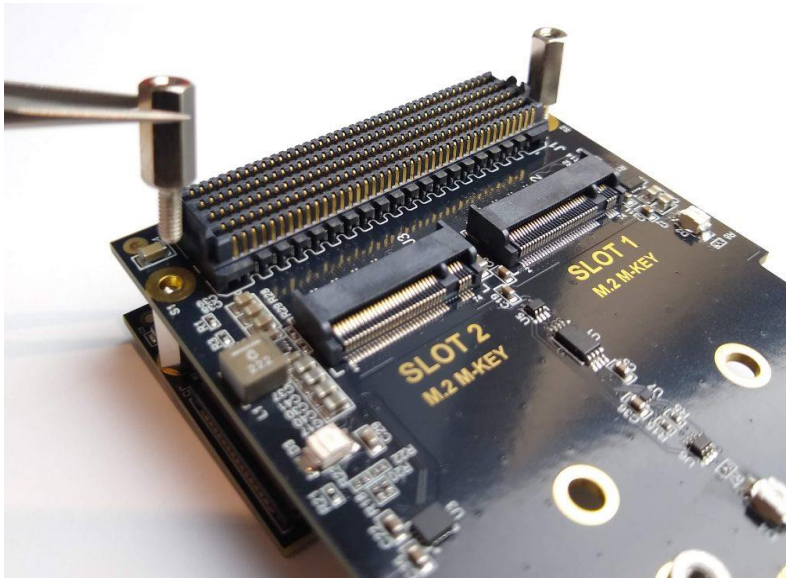
Remove standoffs from M.2 M-key Stack FMC

2. Flip the board over so that the M.2 connectors are facing down. Connect the second FMC to the M.2 M-key Stack FMC by plugging it into the carrier-side FMC connector. In the example shown below, we have attached the RPi Camera FMC.



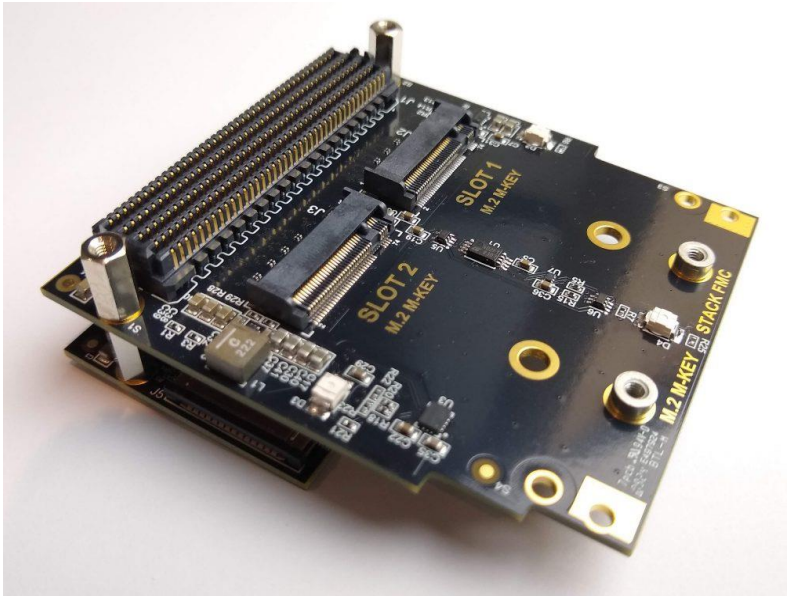
Attach the second FMC

3. Flip the board over again so that the M.2 connectors are facing upwards. Screw the provided V6622C standoffs into the standoffs of the second FMC, through the mounting holes of the M.2 M-key Stack FMC



Screw the standoffs into the M.2 M-key Stack FMC

The resulting stacked FMC should look like the image below:



M.2 M-key Stack with RPi Camera FMC

Clearance from M.2 standoff hardware

The M.2 M-key Stack FMC comes pre-assembled with 2x round M.2 standoffs that are fixed to the board with machine screws and white nylon spacers. This method for fixing the M.2 spacers to the board allows the position of the spacers to be easily changed to

suit the M.2 modules being used. The screws and nylon spacers are highlighted in the image below.

M.2 M-key Stack FMC nylon spacers

Some mezzanine cards, when used as the second FMC, may not have sufficient clearance from the screws and nylon spacers holding the M.2 standoffs. When using such mezzanine cards, remove the screws and nylon spacers and instead attach the M.2 standoffs by soldering them or gluing them with a conductive epoxy. Before gluing or soldering, be sure to use the correct mounting holes to suit your M.2 modules.

Software setup

In order to build our example designs, you will need to setup your PC with the AMD Xilinx development tools:

- Vivado ML
- Vitis
- PetaLinux

The Vivado and Vitis tools support most operating systems, whereas the PetaLinux tools can only be installed under Linux.

For the specific versions required, please refer to the release notes in the Git repository of the particular example design you wish to build.

Compatible Boards

The following development boards are compatible with the M.2 M-key Stack FMC and can support at least one M.2 slot. If you know of a board that is not listed here and you would like to know if it is compatible, please contact us.

Note that we don't currently have example designs for all of these carrier boards. For a list of carrier boards for which we do have example designs, please refer to the list of supported carriers in the reference design documentation.

Series-7 boards

Carrier	FMC	Ref design	PCIe	M.2 Slot 1	M.2 Slot 2
AMD Xilinx KC705 Kintex-7 Development board	HPC	Yes	Gen2	4-lanes	Not supported
AMD Xilinx KC705 Kintex-7 Development board	LPC	Yes	Gen2	1-lane [1]	Not supported [2]
AMD Xilinx VC707 Virtex-7 Development board	HPC1	Yes	Gen2	4-lanes	4-lanes
AMD Xilinx VC707 Virtex-7 Development board	HPC2	Yes	Gen2	4-lanes	4-lanes
AMD Xilinx VC709 Virtex-7 Development board	HPC	Yes	Gen3	4-lanes	4-lanes
AMD Xilinx ZC706 Zynq-7000 Development board	HPC	Yes	Gen2	4-lanes	Not supported [3]
AMD Xilinx ZC706 Zynq-7000 Development board	LPC	Yes	Gen2	1-lane [4]	Not supported [5]

[1] LPC connectors can only support 1-lane PCIe

[2] LPC connectors can only support 1-lane PCIe

[3] Zynq-7000 devices only have 1 PCIe block

[4] LPC connectors can only support 1-lane PCIe

[5] LPC connectors can only support 1-lane PCIe

Avnet PicoZed FMC Carrier Card V2 Zynq-7000 Development Board	LPC	Yes	Gen2	1-lane [6]	Not supported [7]

UltraScale boards

Carrier	FMC	Ref design	PCIe	M.2 Slot 1	M.2 Slot 2
AMD Xilinx KCU105 Kintex UltraScale Development board	HPC	Yes	Gen3	4-lanes	4-lanes
AMD Xilinx KCU105 Kintex UltraScale Development board	LPC	Yes	Gen3	1-lane [8]	Not supported [9]
AMD Xilinx VCU108 Virtex UltraScale Development board	HPC0	No	Gen3	4-lanes	4-lanes
AMD Xilinx VCU108 Virtex UltraScale Development board	HPC1	No	Gen3	4-lanes	4-lanes

Zynq Ultrascale+ boards

Carrier	FMC	Ref design	PCIe	M.2 Slot 1	M.2 Slot 2
AMD Xilinx ZCU104 Zynq UltraScale+ Development board	LPC	Yes	Gen3	1-lane [10]	Not supported [11]

[6] LPC connectors can only support 1-lane PCIe

[7] LPC connectors can only support 1-lane PCIe

[8] LPC connectors can only support 1-lane PCIe

[9] LPC connectors can only support 1-lane PCIe

[10] LPC connectors can only support 1-lane PCIe

[11] LPC connectors can only support 1-lane PCIe

AMD Xilinx ZCU102 Zynq UltraScale+ Development board	HPC0	No	Gen3	4-lanes [12]	4-lanes [13]
AMD Xilinx ZCU102 Zynq UltraScale+ Development board	HPC1	No	Gen3	4-lanes [14]	4-lanes [15]
AMD Xilinx ZCU106 Zynq UltraScale+ Development board	HPC0	Yes	Gen3	4-lanes	4-lanes
AMD Xilinx ZCU106 Zynq UltraScale+ Development board	HPC1	Yes	Gen3	1-lanes	Not supported
AMD Xilinx ZCU111 Zynq UltraScale+ Development board	FMC+	Yes	Gen3	4-lanes	4-lanes
AMD Xilinx ZCU208 Zynq UltraScale+ Development board	FMC+	Yes	Gen3	4-lanes	4-lanes
Avnet UltraZed EV Carrier Zynq UltraScale+ Development board	HPC	Yes	Gen3	4-lanes	4-lanes
Trenz UltraITX+ Baseboard Zynq UltraScale+ Development board	HPC	No	Gen3	4-lanes [16]	4-lanes [17]

[12] This board's device does not have integrated PCIe blocks, but it can be used with 3rd party IP to implement the required PCIe root complex

[13] This board's device does not have integrated PCIe blocks, but it can be used with 3rd party IP to implement the required PCIe root complex

[14] This board's device does not have integrated PCIe blocks, but it can be used with 3rd party IP to implement the required PCIe root complex

[15] This board's device does not have integrated PCIe blocks, but it can be used with 3rd party IP to implement the required PCIe root complex

[16] This board's device does not have integrated PCIe blocks, but it can be used with 3rd party IP to implement the required PCIe root complex

[17] This board's device does not have integrated PCIe blocks, but it can be used with 3rd party IP to implement the required PCIe root complex

Ultrascale+ boards

Carrier	FMC	Ref design	PCIe	M.2 Slot 1	M.2 Slot 2
AMD Xilinx VCU118 Virtex UltraScale+ Development board	HPC	No	Gen3	Not supported	Not supported
AMD Xilinx VCU118 Virtex UltraScale+ Development board	FMC+	No	Gen3	4-lanes	4-lanes

Versal boards

Carrier	FMC	Ref design	PCIe	M.2 Slot 1	M.2 Slot 2
AMD Xilinx VCK190 Versal AI Core Development board	FMC+1	No	Gen4	4-lanes	4-lanes
AMD Xilinx VCK190 Versal AI Core Development board	FMC+2	No	Gen4	4-lanes	4-lanes
AMD Xilinx VMK180 Versal Prime Series Development board	FMC+1	No	Gen4	4-lanes	4-lanes
AMD Xilinx VMK180 Versal Prime Series Development board	FMC+2	No	Gen4	4-lanes	4-lanes
AMD Xilinx VPK120 Versal Premium Series Development board	FMC+	No	Gen4	4-lanes	4-lanes

Compatibility requirements

If you need to determine the compatibility of a development board that is not listed here, or you are designing a carrier board to mate with the M.2 M-key Stack FMC, you can check your board against the list of requirements below.

Gigabit transceivers

The FPGA or MPSoC device must have gigabit transceivers and they must be routed to the FMC connector. For support of both M.2 slots, transceivers DP0-DP7 must all be

connected to the FPGA. In the AMD Xilinx devices, the transceivers are typically grouped into quads containing 4 transceivers. Ideally, each M.2 slot should be connected to a single quad and the lane ordering should match the MGT ordering as shown in the tables below:

Quad 1

The first quad should be connected to M.2 slot 1 as follows:

FPGA pin	PCIe lane	FMC Pin	FMC name	Net name
MGT_RXP/N0	0	C6/C7	DP0_M2C_P/N	SSDA2FPGA_0_P/N
MGT_TXP/N0	0	C2/C3	DP0_C2M_P/N	FPGA2SSDA_0_P/N
MGT_RXP/N1	1	A2/A3	DP1_M2C_P/N	SSDA2FPGA_1_P/N
MGT_TXP/N1	1	A22/A23	DP1_C2M_P/N	FPGA2SSDA_1_P/N
MGT_RXP/N2	2	A6/A7	DP2_M2C_P/N	SSDA2FPGA_2_P/N
MGT_TXP/N2	2	A26/A27	DP2_C2M_P/N	FPGA2SSDA_2_P/N
MGT_RXP/N3	3	A10/A11	DP3_M2C_P/N	SSDA2FPGA_3_P/N
MGT_TXP/N3	3	A30/A31	DP3_C2M_P/N	FPGA2SSDA_3_P/N

The clock reference for this M.2 slot (FMC pins GBTCLK0_M2C_P/N) should be connected to MGTREFCLK0P/N or MGTREFCLK1P/N of this quad.

Quad 2

The second quad should be connected to M.2 slot 2 as follows:

Direction	PCIe lane	FMC Pin	FMC name	Net name
MGT_RXP/N0	0	A14/A15	DP4_M2C_P/N	SSDB2FPGA_0_P/N
MGT_TXP/N0	0	A34/A35	DP4_C2M_P/N	FPGA2SSDB_0_P/N
MGT_RXP/N1	1	A18/A19	DP5_M2C_P/N	SSDB2FPGA_1_P/N
MGT_TXP/N1	1	A38/A39	DP5_C2M_P/N	FPGA2SSDB_1_P/N
MGT_RXP/N2	2	B16/B17	DP6_M2C_P/N	SSDB2FPGA_2_P/N
MGT_TXP/N2	2	B36/B37	DP6_C2M_P/N	FPGA2SSDB_2_P/N

MGT_RXP/N3	3	B12/B13	DP7_M2C_P/N	SSDB2FPGA_3_P/N
MGT_TXP/N3	3	B32/B33	DP7_C2M_P/N	FPGA2SSDB_3_P/N

The clock reference for this M.2 slot (FMC pins GBTCLK1_M2C_P/N) should be connected to MGTREFCLK0P/N or MGTREFCLK1P/N of this quad.

Example Designs

The example designs for the M.2 M-key Stack FMC are released open source under the MIT license and maintained on Github. We *strongly* encourage community contributions to the example designs.

Detailed information about the example designs can be found on the online documentation.

Programming Guide

This section provides the details of the programming requirements to operate the M.2 M-key Stack FMC hardware and customize functionality.

EEPROM

The 2K EEPROM is intended to store information that identifies the mezzanine card and also specifies the power supplies required by the card. This information is typically read by the system power management on the carrier board when it is powered up. In typical user applications, it should not be necessary to read the data on the EEPROM, and we highly recommend against writing to the EEPROM.

As the M.2 M-key Stack FMC does not make use any of the FMC I/O signals, it does not require any particular voltage level to be applied to VADJ. The EEPROM was included on the mezzanine card to satisfy the VITA 57.1 standard and to ensure compatibility with all standard FMC carriers. The EEPROM is programmed to accept a VADJ voltage between 1.2V and 3.3V.

Address switching

The I2C address of the EEPROM is switched between 0x50 and 0x54, by use of the device's A2 input pin. The device's address depends on the presence of a second mezzanine card "stacked" on top of the M.2 M-key Stack FMC. Switching of the I2C address of the EEPROM is necessary to avoid a bus conflict with the second mezzanine card's EEPROM.

When a second mezzanine card is "stacked" onto the M.2 M-key Stack FMC, it is the second mezzanine card's EEPROM that will determine the VADJ voltage provided by the carrier board. To prevent the power controller from reading the EEPROM of the M.2 M-key Stack FMC in this case, it detects when a second mezzanine card is present (using the PRSNT_M2C_L signal) and changes it's own EEPROM's address by driving it's A2 input HIGH.

Address without 2nd mezzanine

The EEPROM address when the M.2 M-key Stack FMC is used without a second mezzanine card.

A6	A5	A4	A3	A2	A1	A0	Hexadecimal
1	0	1	0	0	0	0	0x50

Address with 2nd mezzanine

The EEPROM address when a second mezzanine is attached.

A6	A5	A4	A3	A2	A1	A0	Hexadecimal
1	0	1	0	1	0	0	0x54

The addresses shown above assume that FMC signals GA0 and GA1 from the FMC carrier board are both LOW (0), which is the case for most FPGA/MPSoC development boards. If GA0 and GA1 are not LOW, then the actual addresses can be determined by setting A1=GA0 and A0=GA1.

The FMC pins of the EEPROM's I2C bus are shown below, and it is up to the user to determine their corresponding connections to the FPGA/MPSoC on the carrier board being used.

I2C bus signal	FMC pin name	FMC pin number
SCL (clock)	SCL	C30
SDA (data)	SDA	C31

Be aware that on some carrier boards, the FMC I2C bus passes through an I2C MUX. On some boards it connects to FPGA pins whereas on others it connects to PS pins. If you wish to communicate with the EEPROM, it is necessary to check the schematic drawing of your carrier board to determine the structure of the I2C bus and to which pins it connects.

FMC EEPROM Tool

The Opsero FMC EEPROM Tool can be used to verify, reprogram or update the EEPROM contents of Opsero FMC products using an FPGA or MPSoC board such as the ZCU102 or VCU118 board.

Only use this tool with Opsero FMC products. The use of this tool with FMCs from other manufacturers is strictly prohibited and may result in damage to the FMC or to the carrier board.

Do not use this tool with the M.2 M-key Stack FMC while it has a second mezzanine "stacked" on top.

Supported boards

The tool currently supports the following FPGA/MPSoC boards. You must have at least one of these boards in order to use the tool.

- KC705
- KCU105
- VCU118
- VCK190
- VMK180
- ZedBoard
- ZCU102 Rev1.0 and Rev1.1
- ZCU104
- ZCU106

Download

The tool can be downloaded at the link below:

Opsero FMC EEPROM Tool v1.5

The zip file contains a boot file (bitstream or BOOT.bin) for each of the supported boards.

Usage instructions

To run the tool, follow these steps:

1. Plug the FMC card you wish to reprogram into one of the FMC connectors of your FPGA/MPSoC board. The tool is designed to probe all of the FMC connectors on the FPGA/MPSoC board.
2. If you are using the ZedBoard, be sure to set the VADJ jumper setting to 1.8V. If you are using the KC705, be sure that your FMC card can support a VADJ of 2.5V, which is the default setting of that board.
3. Connect the UART of your FPGA/MPSoC board to a PC.
4. For Zynq and Zynq MP boards, a BOOT.bin file is provided. Copy this file to your board's SD card and configure it to boot from SD card. Then plug the SD card back into the board and power it up.
5. For FPGA boards, a bitstream is provided with an embedded ELF file. Power up your FPGA/MPSoC board and then download the bitstream to the FPGA board using the Vivado Hardware Manager tool.
6. Open a terminal program such as Putty and connect to the serial port of your FPGA/MPSoC board. If you see nothing in the terminal window, press ENTER to redisplay the menu.
7. Use the menu options to do the following:
   - **Program the EEPROM (p)**
     You will be asked to select the FMC product from a list, and also to enter

the product's serial number. Note that entering incorrect information here can lead to your FMC card being damaged by a VADJ voltage that is greater than it's true rating. If you are not sure about the product to select here, please contact Opsero first.

I/O Expander

As the M.2 M-key Stack FMC passes through all I/O (except gigabit transceivers) to the second mezzanine card, it has an I/O expander (TI, IO Expander, TCA9536DTMR) to allow the FPGA/MPSoC board to control each M.2 module's reset signal (PERST_A# and PERST_B#) over the I2C bus. The I/O expander can also be used to read the PRSNT_M2C_L signal that indicates whether a second mezzanine card is present. An illustration of the I/O expander's connections is provided in the I2C section. More detailed information regarding the use of the I/O expander can be found in the datasheet.

I2C address

The I/O expander can be accessed over the I2C bus using the address 0x41.

A6	A5	A4	A3	A2	A1	A0	Hexadecimal
1	0	0	0	0	0	1	0x41

I2C registers

The table below lists the registers of the I/O expanders.

Address	Register	RW
0x00	Input port	R
0x01	Output port	RW
0x02	Polarity inversion	RW
0x03	Configuration	RW
0x50	Special function	RW

For registers 0x00, 0x01, 0x02 and 0x03, the bits 0 to 3 refer to the expander's IOs: P0, P1, P2 and P3.

I/Os

The I/O expanders have 4x GPIOs, labelled P0, P1, P2 and P3. On the M.2 M-key Stack FMC, these I/Os are connected as follows:

Expander I/O pin	Bit mask	Connects to	Description
P0	0x01	PERST_A#	M2 Slot 1 reset (active-low)
P1	0x02	PERST_B#	M2 Slot 2 reset (active-low)
P2	0x04	PRSNT_M2C_L	2nd Mezzanine present
P3	0x08	Not connected	

All of the I/O expander GPIOs default to inputs on power-up. The PERST_A# and PERST_B# signals are connected to pull-up resistors, to ensure that the M.2 modules are released from reset on power-up, even if the FPGA/MPSoC has not configured the I/O expander. Most applications can leave the I/O expander in it's default configuration.

Troubleshooting

This section describes some of the common issues that can arise when using the mezzanine card.

Board Revision History

Rev A

- The M.2 M-key Stack FMC (OP073) is a variation of the FPGA Drive FMC Gen4 (OP063) product.
- Date of first manufacture: 2023-02-11
- Commercially released

References

Board Files

Rev-A

- M.2 M-key Stack FMC Rev-A Schematics PDF
- M.2 M-key Stack FMC Rev-A Assembly Drawing PDF
- M.2 M-key Stack FMC Rev-A 3D STEP model

Part Datasheets

Use the links below to access the datasheets of the significant parts on the mezzanine card.

- Samtec, High pin count FMC connector, Module side, ASP-134488-01 datasheet
- Samtec, High pin count FMC connector, Carrier side, ASP-134486-01 datasheet
- Amphenol, PCIe M.2 connector, MDT420M02003 datasheet
- TI, 3-16V 5A Buck Converter, TPS565247DRLR datasheet
- MicroChip, 2x Output PCIe Clock Generator, DSC557-0334FI1 datasheet
- ST, 2K EEPROM, M24C02-FDW6TP datasheet
- TI, IO Expander, TCA9536DTMR datasheet
- TI, Dual Inverter, SN74LVC2G14DCKR datasheet
- TI, Bus Switch, SN74CBTLV1G125DCKR datasheet

Revision History

Date	Version	Description
2024-04-24	1.0	Initial PDF release.

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