N and P Channel Enhancement Mode Power MOSFET

Description

The G18NP06Y uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge. It can be used in a wide variety of applications.

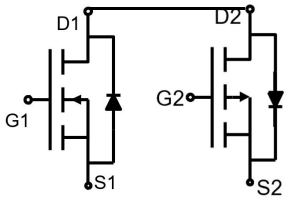
General Features

- NMOS
- V_{DS} 60V
- I_D (at V_{GS} = 10V) 18A
- $R_{DS(ON)}$ (at V_{GS} = 10V) < 35mΩ
- $R_{DS(ON)}$ (at V_{GS} = 4.5V) < 40mΩ
- 100% Avalanche Tested
- RoHS Compliant

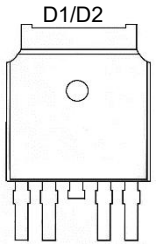
- PMOS
- V_{DS} -60V
- I_D (at V_{GS} = -10V) -18A
- $R_{DS(ON)}$ (at V_{GS} = -10V) < 45mΩ
- 100% Avalanche Tested
- RoHS Compliant

Application

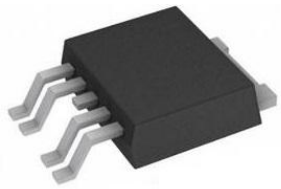
- Power switch
- DC/DC converters



Schematic diagram



pin assignment



TO-252-4 Dual

Ordering Information

Device	Package	Marking	Packaging
G18NP06Y	TO-252-4 Dual	G18NP06	2500pcs/Reel

Absolute Maximum Ratings T_C = 25ºC, unless otherwise noted

Parameter	Symbol	NMOS	PMOS	Unit
Drain-Source Voltage	V_{DS}	60	-60	V
Continuous Drain Current	I_D	18	-18	A
Pulsed Drain Current (note1)	I_{DM}	72	-72	A
Gate-Source Voltage	V_{GS}	±20	±20	V
Power Dissipation	P_D	45	50	W
Single pulse avalanche energy （note2）	E_{AS}	20	56	mJ
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 To 150	-55 To 150	ºC

Thermal Resistance

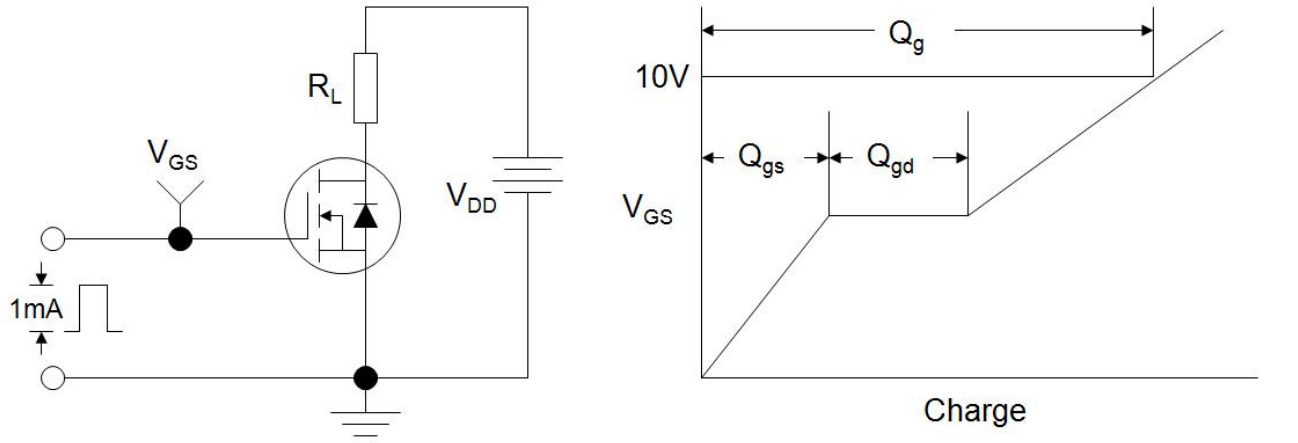
Parameter	Symbol	NMOS	PMOS	Unit
Thermal Resistance, Junction-to-Ambient	R_{thJA}	50	50	ºC/W
Maximum Junction-to-Case	R_{thJC}	2.8	2.5	ºC/W

NMOS Specifications T_J = 25ºC, unless otherwise noted						
Parameter	**Symbol**	**Test Conditions**	**Value**			**Unit**
			Min.	**Typ.**	**Max.**	
Static Parameters						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250μA	60	--	--	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 60V, V_{GS} = 0V	--	--	1	μA
Gate-Source Leakage	I_{GSS}	V_{GS} = ±20V	--	--	±100	nA
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	1.0	1.7	2.5	V
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = 10V, I_D = 12A	--	26	35	mΩ
		V_{GS} = 4.5V, I_D = 12A	--	30	40	
Forward Transconductance	g_{FS}	V_{GS} = 5V, I_D = 12A	--	22	--	S
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = 30V, f = 1.0MHz	--	1446	--	pF
Output Capacitance	C_{oss}		--	135	--	
Reverse Transfer Capacitance	C_{rss}		--	96	--	
Total Gate Charge	Q_g	V_{DD} = 30V, I_D = 12A, V_{GS} = 10V	--	22	--	nC
Gate-Source Charge	Q_{gs}		--	3	--	
Gate-Drain Charge	Q_{gd}		--	5	--	
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = 30V, I_D = 12A, R_G = 3Ω	--	5	--	ns
Turn-on Rise Time	t_r		--	3	--	
Turn-off Delay Time	$t_{d(off)}$		--	17	--	
Turn-off Fall Time	t_f		--	2.5	--	
Drain-Source Body Diode Characteristics						
Continuous Body Diode Current	I_S	T_C = 25ºC	--	--	18	A
Body Diode Voltage	V_{SD}	T_J = 25ºC, I_{SD} = 12A, V_{GS} = 0V	--	--	1.2	V
Reverse Recovery Charge	Qrr	I_F = 12A, V_{GS} = 0V di/dt=100A/us	--	50	--	nC
Reverse Recovery Time	Trr		--	29	--	ns

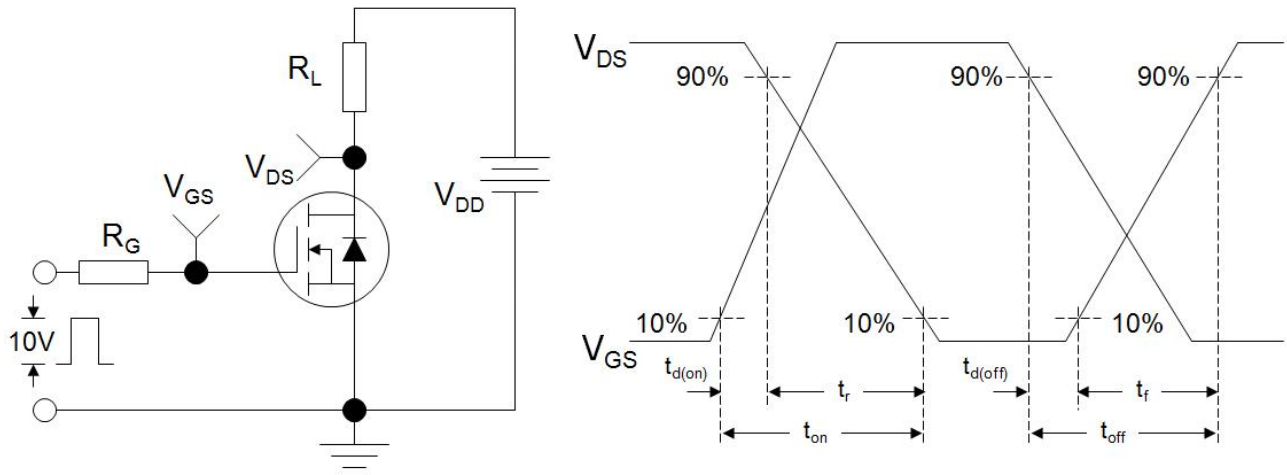
Notes

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. EAS condition : Tj=25℃ ,VDD=50V,VGS=10V,L=0.5mH,Rg=25Ω
   The table shows the minimum avalanche energy, which is 56mJ when the device is tested until failure
3. Identical low side and high side switch with identical R_G

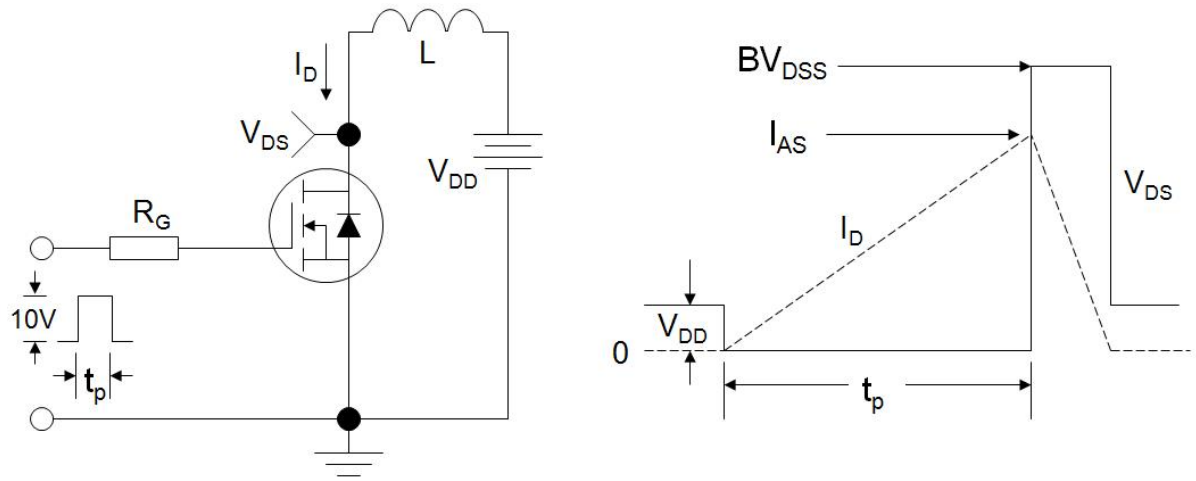
Gate Charge Test Circuit



Switch Time Test Circuit



EAS Test Circuit



NMOS Typical Characteristics T_J = 25ºC, unless otherwise noted

Figure 1. Output Characteristics

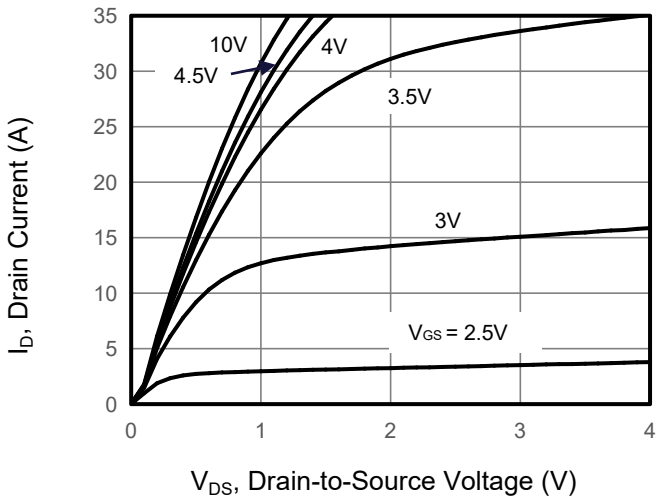


Figure 2. Transfer Characteristics

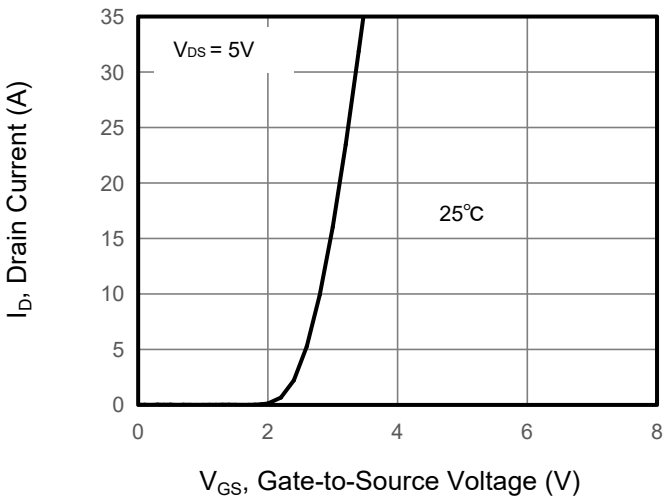


Figure 3. Drain Source On Resistance

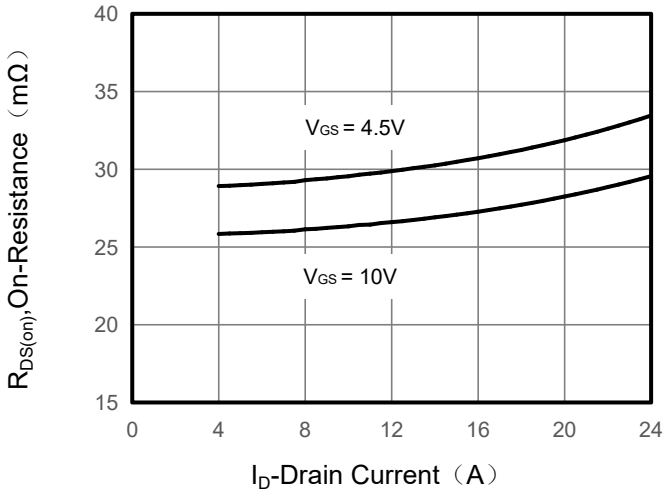


Figure 4. Gate Charge

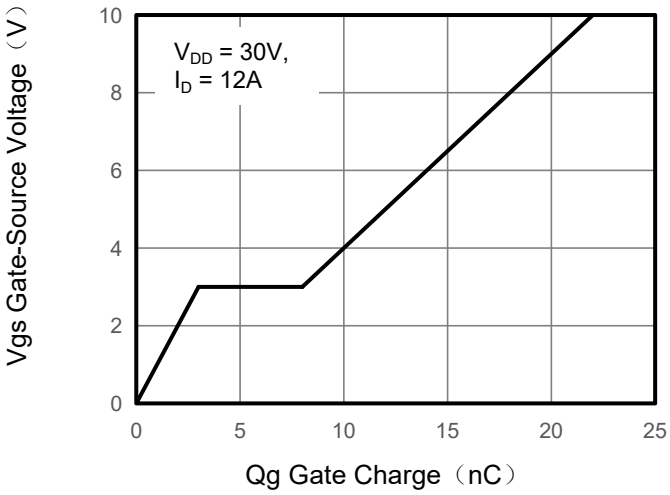


Figure 5. Capacitance

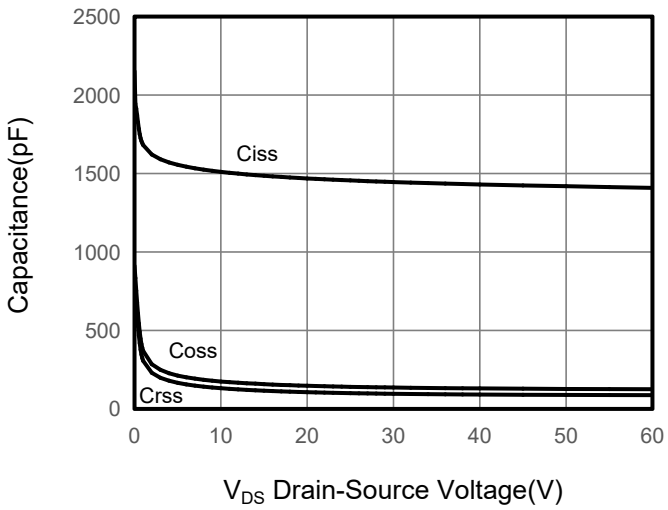
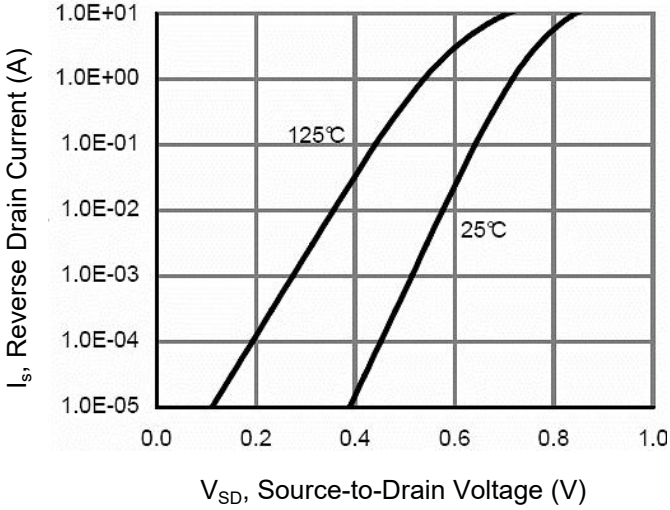


Figure 6. Source-Drain Diode Forward



NMOS Typical Characteristics T_J = 25ºC, unless otherwise noted

Figure 7. Drain-Source On-Resistance

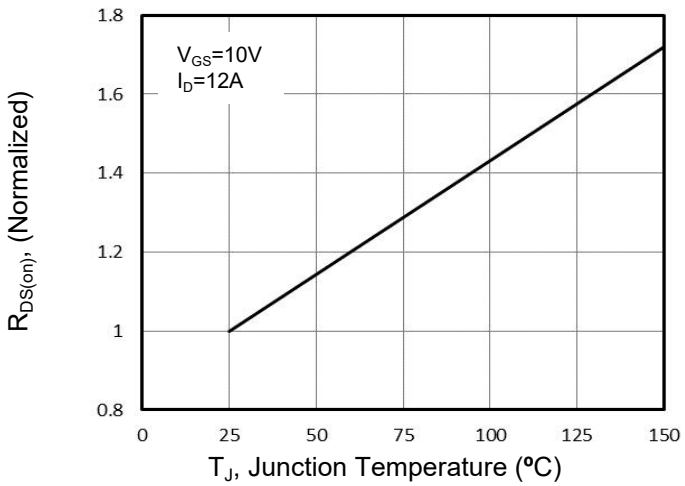


Figure 8. Safe Operation Area

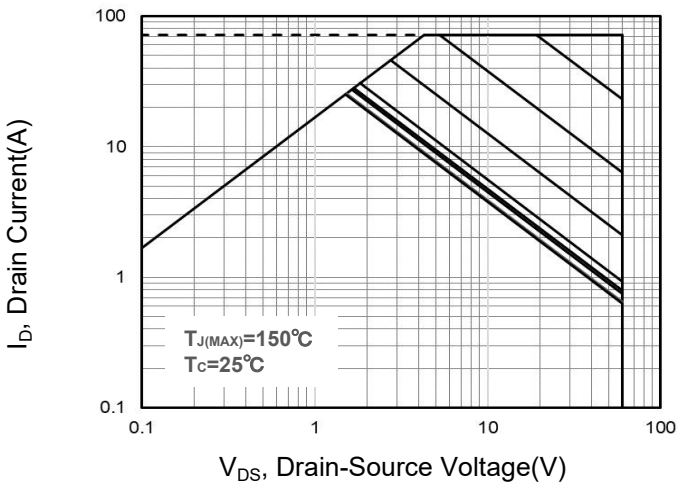
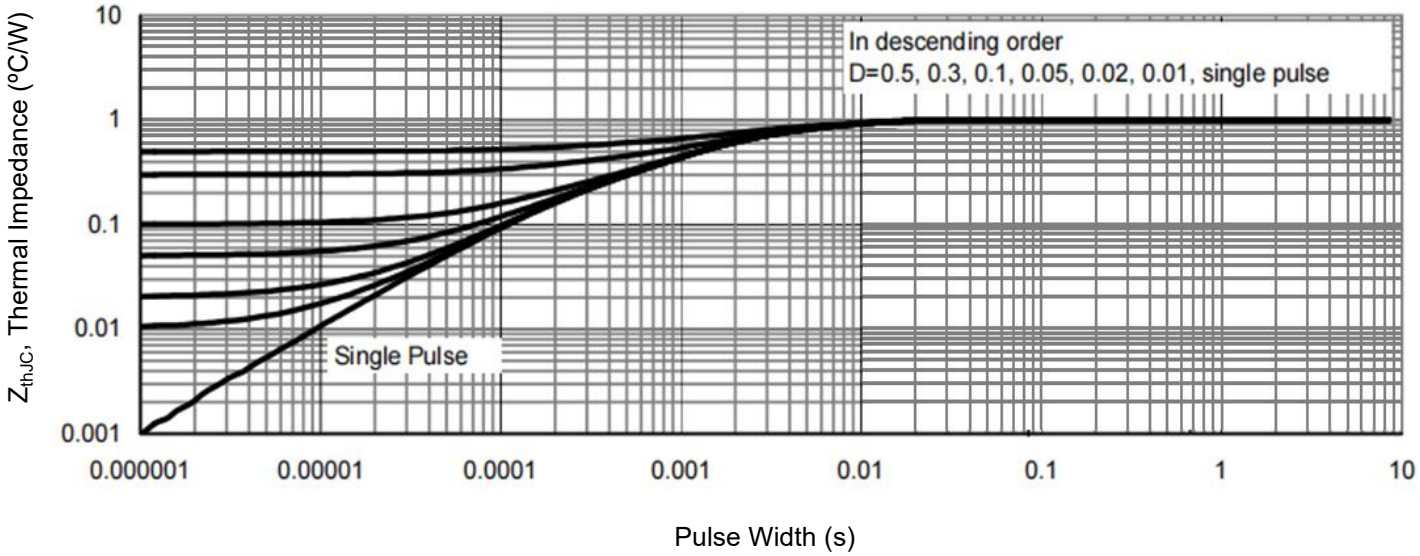


Figure 9. Normalized Maximum Transient Thermal Impedance

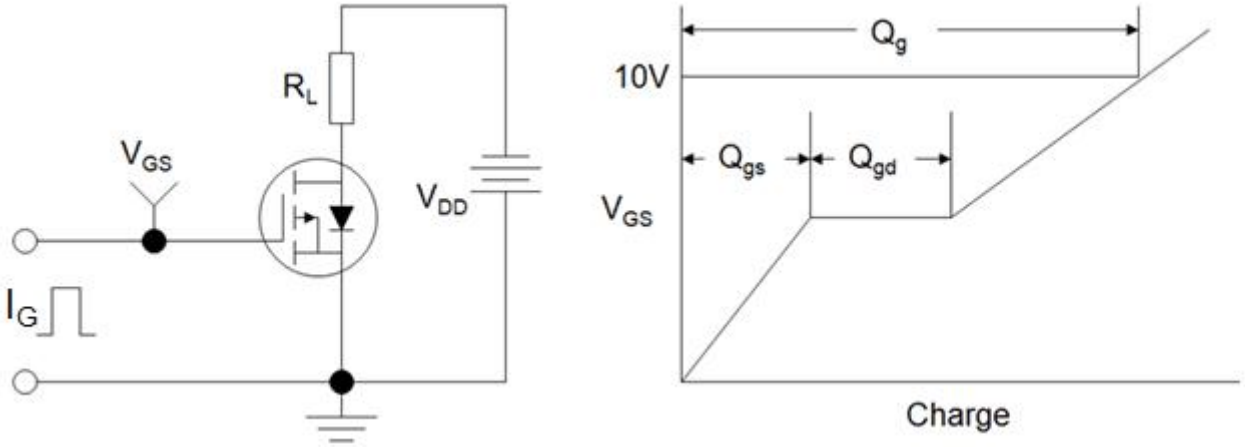


PMOS Specifications T_J = 25ºC, unless otherwise noted						
Parameter	**Symbol**	**Test Conditions**	**Value**			**Unit**
			Min.	**Typ.**	**Max.**	
Static Parameters						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = -250μA	-60	--	--	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -60V, V_{GS} = 0V	--	--	-1	μA
Gate-Source Leakage	I_{GSS}	V_{GS} = ±20V	--	--	±100	nA
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250μA	-1.5	-2.5	-3.5	V
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = -10V, I_D = -12A	--	33	45	mΩ
Forward Transconductance	g_{FS}	V_{DS} = -5V,I_D = -12A	--	9	--	S
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = -30V, f = 1.0MHz	--	2696	--	pF
Output Capacitance	C_{oss}		--	201	--	
Reverse Transfer Capacitance	C_{rss}		--	160	--	
Total Gate Charge	Q_g	V_{DD} = -30V, I_D = -12A, V_{GS} = -10V	--	25	--	nC
Gate-Source Charge	Q_{gs}		--	4	--	
Gate-Drain Charge	Q_{gd}		--	7	--	
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = -30V, I_D = -12A, R_G = 6Ω	--	15	--	ns
Turn-on Rise Time	t_r		--	58	--	
Turn-off Delay Time	$t_{d(off)}$		--	30	--	
Turn-off Fall Time	t_f		--	36	--	
Drain-Source Body Diode Characteristics						
Continuous Body Diode Current	I_S	T_C = 25ºC	--	--	-18	A
Body Diode Voltage	V_{SD}	T_J = 25ºC, I_{SD} = -12A, V_{GS} = 0V	--	--	-1.2	V
Reverse Recovery Charge	Q_{rr}	I_F = -12A, V_{GS} = 0V di/dt=-100A/us	--	19	--	nC
Reverse Recovery Time	T_{rr}		--	20	--	ns

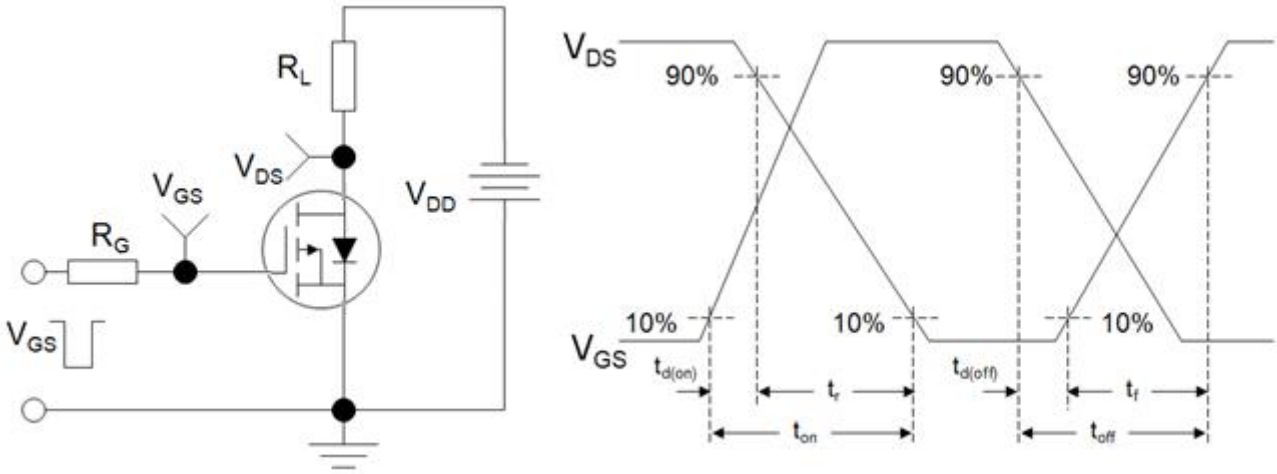
Notes

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. EAS condition : Tj=25℃ ,VDD=-50V,VGS=-10V,L=0.5mH,Rg=25Ω
   The table shows the minimum avalanche energy, which is 156mJ when the device is tested until failure
3. Identical low side and high side switch with identical R_G

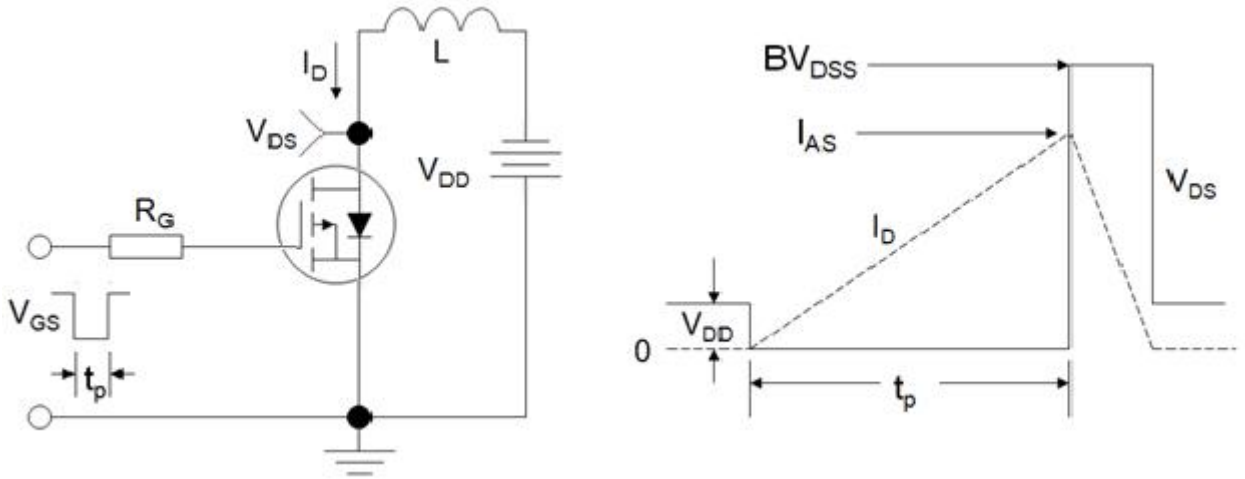
Gate Charge Test Circuit



Switch Time Test Circuit



EAS Test Circuit



PMOS Typical Characteristics T_J = 25ºC, unless otherwise noted

Figure 1. Output Characteristics

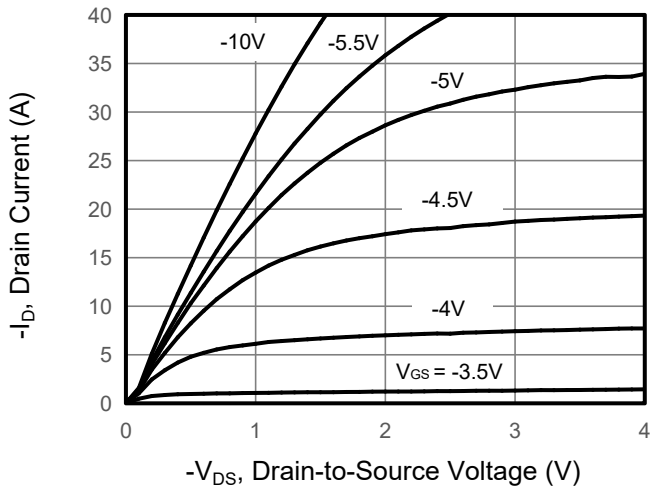


Figure 2. Transfer Characteristics

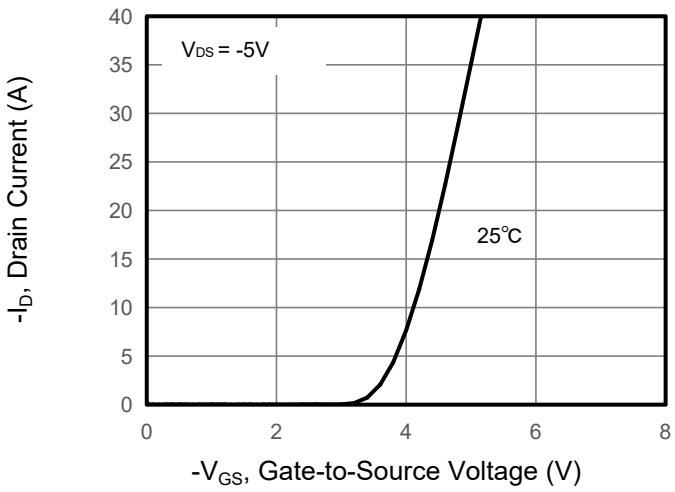


Figure 3.Drain Source On Resistance

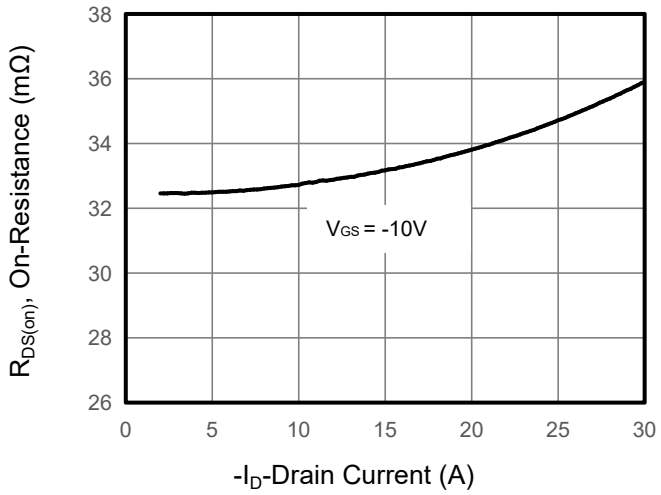


Figure 4. Gate Charge

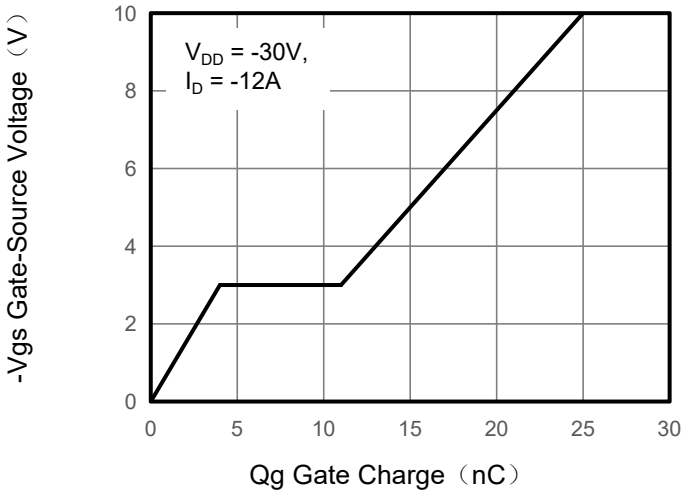


Figure 5. Capacitance

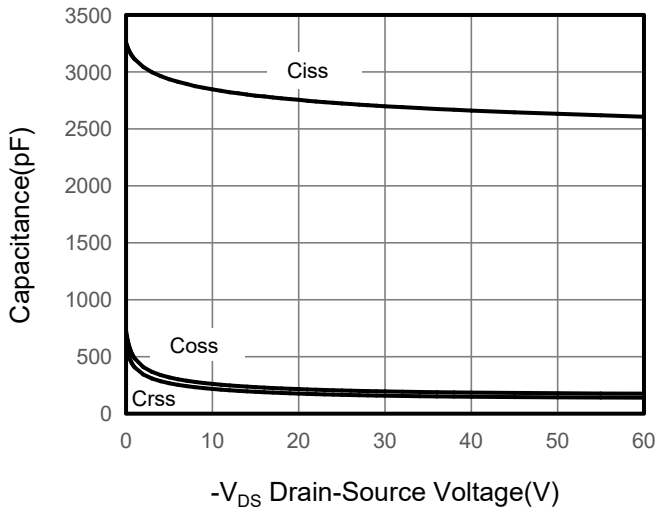
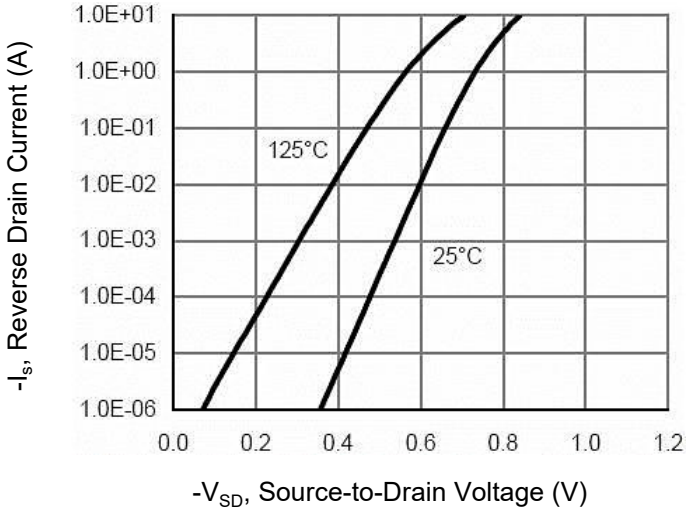


Figure 6. Source-Drain Diode Forward



PMOS Typical Characteristics T_J = 25ºC, unless otherwise noted

Figure 7. Drain-Source On-Resistance

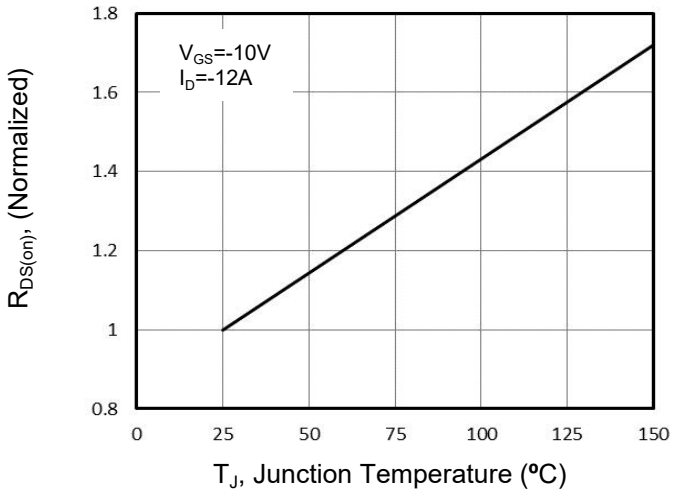


Figure 10. Safe Operation Area

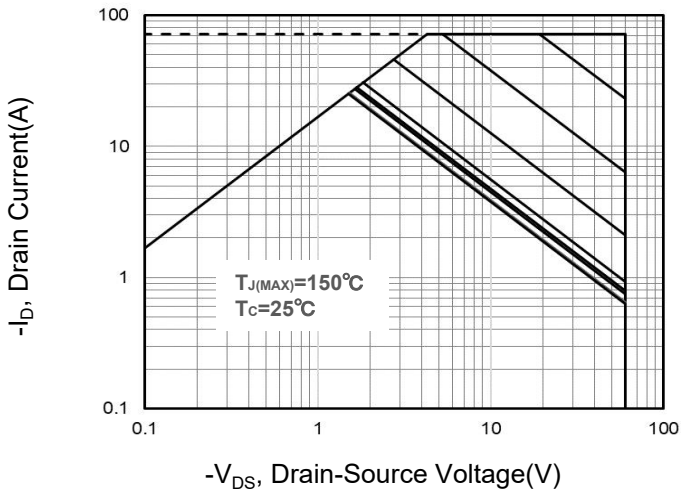
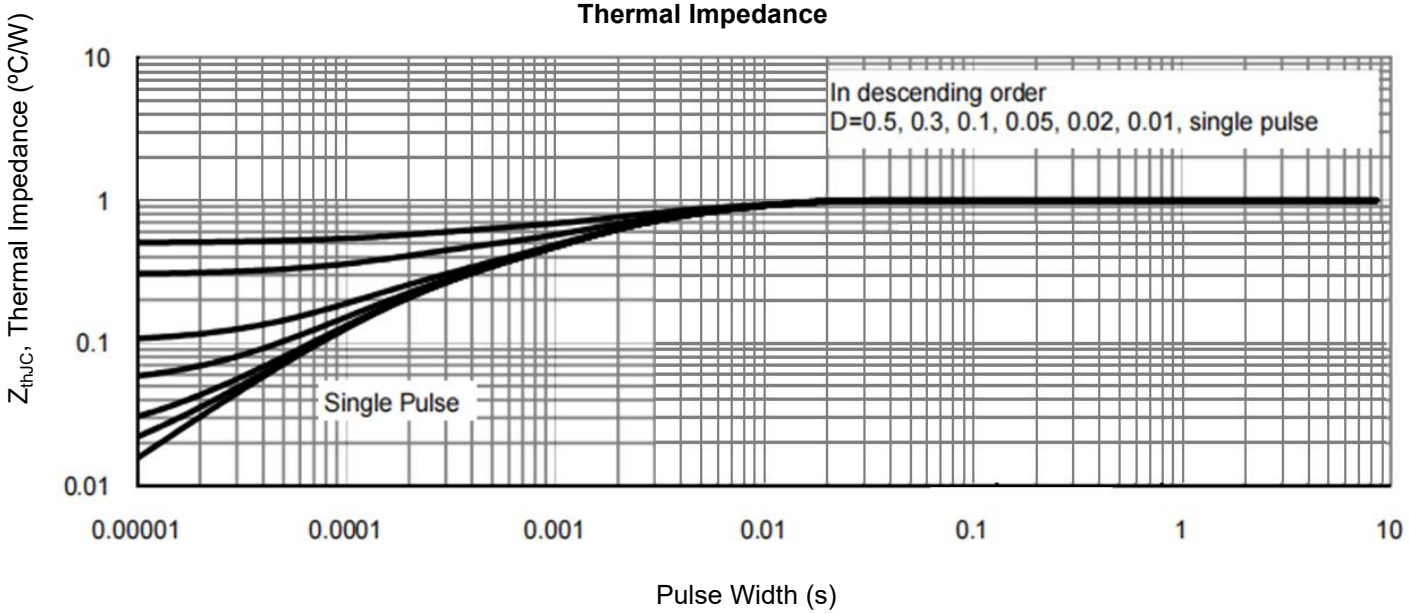
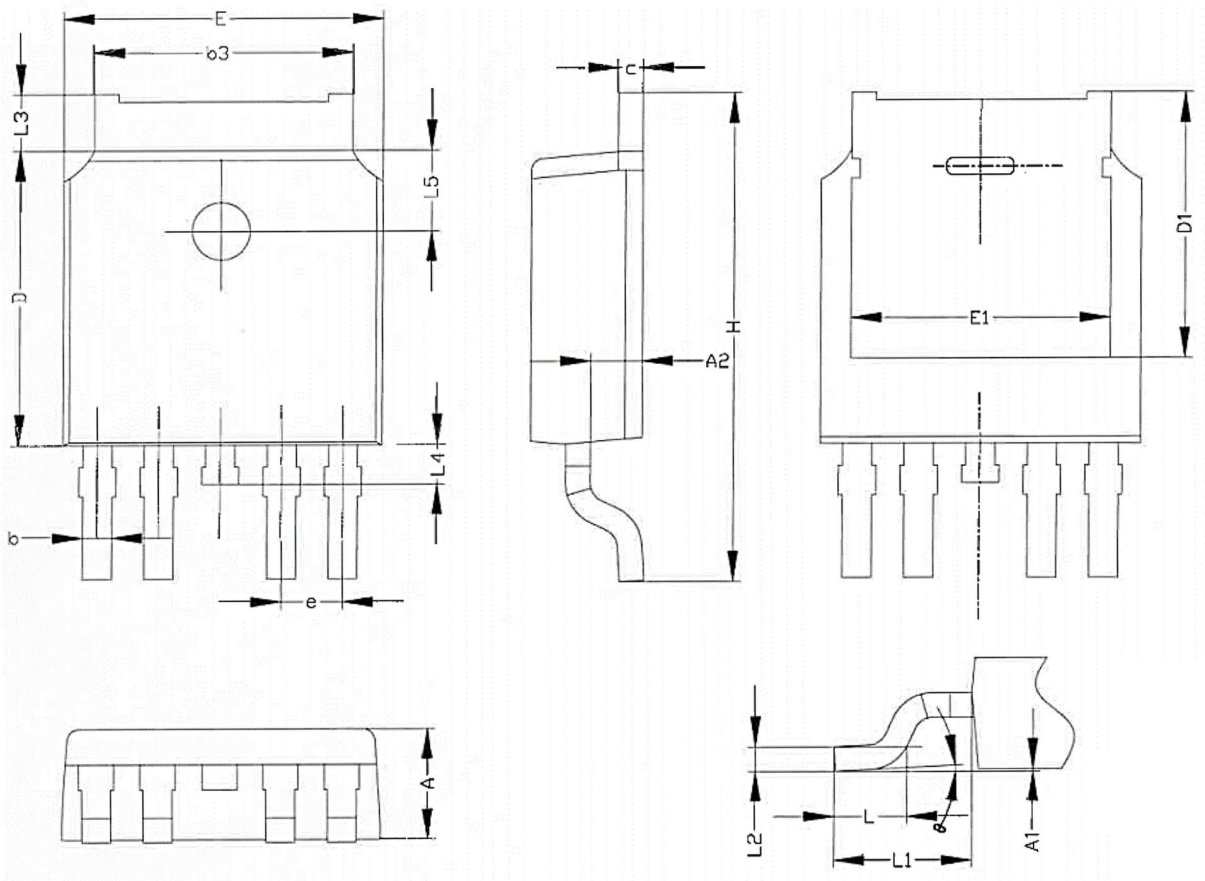


Figure 9. Normalized Maximum Transient Thermal Impedance



TO-252-4 Dual Package Information



SYMBOL	mm		
	MIN	NOM	MAX
A	2.20	2.30	2.38
A1	0.00	–	0.20
A2	0.97	1.07	1.17
b	0.55	0.62	0.70
b3	5.20	5.33	5.46
c	0.43	0.53	0.61
D	5.98	6.10	6.22
D1	5.30REF		
E	6.40	6.60	6.73
E1	5.10	–	–
e	1.27BSC		
H	9.40	10.10	10.50
L	1.38	1.50	1.75
L1	2.90REF		
L2	0.51BSC		
L3	0.88	–	1.28
L4	0.50	–	1.00
L5	1.65	1.80	1.95
θ	0°	–	8°