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TFT | CHARACTER | UWVD | FSC | SEGMENT | CUSTOM | REPLACEMENT

Character OLED Module

Part Number

O204B-CY-YS5

Overview:

- 20x4 Character OLED
- Yellow Pixel Color
- 92.0mm W x 31.5mm H
- Parallel and Serial Interfaces
- -40C to 80C Operating Temperature
- 2.4V-5.5V Input Voltage
- Controller: US2066
- RoHS Compliant

Character OLED Features:

Characters: 20x4

Interface: 4/8 Bit Parallel / SPI / I2C

Controller: US2066

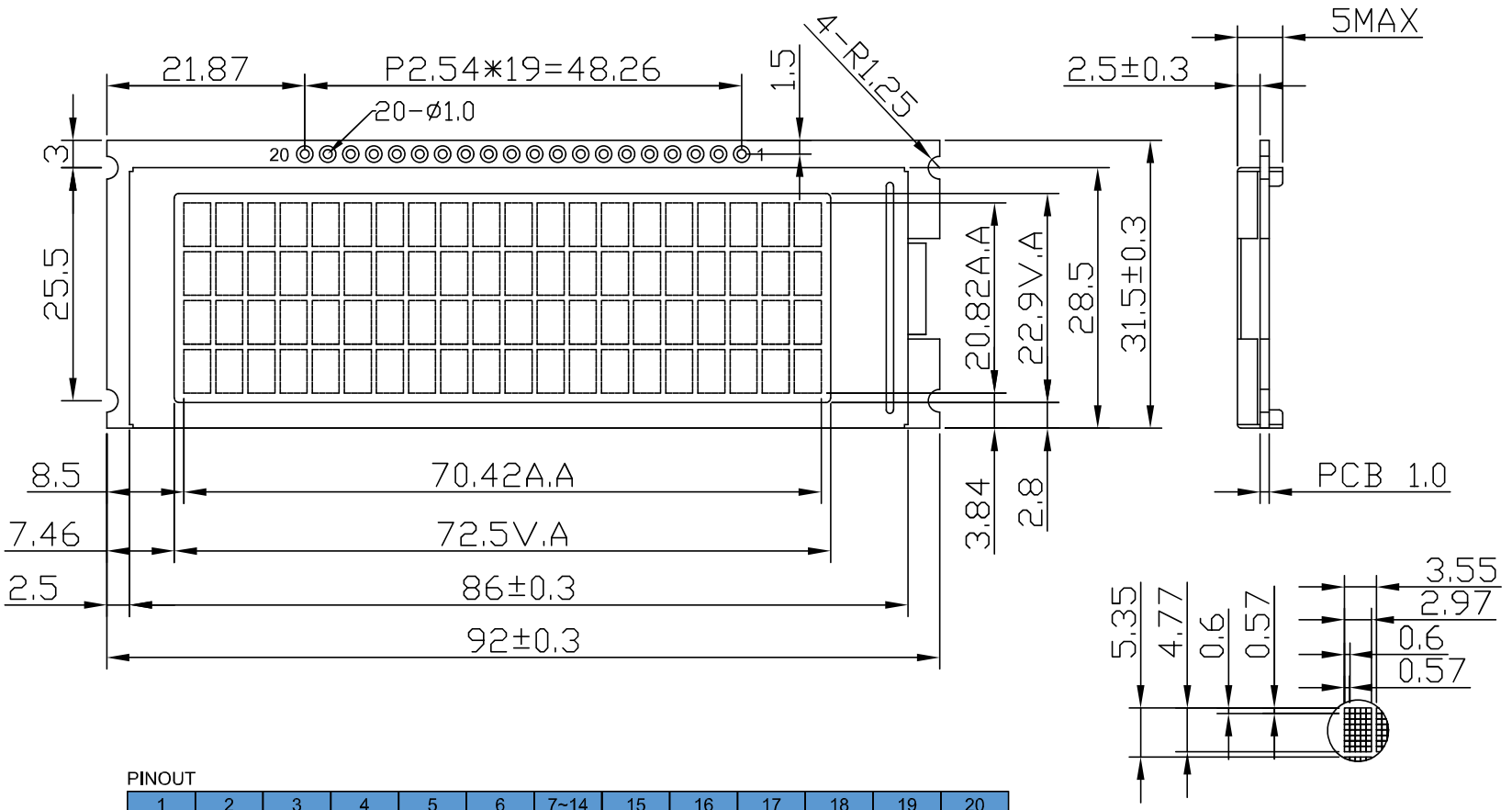
RoHS Compliant

General Information Items	Specification	Unit	Note
	Main Panel		
Viewing Area	72.5 x 22.9	mm	-
Pixel Color	Yellow	-	-
Viewing Direction	Free	-	-
Voltage	2.8~5.5	V	-
Characters	20x4	-	-
Controller IC	US2066	-	-
Interface	4/8 Bit Parallel / SPI / I2C	-	-
Operating temperature	-40～+85	℃	-
Storage temperature	-40～+90	℃	-

Mechanical Information

Item		Min	Typ.	Max	Unit	Note
Module size	X (Width)	-	92	-	mm	-
	Y (Height)	-	31.5	-	mm	-
	Z (Depth)	-	-	5	mm	-

Outline Drawings



PINOUT

1	2	3	4	5	6	7~14	15	16	17	18	19	20
VSS	VDD	REGVDD	D/C	R/W(WR)	E(RD)	D0~D7	CS	RES	BS0	BS1	BS2	FGND

Notes:

1. Display Mode: Passive Matrix
2. Display Color: Yellow (Monochrome)
3. Supply Voltage: 2.4V-5.5V
4. Viewing Angle: Free
5. Driver IC: US2066
6. Interface: 4/8 Bit Parallel / SPI / I2C
7. Operating Temp: -40°C to 80°C
8. Storage Temp: -40°C to 90°C
9. RoHS Compliant

Model Name: O204B-CY-YS5		FocusLCDs.com LCDs MADE SIMPLE®	
General Tol: ± 0.3			
Approvals	Date	Drawing No.:	Scale:
DWN:			
CHK:		Size:	Unit: / Page: 1/1
APP:			

2. Input Terminal Pin Assignment

NO.	Symbol	Description	I/O
1	VSS	Negative Power Supply, Ground	-
2	VDD	Positive Power Supply	-
3	REGVDD	5V I/O Regulator Configuration	-
4	D/C	Data/Command Control	I
5	R/W(WR)	Read/Write Select or Write	I
6	E(RD)	Read/Write Enable or Read	I/O
7~14	D0~D7	Host Data Input/Output Bus These pins are 8-bit bi-directional data bus to be connected to the microprocessor's data bus. When serial mode is selected, D0 will be the serial clock input SCLK; D1 will be the serial data input SID and D2 will be the serial clock output SOD. When I2C mode is selected, D2, D1 should be tired together and serve as SDAOUT, SDAIN in application and D0 is the serial clock input, SCL. Unused pins must be connected to VSS	I/O
15	CS	Chip Select	O
16	RES	Power Reset for Controller and Driver	O
17~19	BS0~BS2	Communicating Protocol Selection 010: I2C; 000: SPI 101: 4bit 6800; 111: 4bit 8080 001: 8bit 6800; 011: 8bit 8080	O
20	FGND	Frame Ground	

3. Optical Characteristics

Item		Symbol	Condition	Min	Typ.	Max	Unit	Note
Contrast Ratio		CR		--	10000:1	--	--	
CIE (Yellow)	x	TR		0.46	0.50	0.54		
	y	TF		0.45	0.49	0.53		
Viewing Angle				--	Free	--	degree	
Brightness		Lbr		100	120	-	nits	

4. Electrical Characteristics

4.1 Absolute Maximum Rating (Ta=25 ˚C, VSS=0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Operating Temperature	TOP	-40	-	+85	□C
Storage Temperature	TST	-40	-	+90	□C
Supply Voltage for Logic	Vdd	-0.3		6.0	V
Supply Voltage for I/O Pins	Vddio	-0.3		6.0	V
Supply Voltage for Display	Vcc	0	-	15	V
Life Time(120 cd/m2)		40000	-	-	hour
Life Time(100 cd/m2)		1500000	-	-	hour

NOTE: If the absolute maximum rating of the above parameters is exceeded, even momentarily, the quality of the product may be degraded. Absolute maximum ratings specify the values which the product may be physically damaged if exceeded. Be sure to use the product within the range of the absolute maximum ratings.

4.2 DC Electrical Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage for Logic	VDD	-	2.4	2.8	VDDIO	V
Supply Voltage for I/O Pins	VDDIO	Ta=25□C	2.4	2.8	3.6	V
Supply Voltage for Logic	VDD	(5V I/O Application)	-	-	-	V
Supply Voltage For I/O Pins	VDDIO		4.4	5.0	5.5	V
Supply Voltage For I/O Display	Vcc	VF=3.5V	11.5	12.0	12.5	V
High Level Input	VIH	IOUT=100uA,3.3MHz	0.8x VDDIO		VDDIO	V
Low Level Input	VIL		0	-	0.2xVDD IO	V
High Level Input	VOH		0.9x VDDIO	-	VDDIO	V
Low Level Input	VOL		0	-	0.1xVDD IO	V
Operating Current for VDD	IDD	VDDIO = 2.8V or 5.0V, VCC = 12.0V	--	0.18	0.3	mA
Operating Current for VCC	ICC		-	15.2	60	mA
Sleep Mode Current for VDD	IDD,SLEEP		-	1	10	uA
Sleep Mode Current for VCC	ICC,SLEEP		-	2	10	uA

5. Signal Timing Characteristics

5.1 6800-Series MCU Parallel Interface Timing Characteristics

(TA = 25 °C , V_{DDIO} = 2.4-3.6/ 4.4-5.5V, V_{SS} =0V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time (write cycle)	400	-	-	ns
t_{AS}	Address Setup Time	13	-	-	ns
t_{AH}	Address Hold Time	17	-	-	ns
t_{CS}	Chip Select Time	0	-	-	ns
t_{CH}	Chip Select Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	35	-	-	ns
t_{DHW}	Write Data Hold Time	18	-	-	ns
t_{DHR}	Read Data Hold Time	13	-	-	ns
t_{OH}	Output Disable Time	-	-	90	ns
t_{ACC}	Access Time (RAM) Access Time (command)	-	-	200	ns ns
PW_{CSL}	Chip Select Low Pulse Width (read RAM) Chip Select Low Pulse Width (read Command) Chip Select Low Pulse Width (write)	250 250 50	- - -	- - -	ns ns ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	155 55	- -	- -	ns ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Note
(1) All timings are based on 20% to 80% of V_{DDIO}-V_{SS}

Figure 12-1: 6800-series parallel interface characteristics (Form 1: CS# low pulse width > E high pulse width)

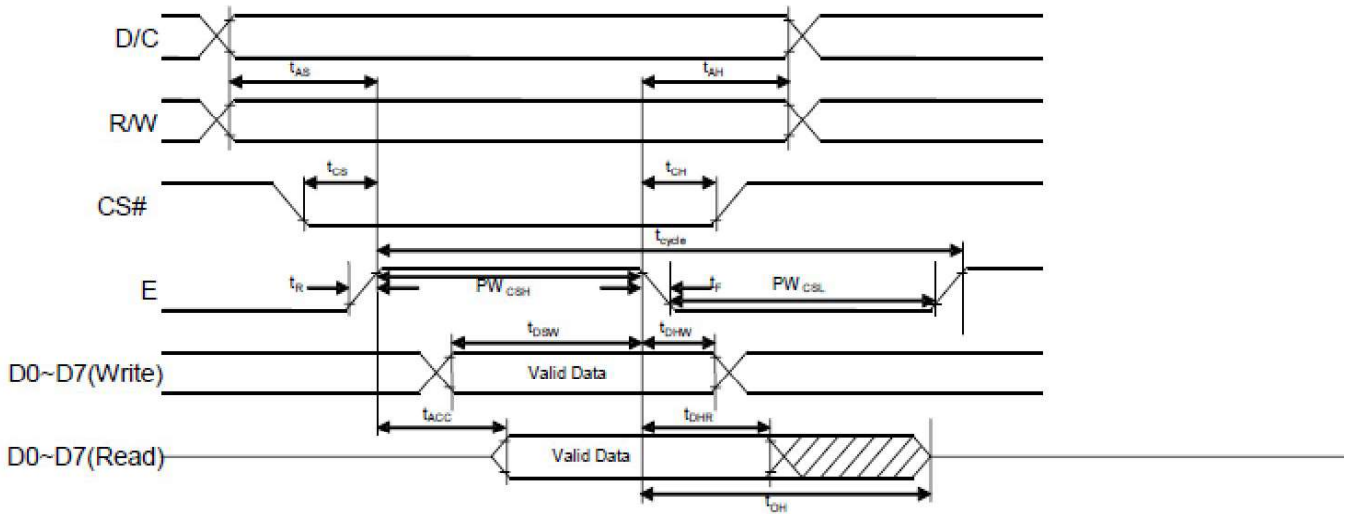
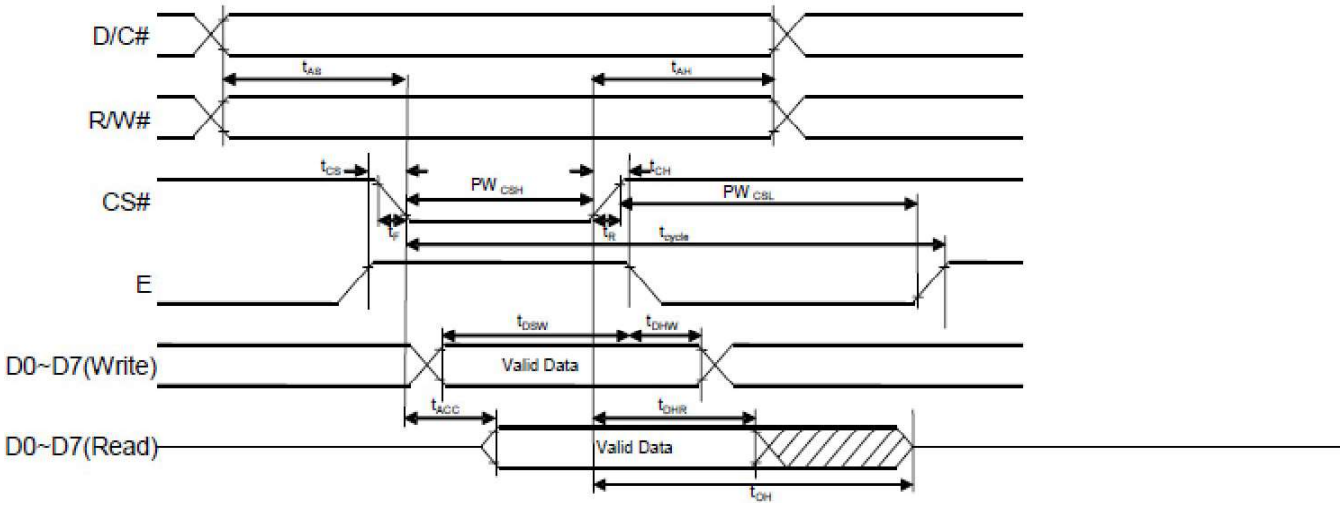


Figure 12-2: 6800-series parallel interface characteristics (Form 2: CS# low pulse width < E high pulse width)



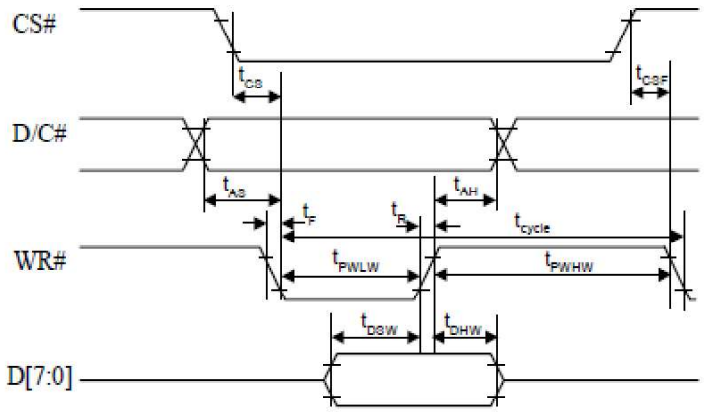
5.2 8080-Series MCU Parallel Interface Timing Characteristics

(T_A = 25°C, V_{DDIO} = 2.4-3.6/ 4.4-5.5V, V_{SS} =0V)

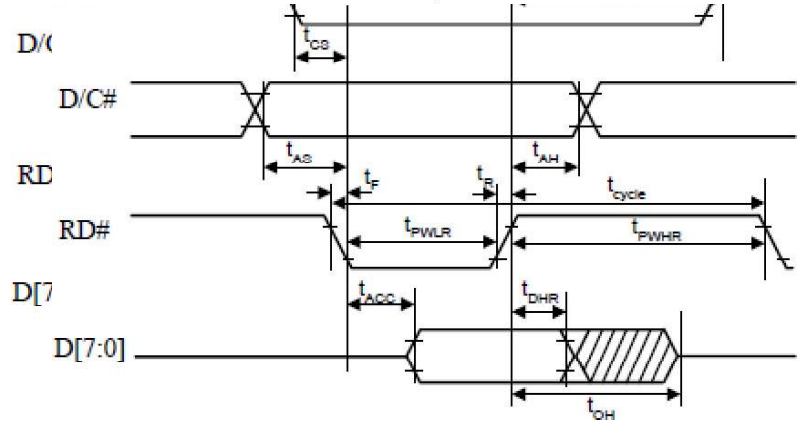
Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time (write cycle)	400	-	-	ns
t_{AS}	Address Setup Time	13	-	-	ns
t_{AH}	Address Hold Time	17	-	-	ns
t_{CS}	Chip Select Time	0	-	-	ns
t_{CSH}	Chip select hold time to read signal	.0	-	-	ns
t_{CSF}	Chip select hold time	0	-	-	ns
t_{DSW}	Write Data Setup Time	35	-	-	ns
t_{DHW}	Write Data Hold Time	18	-	-	ns
t_{DHR}	Read Data Hold Time	13	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time (RAM) Access Time (command)	-	-	200	ns ns
PW_{CSL}	Chip Select Low Pulse Width (read RAM) - t_{PWLR} Chip Select Low Pulse Width (read Command) - t_{PWLR} Chip Select Low Pulse Width (write) - t_{PWLW}	250 250 50	- - -	- - -	ns ns ns
PW_{CSH}	Chip Select High Pulse Width (read) - t_{PWHR} Chip Select High Pulse Width (write) - t_{PWHW}	155 55	- -	- -	ns ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Figure 12-3 : 8080-series parallel interface characteristics

Write cycle



Read Cycle



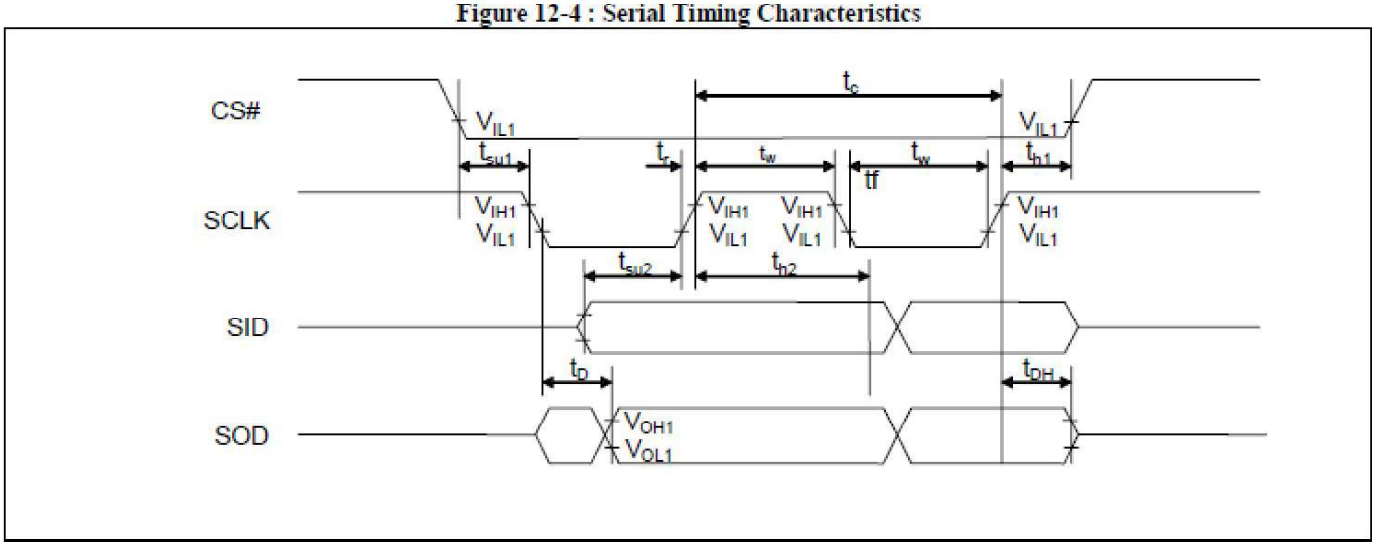
5.3 Serial Interface Timing Characteristics

(T_A = 25°C, V_{DDIO} = 2.4-3.6/ 4.4-5.5V, V_{SS} =0V)

Symbol	Parameter	Min	Typ	Max	Unit
t_c	Serial clock cycle time	1	-	20	us
t_r, t_f	Serial clock rise/fall time	-	-	15	ns
t_w	Serial clock width (high, low)	400	-	-	ns
t_{su1}	Chip select setup time	60	-	-	ns
t_{h1}	Chip select hold time	20	-	-	ns
t_{su2}	Serial input data setup time	200	-	-	ns
t_{h2}	Serial input data hold time	20	-	-	ns
t_D	Serial output data delay time	200	-	-	ns
t_{DH}	Serial output data hold time	10	-	-	ns

Note: All timings are based on 20% to 80% of V_{DDIO}-V_{SS}

Figure 12-4 : Serial Timing Characteristics



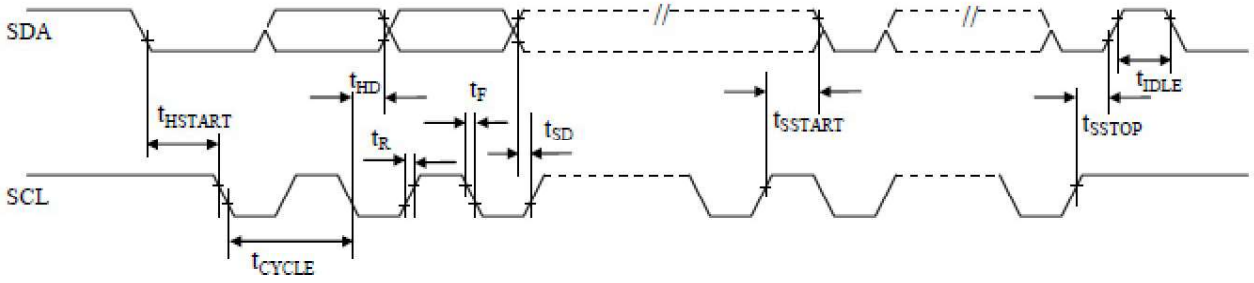
5.4 I2C Timing Characteristics

(T_A = 25°C, V_{DDIO} = 2.4-3.6/ 4.4-5.5V, V_{SS} =0V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	2.5	-	-	us
t_{HSTART}	Start condition Hold Time	0.6	-	-	us
t_{HD}	Data Hold Time (for "SDA_{OUT}" pin)	5	-	-	ns
	Data Hold Time (for "SDA_{IN}" pin)	460	-	-	ns
t_{SD}	Data Setup Time	100	-	-	ns
t_{SSTART}	Start condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	-	us
t_{SSTOP}	Stop condition Setup Time	0.6	-	-	us
t_R	Rise Time for data and clock pin	-	-	300	ns
t_F	Fall Time for data and clock pin	-	-	300	ns
t_{IDLE}	Idle Time before a new transmission can start	1.3	-	-	us

Note: All timings are based on 20% to 80% of V_{DDIO}-V_{SS}

Figure 12-5 : I²C Timing Characteristics



6. Command Summary

1. Fundamental Command Set													
Command	IS	RE	SD	Instruction Code D/C#	R/W# (WR#)	D7	D6	D5	D4	D3	D2	D1	D0	Description
Clear Display	X	X	0	0	0	0	0	0	0	0	0	0	1	Write "20H" to DDRAM and set DDRAM address to "00H" from AC.
Return Home	X	0	0	0	0	0	0	0	0	0	0	1	*	Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed.
Entry Mode Set	X	0	0	0	0	0	0	0	0	0	1	I/D	S	Assign cursor / blink moving direction with DDRAM address. I/D = "1": cursor/ blink moves to right and DDRAM address is increased by 1 (POR) I/D = "0": cursor/ blink moves to left and DDRAM address is decreased by 1 Assign display shift with DDRAM address. S = "1": make display shift of the enabled lines by the DS4 to DS1 bits in the shift enable instruction. Left/ right direction depends on I/D bit selection. S = "0": display shift disable (POR)
	X	1	0	0	0	0	0	0	0	0	1	BDC	BDS	Common bi-direction function. BDC = "0": COM31 -> COM0 BDC = "1": COM0 -> COM31 Segment bi-direction function. BDS = "0": SEG99 -> SEG0, BDS = "1": SEG0 -> SEG99
Display ON / OFFControl	X	0	0	0	0	0	0	0	0	1	D	C	B	Set display/cursor/blink ON/OFF D = "1": display ON, D = "0": display OFF (POR), C = "1": cursor ON, C = "0": cursor OFF (POR), B = "1": blink ON, B = "0": blink OFF (POR). **Note**: It is recommended to turn off the cursor and blinking effects when updating internal RAM contents for better visual performance; refer to Section 9.1.4 for details

1. Fundamental Command Set														
Command	IS	RE	SD	Instruction Code										Description
				D/C#	R/W# (WR#)	D7	D6	D5	D4	D3	D2	D1	D0	
Clear Display	X	X	0	0	0	0	0	0	0	0	0	0	1	Write "20H" to DDRAM and set DDRAM address to "00H" from AC.
Return Home	X	0	0	0	0	0	0	0	0	0	0	1	*	Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed.
Entry Mode Set	X	0	0	0	0	0	0	0	0	0	1	I/D	S	Assign cursor / blink moving direction with DDRAM address. I/D = "1": cursor/ blink moves to right and DDRAM address is increased by 1 (POR) I/D = "0": cursor/ blink moves to left and DDRAM address is decreased by 1 Assign display shift with DDRAM address. S = "1": make display shift of the enabled lines by the DS4 to DS1 bits in the shift enable instruction. Left/ right direction depends on I/D bit selection. S = "0": display shift disable (POR)
	X	1	0	0	0	0	0	0	0	0	1	BDC	BDS	Common bi-direction function. BDC = "0": COM31 -> COM0 BDC = "1": COM0 -> COM31 Segment bi-direction function. BDS = "0": SEG99 -> SEG0, BDS = "1": SEG0 -> SEG99
Display ON / OFFControl	X	0	0	0	0	0	0	0	0	1	D	C	B	Set display/cursor/blink ON/OFF D = "1": display ON, D = "0": display OFF (POR), C = "1": cursor ON, C = "0": cursor OFF (POR), B = "1": blink ON, B = "0": blink OFF (POR). **Note**: It is recommended to turn off the cursor and blinking effects when updating internal RAM contents for better visual performance; refer to Section 9.1.4 for details

1. Fundamental Command Set														
Command	IS	RE	SD	Instruction Code D/C#	R/W# (WR#)	D7	D6	D5	D4	D3	D2	D1	D0	Description
Function Set	X	0	0	0	0	0	0	1	*	N	DH	RE (0)	IS	Numbers of display line, N when N = "1" (POR): 2-line (NW=0b) / 4-line (NW=1b), when N = "0": 1-line (NW=0b) / 3-line (NW=1b) DH = " 1/0": Double height font control for 2-line mode enable/ disable (POR=0) Extension register, RE ("0") Extension register, IS
	X	1	0	0	0	0	0	1	*	N	BE	RE (1)	REV	CGRAM blink enable BE = 1b: CGRAM blink enable BE = 0b: CGRAM blink disable (POR) Extension register, RE ("1") Reverse bit REV = "1": reverse display, REV = "0": normal display (POR)
Set CGRAM address	0	0	0	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter. (POR=00 0000)
Set DDRAM Address	X	0	0	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address counter. (POR=000 0000)
Set Scroll Quantity	X	1	0	0	0	1	*	SQ5	SQ4	SQ3	SQ2	SQ1	SQ0	Set the quantity of horizontal dot scroll. (POR=00 0000) Valid up to SQ[5:0] = 110000b
Read Busy Flag and Address/ Part ID	X	X	0	0	1	BF	AC6 / ID6	AC5 / ID5	AC4 / ID4	AC3 / ID3	AC2 / ID2	AC1 / ID1	AC0 / ID0	Can be known whether during internal operation or not by reading BF. The contents of address counter or the part ID can also be read. When it is read the first time, the address counter can be read. When it is read the second time, the part ID can be read. BF = "1": busy state BF = "0": ready state
Write data	X	X	0	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM / CGRAM).
Read data	X	X	0	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM / CGRAM).

Notes
(1) POR stands for Power On Reset Values.
(2) "*" and "X" stand for "Don't care".

2. Extended Command Set

Command	IS	RE	SD	Instruction Code											Description
				D/C#	R/W# (WR#)	Hex	D7	D6	D5	D4	D3	D2	D1	D0	
Function Selection A	X	1	0	0	0	71	0	1	1	1	0	0	0	1	A[7:0] = 00h, Disable internal V_{DD} regulator at 5V I/O application mode A[7:0] = 5Ch, Enable internal V_{DD} regulator at 5V I/O application mode (POR)
	X	1	0	1	0	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	
Function Selection B	X	1	0	0	0	72	0	1	1	1	0	0	1	0	OP[1:0]: Select the character no. of character generator OP[1:0] / CGROM / CGRAM 00b / 240 / 8 01b / 248 / 8 10b / 250 / 6 11b / 256 / 0 RO[1:0]: Select character ROM RO[1:0] / ROM 00b / A 01b / B 10b / C 11b / Invalid **Note:** It is recommended to turn off the disply (cmd 08h) before setting no. of CGRAM and defining character ROM, while clear display (cmd 01h) is recommended to sent afterwards
	X	1	0	1	0		*	*	*	*	RO1	RO0	OP1	OP0	
OLED Characterization	X	1	X	0	0	78 / 79	0	1	1	1	1	0	0	SD	Extension register, SD SD = 0b: OLED command set is disabled (POR) SD = 1b: OLED command set is enabled Details refer to Table 8-3.

Notes
(1) POR stands for Power On Reset Values.
(2) "*" and "X" stand for "Don't care".

3. OLED Command Set

Command	IS	RE	SD	D/C#	R/W# (WR#)	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Description
Set Contrast Control	X	1	1	0	0	81	1	0	0	0	0	0	0	1	Double byte command to select 1 out of 256 contrast steps. Contrast increases as the value increases. (POR = 7Fh)
	X	1	1	0	0	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	
Set Display Clock Divide Ratio/Oscillator Frequency	X	1	1	0	0	D5	1	1	0	1	0	1	0	1	A[3:0] : Define the divide ratio (D) of the display clocks (DCLK): Divide ratio= A[3:0] + 1 (POR=0000b) A[7:4] : Set the Oscillator Frequency, F_{OSC}. Oscillator Frequency increases with the value of A[7:4] and vice versa. (POR=0111b) Range:0000b~1111b Frequency increases as setting value ncreases.
	X	1	1	0	0	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	
Set Phase Length	X	1	1	0	0	D9	1	1	0	1	1	0	0	1	A[3:0] : Phase 1 period of up to 32 DCLK; clock 0 is an valid entry with 2 DCLK (POR=1000b) A[7:4] : Phase 2 period of up to 15 DCLK; clock 0 is invalid entry (POR=0111b)
	X	1	1	0	0	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	
Set SEG Pins Hardware Configuration	X	1	1	0	0	DA	1	1	0	1	1	0	1	0	A[4]=0b, Sequential SEG pin configuration A[4]=1b (POR), Alternative (odd/even) SEG pin configuration A[5]=0b (POR), Disable SEG Left/Right remap A[5]=1b, Enable SEG Left/Right remap Refer to Table 8-4 for details
	X	1	1	0	0	A[5:4]	0	0	A_5	A_4	0	0	0	0	
Set V_{COMH} Deselect Level	X	1	1	0	0	DB	1	1	0	1	1	0	1	1	
	X	1	1	0	0	A[6:4]	0	A_6	A_5	A_4	0	0	0	0	

A[6:4]	Hex code	V_{COMH} deselect level
000b	00h	~ 0.65 x V_{CC}
001b	10h	~ 0.71 x V_{CC}
010b	20h	~ 0.77 x V_{CC} (POR)
011b	30h	~ 0.83 x V_{CC}
100b	40h	1 x V_{CC}

3. OLED Command Set

Command	IS	RE	SD	D/C#	R/W# (WR#)	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Description
Function Selection C	X	1	1	0	0	DC	1	1	0	1	1	1	0	0	Set VSL & GPIO
	X	1	1	0	0	A[7:0]	A_7	0	0	0	0	0	A_1	A_0	Set VSL: A[7] = 0b: Internal VSL (POR) A[7] = 1b: Enable external VSL Set GPIO: A[1:0] = 00b represents GPIO pin HiZ, input disabled (always read as low) A[1:0] = 01b represents GPIO pin HiZ, input enabled A[1:0] = 10b represents GPIO pin output Low (RESET) A[1:0] = 11b represents GPIO pin output High
Set Fade Out and Fade in / out	X	1	1	0	0	23	0	0	1	0	0	0	1	1	A[5:4] = 00b Disable Fade Out / Blinking Mode[RESET] A[5:4] = 10b Enable Fade Out mode. Once Fade Mode is enabled, contrast decrease gradually to all pixels OFF. Output follows RAM content when Fade mode is disabled. A[5:4] = 11b Enable Fade in / out mode. Once Fade in / out mode is enabled, contrast decrease gradually to all pixels OFF and than contrast increase gradually to normal display. This process loop continuously until the Fade in / out mode is disabled. A[3:0] : Set time interval for each fade step
	X	1	1	0	0	A[5:0]	*	*	A_5	A_4	A_3	A_2	A_1	A_0	

A[3:0]	Time interval for each fade step
0000b	8 Frames
0001b	16 Frames
0010b	24 Frames
:	:
1110b	120 Frames
1111b	128 Frames

Note
(1) POR stands for Power On Reset Values.
(2) "*" and "X" stand for "Don't care".
(3) The locked OLED driver IC MCU interface prohibits all commands access except logic bit SD is set to 1b.
(4) Refer to Table 8-1 and
Table 8-2 for the details of logic bits IS, RE and SD.

7. Cautions and Handling Precautions

7.1 Handling and Operating the Module

1. When the module is assembled, it should be attached to the system firmly. Do not warp or twist the module during assembly work.
2. Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.
3. Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.
4. Do not allow drops of water or chemicals to remain on the display surface. If you have the droplets for a long time, staining and discoloration may occur.
5. If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.
6. The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane. Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.
7. If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.
8. Protect the module from static, it may cause damage to the CMOS ICs.
9. Use fingerstalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.
10. Do not disassemble the module.
11. Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.
12. Pins of I/F connector shall not be touched directly with bare hands.
13. Do not connect, disconnect the module in the “Power ON” condition.
14. Power supply should always be turned on/off by the item Power On Sequence & Power Off Sequence.

7.2 Storage and Transportation

1. Do not leave the panel in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35 ℃ and relative humidity of less than 70%
2. Do not store the OLED module in direct sunlight.
3. The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.
4. It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module. In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.
5. This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.