

N-Channel Enhancement Mode Power MOSFET

Description

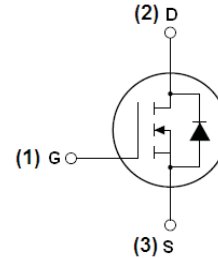
The RM100N40DF uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

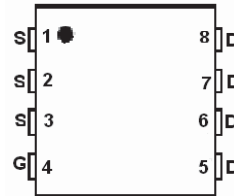
- $V_{DS} = 40V, I_D = 100A$
 $R_{DS(ON)} < 3.2 \text{ m}\Omega @ V_{GS} = 10V$
 $R_{DS(ON)} < 4.6 \text{ m}\Omega @ V_{GS} = 4.5V$
- High density cell design for ultra low R_{dson}
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

Application

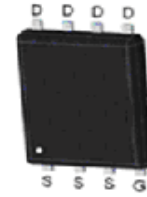
- Load switching
- Hard switched and high frequency circuits
- Uninterruptible power supply
- Halogen-free



Schematic diagram



Marking and pin assignment



DFN5X6-8L top view

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
100N40	RM100N40DF	DFN5X6-8L	-	-	-

Absolute Maximum Ratings ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ($T_C = 25^\circ\text{C}$)	I_D	100	A
Continuous Drain Current ($T_C = 100^\circ\text{C}$)	I_D	62	A
Pulsed Drain Current ⁽¹⁾	I_{DM}	420	A
Single Pulsed Avalanche Energy ⁽²⁾	E_{AS}	100	mJ
Power Dissipation	P_D	75	W
Thermal Resistance from Junction to Case	$R_{\theta JC}$	2	$^\circ\text{C}/\text{W}$
Thermal Resistance- Junction to Ambient	$R_{\theta JA}$	48	$^\circ\text{C}/\text{W}$
Junction Temperature	T_J	175	$^\circ\text{C}$
Storage Temperature	T_{STG}	-55~ +175	$^\circ\text{C}$

Electrical Characteristics (T_C=25°C unless otherwise noted)

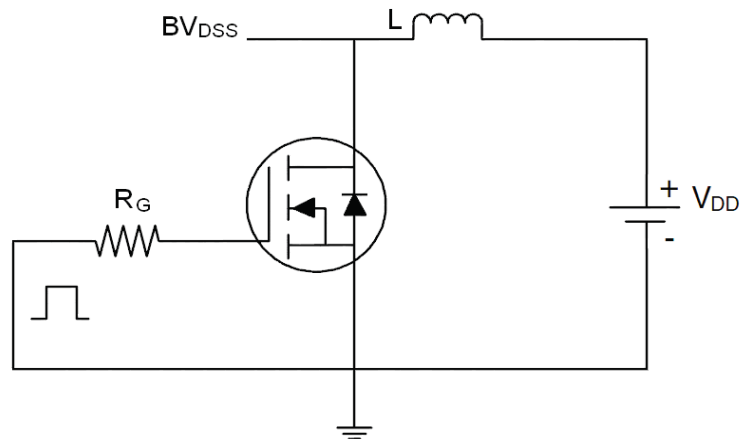
Parameter	Symbol	Test Condition	Min	Type	Max	Unit
Static Characteristics						
Drain-source breakdown voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = 250μA	40	-	-	V
Zero gate voltage drain current	I _{DSS}	V _{DS} = 40V, V _{GS} = 0V	-	-	1	μA
Gate-body leakage current	I _{GSS}	V _{GS} = ±20V, V _{DS} = 0V	-	-	±100	nA
Gate threshold voltage ⁽³⁾	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250μA	1.2	1.7	2.2	V
Drain-source on-resistance ⁽³⁾	R _{DSON}	V _{GS} = 10V, I _D = 30A	-	2.7	3.2	mΩ
		V _{GS} = 4.5V, I _D = 20A	-	3.8	4.6	
Gate Resistance	R _g	V _{DS} = V _{GS} = 0V, f = 1MHz	-	3.8	-	Ω
Dynamic characteristics						
Input Capacitance	C _{iss}	V _{DS} = 20V, V _{GS} = 0V, f = 1MHz	-	1827	-	pF
Output Capacitance	C _{oss}		-	623	-	
Reverse Transfer Capacitance	C _{rss}		-	22	-	
Switching characteristics						
Turn-on delay time	t _{d(on)}	V _{DD} = 20V, I _D = 20A, V _{GS} = 10V, R _G = 6Ω	-	6.2	-	ns
Turn-on rise time	t _r		-	27.4	-	
Turn-off delay time	t _{d(off)}		-	39.8	-	
Turn-off fall time	t _f		-	16.6	-	
Total Gate Charge	Q _g	V _{DS} = 20V, I _D = 20A, V _{GS} = 10V	-	28.3	-	nC
Gate-Source Charge	Q _{gs}		-	6.17	-	
Gate-Drain Charge	Q _{gd}		-	4.55	-	
Reverse Recovery Charge	Q _{rr}	I _F = 20A, di/dt = 100A/us	-	20	-	nC
Reverse Recovery Time	T _{rr}	I _F = 20A, di/dt = 100A/us	-	36	-	ns
Source-Drain Diode characteristics						
Diode Forward voltage ⁽³⁾	V _{SD}	V _{GS} = 0V, I _S = 50A	-	-	1.2	V
Diode Forward current ⁽⁴⁾	I _S		-	-	70	A

Notes:

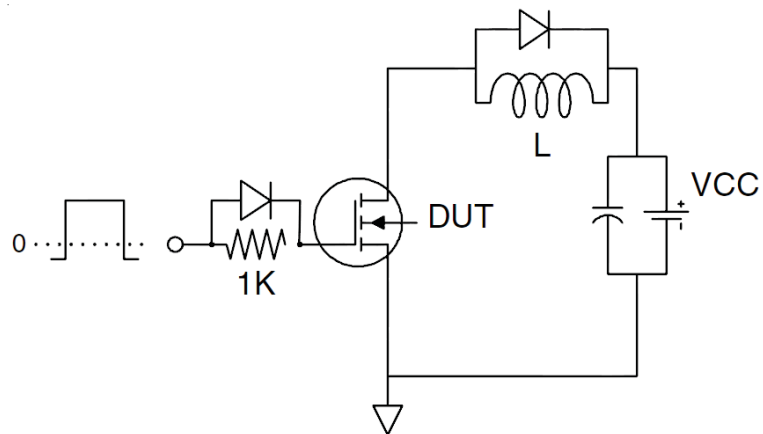
1. Repetitive Rating: pulse width limited by maximum junction temperature
2. EAS Condition: T_J = 25°C, V_{DD} = 20V, R_G = 25 Ω, L = 0.5mH, I_{AS} = 20A
3. Pulse Test: pulse width ≤ 300μs, duty cycle ≤ 2%
4. Surface Mounted on FR4 Board, t ≤ 10 sec

Test circuit

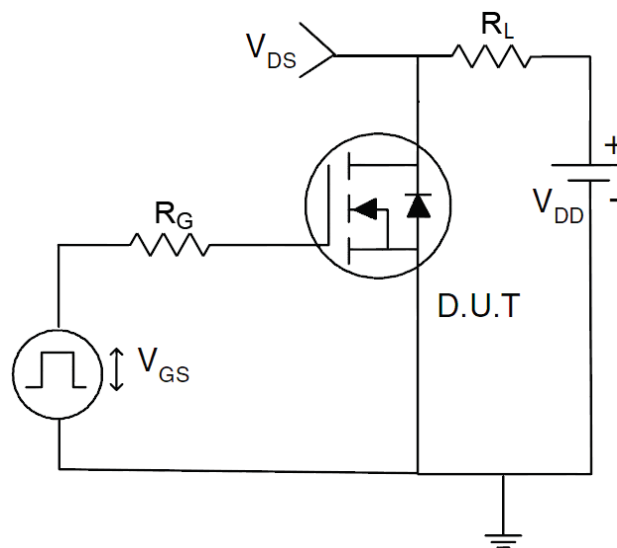
1) E_{AS} Test Circuit



2) Gate Charge Test Circuit



3) Switch Time Test Circuit



RATING AND CHARACTERISTICS CURVES (RM100N40DF)

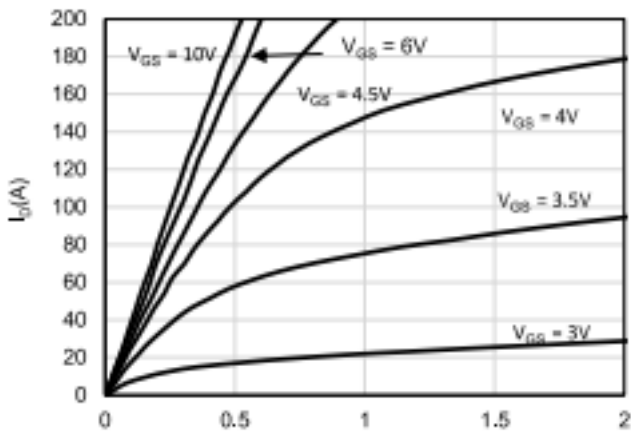


Figure 1: On-Region Characteristics

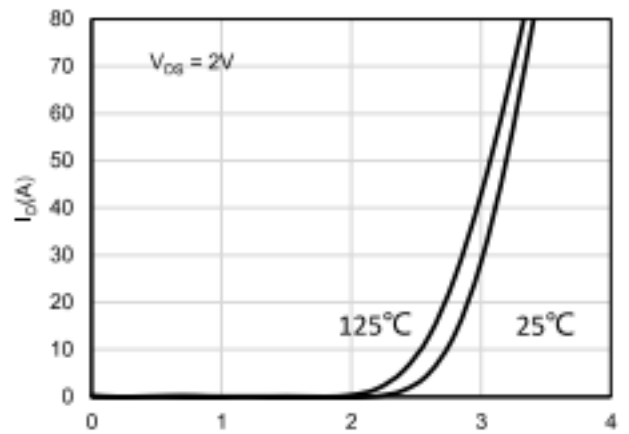


Figure 2: Transfer Characteristics

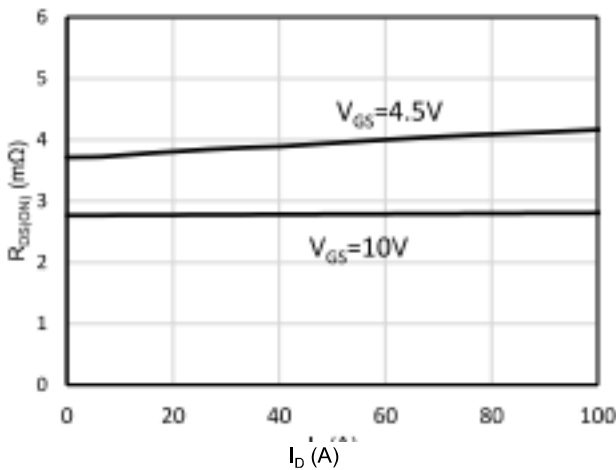


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

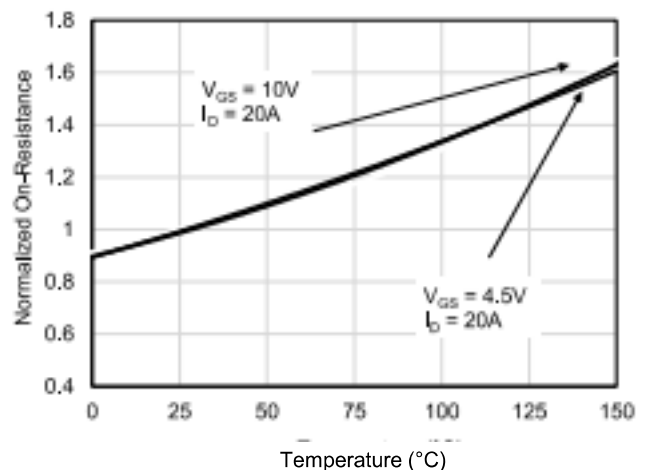


Figure 4: On-Resistance vs. Junction Temperature

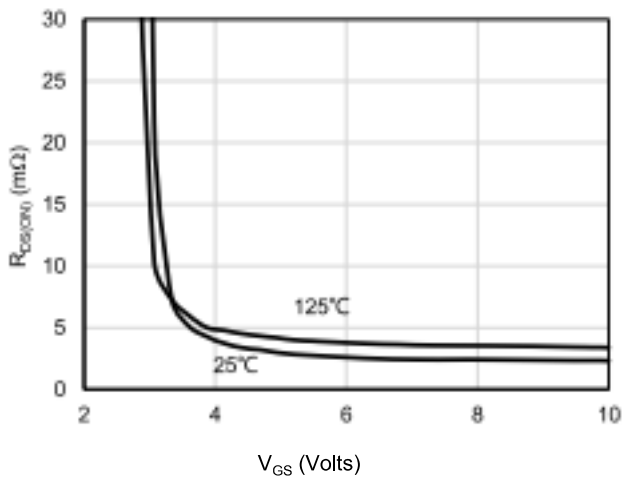


Figure 5: On-Resistance vs. Gate-Source Voltage

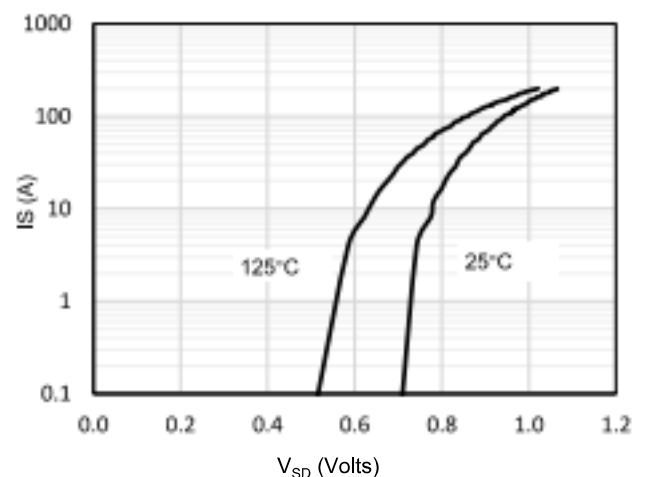


Figure 6: Body-Diode Characteristics

RATING AND CHARACTERISTICS CURVES (RM100N40DF)

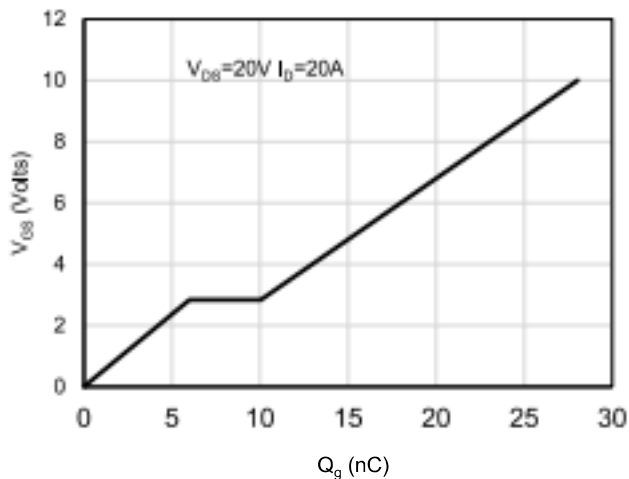


Figure 7: Gate-Charge Characteristics

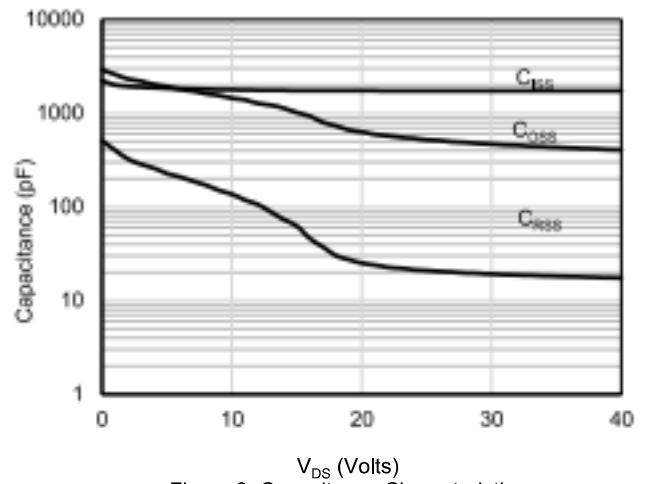


Figure 8: Capacitance Characteristics

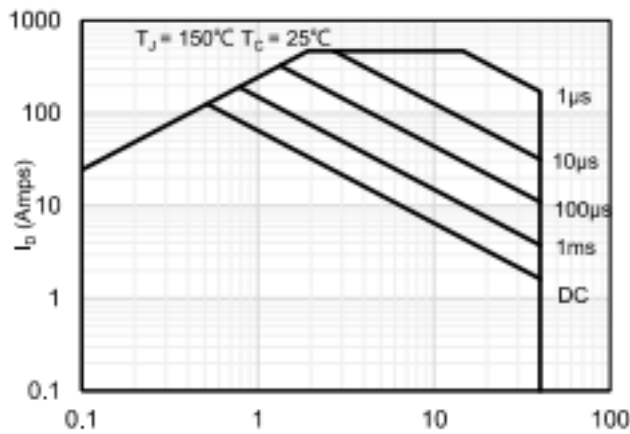


Figure 9: Maximum Forward Biased Safe Operating Area

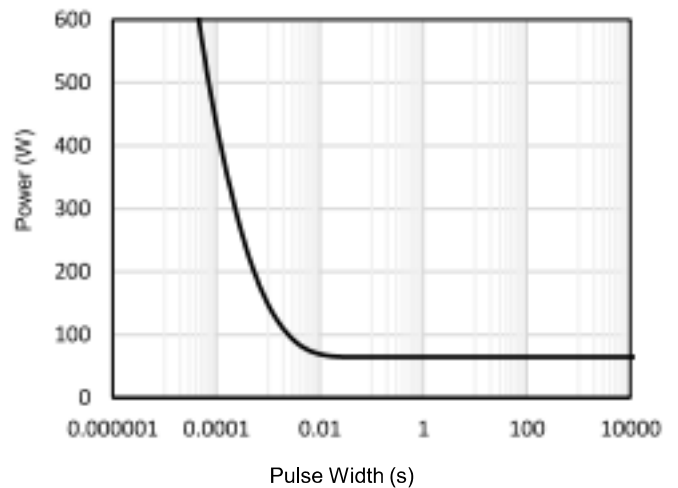


Figure 10: Single Pulse Power Rating Junction-to-Case

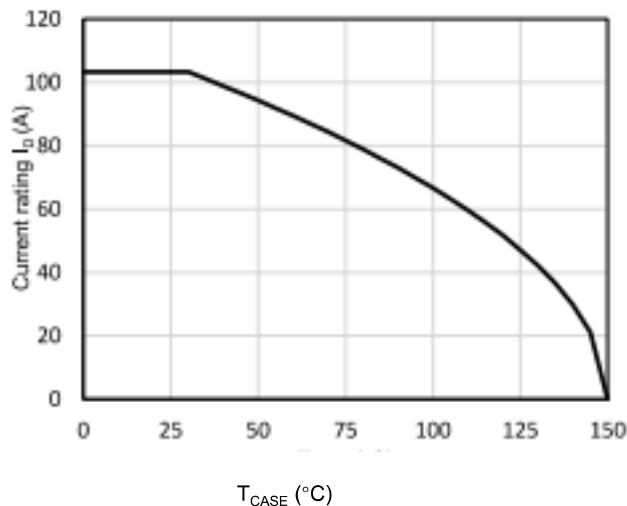


Figure 11: Current De-rating

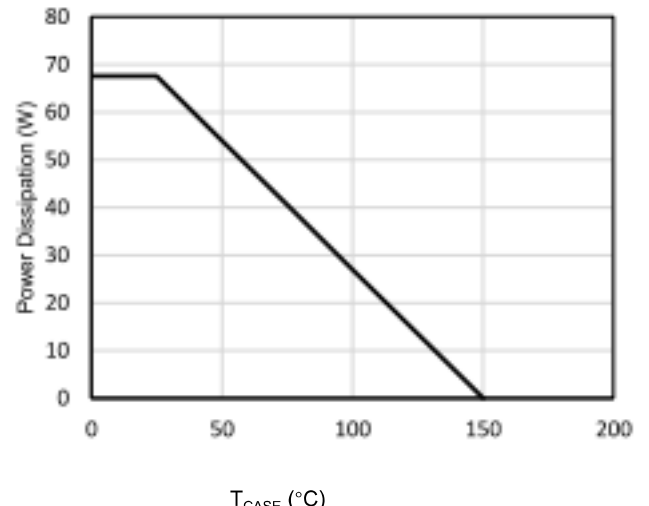


Figure 12: Power De-rating

RATING AND CHARACTERISTICS CURVES (RM100N40DF)

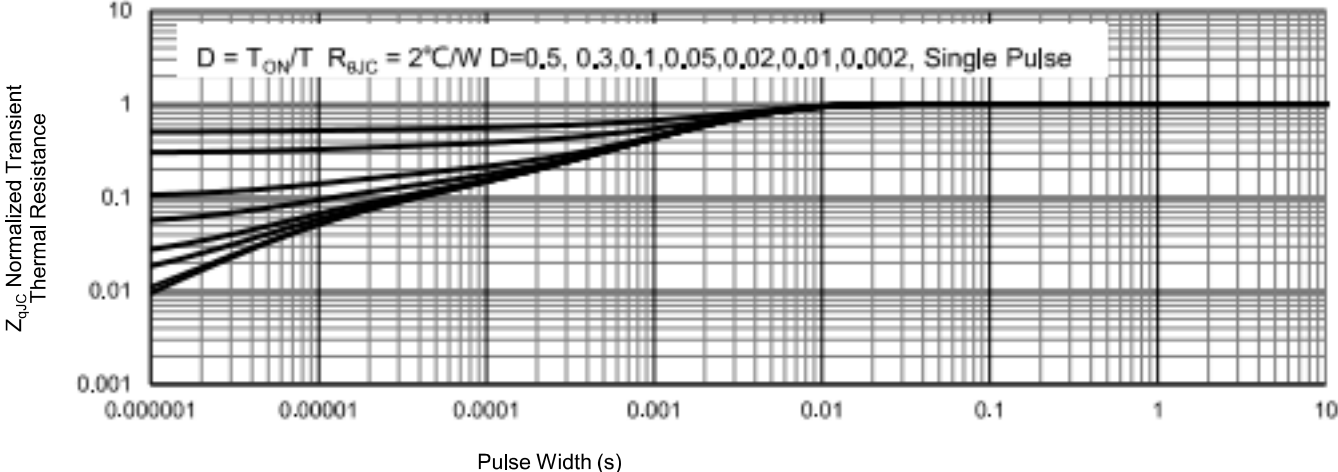
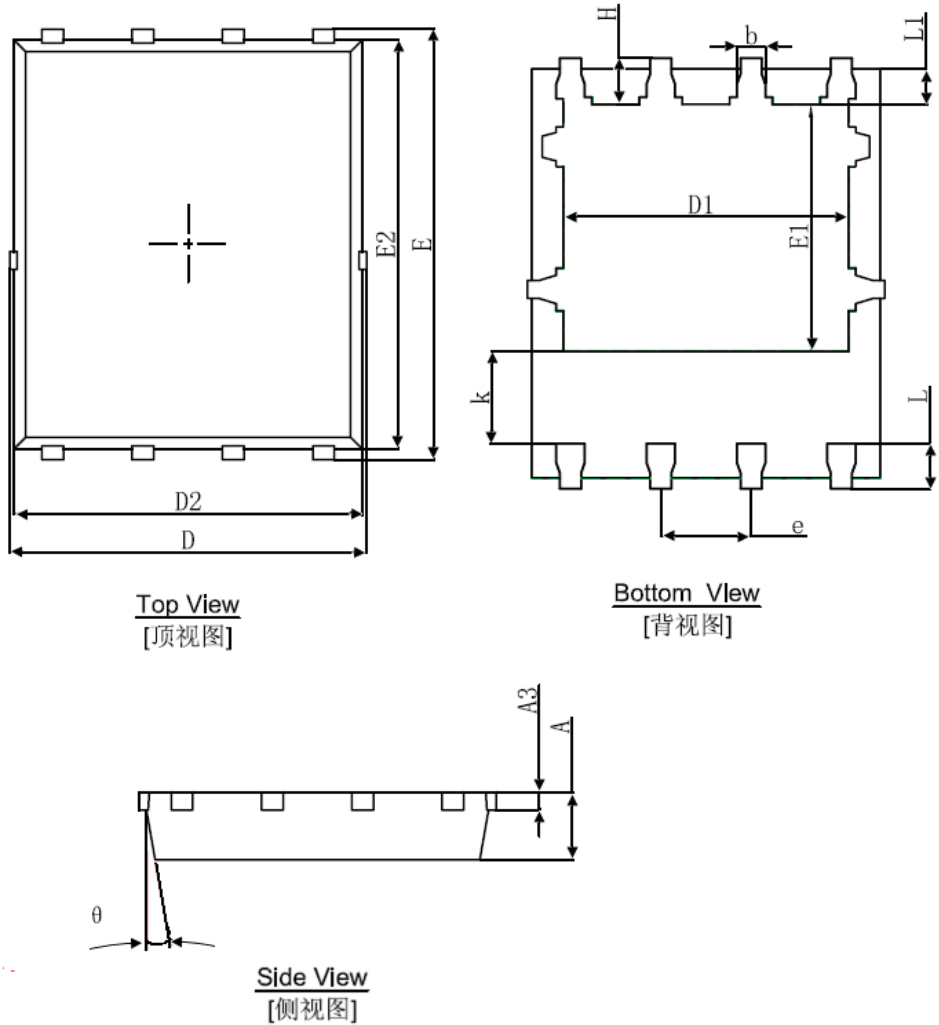


Figure 13: Normalized Maximum Transient Thermal Impedance

DFN5X6-8L Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.000	0.035	0.039
A3	0.254REF.		0.010REF.	
D	4.944	5.096	0.195	0.201
E	5.974	6.126	0.235	0.241
D1	3.910	4.110	0.154	0.162
E1	3.375	3.575	0.133	0.141
D2	4.824	4.976	0.190	0.196
E2	5.674	5.826	0.223	0.229
k	1.190	1.390	0.047	0.055
b	0.350	0.450	0.014	0.018
e	1.270TYP.		0.050TYP.	
L	0.559	0.711	0.022	0.028
L1	0.424	0.576	0.017	0.023
H	0.574	0.726	0.023	0.029
θ	8°	12°	8°	12°

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