Automotive Dual 5-A High-Speed, Low-Side Gate Driver

Features

- Industry-Standard Pin-out
- Automotive AEC-Q100 Grade 1 Qualified
- 4.5-V to 23-V Single-Supply Range
- Dual Independent Channels
- 5-A Peak Source and Sink-Drive Current
- Independent-Enable Function for Each Output
- TTL and CMOS Compatible Threshold
- Outputs Held Low during VDD-UVLO or Input Floating
- Low Propagation Delay (14-ns Typical)
- Fast Rise-and-Fall Times (7-ns and 6-ns Typical)
- <1-ns Typical Delay Matching between Two Channels
- Two Outputs used in Parallel for Higher Drive Current
- ESD Protection Exceeds JESD 22 – 6-kV HBM, 1.5-kV CDM
- Available in SOP8, EMSOP8, and DFN2X2-8 Packages

Description

The TPM27524Q family is a series of dual-channel low-side gate drivers for MOSFET, IGBT, and GaN power switches.

High sourcing and sinking current capability of 5 A allows for improving switching efficiencies by minimizing slew time and switching loss. The device supports maximum 25-V supply voltage and −5 V DC input voltage capability, which improves system robustness, especially in noisy industrial applications. Ultra-low propagation delay and excellent matching between two channels are designed for applications with tight timing requirements.

The TPM27524Q family consists of a set of gate drivers with different polarities, allowing customers to select based on application needs. The wide range of package supports SOP-8 and EMSOP-8. An extra ultra-small DFN2X2-8 assists the design of ultra-compact synchronous rectifiers in power applications.

Applications

- Switched-Mode Power Supplies
- DC-DC Converters
- Motor Control, Solar Inverters
- Gate & IGBT Drive

Typical Application Circuit

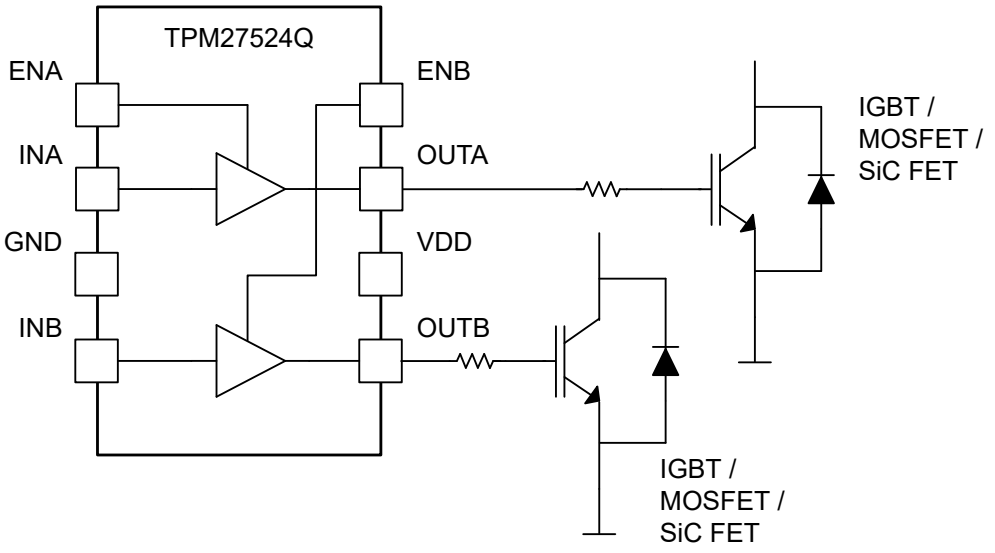


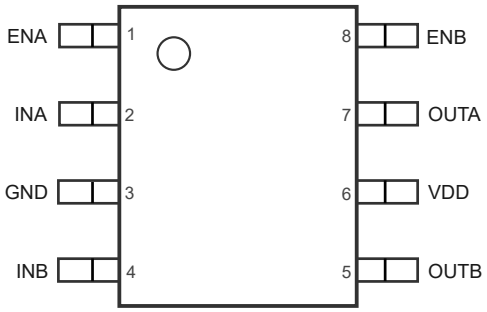
Table of Contents

Revision History

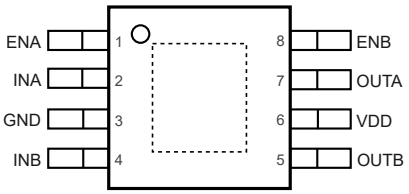
Date	Revision	Notes
2022-12-17	Rev P.0	Draft
2022-12-28	Rev A.0	Initial release
2023-04-09	Rev A.1	Updated electrical characteritics on timing parameters and Rdson

Pin Configuration and Functions

TPM27524Q
SOP8
Top View



TPM27524Q
EMSOP8
Top View



TPM27524Q
DFN2X2-8
Top View

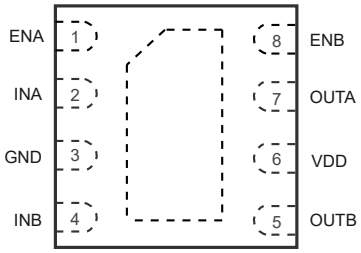


Table 1. Pin Functions: TPM27524Q

Pin	Name	I/O	Description
1	ENA	Input	Channel A enable input
8	ENB	Input	Channel B enable input
3	GND	Ground	Device ground
2	INA	Input	Logic input. Non-inverting input
4	INB	Input	Logic input. Non-inverting input
7	OUTA	Output	Channel A output
5	OUTB	Output	Channel B output
6	VDD	Power	Power supply input

Specifications

Absolute Maximum Ratings (1)

Parameter		Min	Max	Unit
	Power Supply Voltage, VDD	−0.3	25	V
	Output Voltage Range OUTA, OUTB	−0.3	VDD + 0.3	V
		−2	VDD + 0.3 (200-ns pulse)	
	Input Voltage Range INA, INB, ENA, ENB	−5	20	V
	Continuous Output Channel Current OUTA, OUTB	−300	300	mA
	Pulsed Output Channel Current OUTA, OUTB (500 ns)	−5	5	A
	Operating Junction Temperature Range	−40	150	°C
T_{STG}	Storage Temperature Range	−65	150	°C
T_L	Lead Temperature (Soldering, 10 sec)		260	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
(2) The inputs are protected by ESD protection diodes to each power supply. If the input extends more than 300 mV beyond the power supply, the input current should be limited to less than 10 mA.
(3) Power dissipation and thermal limits must be observed.

ESD, Electrostatic Discharge Protection

Parameter		Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	±6	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	±1.5	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter	Min	Max	Unit
Power Supply Voltage, VDD	4.5	23	V
Input Voltage Range INA, INB, ENA, ENB	0	20	V
Operating Ambient Temperature Range	−40	125	°C

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
SOP8	122.3	60.4	°C/W
EMSOP8	63.0	42.6	°C/W
DFN2X2-8	55	50	°C/W

Electrical Characteristics

All test conditions: V_{DD} = 12 V, T_J = −40 °C to 150 °C, and 1-µF capacitor between V_{DD} and GND, unless otherwise noted.

Parameter		Conditions	Min	Typ	Max	Unit
$I_{DD(off)}$	Start-up Current, based on TPM27524Q Circuitry	VDD = 3.4 V, INA = H, INB = H		40	100	µA
		VDD = 3.4 V, INA = L, INB = L		40	100	
V_{ON}	Supply Under Voltage Lock Out Rising Threshold	T_J = 25 °C	3.91	4.2	4.5	V
		T_J = −40 °C – 150 °C	3.7	4.2	4.65	
V_{OFF}	Supply Under Voltage Lock Out Falling Threshold	T_J = −40 °C – 150 °C	3.4	3.9	4.4	V
V_{DD_H}	Supply Under Voltage Lock Out Hysteresis		0.2	0.3	0.5	V
V_{EN_H}	Enable High Threshold	Enable high threshold		1.9	2.3	V
V_{EN_L}	Enable Low Threshold	Enable low threshold	1	1.2		V
V_{EN_HYS}	Enable Hysteresis			0.7		V
V_{IN_H}	Input Signal High Threshold	Input high threshold		1.95	2.3	V
V_{IN_L}	Input Signal Low Threshold	Input low threshold	1	1.25		V
V_{IN_HYS}	Input Hysteresis			0.7		V
I_{OUT}	Output Peak Current	C_{LOAD} = 0.22 µF, F_{SW} = 1 kHz		±5		A
$V_{DD} – V_{OH}$	Output High Voltage	I_{OUT} = −10 mA			40	mV
V_{OL}	Output Low Voltage	I_{OUT} = 10 mA			10	mV
R_{OH}	Output Pull-up Resistance, PMOS Pull-up only	I_{OUT} = −10 mA	0.8	1.6	3	Ω
R_{OL}	Output Pull-down Resistance	I_{OUT} = 10 mA	0.15	0.5	1	Ω
t_R(1)	Output Rise-time	C_{LOAD} = 1.8 nF		7	18	ns
t_F(1)	Output Fall-time	C_{LOAD} = 1.8 nF		6	10	ns
t_M	Delay Matching between OUTA and OUTB	INA = INB, OUTA and OUTB measured at 50%		1	4	ns
t_{PW}	Minimal Pulse Width			15	25	ns
t_{D1}(1)	Input to Output Propagation Delay	C_{LOAD} = 1.8 nF, 5-V INx pulse	6	14	23	ns
t_{D2}(1)	Input to Output Propagation Delay	C_{LOAD} = 1.8 nF, 5-V INx pulse	6	14	23	ns
t_{D3}(1)	Enable to Output Propagation Delay	C_{LOAD} = 1.8 nF, 5-V ENx pulse	6	14	23	ns
t_{D4}(1)	Enable to Output Propagation Delay	C_{LOAD} = 1.8 nF, 5-V ENx pulse	6	14	23	ns

(1) Guranteed by design, evaluated in bench tests, not tested in production.

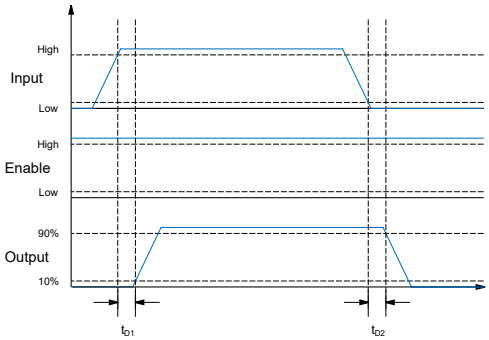


Figure 1. Input Timing Diagram

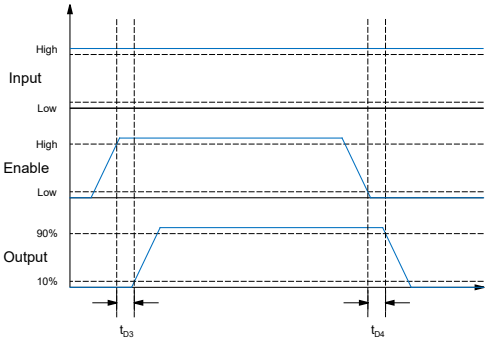


Figure 2. Enable Timing Diagram

Typical Performance Characteristics

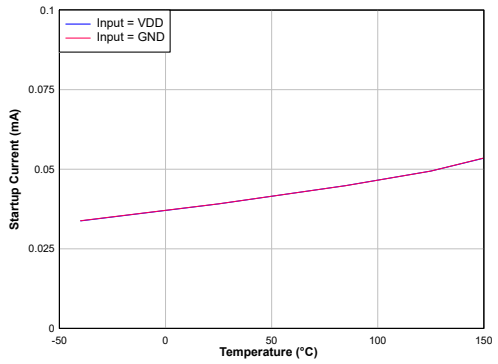


Figure 3. Start-up Current vs. Temperature

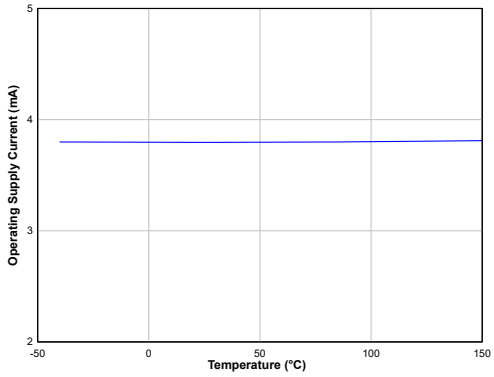


Figure 4. Operating Current vs Ambient Temperature

f = 500 kHz, C_L = 500 pF, V_{DD} = 12 V

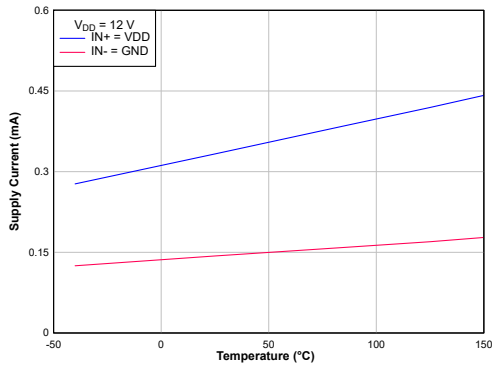


Figure 5. Supply Current vs Temperature (On/Off)

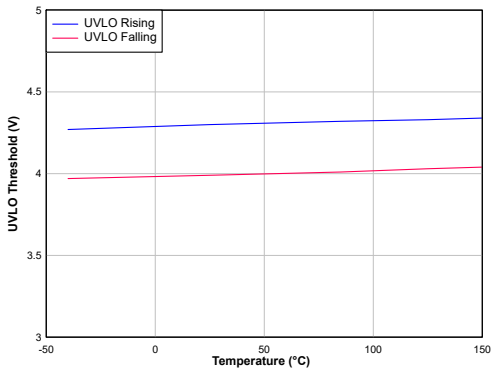


Figure 6. UVLO Threshold vs Temperature

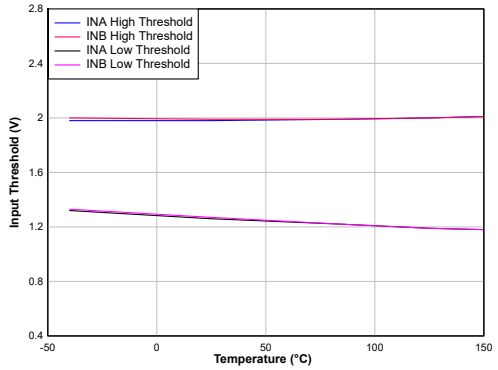


Figure 7. Input Threshold vs Temperature

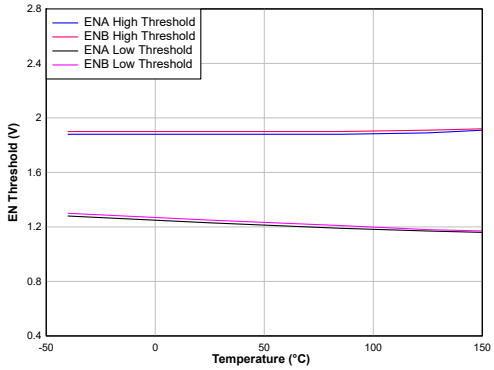


Figure 8. Enable Threshold vs Temperature

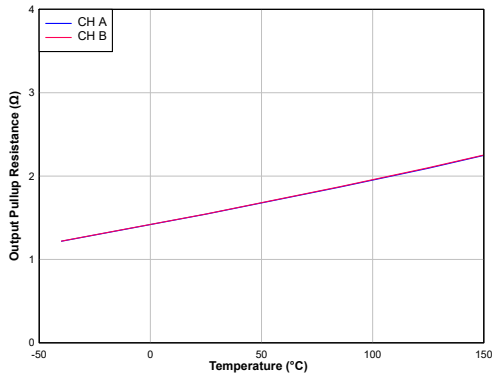


Figure 9. Output Pull-up Resistance vs Temperature

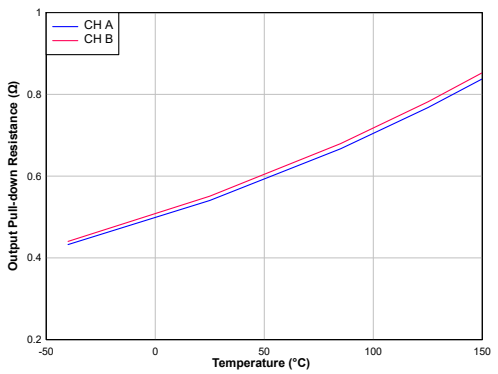


Figure 10. Output Pull-down Resistance vs Temperature

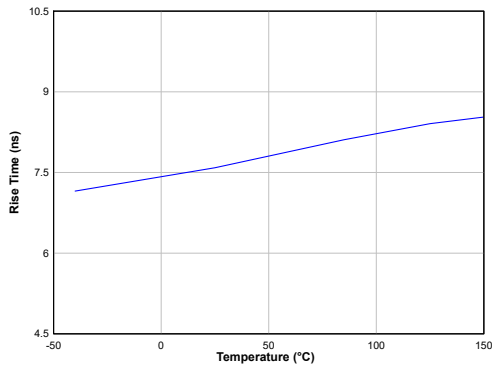


Figure 11. Rise-time vs Temperature

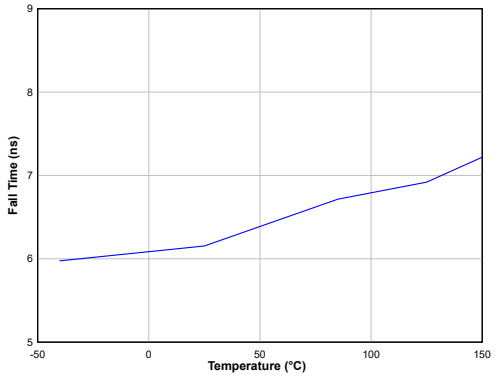


Figure 12. Fall-time vs Temperature

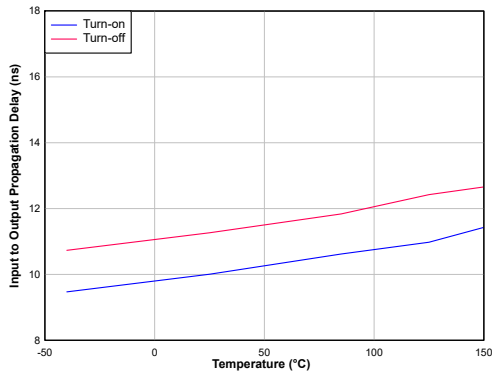


Figure 13. Input to Output Propagation Delay vs Temperature

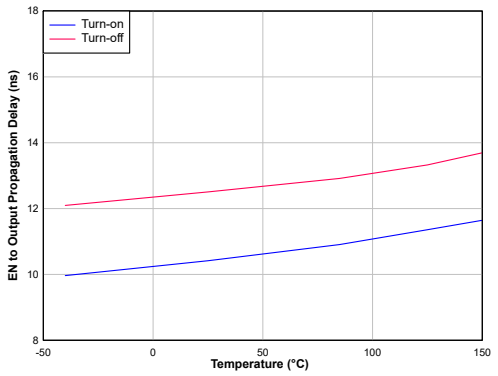


Figure 14. Enable to Output Propagation Delay vs Temperature

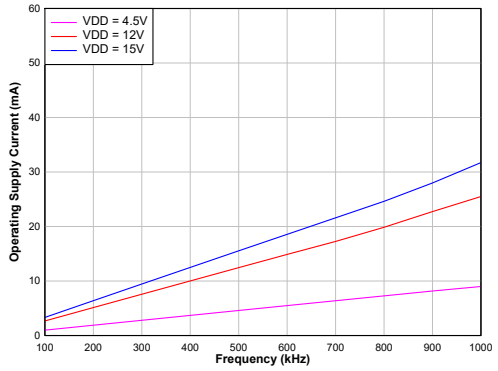


Figure 15. Operating Supply Current vs Frequency

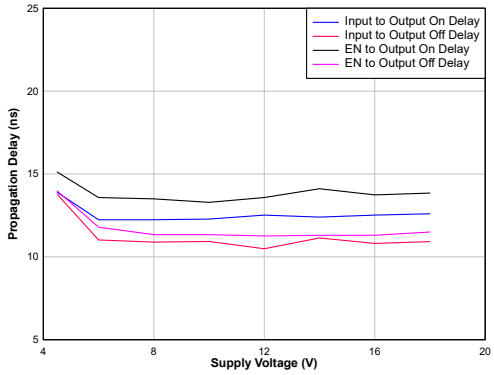


Figure 16. Propagation Delay vs Supply Voltage

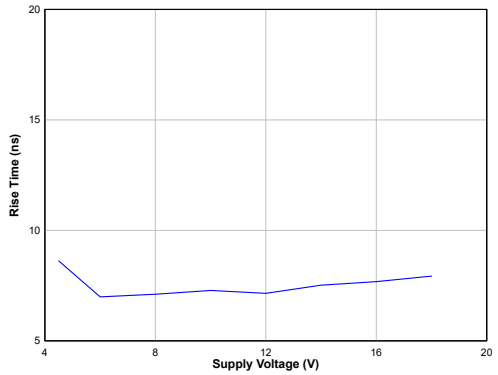


Figure 17. Rise-time vs Supply Voltage

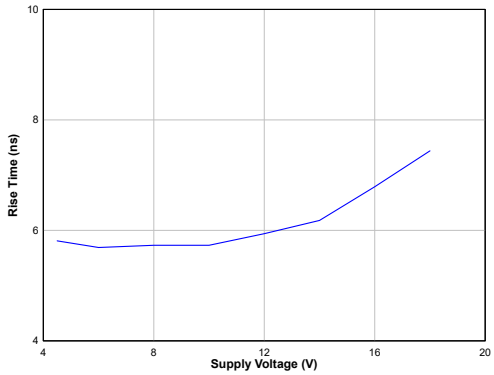


Figure 18. Fall-time vs Supply Voltage

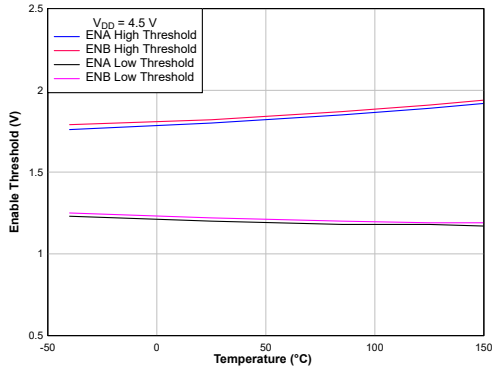


Figure 19. Enable Threshold vs Temperature

VDD = 4.5 V

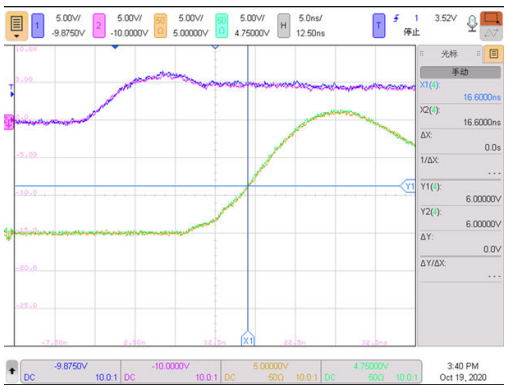


Figure 20. Rising Edge

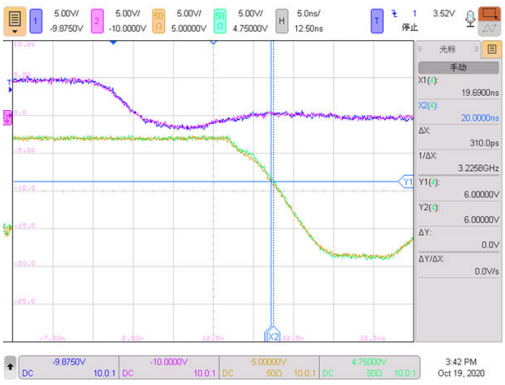


Figure 21. Falling Edge

Detailed Description

Overview

The TPM27524Q series of dual-channel low-side gate drivers are designed for automotive high-performance power supplies, motor controls, and inverters. Designed with industrial standard pin-out and package, the TPM27524Q accelerates design process. With extended voltage ranges of supply voltage and negative input voltage on inputs, the TPM27524Q improves system-level reliability. 5-A strong driving capability improves gate driver efficiency and lowers heat generation, especially in high-frequency switching applications.

Functional Block Diagram

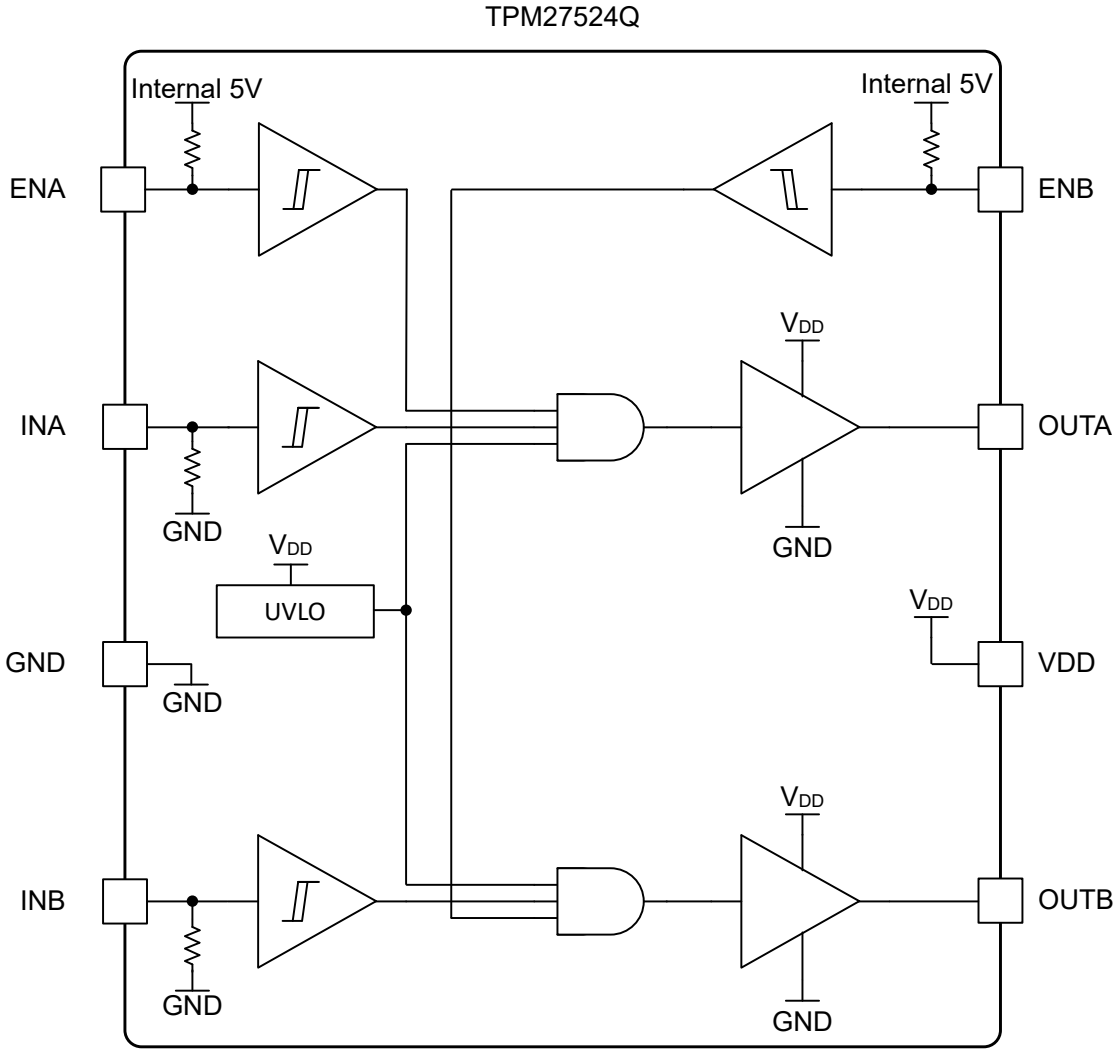


Figure 22. Functional Block Diagram

Feature Description

Low Propagation Delay Driver Outputs

The low-propagation-delay design allows the device to achieve industrial leading low propagation delay between inputs and outputs. The low delay enhances driver performance in high-frequency switching regulators. Matching between two channels is optimized to support parallel driving. 3PEAK recommends tying IN1 and IN2 locally together with a high-input slew rate, to avoid shoot-through between the two well-matched channels. Capacitors are not recommended on IN1 and IN2 nodes when used in parallel.

Supply and UVLO

The device monitors the supply voltage with under-voltage lock-out (UVLO). When the supply voltage is below the UVLO threshold, the outputs are held low in UVLO to avoid glitches during power rising and falling.

The device quiescent current and operating current are measured as shown in Figure 5. The current is related to internal quiescent current consumption as well as the output current. The output current can be calculated using external transistor gate charge times switching frequency f_{sw}.

Channel Input

The input of the TPM27524Q gate drivers supports TTL and CMOS input with the threshold voltage independent of the supply voltage. The threshold is also designed to support a wide range of ambient temperatures. Wide hysteresis enhances system-level noise immunity. The integrated pull-up and pull-down resistors set the device state when inputs are floating. EN supports NC connection with the help of internal pull-up resistors.

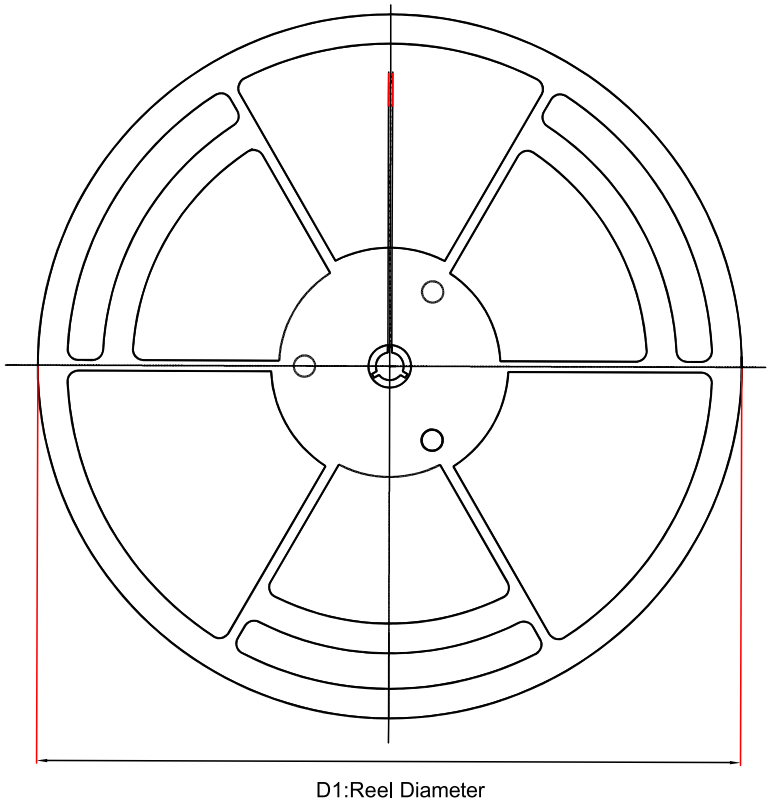
Inputs can withstand DC −5 V, to improve robustness on ground bouncing.

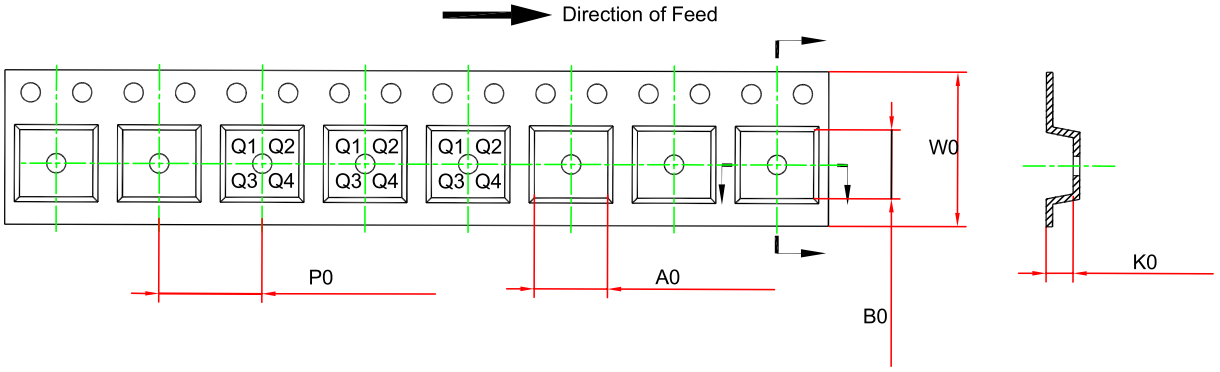
Output Stage

The TPM27524Q output stage is able to deliver high current sourcing and sinking up to 5 A with low propagation delay. The delay matching between dual channels is also optimized within 1-ns.

In the case of higher output driving capabilities needed, the TPM27524Q can allow paralleling the dual channel to achieve a higher driving current. In this case, it is recommended to use a high slew rate on IN1 and IN2 and connect IN1 and IN2 to avoid shoot through between channels.

Tape and Reel Information



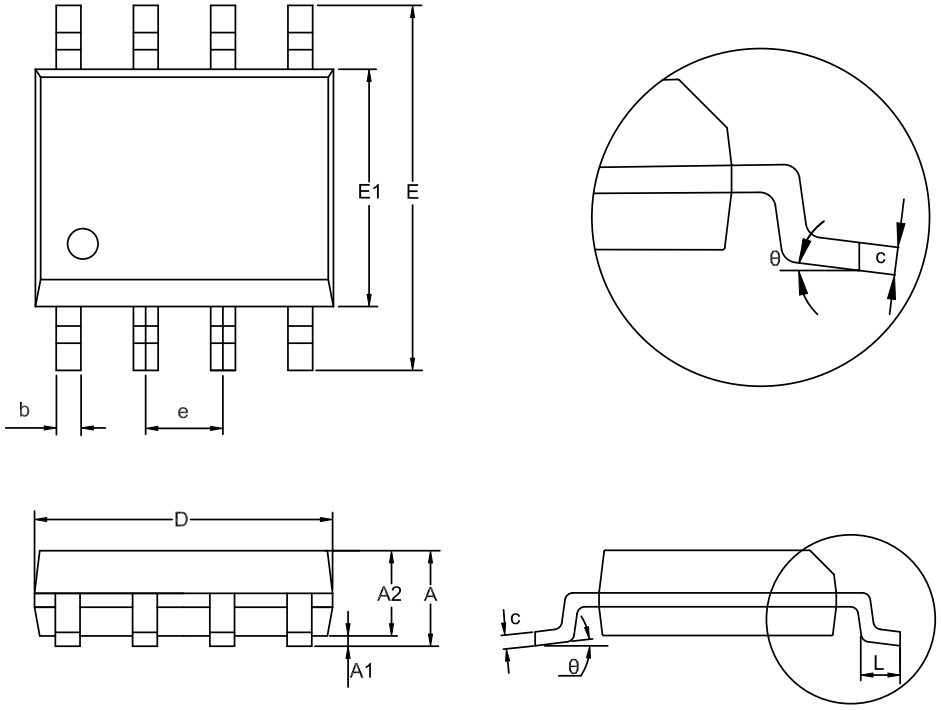


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPM27524Q-DF4R-S	DFN2X2-8	180.0	13.1	2.3	2.3	1.1	4.0	8.0	Q1
TPM27524Q-EV1R-S	EMSOP8	330.0	17.6	5.2	3.3	1.5	8.0	12.0	Q1
TPM27524Q-SO1R-S	SOP8	330.0	17.6	6.4	5.4	2.1	8.0	12.0	Q1

Package Outline Dimensions

SOP8

Package Outline Dimensions SO1(SOP-8-A)



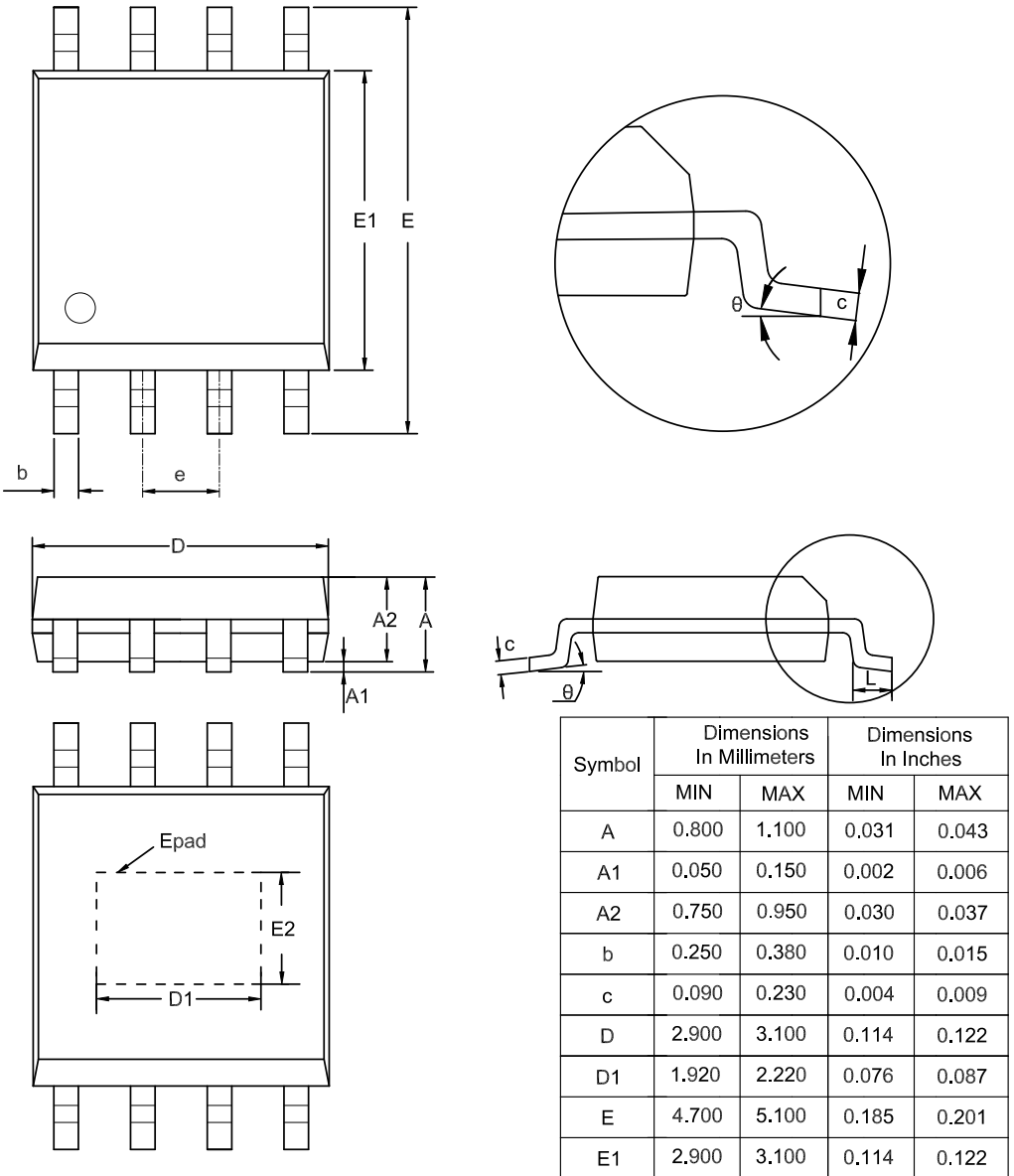
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.050	0.250	0.002	0.010
A2	1.250	1.550	0.049	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
e	1.270 BSC		0.050 BSC	
L	0.400	1.000	0.016	0.039
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

EMSOP8

Package Outline Dimensions EV1(EMSOP-8-B)



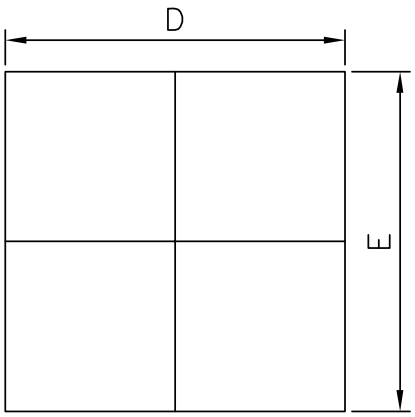
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.800	1.100	0.031	0.043
A1	0.050	0.150	0.002	0.006
A2	0.750	0.950	0.030	0.037
b	0.250	0.380	0.010	0.015
c	0.090	0.230	0.004	0.009
D	2.900	3.100	0.114	0.122
D1	1.920	2.220	0.076	0.087
E	4.700	5.100	0.185	0.201
E1	2.900	3.100	0.114	0.122
E2	1.450	1.750	0.057	0.069
e	0.650 BSC		0.026 BSC	
L	0.400	0.800	0.016	0.031
θ	0	8°	0	8°

NOTES

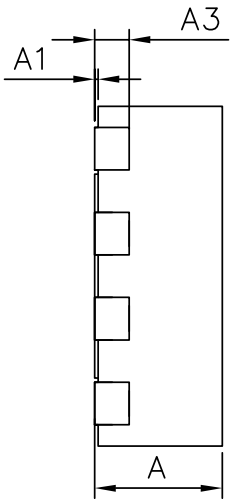
1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

DFN2X2-8

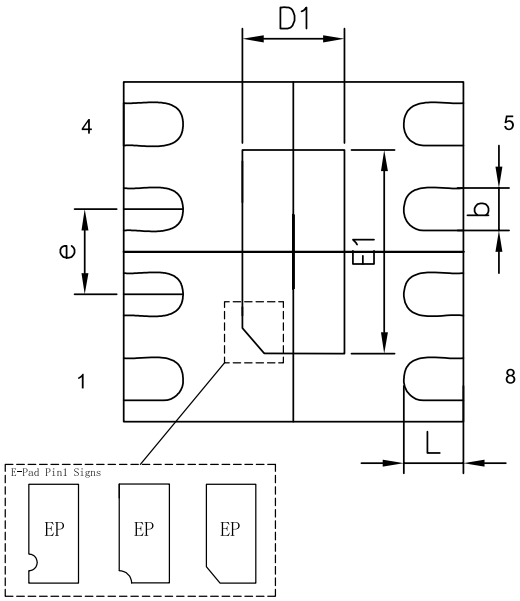
Package Outline Dimensions DF4(DFN2X2-8-D)



Top View



Side View



Bottom View

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
b	0.180	0.300	0.007	0.012
A3	0.150	0.250	0.006	0.010
D	1.900	2.100	0.075	0.083
D1	0.800	1.000	0.031	0.039
E	1.900	2.100	0.075	0.083
E1	1.500	1.700	0.059	0.067
e	0.500 BSC		0.020BSC	
L	0.250	0.350	0.010	0.014

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.
3. The many types of E-pad Pin1 signs may appear in the product.

Order Information

Order Number	Operating Ambient Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPM27524Q-DF4R-S (2)	−40 °C – 125 °C (1)	DFN2X2-8	54Q	2	Tape and Reel, 3000	Green
TPM27524Q-EV1R-S (2)	−40 °C – 125 °C (1)	EMSOP8	M524Q	1	Tape and Reel, 3000	Green
TPM27524Q-SO1R-S (2)	−40 °C – 125 °C (1)	SOP8	M524Q	1	Tape and Reel, 4000	Green

(1) Ambient temperature indicates device operation condition range. Application thermal behavior needs to be taken care of when operating in high-temperature scenarios.
(2) Contact 3PEAK representatives for more information.

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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