Data Sheet

ADPL13602

3.5V to 36V, 2.4A, High-Efficiency, Synchronous Step-Down DC-DC Converter

FEATURES

- Reduces External Components and Total Cost
  - No Schottky—Synchronous Operation
  - Internal Compensation Components
  - All-Ceramic Capacitors, Compact Layout
- Reduces the Number of DC-DC Regulators to Stock
  - Wide 3.5V to 36V Input
  - Adjustable Output Voltage Range from 1V up to 90% of V_{IN}
  - Delivers Up to 2.4A Over the Temperature Range
  - 400kHz to 1.5MHz Adjustable Frequency
- Reduces Power Dissipation
  - Peak Efficiency of 95%
  - Wide 2.4V to 12V Bootstrap Bias Input (EXTVCC) for Improved Efficiency
- Operates Reliably in Adverse Industrial Environments
  - Hiccup-Mode Overload Protection
  - Adjustable and Monotonic Startup with Prebiased Output Voltage
  - Built-in Output-Voltage Monitoring with $\overline{\text{RESET}}$
  - Programmable EN/UVLO Threshold
  - Wide Industrial -40°C to +125°C Ambient Operating Temperature Range or -40°C to +150°C Junction Temperature Range

GENERAL DESCRIPTION

The ADPL13602 is a high-efficiency, synchronous step-down DC-DC converter with integrated MOSFETs operating over an input-voltage range of 3.5V to 36V. It can deliver up to 2.4A current. Output voltage is programmable from 1V up to 90% of V_{IN}. Built-in compensation across the output-voltage range eliminates the need for external compensation components.

The ADPL13602 features a peak-current-mode control architecture. The ADPL13602 can be operated in forced pulse-width modulation (PWM) or discontinuous-conduction mode (DCM) to enable high efficiency under full-load and light-load conditions. The ADPL13602 offers a low minimum on-time that allows high switching frequencies and a smaller solution size.

The feedback-voltage regulation accuracy over -40°C to +125°C is ±1.5%. The device is available in a 16-pin (3mm x 3mm) TQFN-EP package. Simulation models are available.

APPLICATIONS

- Industrial Control Power Supplies
- Distributed Supply Regulation
- Wall Transformer Regulation
- High-Voltage, Single-Board Systems

SIMPLIFIED APPLICATION DIAGRAM

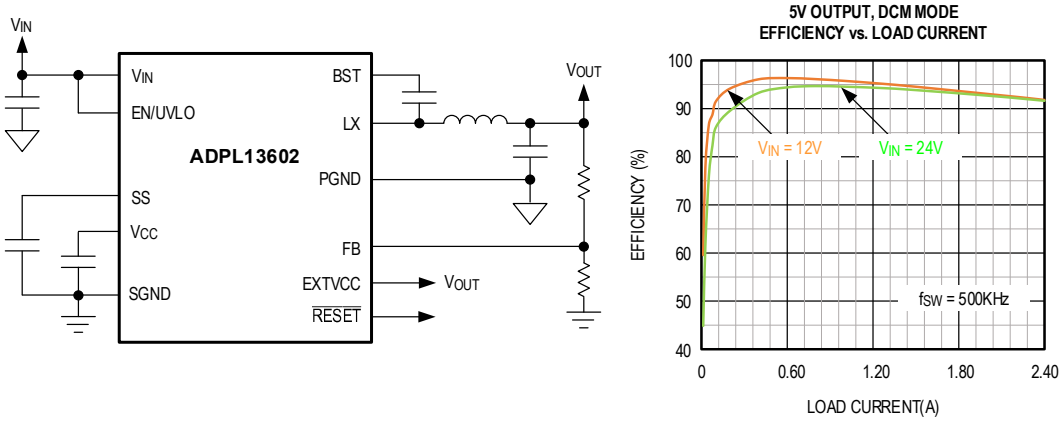

Figure 1. Simplified Application Diagram and Efficiency vs. Load Current

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REVISION HISTORY

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/23	Initial release	—

SPECIFICATIONS

Table 1. Electrical Characteristics

(V_{IN} = $V_{EN/UVLO}$ = 24V, RT = Unconnected (f_{SW} = 500kHz), C_{VCC} = 2.2uF, V_{MODE} = V_{EXTVCC} = V_{SGND} = V_{PGND} = 0, V_{FB} = 0.64V, LX = SS = $\overline{RESET}$ = Open, V_{BST} to V_{LX} = 1.8V, T_A = T_J = -40°C to 125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND unless otherwise noted. (Note 1))

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
INPUT SUPPLY (VIN)						
Input Voltage Range	V_{IN}		3.5		36	V
Input Shutdown Current	I_{IN_SH}	$V_{EN/UVLO}$ = 0V (Shutdown mode)		6.5	24	µA
Input Quiescent Current	I_{Q_DCM}	DCM mode, V_{LX} = 0.1V		2		mA
	I_{Q_PWM}	Normal Switching mode, V_{FB} = 0.58V		8.2		
Input UVLO	$V_{IN\_UVLO\_R}$	V_{IN} rising	2.95		3.26	V
	V_{IN_HYS}	Hysteresis		0.246		
ENABLE/INPUT UNDERVOLTAGE LOCKOUT (EN/UVLO)						
EN/UVLO Threshold	V_{ENR}	$V_{EN/UVLO}$ rising	1.194	1.25	1.303	V
	V_{EN_HYS}	Hysteresis		0.1		
	V_{EN_TRUESD}	$V_{EN/UVLO}$ falling, true shutdown		0.75		
EN/UVLO Input Leakage Current	I_{EN}	$V_{EN/UVLO}$ = 0V, T_A = +25°C	-50	0	+50	nA
LINEAR REGULATOR (V_{CC}, EXTVCC)						
V_{CC} Output Voltage Range	V_{CC}	3.5V < V_{IN} < 36V, I_{VCC} = 1mA	1.74	1.80	1.86	V
		1mA < I_{VCC} < 25mA	1.70	1.80	1.86	
V_{CC} UVLO	V_{CC_UVR}	VCC rising	1.605	1.640	1.683	V
	V_{CC_HYS}	Hysteresis		0.065		
EXTVCC Operating Voltage Range			2.448		12	V
EXTVCC Switchover Threshold		EXTVCC rising	2.348	2.400	2.448	V
		Hysteresis		0.09		

(V_{IN} = $V_{EN/UVLO}$ = 24V, RT = Unconnected (f_{SW} = 500kHz), C_{VCC} = 2.2uF, V_{MODE} = V_{EXTVCC} = V_{SGND} = V_{PGND} = 0, V_{FB} = 0.64V, LX = SS = $\overline{RESET}$ = Open, V_{BST} to V_{LX} = 1.8V, T_A = T_J = -40°C to 125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND unless otherwise noted. (Note 1))

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
POWER MOSFETS						
High-Side nMOS On-Resistance	R_{DS_ONH}	I_{LX} = 0.3A, sourcing		0.14	0.27	Ω
Low-Side nMOS On-Resistance	R_{DS_ONL}	I_{LX} = 0.3A, sinking		0.1	0.19	Ω
LX Leakage Current	I_{LX_LKG}	V_{IN} = 36V, T_A = +25°C, V_{LX} = (V_{PGND} + 1)V to (V_{IN} -1)V, $V_{EN/UVLO}$ = 0V	-2		+2	µA
SOFT-START (SS)						
Charging Current	I_{SS}	V_{SS} = 0.3V	4.7	5	5.3	µA
FEEDBACK (FB)						
FB Regulation Voltage	V_{FB_REG}		0.591	0.600	0.609	V
FB Input Bias Current	I_{FB}	V_{FB} = 1V, T_A = +25°C	-50		+50	nA
MODE SELECTION (MODE)						
MODE Threshold	V_{M_DCM}	DCM mode	1.22			V
	V_{M_PWM}	PWM mode			0.66	
CURRENT LIMIT						
Peak Current-Limit Threshold	I_{PEAK_LIMIT}		2.8	3.4	4.1	A
Valley Current-Limit Threshold	I_{VALLEY_LIMIT}	DCM Mode		0.1		A
		PWM Mode		-1.8		
OSCILLATOR (RT)						
Programmable Switching Frequency Range	f_{SW}		400		1500	kHz
Switching Frequency Accuracy			-10		+10	%

(V_{IN} = $V_{EN/UVLO}$ = 24V, RT = Unconnected (f_{SW} = 500kHz), C_{VCC} = 2.2uF, V_{MODE} = V_{EXTVCC} = V_{SGND} = V_{PGND} = 0, V_{FB} = 0.64V, LX = SS = $\overline{RESET}$ = Open, V_{BST} to V_{LX} = 1.8V, T_A = T_J = -40°C to 125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND unless otherwise noted. (Note 1))

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
V_{FB} Undervoltage Trip Level to Cause Hiccup	V_{FB_HICF}		0.375	0.390	0.405	V
HICCUP Timeout		(Note 2)		32768		Cycles
Minimum On-Time	t_{ON_MIN}			60	90	ns
Minimum Off-Time	t_{OFF_MIN}		100		150	ns
OUTPUT STATUS MONITORING ($\overline{RESET}$)						
$\overline{RESET}$ Output Level Low	V_{RESETL}	$I_{\overline{RESET}}$ = 10mA			0.4	V
$\overline{RESET}$ Output Leakage Current	$I_{RESETLKG}$	T_A = T_J = +25°C	-0.1		+0.1	µA
FB Threshold for $\overline{RESET}$ Deassertion	V_{FB_OKR}	V_{FB} rising	93.1	95.0	97.0	% of V_{FB_REG}
FB Threshold for $\overline{RESET}$ Assertion	V_{FB_OKF}	V_{FB} falling	89.8	92.0	93.2	% of V_{FB_REG}
$\overline{RESET}$ Delay After FB Reaches 95% Regulation				1024		Cycles
THERMAL SHUTDOWN						
Thermal-Shutdown Threshold		Temperature rising		160		°C
Thermal-Shutdown Hysteresis				20		°C

1 Electrical specifications are production tested at T_A = +25°C. Specifications over the entire operating temperature range are guaranteed by design and characterization.

2 See *Overcurrent Protection (OCP)/Hiccup Mode* section for more details.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C unless otherwise specified.

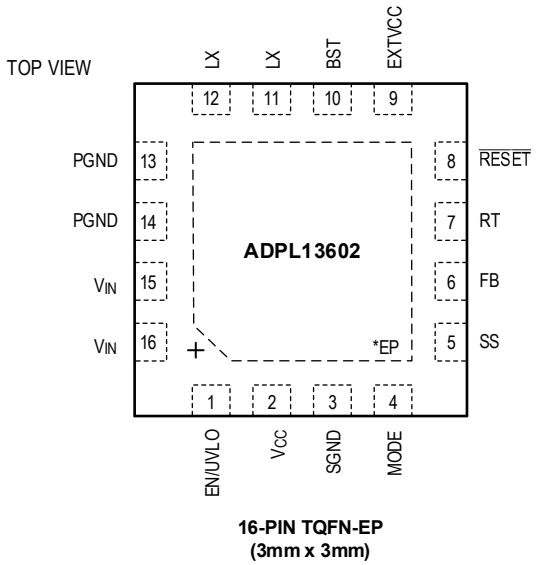
Table 2. Absolute Maximum Ratings

PARAMETER	RATING
V_{IN} to PGND	-0.3V to +40V
EN/UVLO to SGND	-0.3V to +40V
LX to PGND	-0.3V to (V_{IN} + 0.3V)
EXTVCC to SGND	-0.3V to +14V
BST to PGND	-0.3V to +42V
BST to LX	-0.3V to +2.2V
BST to V_{CC}	-0.3V to +40V
FB, VCC to SGND	-0.3V to +2.2V
SS, RT to SGND	-0.3V to (V_{CC} + 0.3V)
MODE, $\overline{\text{RESET}}$ to SGND	-0.3V to +6V
PGND to SGND	-0.3V to +0.3V
LX Steady State RMS current	±3.0A
Output Short-Circuit duration	Continuous
Continuous Power Dissipation (T_A = +70°C)	
TQFN Multilayer Board (derate 23.1mW/°C above +70°C)	1847.6mW
Operating Temperature Range (Note 3)	-40°C to +125°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C

[1] Junction temperature greater than +125°C degrades operating lifetimes.

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



16-PIN TQFN-EP
(3mm x 3mm)

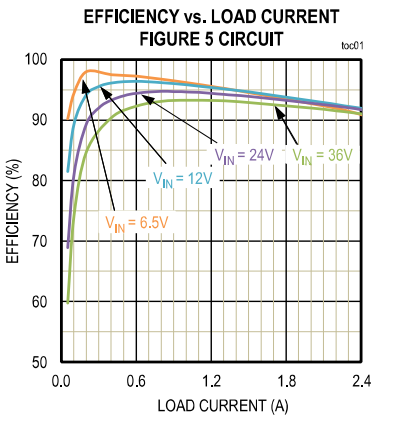
Table 3. Pin Descriptions

PIN	NAME	DESCRIPTION
1	EN/UVLO	Enable/Undervoltage Lockout Pin. Drive EN/UVLO high to enable the output. Connect to the center of the resistor divider between V_{IN} and SGND to set the input voltage at which the part turns on. Connect to V_{IN} pins for always-on operation. Pull low (lower than V_{EN_TRUESD}) for disabling the device.
2	V_{CC}	1.8V LDO Output. Bypass V_{CC} with a 2.2µF ceramic capacitance to SGND. LDO does not support the external loading on V_{CC}.
3	SGND	Signal Ground
4	MODE	The MODE pin configures the device to operate in either PWM or DCM modes of operation. Connect MODE to SGND for constant-frequency PWM operation at all loads. Connect MODE to V_{CC} for DCM operation (at light loads). See the *Mode Selection (MODE)* section for more details.
5	SS	Soft-Start Input. Connect a capacitor from SS to SGND to set the soft-start time.
6	FB	Feedback Input. Connect FB to the centre node of an external resistor-divider from the output to SGND to set the output voltage. See the *Adjusting Output Voltage* section for more details.
7	RT	Programmable Switching Frequency Input. Connect a resistor from RT to SGND to set the regulator's switching frequency between 400kHz and 1.5MHz. Leave the RT pin open for the default 500kHz frequency. See the *Setting the Switching Frequency (RT)* section for more details.

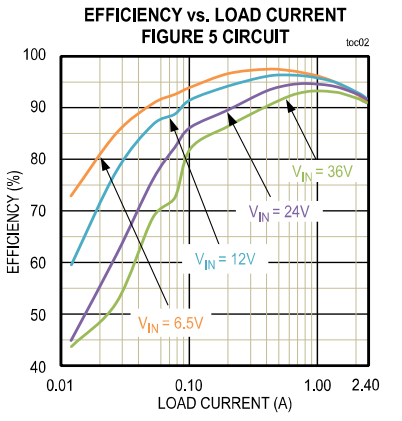
8	$\overline{\text{RESET}}$	Open-Drain $\overline{\text{RESET}}$ Output. The $\overline{\text{RESET}}$ output is driven low if FB drops below V_{FB_OKF}. $\overline{\text{RESET}}$ goes high 1024 cycles after FB rises above V_{FB_OKR}.
9	EXTVCC	External Bias Input. Applying a voltage between 2.448V and 12V at EXTVCC will bypass the IN-LDO and improve overall converter efficiency. Connect a buck regulator output to EXTVCC through an RC filter (4.7Ω, 0.1µF) to protect the EXTVCC pin from reaching its absolute maximum rating (-0.3V) during an output short-circuit condition. When EXTVCC is not used, connect it to SGND.
10	BST	Bootstrap Capacitor. Connect a 0.1µF ceramic capacitor between BST and LX.
11, 12	LX	Switching Node Pins. Connect LX pins to the switching side of the inductor.
13, 14	PGND	Power Ground Pins of the Converter. Connect externally to the power ground plane. Refer to the ADPL13602 Evaluation Kit data sheet for a layout example.
15, 16	V_{IN}	Power-Supply Input Pins. 3.5V to 36V input-supply range. Decouple to PGND with a minimum 2.2µF capacitor; place the capacitor close to the V_{IN} and PGND pins. See *Input Capacitor Selection* for more details.
—	EP	Exposed Pad. Always connect EP to the SGND pin of the IC. Also, connect EP to a large plane with several thermal vias for best thermal performance. Refer to the ADPL13602 Evaluation Kit data sheet for an example of the correct method for EP connection and thermal vias.

TYPICAL PERFORMANCE CHARACTERISTICS

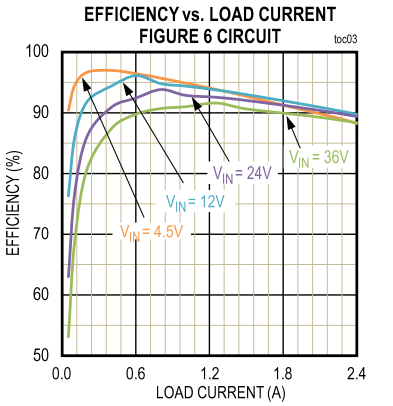
($V_{EN/UVLO}$ = V_{IN} = 24V, V_{SGND} = V_{PGND} = 0V, C_{VCC} = 2.2µF, C_{BST} = 0.1µF, C_{SS} = 6800pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND, unless otherwise noted.)



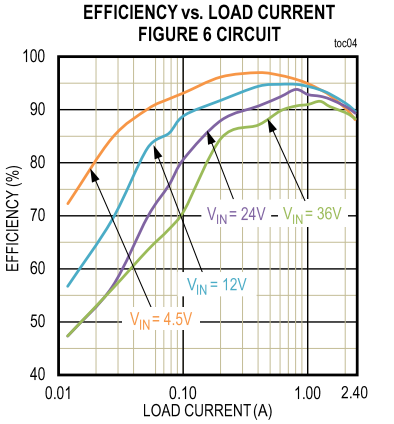
CONDITIONS: 5V OUTPUT, PWM MODE, f_{SW} = 500kHz



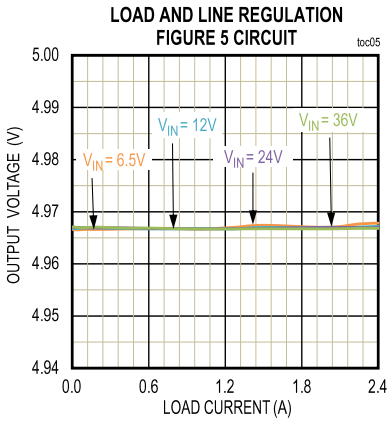
CONDITIONS: 5V OUTPUT, DCM MODE, f_{SW} = 500kHz



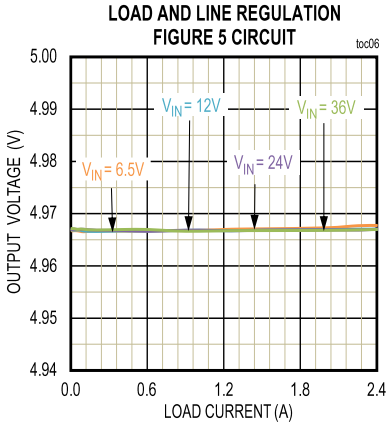
CONDITIONS: 3.3V OUTPUT, PWM MODE, f_{SW} = 500kHz



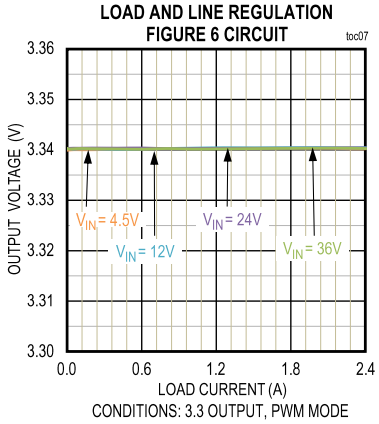
CONDITIONS: 3.3V OUTPUT, DCM MODE, f_{SW} = 500kHz



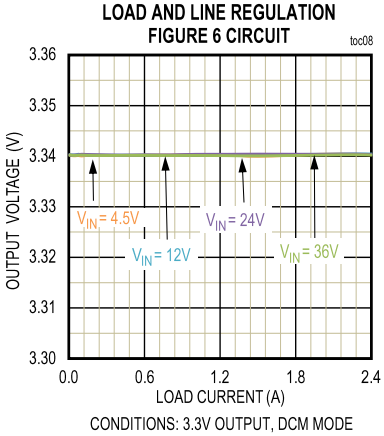
CONDITIONS: 5V OUTPUT, PWM MODE



CONDITIONS: 5V OUTPUT, DCM MODE



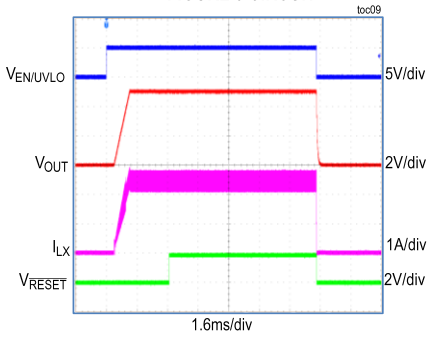
CONDITIONS: 3.3 OUTPUT, PWM MODE



CONDITIONS: 3.3V OUTPUT, DCM MODE

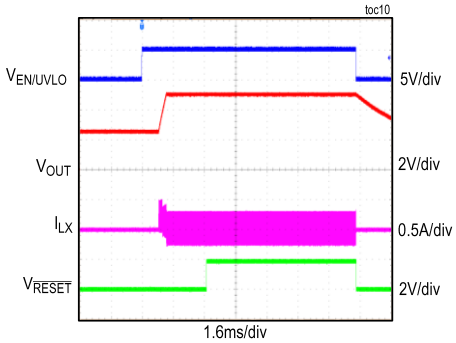
($V_{EN/UVLO}$ = V_{IN} = 24V, V_{SGND} = V_{PGND} = 0V, C_{VCC} = 2.2µF, C_{BST} = 0.1µF, C_{SS} = 6800pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND, unless otherwise noted.)

SOFT-START/SHUTDOWN THROUGH EN/UVLO
FIGURE 5 CIRCUIT



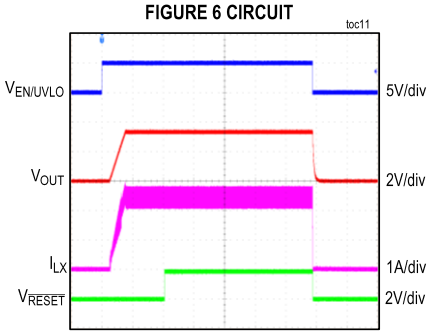
CONDITIONS: 5V OUTPUT, PWM MODE, 2.08Ω RESISTIVE LOAD

SOFT-START WITH PREBIAS VOLTAGE OF 2.5V
FIGURE 5 CIRCUIT



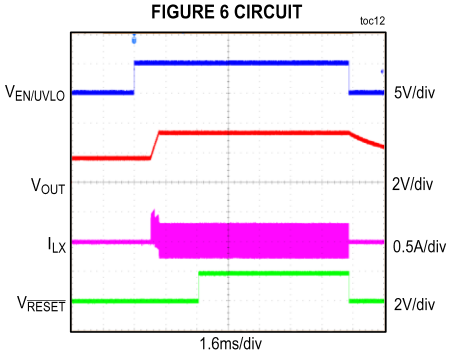
CONDITIONS: 5V OUTPUT, PWM MODE, 250Ω RESISTIVE LOAD

SOFT-START/SHUTDOWN THROUGH EN/UVLO
FIGURE 6 CIRCUIT



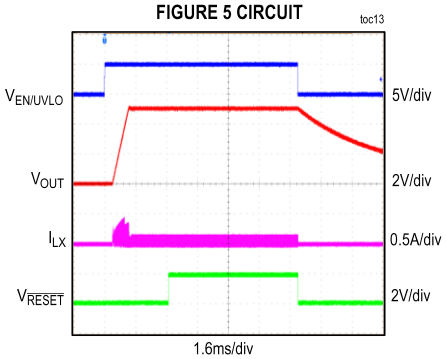
CONDITIONS: 3.3V OUTPUT, PWM MODE, 1.38Ω RESISTIVE LOAD

SOFT-START WITH PREBIAS VOLTAGE OF 1.65V
FIGURE 6 CIRCUIT



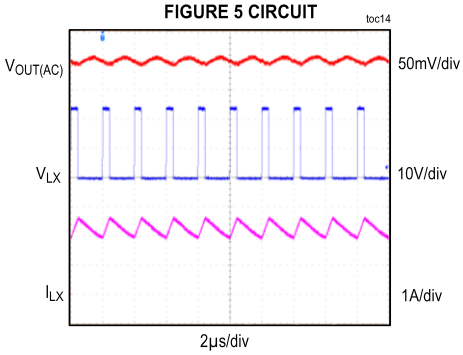
CONDITIONS: 3.3V OUTPUT, PWM MODE, 165Ω RESISTIVE LOAD

SOFT-START/SHUTDOWN THROUGH EN/UVLO
FIGURE 5 CIRCUIT



CONDITIONS: 5V OUTPUT, DCM MODE, 250Ω RESISTIVE LOAD

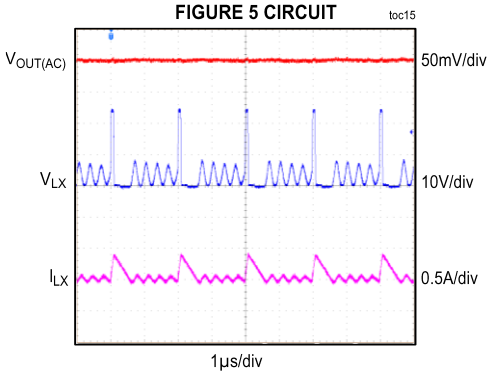
STEADY-STATE PERFORMANCE
FIGURE 5 CIRCUIT



CONDITIONS: 5V OUTPUT, PWM MODE, 2.4A LOAD

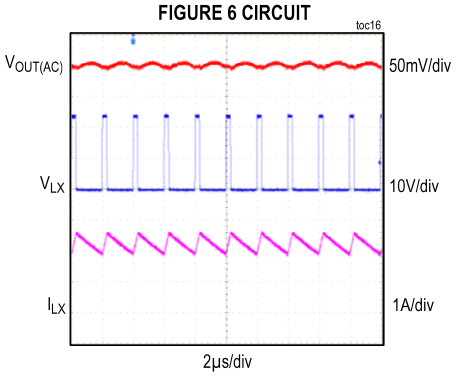
($V_{EN/UVLO}$ = V_{IN} = 24V, V_{SGND} = V_{PGND} = 0V, C_{VCC} = 2.2µF, C_{BST} = 0.1µF, C_{SS} = 6800pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND, unless otherwise noted.)

STEADY-STATE PERFORMANCE
FIGURE 5 CIRCUIT



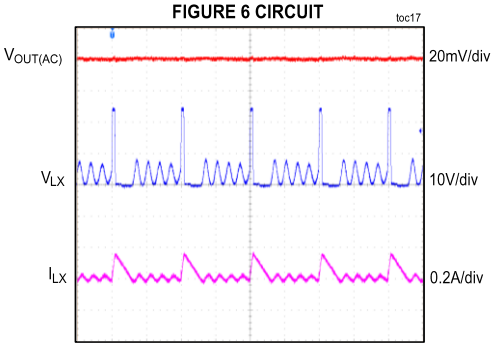
CONDITIONS: 5V OUTPUT, DCM MODE, 20mA LOAD

STEADY-STATE PERFORMANCE
FIGURE 6 CIRCUIT



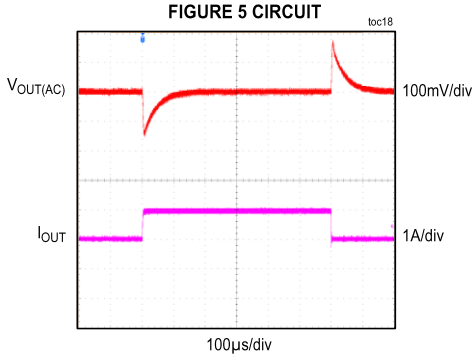
CONDITIONS: 3.3V OUTPUT, PWM MODE, 2.4A LOAD

STEADY-STATE PERFORMANCE
FIGURE 6 CIRCUIT



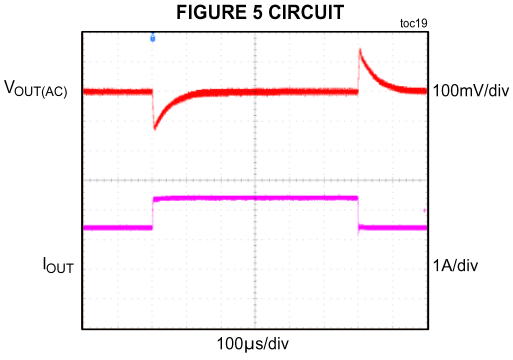
CONDITIONS: 3.3V OUTPUT, DCM MODE, 20mA LOAD

LOAD TRANSIENT BETWEEN 0A AND 1A
FIGURE 5 CIRCUIT



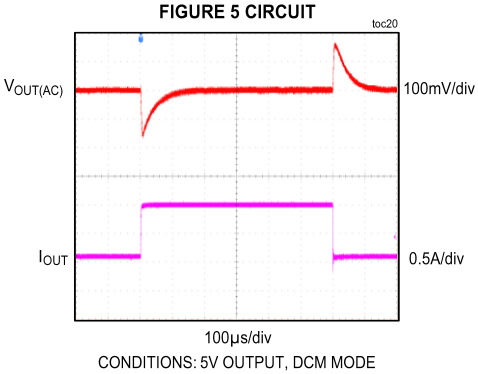
CONDITIONS: 5V OUTPUT, PWM MODE

LOAD TRANSIENT BETWEEN 1.4A AND 2.4A
FIGURE 5 CIRCUIT



CONDITIONS: 5V OUTPUT, PWM/DCM MODE

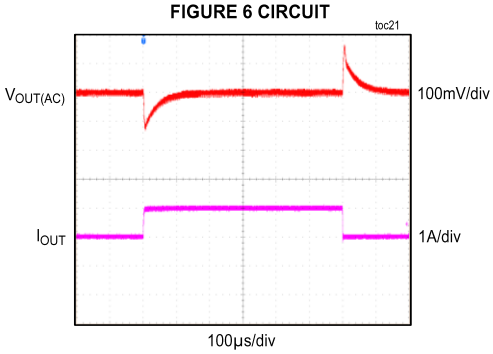
LOAD TRANSIENT BETWEEN 100mA AND 1A
FIGURE 5 CIRCUIT



CONDITIONS: 5V OUTPUT, DCM MODE

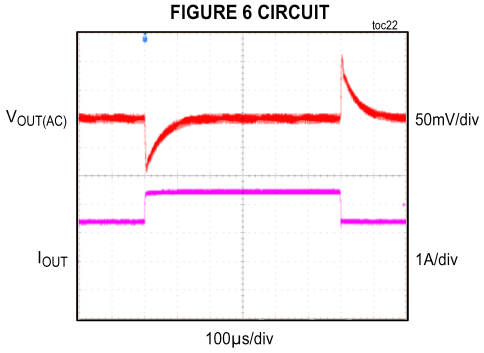
($V_{EN/UVLO}$ = V_{IN} = 24V, V_{SGND} = V_{PGND} = 0V, C_{VCC} = 2.2µF, C_{BST} = 0.1µF, C_{SS} = 6800pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND, unless otherwise noted.)

LOAD TRANSIENT BETWEEN 0A AND 1A
FIGURE 6 CIRCUIT



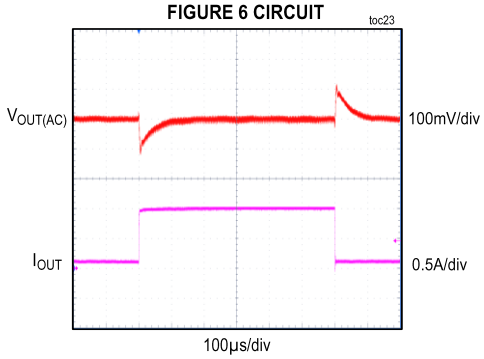
CONDITIONS: 3.3V OUTPUT, PWM MODE

LOAD TRANSIENT BETWEEN 1.4A AND 2.4A
FIGURE 6 CIRCUIT



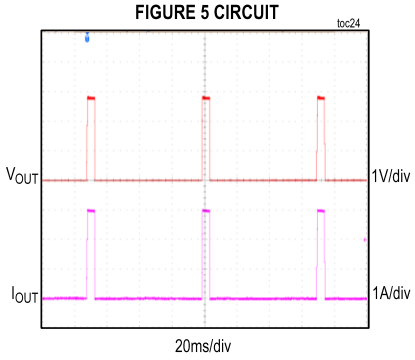
CONDITIONS: 3.3V OUTPUT, PWM/DCM MODE

LOAD TRANSIENT BETWEEN 100mA AND 1A
FIGURE 6 CIRCUIT



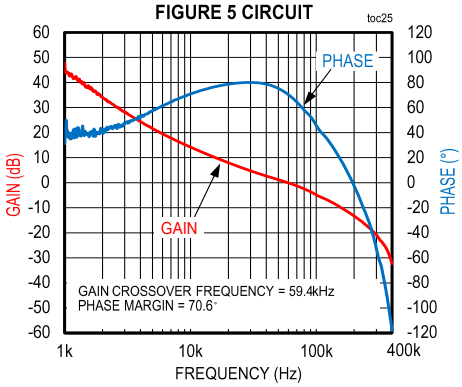
CONDITIONS: 3.3V OUTPUT, DCM MODE

OVERLOAD PROTECTION
FIGURE 5 CIRCUIT



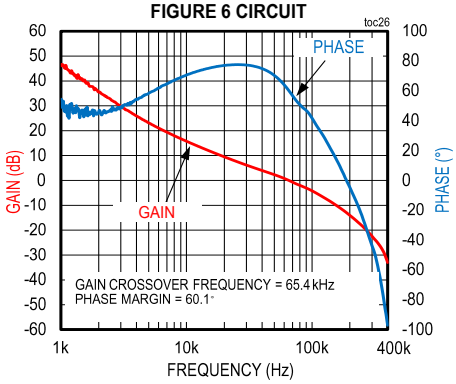
CONDITIONS: 5V OUTPUT, PWM MODE, R_{LOAD} = 1.1Ω

BODE PLOT
FIGURE 5 CIRCUIT



CONDITIONS: 5V OUTPUT, 2.4A LOAD

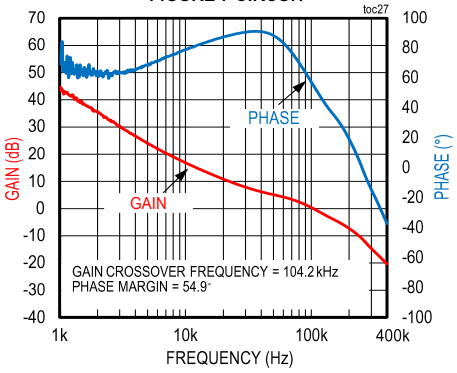
BODE PLOT
FIGURE 6 CIRCUIT



CONDITIONS: 3.3V OUTPUT, 2.4A LOAD

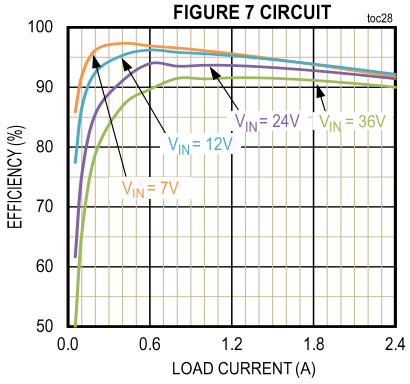
($V_{EN/UVLO}$ = V_{IN} = 24V, V_{SGND} = V_{PGND} = 0V, C_{VCC} = 2.2µF, C_{BST} = 0.1µF, C_{SS} = 6800pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND, unless otherwise noted.)

BODE PLOT
FIGURE 7 CIRCUIT



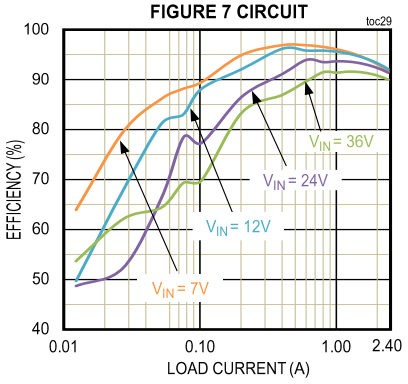
CONDITIONS: 5V OUTPUT, 2.4A LOAD, f_{SW} = 1MHz

EFFICIENCY vs. LOAD CURRENT
FIGURE 7 CIRCUIT



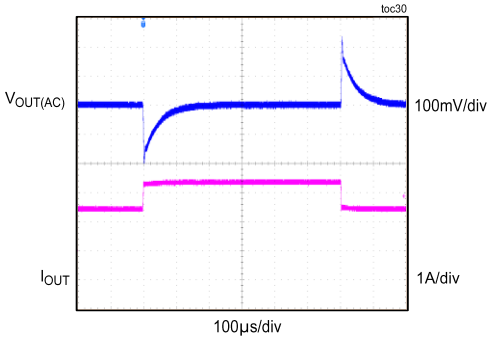
CONDITIONS: 5V OUTPUT, PWM MODE, f_{SW} = 1MHz

EFFICIENCY vs. LOAD CURRENT
FIGURE 7 CIRCUIT



CONDITIONS: 5V OUTPUT, DCM MODE, f_{SW} = 1MHz

LOAD TRANSIENT BETWEEN 1.4A AND 2.4A
FIGURE 7 CIRCUIT



CONDITIONS: 5V OUTPUT, PWM MODE, f_{SW} = 1MHz

BLOCK DIAGRAM

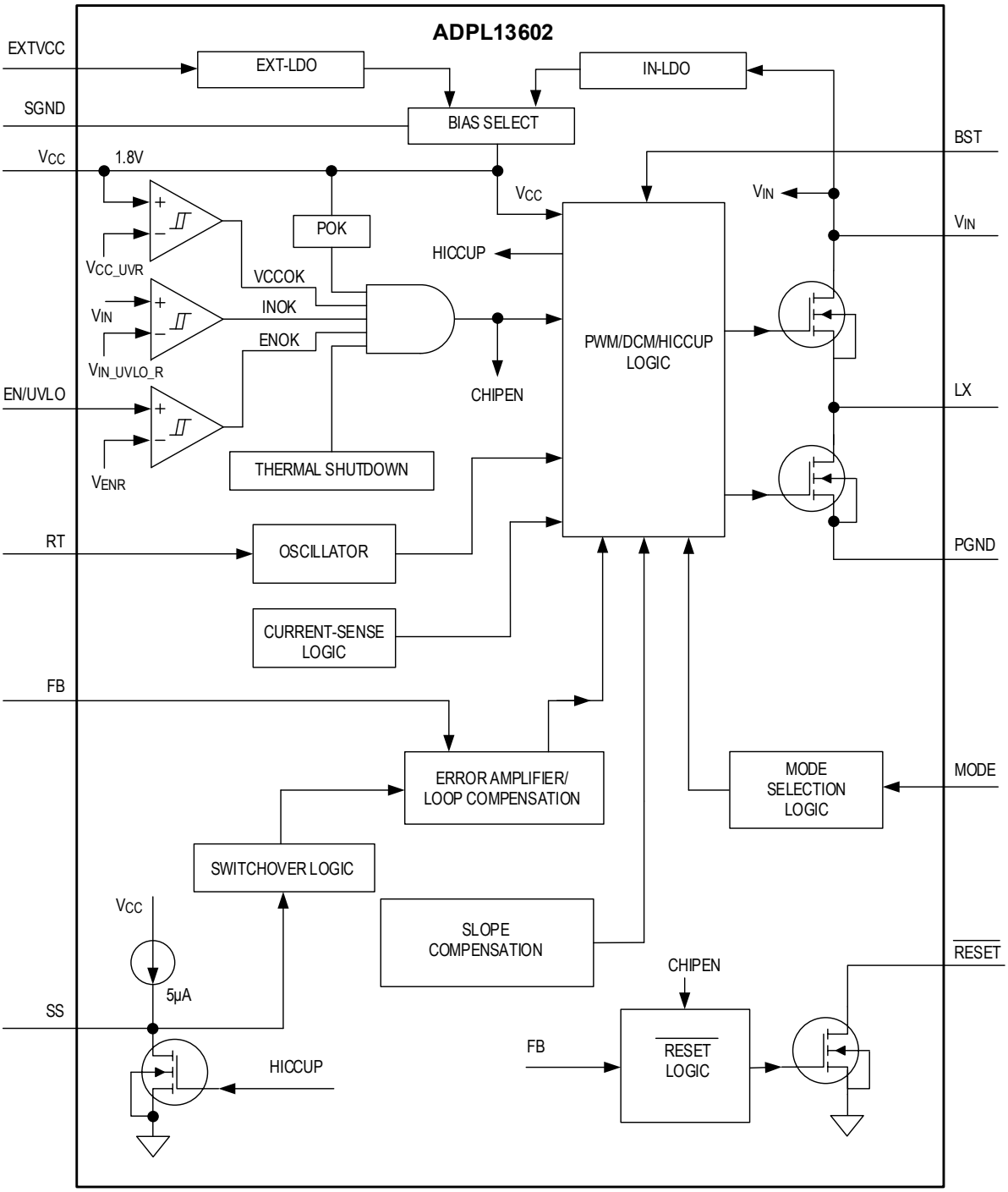


Figure 2. Block Diagram

DETAILED DESCRIPTION

The ADPL13602 is a high-efficiency, synchronous step-down DC-DC converter with integrated MOSFETs. It can deliver up to 2.4A over an input voltage range of 3.5V to 36V. Built-in compensation across the output-voltage range eliminates the need for external compensation components. The feedback-voltage regulation accuracy over -40°C to +125°C is ±1.5%.

The device features a peak-current-mode control architecture. An internal transconductance error amplifier produces an integrated error voltage at an internal node, which sets the duty cycle using a PWM comparator, a high-side current-sense amplifier, and a slope-compensation generator. At each rising edge of the clock, the high-side MOSFET turns on and remains on until either the appropriate or maximum duty cycle is reached, or the peak current limit is detected. During the high-side MOSFET's on-time, the inductor current ramps up. During the second half of the switching cycle, the high-side MOSFET turns off, and the low-side MOSFET turns on. The inductor releases the stored energy as its current ramps down and provides current to the output.

The device features a MODE pin that can be used to operate the device in PWM or DCM mode. The device also features an adjustable-input undervoltage lockout, adjustable soft-start, and output voltage monitoring with open-drain $\overline{\text{RESET}}$. The ADPL13602 offers a low minimum on time, allowing high switching frequencies and a smaller solution size.

Mode Selection (MODE)

The ADPL13602 supports forced PWM and DCM modes of operation. The device enters the required mode of operation based on the setting of the MODE pin as detected during power-up after V_{IN}, V_{CC}, and EN/UVLO voltages exceed their respective UVLO rising thresholds ($V_{IN\_UVLO\_R}$, V_{CC_UVR}, V_{ENR}). If the state of the MODE pin is high (> V_{M_DCM}), the device operates in DCM mode at light loads. If the state of the MODE pin is low (< V_{M_PWM}), the device operates in constant-frequency PWM mode at all loads. See the MODE section in the *Specifications* table for details.

PWM Mode Operation

In PWM mode, the inductor current is allowed to go negative. PWM operation provides constant frequency operation at all loads and is useful in applications sensitive to switching frequency. However, the PWM mode of operation gives lower efficiency at light loads than the DCM mode of operation.

DCM Mode Operation

In the DCM mode of operation, the inductor current can be discontinuous at light loads. The inductor current is not allowed to go negative. Switching pulses are skipped when the buck converter is operated close to no-load condition. DCM operation offers better efficiency performance compared to PWM at light loads. The steady-state output voltage ripple in DCM mode is comparable to that in PWM mode.

Linear Regulator (V_{cc} and EXTVCC)

The ADPL13602 has two built-in low dropout (LDO) linear regulators that power V_{CC}. One LDO is powered from V_{IN} (IN-LDO), while the other LDO is powered from EXTVCC (EXT LDO). The IN-LDO is enabled either during power-up or when the voltage on the EN/UVLO pin is recycled. Only one of the two LDOs is in operation at a time, depending on the voltage present at EXTVCC. If EXTVCC is greater than 2.4V (typ), V_{CC} is powered by EXT LDO. Powering V_{CC} from EXTVCC increases efficiency at higher input voltages. The typical V_{CC} output voltage is 1.8V. Bypass V_{CC} to SGND with a 2.2µF low-ESR ceramic capacitor. V_{CC} powers the internal blocks and the low-side MOSFET driver. V_{CC} also recharges the external bootstrap capacitor.

The ADPL13602 employs an undervoltage-lockout circuit that forces the buck converter off when V_{CC} falls below the falling threshold (V_{CC_UVR} - V_{CC_HYS}). The buck converter can be immediately enabled again when $V_{CC} > V_{CC\_UVR}$. The 65mV (typ) UVLO hysteresis prevents chattering on power-up/power-down.

If the buck converter output is shorted to ground in applications where the converter output is connected to the EXTVCC pin, then the transfer from EXT LDO to the IN-LDO happens seamlessly without any impact to normal functionality. Add a local bypass capacitor of 0.1µF on the EXTVCC pin to SGND and a 4.7Ω resistor from the buck regulator output node to the EXTVCC pin to protect the EXTVCC pin from reaching its absolute maximum rating (-0.3V) during output short-circuit conditions. Connect EXTVCC pin to SGND when not in use.

Setting the Switching Frequency (RT)

The switching frequency of the device can be programmed between 400kHz and 1.5MHz by using a resistor connected from the RT pin to SGND. The switching frequency (f_{SW}) is related to the resistor connected at the RT pin (R_{RT}) by the following equation:

$$R_{RT} = \frac{20625}{f_{SW}} - 1$$

where, R_{RT} is in kΩ and f_{SW} is in kHz. Leaving the RT pin open makes the device operate at the default switching frequency of 500kHz. See *Table 4* for RT resistor values for a few common switching frequencies.

Table 4. Switching Frequency vs. RT Resistor

SWITCHING FREQUENCY (kHz)	RT RESISTOR (kΩ)
400	51.1
500	Open
500	40.2
1500	12.7

Operating Input Voltage Range

The minimum and maximum operating input voltages for a given output voltage setting should be calculated as follows:

$$V_{IN(MIN)} = \frac{V_{OUT} + \left(I_{OUT(MAX)} \times \left(R_{DCR(MAX)} + R_{DS\_ONL(MAX)}\right)\right)}{1 - \left(f_{SW(MAX)} \times t_{OFF\_MIN(MAX)}\right)} + \left(I_{OUT(MAX)} \times \left(R_{DS\_ONH(MAX)} - R_{DS\_ONL(MAX)}\right)\right)$$

$$V_{IN(MAX)} = \frac{V_{OUT}}{f_{SW(MAX)} \times t_{ON\_MIN(MAX)}}$$

where:

V_{OUT} = Programmed steady-state output voltage

$I_{OUT(MAX)}$ = Maximum load current

$R_{DCR(MAX)}$ = Worst-case DC resistance of the inductor

$f_{SW(MAX)}$ = Maximum switching frequency

$t_{OFF\_MIN(MAX)}$ = Worst-case minimum switch off-time (150ns)

$t_{ON\_MIN(MAX)}$ = Worst-case minimum switch on-time (90ns)

$R_{DS\_ONL(MAX)}$ and $R_{DS\_ONH(MAX)}$ = Worst-case on-state resistances of low-side and high-side internal MOSFETs, respectively.

The maximum slew rate that can be applied on input voltage is 30V/µsec.

Overcurrent Protection (OCP)/Hiccup Mode

The ADPL13602 features a robust overcurrent-protection (OCP) scheme that protects the device during overload and output short-circuit conditions.

The OCP scheme protects the device by using a hysteretic current control during startup. The startup time is the sum of the programmed soft-start time and 2048 programmed switching frequency clock cycles. When the inductor current exceeds I_{PEAK_LIMIT} (3.4A (typ)), the high-side MOSFET is turned off, and the low-side MOSFET is turned on. After the inductor current falls below 0.85 x I_{PEAK_LIMIT}, the low-side MOSFET is turned off, and the high-side MOSFET is turned on at the next clock rising edge.

In a steady state, the device operates in a cycle-by-cycle peak current limit that turns off the high-side MOSFET when the inductor current exceeds I_{PEAK_LIMIT} and turns on the low-side MOSFET. The low-side switch is turned off, and the high-side switch is turned on at the next clock rising edge. If the feedback voltage drops below V_{FB_HICF} due to a fault condition any time after startup time is complete, the hiccup mode is triggered.

In hiccup mode, the converter is protected by suspending switching for a hiccup timeout period of 32,768 clock cycles of the programmed switching frequency before soft-start is attempted again. During startup time, if feedback voltage does not exceed V_{FB_HICF}, the device continues to operate in hysteretic control. The hiccup mode of operation ensures low average power dissipation under output short-circuit conditions.

$\overline{\text{RESET}}$ Output

The device includes a $\overline{\text{RESET}}$ comparator to monitor the status of the output voltage. The open-drain $\overline{\text{RESET}}$ output requires an external pullup resistor. $\overline{\text{RESET}}$ goes high (high impedance) 1024 switching cycles after the FB voltage increases above V_{FB_OKR}. $\overline{\text{RESET}}$ goes low when the FB voltage drops to below V_{FB_OKF}. $\overline{\text{RESET}}$ also goes low during thermal shutdown or when the EN/UVLO pin goes below the EN/UVLO falling threshold (V_{ENR} - V_{EN_HYS}).

Prebiased Output

In a prebiased output condition, both the high-side and the low-side switches are turned off so that the converter does not sink current from the output. High-side and low-side switches do not start switching until the PWM comparator commands the first PWM pulse, at which point switching commences. The output voltage is then smoothly ramped up to the target value in alignment with the internal reference.

Thermal Shutdown Protection

Thermal shutdown protection limits the junction temperature of the device. When the device's junction temperature exceeds +160°C, an on-chip thermal sensor shuts down the device, allowing the device to cool. The device turns on with soft-start after the junction temperature reduces by 20°C. Carefully evaluate the total power dissipation (see the *Power Dissipation* section) to avoid unwanted triggering of thermal shutdown during normal operation.

APPLICATIONS INFORMATION

Input Capacitor Selection

The input filter capacitor reduces peak currents drawn from the power source, reducing noise and voltage ripple on the input caused by the circuit's switching. The following equation defines the input capacitor RMS current requirement (I_{RMS}).

$$I_{RMS} = I_{OUT(MAX)} \times \frac{\sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}}$$

where, $I_{OUT(MAX)}$ is the maximum load current. I_{RMS} has a maximum value when the input voltage equals twice the output voltage ($V_{IN} \approx 2 \times V_{OUT}$), so

$$I_{RMS(MAX)} = \frac{I_{OUT(MAX)}}{2}.$$

Choose an input capacitor that exhibits less than +10°C temperature rise at the RMS input current for optimal long-term reliability. Use low-ESR ceramic capacitors with high-ripple-current capability at the input. X7R capacitors are recommended in industrial applications for their temperature stability. Calculate the input capacitance using the following equation:

$$C_{IN} = \frac{I_{OUT(MAX)} \times D \times (1 - D)}{\eta \times f_{SW} \times \Delta V_{IN}}$$

where:

$D = V_{OUT}/V_{IN}$ is the duty ratio of the converter

f_{SW} = switching frequency

ΔV_{IN} = allowable input-voltage ripple

η = efficiency

In applications where the source is located distant from the device input, an appropriate electrolytic capacitor should be added in parallel to the ceramic capacitor to provide necessary damping for potential oscillations caused by the inductance of the longer input power path and input ceramic capacitor.

Inductor Selection

Three key inductor parameters must be specified for operation with the device: inductance value (L), inductor saturation current (I_{SAT}) and DC resistance (R_{DCR}). The switching frequency and output voltage determine the inductor value as follows:

$$L = \frac{1.5 \times V_{OUT}}{f_{SW}}$$

where V_{OUT} and f_{SW} are nominal values and f_{SW} is in Hz. Select an inductor whose value is nearest to the value calculated by the previous formula. Select a low-loss inductor closest to the calculated value with acceptable dimensions and having the lowest possible DC resistance. The saturation current rating (I_{SAT}) of the inductor must be high enough to ensure that saturation can occur only above the peak current-limit value of I_{PEAK_LIMIT}.

Output Capacitor Selection

X7R ceramic output capacitors are preferred due to their stability over temperature in industrial applications. The output capacitors are usually sized to support a step load of 40% of the maximum output current in the application, so output-voltage deviation is contained to 3% of the output-voltage change. The minimum required output capacitance can be calculated as follows:

$$C_{OUT} = \frac{1}{2} \times \frac{I_{STEP} \times t_{RESPONSE}}{\Delta V_{OUT}}$$

$$t_{RESPONSE} \cong \frac{0.33}{f_C}$$

where:

I_{STEP} = Load current step

$t_{RESPONSE}$ = Response time of the controller

ΔV_{OUT} = Allowable output-voltage deviation

f_C = Target closed-loop crossover frequency

f_{SW} = Switching frequency.

Select f_C to be 1/9th of f_{SW} if the switching frequency is less than or equal to 900kHz. If the switching frequency is more than 900kHz, select f_C to be 100kHz. Actual derating of ceramic capacitors with DC-bias voltage must be considered while selecting the output capacitor. Derating curves are available from all major ceramic capacitor manufacturers.

Soft-Start Capacitor Selection

The device implements an adjustable soft-start operation to reduce inrush current. A capacitor connected from the SS pin to SGND programs the soft-start time. The selected output capacitance (C_{SEL}) and the output voltage (V_{OUT}) determine the minimum required soft-start capacitor as follows:

$$C_{SS} \geq 28 \times 10^{-6} \times C_{SEL} \times V_{OUT}$$

The soft-start time (t_{SS}) is related to the capacitor connected at SS (C_{SS}) by the following equation:

$$t_{SS} = \frac{C_{SS}}{8.325 \times 10^{-6}}$$

For example, to program a 0.82ms soft-start time, a 6.8nF capacitor should be connected from the SS pin to SGND. During startup, the device operates at half the programmed switching frequency until the FB pin voltage rises above 0.44V.

Setting the Input Undervoltage-Lockout Level

The device offers an adjustable input undervoltage-lockout level. Set the voltage at which the device turns on with a resistive voltage-divider connected from V_{IN} to SGND (See *Figure 3*). Connect the center node of the divider to EN/UVLO. Choose R1 to be 3.3MΩ and then calculate R2 as follows:

$$R2 = \frac{R1 \times 1.25}{(V_{INU} - 1.25)}$$

where V_{INU} is the input-voltage level at which the device is required to turn on. Ensure that V_{INU} is higher than 0.8 x V_{OUT} to avoid hiccup during slow power-up (slower than soft-start)/power-down. If the EN/UVLO pin is driven from an external signal source, a series resistance of a minimum of 1kΩ is recommended to be placed between the output pin of the signal source and the EN/UVLO pin to reduce voltage ringing on the line.

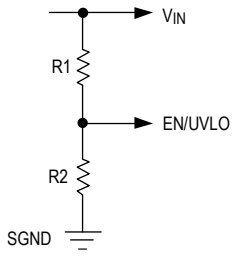


Figure 3. Setting the Input Undervoltage Lockout

Adjusting Output Voltage

The output voltage of the buck converter can be programmed between 1V to 90% of V_{IN}. Set the output voltage with a resistive voltage-divider connected from the output-voltage node (V_{OUT}) to SGND (see *Figure 4*). Connect the center node of the divider to the FB pin. Use the following procedure to choose the resistive voltage-divider values:

Calculate resistor R_{TOP} from the output to the FB pin as follows:

$$R_{TOP} = \frac{227}{(f_C \times C_{OUT\_SEL})}$$

where:

R_{TOP} is in KΩ

f_C = Crossover frequency in Hz

C_{OUT_SEL} = Actual capacitance of selected output capacitor at DC-bias voltage in F.

Calculate resistor R_{BOT} from the FB pin to SGND as follows:

$$R_{BOT} = \frac{R_{TOP} \times 0.6}{(V_{OUT} - 0.6)}$$

R_{BOT} is in kΩ.

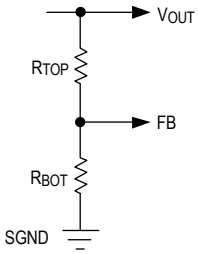


Figure 4. Setting the Output Voltage

Power Dissipation

At a particular operating condition, the power losses that lead to temperature rise of the part are estimated as follows:

$$P_{LOSS} = \left(P_{OUT} \times \left(\frac{1}{\eta} - 1\right)\right) - \left(I_{OUT}{}^2 \times R_{DCR}\right)$$

$$P_{OUT} = V_{OUT} \times I_{OUT}$$

where:

P_{OUT} = Output power

η = Efficiency of the converter

R_{DCR} = DC resistance of the inductor (see the *Typical Performance Characteristics* for more information on efficiency at typical operating conditions).

For a typical multilayer board, the thermal performance metrics for the package are as follows:

θ_{JA} = 38°C/W

θ_{JC} = 4°C/W

The junction temperature of the device can be estimated at any given maximum ambient temperature ($T_{A(MAX)}$) from the following equation:

$$T_{J(MAX)} = T_{A(MAX)} + (\theta_{JA} \times P_{LOSS})$$

If the application has a thermal-management system that ensures that the exposed pad of the device is maintained at a given temperature ($T_{EP(MAX)}$) by using proper heat sinks, then the junction temperature of the device can be estimated at any given maximum ambient temperature as:

$$T_{J(MAX)} = T_{EP(MAX)} + (\theta_{JC} \times P_{LOSS})$$

Note: Junction temperatures greater than +125°C degrade operating lifetimes.

Printed Circuit Board (PCB) Layout Guidelines

All connections carrying pulsed currents must be very short and as wide as possible. The inductance of these connections must be kept to an absolute minimum due to the high di/dt of the currents. Since the inductance of a current-carrying loop is proportional to the area enclosed by the loop, if the loop area is made very small, inductance is reduced. Additionally, small-current loop areas reduce radiated Electromagnetic Interference (EMI).

A ceramic input filter capacitor should be placed close to the V_{IN} pins of the IC. This eliminates as many trace inductance effects as possible and gives the IC a cleaner voltage supply. A bypass capacitor for the V_{CC} pin should also be placed close to the pin to reduce the effects of trace impedance.

When routing the circuitry around the IC, the signal ground and the power ground for switching currents must be kept separate. They should be connected at a point where switching activity is minimal. This helps to keep the signal ground quiet. The power ground plane should be kept continuous (unbroken) as far as possible. No trace carrying a high switching current should be placed directly over any ground plane discontinuity.

PCB layout also affects the thermal performance of the design. A number of thermal throughputs or vias that connect to a large plane should be provided under the exposed pad of the device for efficient heat dissipation.

For a sample layout that ensures first-pass success, refer to the ADPL13602 evaluation kit layout available at *www.analog.com*.

TYPICAL APPLICATION CIRCUITS

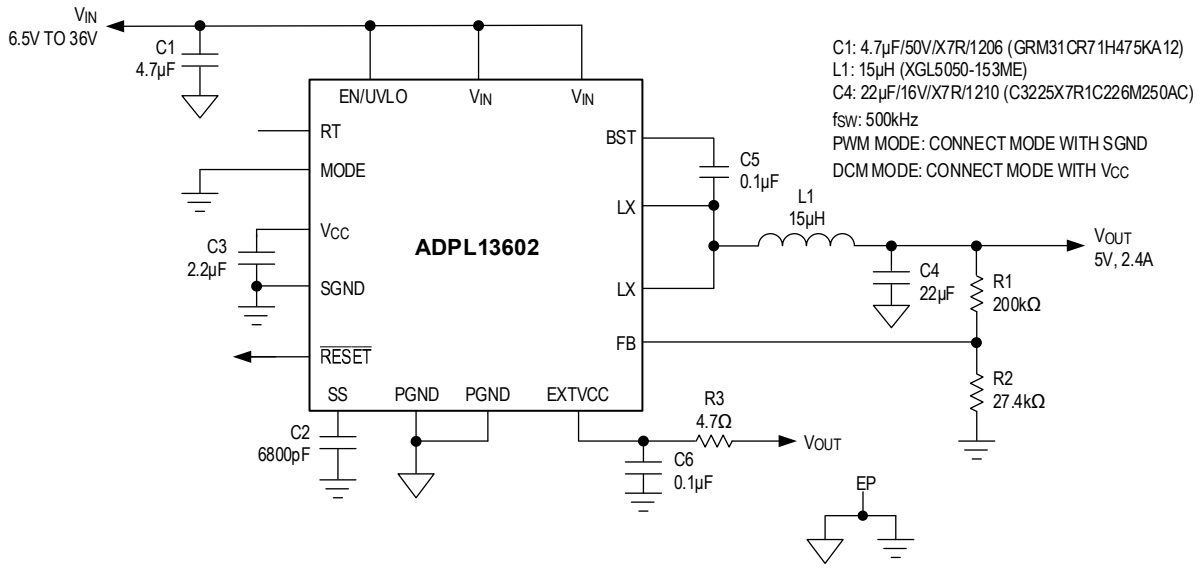


Figure 5. 5V Output with 500kHz Switching Frequency

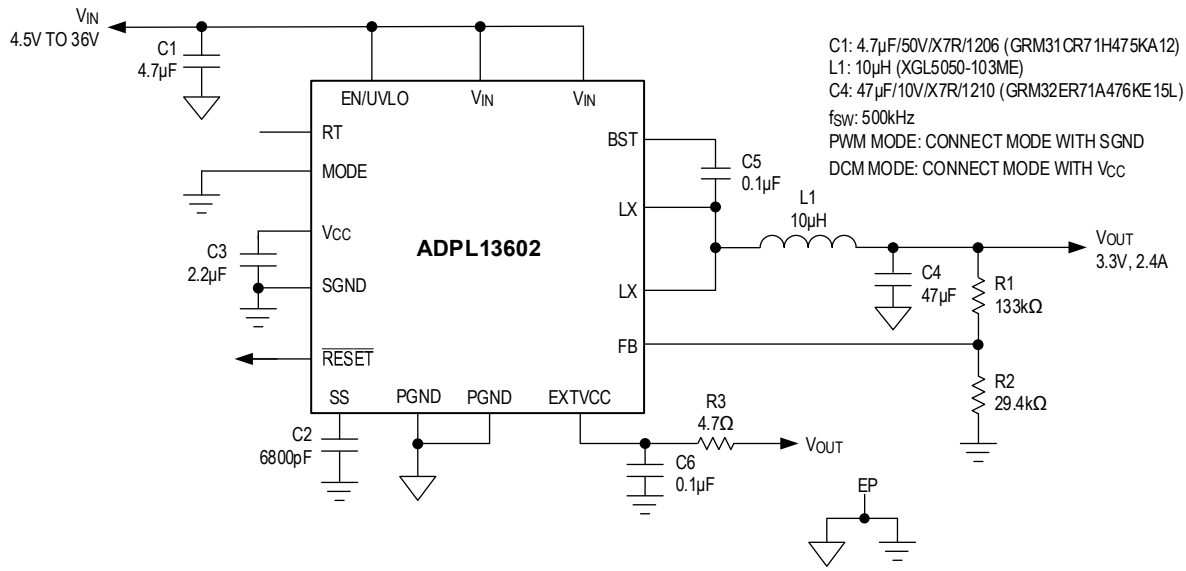


Figure 6. 3.3V Output with 500kHz Switching Frequency

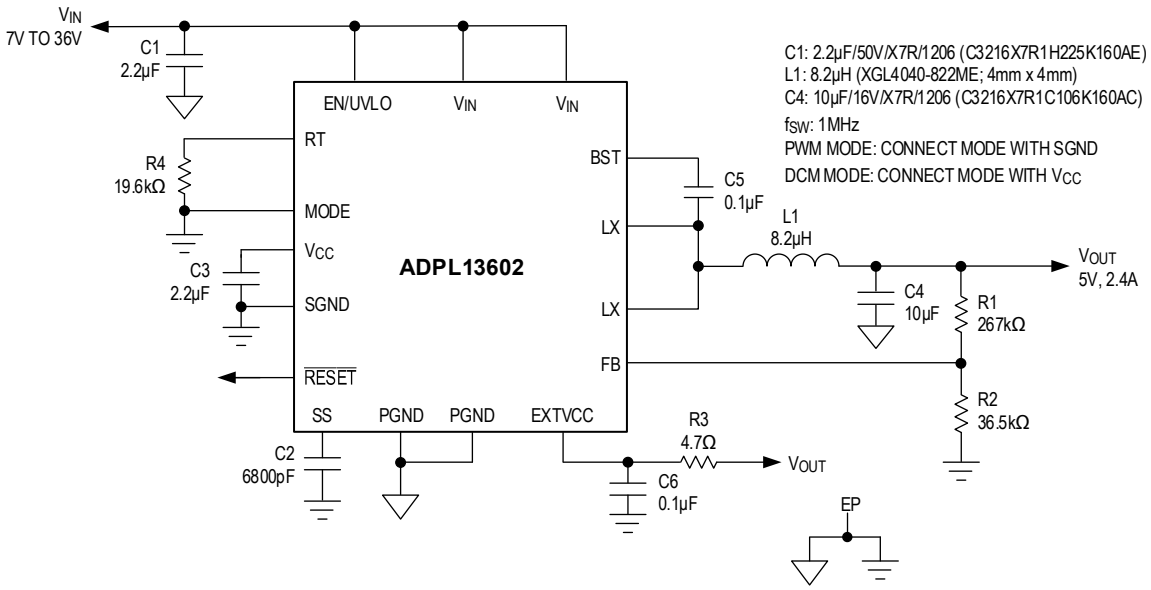
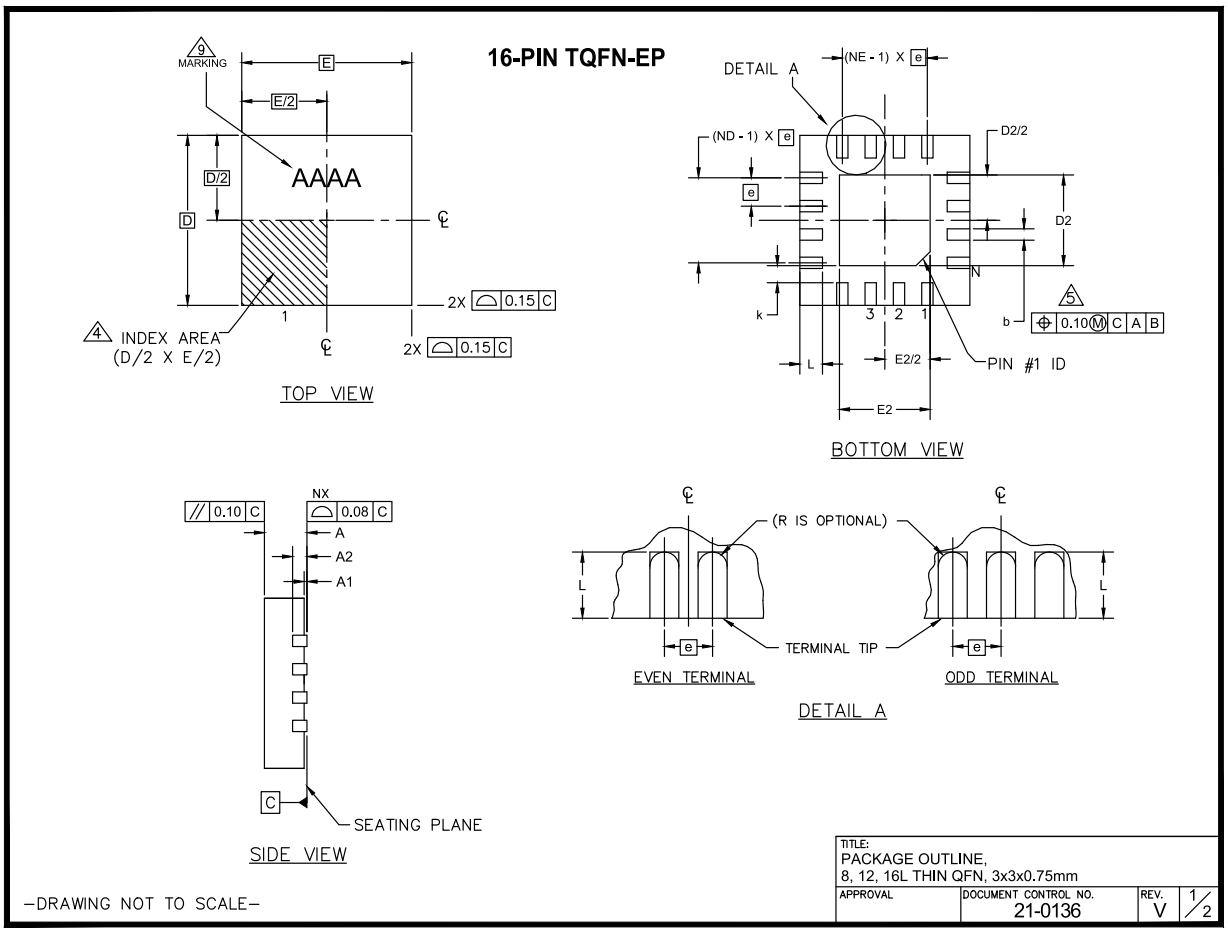


Figure 7. 5V Output with 1MHz Switching Frequency

OUTLINE DIMENSIONS



Package Code: T1633-5C			
PKG	16L 3x3		
REF	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
b	0.20	0.25	0.30
D		3.00 BSC	
E		3.00 BSC	
e		0.50 BSC	
L	0.25	0.35	0.45
N		16	
ND		4	
NE		4	
A1	0	0.02	0.05
A2		0.20 REF	
k	0.25	-	-
D2	0.95	1.10	1.25
E2	0.95	1.10	1.25

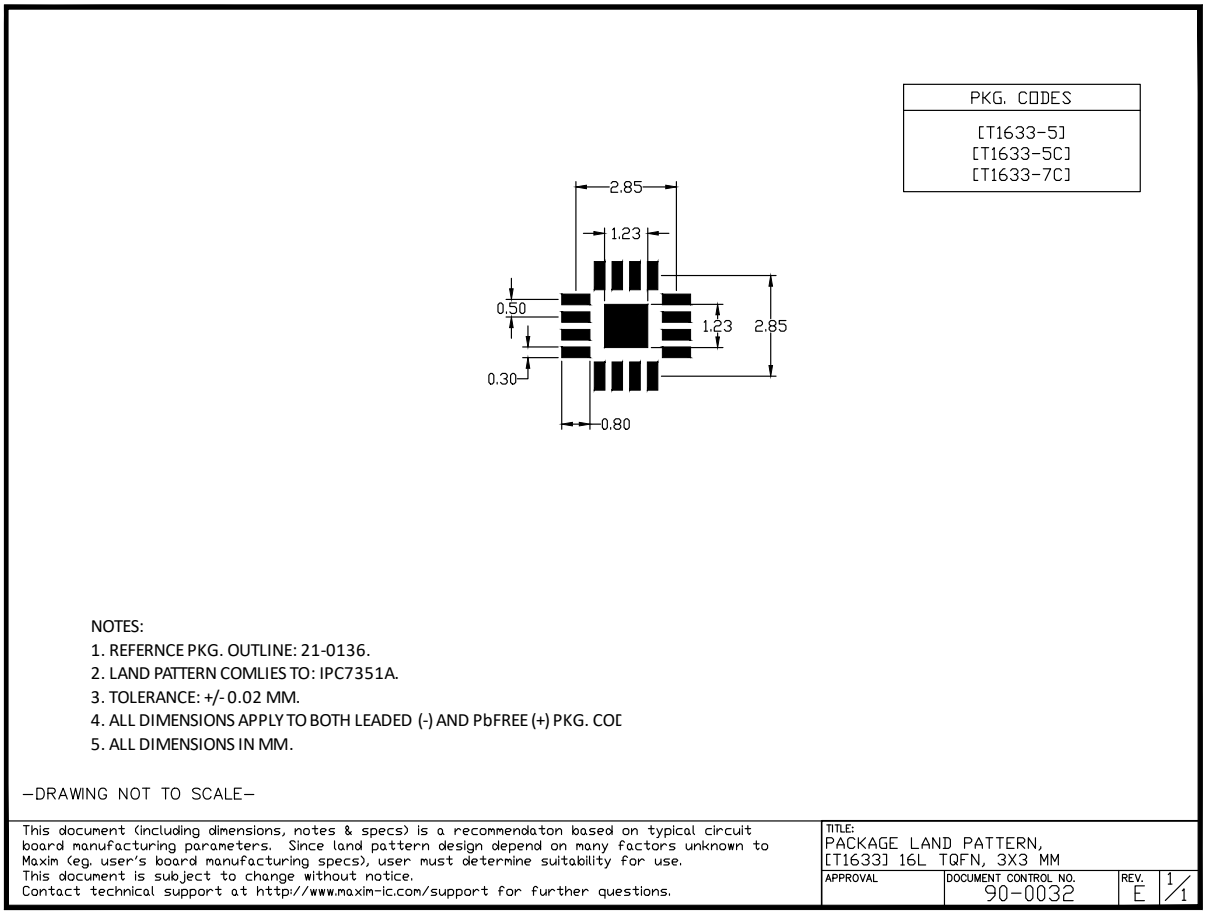
NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
2. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5-2009.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.20 mm AND 0.25 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. DRAWING CONFORMS TO JEDEC MO220 REVISION C. T1233-4, T1233-4C, T1233-5C, T1633-5, T1633-5C AND T1633-7C WITH CUSTOM LEAD DIMENSION.
9. MARKING SHOWN IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
10. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
11. WARPAGE NOT TO EXCEED 0.10mm.
12. MATERIAL MUST BE COMPLIANT WITH MAXIM SPECIFICATION 10-0131 FOR SUBSTANCE CONTENT, MUST BE Eu ROHS COMPLIANT WITHOUT EXEMPTION AND PB-FREE.
13. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND Pb FREE (+) PARTS.

—DRAWING NOT TO SCALE—

TITLE: PACKAGE OUTLINE, 8, 12, 16L THIN QFN, 3x3x0.75mm			
APPROVAL	DOCUMENT CONTROL NO. 21-0136	REV. V	2/2

LAND PATTERN



Refer to the https://www.analog.com/en/design-center/packaging-quality-symbols-footprints.html for the most recent package drawings.

Note that a “+”, “#”, or “-” in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Table 5. Thermal Resistance of 16 TQFN-EP

Thermal Resistance, Four-Layer Board (Note 4)	
Junction-to-Ambient (θ_{JA})	38°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	4°C/W

Note 4: Package thermal resistances were obtained using the ADPL13602 Evaluation Kit with no airflow.

ORDERING GUIDE

PART NUMBER	PIN-PACKAGE
ADPL13602BATE+	16 TQFN-EP* (3mm x 3mm)
ADPL13602BATE+T	16 TQFN-EP* (3mm x 3mm)

+ Denotes a lead (Pb)-free/RoHS-compliant package.
T = Tape and reel.
**EP = Exposed pad.*