Features

- **Exceeds Requirements of EIA-485 Standard**
- **Bus-Polarity Correction within 100 ms meet SGCC spec**
- **Data Rate: 300 bps to 500 kbps**
- **Works with Two Configurations:**
  - **– Failsafe Resistors Only**
  - **– Failsafe and Differential Termination Resistors**
- **Up to 256 Nodes on a Bus (1/8 unit load)**
- **Wide Supply Voltage 3V to 5.5V**
- **SOIC-8 Package for Backward Compatibility**
- **Bus-Pin Protection:**
  - **– ±18 kV HBM protection**
  - **– ±12 kV IEC61000-4-2 Contact Discharge**
  - **– ±15 kV IEC61000-4-2 Air Discharge**

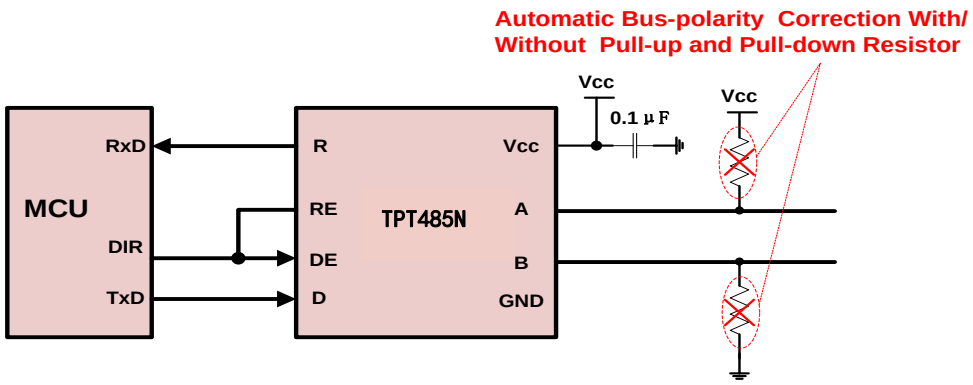
Description

The TPT485N is a low-power RS-485 transceiver with automatic bus-polarity correction and transient protection. Upon hot plug-in, the device detects and corrects the bus polarity within the first 100 ms of bus idling. On-chip transient protection protects the device against IEC61000 ESD and EFT transients. This device has robust drivers and receivers for demanding industrial applications. The bus pins are robust to electrostatic discharge (ESD) events, with high levels of protection to Human-Body Model (HBM), Air-Gap Discharge, and Contact Discharge specifications. The device combines a differential driver and a differential receiver, which operate together from a single 5-V power supply. The driver differential outputs and the receiver differential inputs are connected internally to form a bus port suitable for half-duplex (two-wire bus) communication. The device features a wide common-mode voltage range making the device suitable for multi-point applications over long cable runs. The TPT485N is available in SOP8 package, and is characterized from –40°C to 125°C.

Applications

- E-Metering Networks
- HVAC Systems
- DMX512-Networks

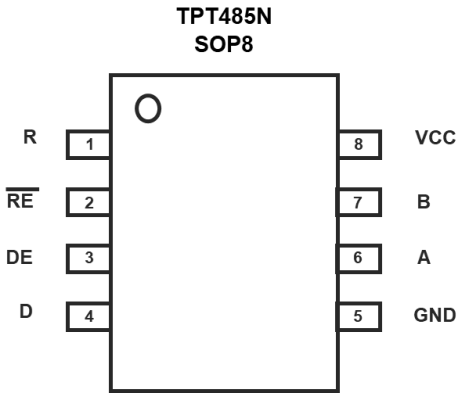
Function Block Diagram



Revision History

Date	Revision	Notes
2018/11/29	Rev. Pre 0	Initial Definition
2020/04/14	Rev. A0	Released version
2021/8/10	Rev. B	Updated Bus-Polarity Correction time
2023/11/02	Rev. B.1	Updated pinout description

Pin Configuration and Functions



Pin No.	Pin Name	I/O	Description
1	R	Digital output	Receiver data output.
2	/RE	Digital input	Receiver Enable, active low.
3	DE	Digital input	Driver Enable, active high.
4	D	Digital input	Driver data input.
5	GND	Ground	Ground.
6	A	Bus input/output	Bus I/O port, A
7	B	Bus input/ouput	Bus I/O port, B
8	V_{CC}	Power	Power Supply.

Order Information

Model Name	Order Number	Package	Transport Media, Quantity	Marking Information
TPT485N	TPT485N-SO1R	8-Pin SOP	Tape and Reel 4,000	T485N

Function Table

DRIVER PIN FUNCTIONS

INPUT	ENABLE	OUTPUTS		DESCRIPTION
D	DE	A	B	
NORMAL MODE				
H	H	H	L	Actively drives bus High
L	H	L	H	Actively drives bus Low
X	L	Z	Z	Driver disabled
X	OPEN	Z	Z	Driver disabled by default
OPEN	H	H	L	Actively drives bus High
POLARITY-CORRECTING MODE(1)				
H	H	L	H	Actively drives bus Low
L	H	H	L	Actively drives bus High
X	L	Z	Z	Driver disabled
X	OPEN	Z	Z	Driver disabled by default
OPEN	H	L	H	Actively drives bus Low

(1) The polarity-correcting mode is entered when $V_{ID} < V_{IT-}$ and $t > t_{FS}$ and DE = low. This state is latched when /RE turns from Low to High.

RECEIVER PIN FUNCTIONS

DIFFERENTIAL INPUT	ENABLE	OUTPUT	DESCRIPTION
$V_{ID} = V_A - V_B$	/RE	R	
NORMAL MODE			
$V_{IT+} < V_{ID}$	L	H	Receive valid bus High
$V_{IT-} < V_{ID} < V_{IT+}$	L	?	Indeterminate bus state
$V_{ID} < V_{IT-}$	L	L	Receive valid bus Low
X	H	Z	Receiver disabled
X	OPEN	Z	Receiver disabled
Open, short, idle Bus	L	H	Out of polarity correction time
POLARITY-CORRECTING MODE(1)			
$V_{IT+} < V_{ID}$	L	L	Receive valid bus Low
$V_{IT-} < V_{ID} < V_{IT+}$	L	?	Indeterminate bus state
$V_{ID} < V_{IT-}$	L	H	Receive polarity corrected bus High
X	H	Z	Receiver disabled
X	OPEN	Z	Receiver disabled
Open, short, idle Bus	L	H	Out of polarity correction time

(1) The polarity-correcting mode is entered when $V_{ID} < V_{IT-}$ and $t > t_{FS}$ and DE = low. This state is latched when /RE turns from Low to High.

Absolute Maximum Ratings

V_{DD} to GND..... -0.3V to +7V

Input Voltages DI, DE, RE……..……..……..... -0.3V to (VCC + 0.3V)

Input/Output Voltages A, B ….....……..……..... -15V to +15V

A, B (Transient Pulse Through 100Ω,Note 1)……..……..……..…. ±100V

R……..……..……..…. -0.3V to (VCC +0.3V)

Short Circuit Duration A, B …….…….. Continuous

ESD Rating……..…. See Specification Table

*** Note:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

(1) This data was taken with the JEDEC low effective thermal conductivity test board.

(2) This data was taken with the JEDEC standard multilayer test boards.

Recommended Operating Conditions Note 2

Supply Voltage……..…… 3V to 5.5V

Temperature Range……..…… -40°C to +125°C

Bus Pin Common Mode Voltage Range ……..…….. -7V to +12V

Thermal Resistance, ΘJA (Typical)

8-Pin SOIC Package ……..……..…… 136°C/W

Maximum Junction Temperature (Plastic Package) ……..…….. +150°C

Maximum Storage Temperature Range ……..…….. -65°C to +150°C

Note 1: Tested according to TIA/EIA-485-A, Section 4.2.6 (±100V for 15μs at a 1% duty cycle).

Note 2: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

ESD Rating

		Value	Unit
Contact Discharge, per IEC 61000-4-2	Bus Pin	12	kV
Air Discharge, per IEC 61000-4-2	Bus Pin	15	kV
HBM, per ANSI/ESDA/JEDEC JS-001 / ANSI/ESD STM5.5.1	Bus Pin	18	kV
	All Pin Except Bus Pin	4	kV
CDM, per ANSI/ESDA/JEDEC JS-002		1500	V

Electrical Characteristics

Test Conditions: VCC = 5V, Over operating free-air temperature range

Parameter		Conditions		Min	Type	Max	Units
$\|V_{OD}\|$	Driver differential-output voltage magnitude	RL = 60 Ω, -7V≤V test ≤12V	See Figure 1B	1.5	3.3		V
		RL = 54 Ω (RS-485)	See Figure 1A	1.65	3.3		
		RL = 100 Ω (RS-485)		2.0	4.4		
$\Delta\|V_{OD}\|$	Change in magnitude of driver differential-output voltage	RL = 54 Ω, CL=50pF	See Figure 1A	-50		50	mV
$V_{OC(SS)}$	Steady-stage common-mode output voltage	Center of two 27-Ω load resistors	See Figure 1A	1	V_{CC}/2	3	V
ΔV_{OC}	Change in differential driver common-mode output voltage			-50		50	mV
$V_{OC(PP)}$ (1)	Peak-to-peak driver common-mode output voltage				600		
V_{IT+}	Positive-going receiver differential-input voltage threshold					100	mV
V_{IT-}	Negative-going receiver differential-input voltage threshold			-100			mV
V_{HYS} (1)	Receiver differential-input voltage threshold hysteresis ($V_{IT+} – V_{IT–}$)				30		mV
V_{IH}	Logic Input High Voltage	DI, DE, $\overline{RE}$		2			V
V_{IL}	Logic Input Low Voltage	DI, DE, $\overline{RE}$				0.8	V
V_{OH}	Receiver high-level output voltage	I_{OH}= -8 mA		4.0			V
V_{OL}	Receiver low-level output voltage	I_{OL}= 8 mA			0.2	0.4	V
I_I	Driver input, driver enable and receiver enable input current			-5		5	μA
I_{OZ}	Receiver high-impedance output current	VO = 0 V or VCC, /RE at VCC				1	μA
$\|I_{OS}\|$	Driver short-circuit output current	$\|I_{OS}\|$ with V_A or V_B from –7 to +12 V				95	mA
I_I	Bus input current(driver disabled)	V_{CC} = 4.5 to 5.5 V or V_{CC} = 0 V, DE at 0 V	VI= 12 V (1)		55		μA
			VI= -7 V	-90		85	
I_{CC}	Supply current(quiescent)	Driver enabled, receiver disabled	DE = VCC, /RE = VCC, No LOAD		560	750	μA
		Driver disabled, receiver enabled	DE = GND, /RE = GND, No LOAD		550	700	
		Driver and receiver disabled	DE = GND, /RE = VCC, D= VCC,		0.1	2	

Note:

(1). Parameter value is provided by lab test, NOT test in production.

(2). V_{IT-} can meet -100mV spec in 5V and 25C room temperature.

Switching Characteristics

Parameter		Conditions		Min	Typ	Max	Units
Driver							
t_r, t_f	Driver differential-output rise and fall times	RL = 54 Ω, CL=50pF	See Figure 2		300	500	ns
t_{PHL}, t_{PLH}	Driver propagation delay				260	400	
$t_{SK(P)}$ (1)	Driver pulse skew, $\|t_{PHL} - t_{PLH}\|$			-10	2	10	
t_{PHZ}, t_{PLZ}	Driver disable time		See Figure 3		50	100	ns
t_{PZH}, t_{PZL}	Driver enable time	RE = 0			200	400	ns
		RE = VCC			2200	4000	
Receiver							
tr, tf (1)	Receiver output rise and fall times	CL=15 pF	See Figure 5	6	10	13	ns
t_{PHL}, t_{PLH}	Receiver propagation delay time				90	110	
$t_{SK(P)}$ (1)	Receiver pulse skew, $\|t_{PHL} - t_{PLH}\|$			-11		11	
t_{PHZ}, t_{PLZ} (1)	Receiver disable time			8		13	ns
t_{PZL}, t_{PZH}	Receiver enable time	DE = VCC	See Figure 6		100	150	ns
t_{PZL}, t_{PZH}		DE = 0	See Figure 6		2100	4000	
t_{FS}	Bus failsafe time	Driver disabled	See Figure 7	40		100	ms

Note:

(1). Parameter value is provided by lab test, NOT test in production.

Test Circuits and Waveforms

Figure 1. DC Driver Test Circuits

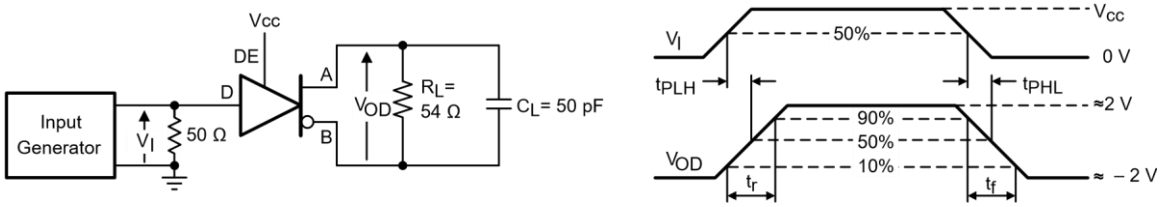


Figure 2. Driver Propagation Delay and Differential Transition Times

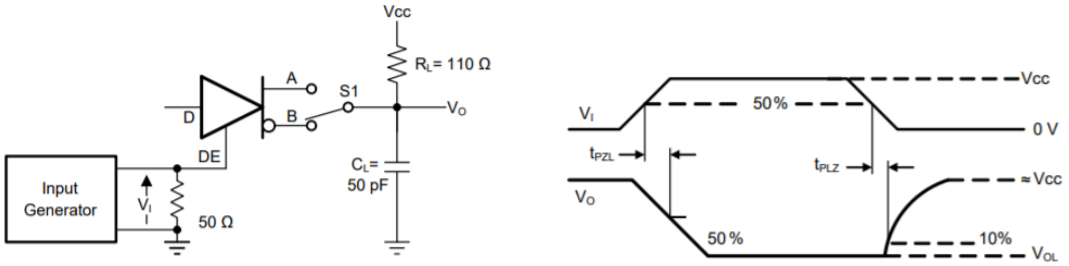


Figure 3. Driver Enable and Disable Times

Figure 4. Driver Propagation Delay and Rise/Fall Time Measurement

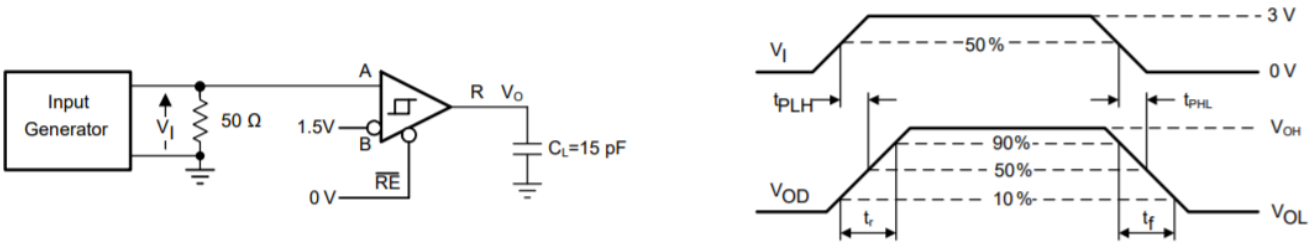


Figure 5. Receiver Propagation Delay and Data rate

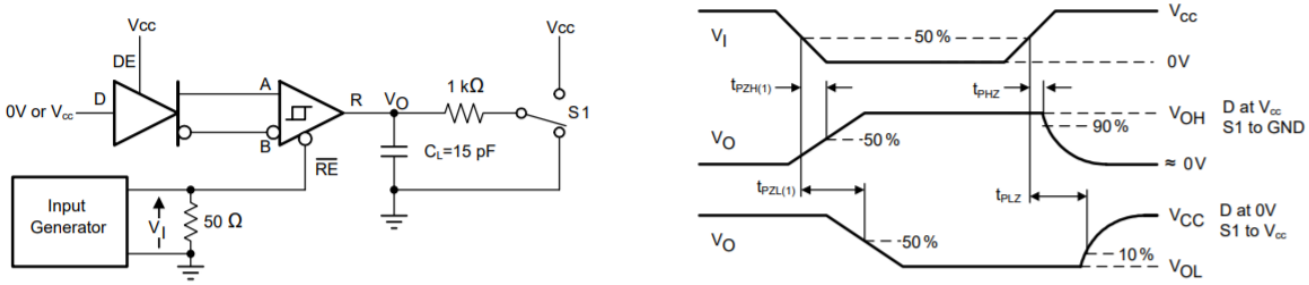
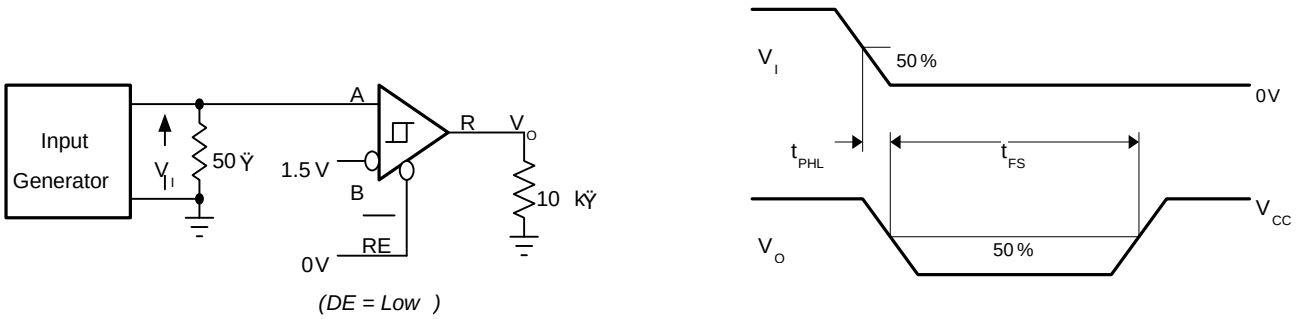


Figure 6. Receiver Enable and Disable Times



(DE = Low)

Figure 7. Measurement of Receiver Polarity-Correction Time With Driver Disabled

Theory of Operation

Overview

The TPT485N device is a half-duplex RS-485 transceiver suitable for data transmission at rates up to 500Kbps over controlled-impedance transmission cable. The TPT485N features a high level of internal transient protection, making it able to withstand ESD strikes up to ±12 kV (per IEC 61000-4-2) without incurring damage. TPT485N is 1/8 load and drive up to 256 units network through a common RS-485 bus. TPT485N supports automatic polarity correction, which detects bus mis-wiring and swaps A and B.

Bus Polarity Correction

TPT485N automatically corrects a wrong bus-signal polarity caused by a mis-wire fault. TPT485N will detect the bus polarity as the following conditions:

• A slave node must enable the receiver (RE = low). Driver can be in either enabled or disabled state

• A and B signals should be static for longer than fail-safe time (tFS)

• The absolute value of the differential voltage at the receiver input should be greater than the receiver thresholds (|V_{IT+}| or |V_{IT-}|)

The receiver input voltage can be defined either by using passive fail-safe resistors or by the master node actively driving the bus.

Application Information

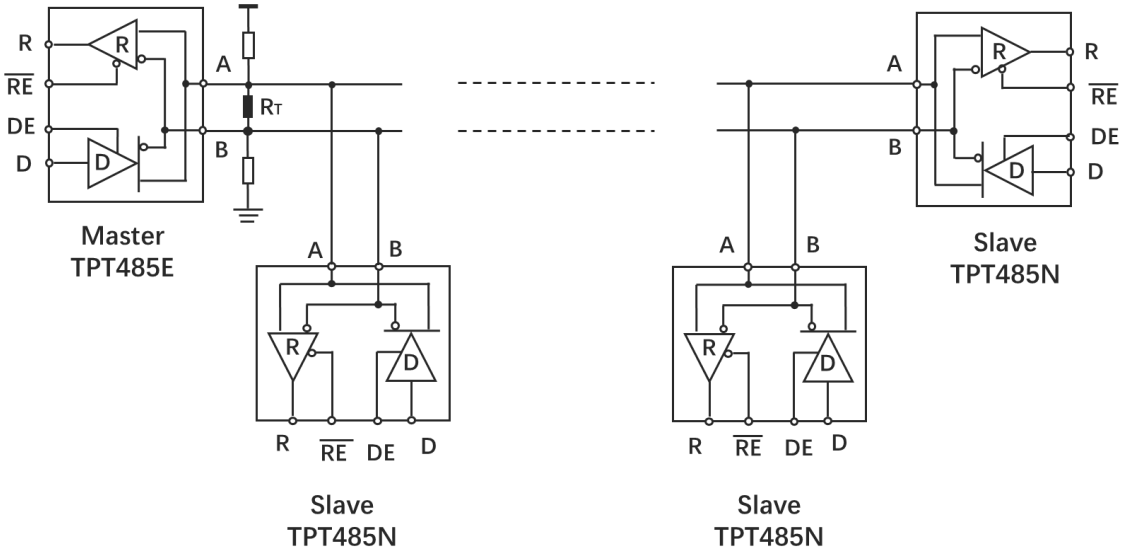
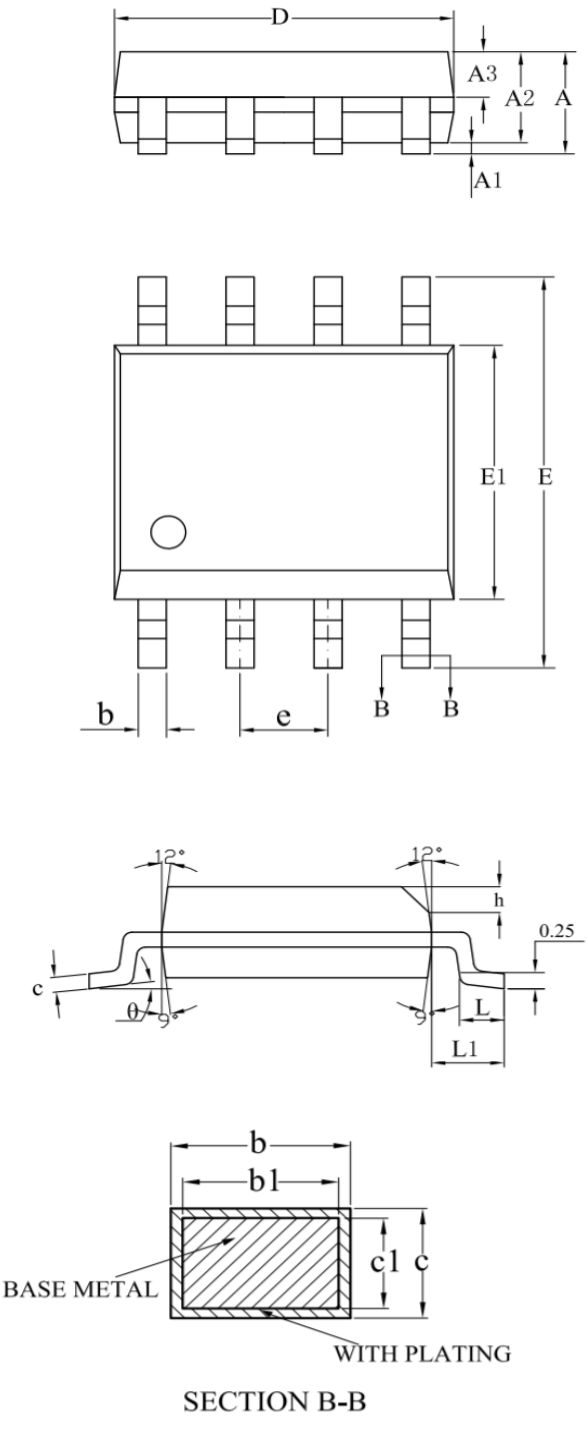


Figure 8. Typical Network Application With Polarity Correction

In the TPT485N application, there is pull up/down resistors master side in the network as the polarity reference, then there is no need pull up/down resistors for rest slave nodes.

Package Outline Dimensions

SO1R (SOP8)



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.10	—	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	—	0.47
b1	0.38	0.41	0.44
c	0.20	—	0.24
c1	0.19	0.20	0.21
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
h	0.25	—	0.50
L	0.50	—	0.80
L1	1.05REF		
θ	0	—	8°

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