EV2721-RH-00A

5A, 1-Cell, I²C-Controlled NVDC Buck Charger Evaluation Board

DESCRIPTION

The EV2721-RH-00A is an evaluation board designed to demonstrate the capabilities of the MP2721, a highly integrated, 5A, switch-mode battery management device for single-cell Li-ion or Li-polymer batteries. The narrow-voltage DC (NVDC) power management structure provides a low-impedance power path that optimizes charging efficiency, reduces battery charging time, and extends battery life during discharging.

USB Battery Charging Specification 1.2 (BC1.2) and non-standard adaptor detection are supported by the input source type identification algorithm.

The I²C interface provides complete operating control, charging parameter configuration, and status/interrupt monitoring.

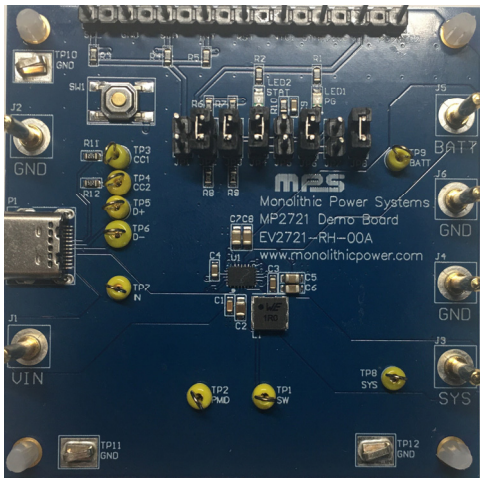
The MP2721 supports a fully customizable JEITA profile with configurable temperature windows and actions.

The EV2721-RH-00A supports input sources up to 16V, including standard USB host ports and high-voltage wall adapters with fast charge capability. The EV2721-RH-00A supports boost mode and On-The-Go (OTG) operation by supplying a voltage between 5V and 5.35V at the IN pin, with up to 3A of current.

PERFORMANCE SUMMARY

Parameters	Value
Input voltage (V_{IN}) supply	4V to 16V
Battery voltage (V_{BATT})	0V to 4.6V
Charge current (I_{CC})	0A to 5A
Input current (I_{IN})	0A to 3.2A
Boost output current (I_{BOOST_OUT})	0A to 3A

EVALUATION BOARD



LxWxH (6.3cmx6.3cmx1.3cm)

Board Number	MPS IC Number
EV2721-RH-00A	MP2721GRH

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QUICK START GUIDE

The EV2721-RH-00A evaluation board is designed for the MP2721. The layout of the EV2721-RH-00A accommodates most commonly used capacitors. The default function of this board is preset for charger mode, and the charge-full voltage is preset to 4.2V for a single-cell Li-ion battery.

Table 1 shows the input/output connections of the EV2721-RH-00A.

Table 1: Input/Output Connections

Connectors	Description
J1/VIN	Positive input source terminal
J2/GND	Negative input source terminal
J3/SYS	Positive system load terminal
J4/GND	Negative system load terminal
J5/BATT	Positive battery pack terminal
J6/GND	Negative battery pack terminal
P1	USB Type-C connector
SCL/SDA/GND	I²C connector

Table 2 shows the jumper set-ups for the EV2721-RH-00A.

Table 2: Jumper Installations

Jumper	Description	Default
JP1	I²C pull up to VCC	Off
JP2	NTC1 on board resistor divider	On
JP3	NTC2 on board resistor divider	On
JP4	LED indication for STAT/IB	On
JP5	IB resistor for STAT/IB. JP4 and JP5 should not be installed simultaneously	Off
JP6	LED indication for PG/NTC2	On
JP7	NTC2 connection to PG/NTC2. JP6 and JP7 should not be installed simultaneously	Off
JP8	BATTSNS connection to BATT	On

Evaluation Platform Preparation

1. The MP2721 evaluation software must be properly installed on the computer.
2. Prepare the USB-to-I²C communication interface (EVKT-USBI2C-02) (See Figure 1).



Figure 1: USB to I²C Communication Interface

3. Configure the test set-up for the MP2721 (see Figure 2 on page 3).

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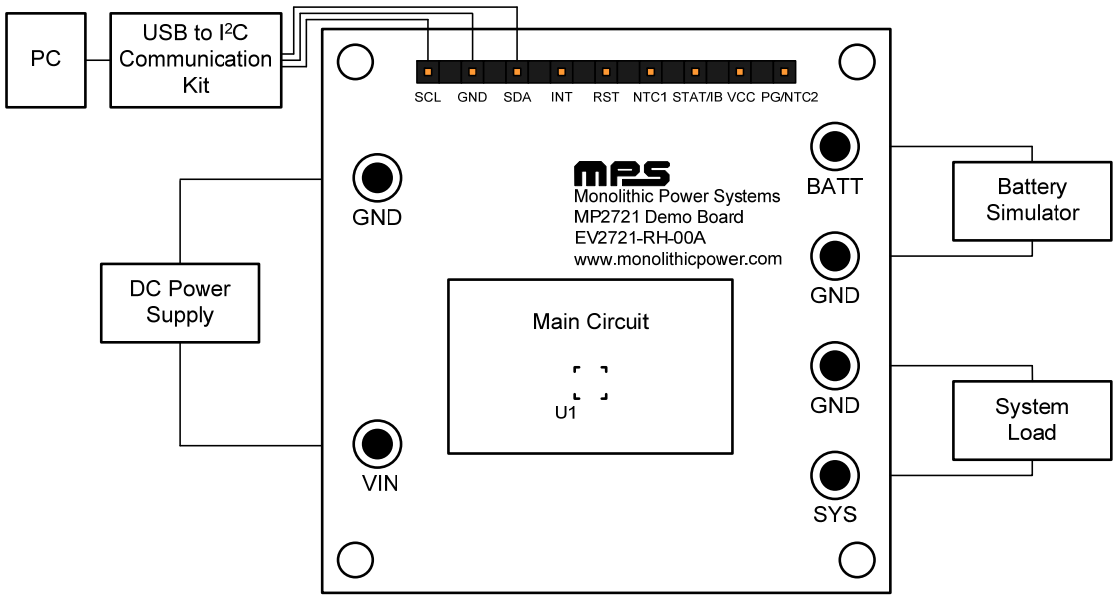


Figure 2: Measurement Equipment Set-Up

Start-Up Procedure

1. Set the battery simulator output to 3.8V with a charge/discharge current limit at 6A, then turn off the battery simulator. Connect the battery simulator to BATT and GND.
2. Set the DC power source output to 5V with an output current limit at 5A, then turn off the DC power source. Connect the DC power source to VIN and GND.
3. Connect the system load (typically an e-load device) to SYS and GND, then set the system load to 0A.
4. Turn on the battery simulator.
5. Turn on the DC power source.
6. If necessary, turn on the system load.
7. Launch the MP2721 evaluation software. Figure 3 shows the GUI software's main window.

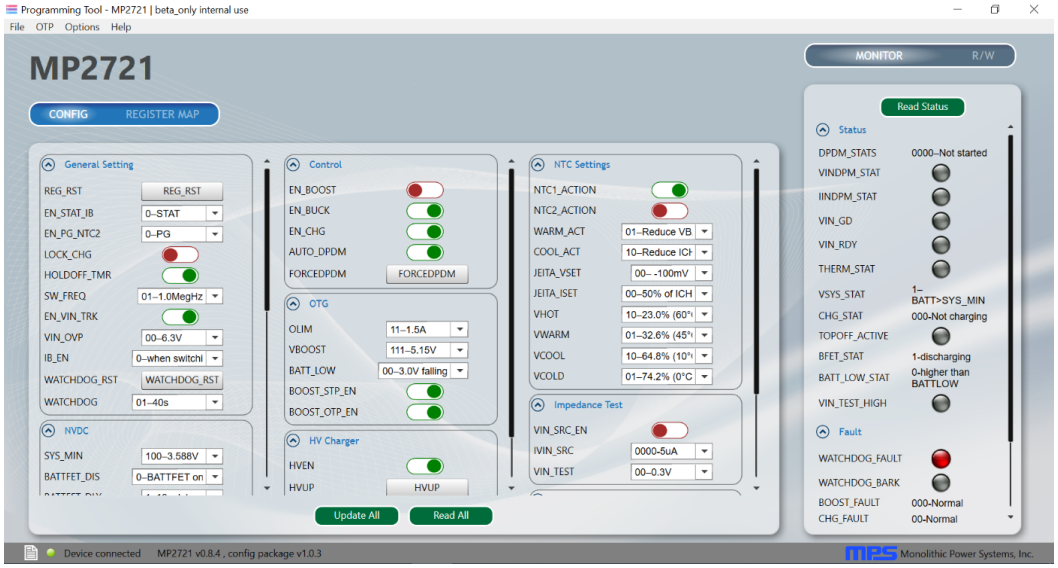


Figure 3: MP2721 Evaluation Software

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GUI Operating Instructions

1. Ensure that all the connections are successful, including the connection between the USB-to-I²C communication interface and the EV2721-RH-00A. Successful connections are indicated in green on the lower-left side of the GUI window (see Figure 3 on page 3). The program is ready to be run once all of the connections are successful.
2. After all connections are successful, click the “Read All” button to update the GUI to the default settings.
3. After modifying any settings with the GUI, click the “Update All” button to write the setting to the MP2721’s registers.

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EVALUATION BOARD SCHEMATIC

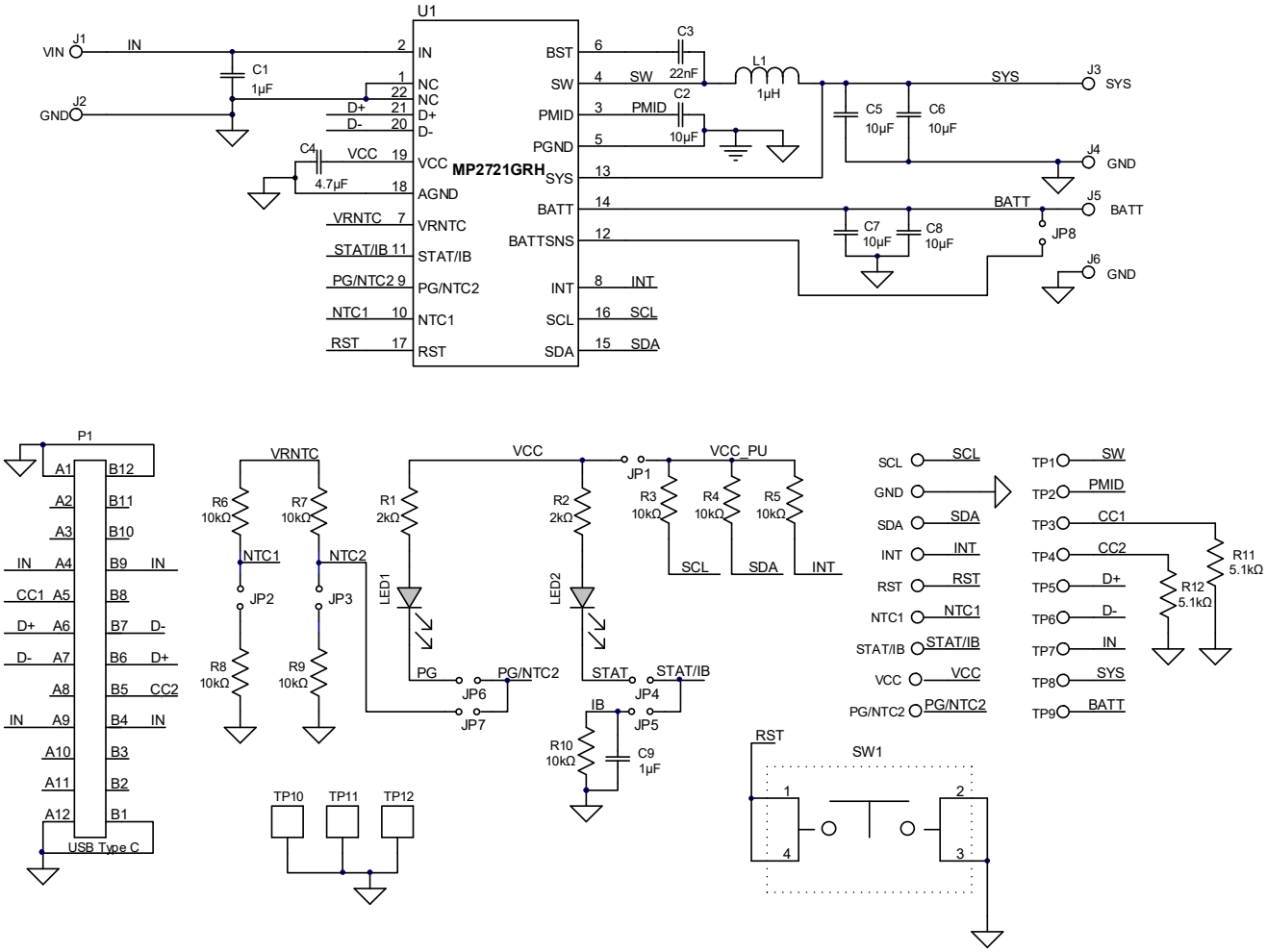


Figure 4: Evaluation Board Schematic

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EV2721-RH-00A BILL OF MATERIALS

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
1	C1	1µF	Ceramic capacitor, 25V, X7R	0603	Murata	GRM188R71E105KA12D
1	C2	10µF	Ceramic capacitor, 25V, X5R	0805	Murata	GRM21BR61E106KA73
1	C3	22nF	Ceramic capacitor, 100V, X7R	0603	Murata	GRM188R72A223KAC4D
1	C4	4.7µF	Ceramic capacitor, 16V, X7R	0603	Murata	GRM188R61C475KAAJD
4	C5, C6, C7, C8	10µF	Ceramic capacitor, 16V, X5R	0805	Murata	GRM21BR61C106KE15L
1	C9	1µF	Ceramic capacitor, 16V, X7R	0603	Murata	GRM188R71C105KA12D
1	L1	1µH	Inductor, R_{DC} = 12mΩ, I_{SAT} = 9A	SMD	Wurth	78438356010
2	R1, R2	2kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-072KL
3	R3, R4, R5	10kΩ	Film resistor, 5%	0603	Yageo	RC0603JR-0710K
5	R6, R7, R8, R9, R10	10kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-0710KL
2	R11, R12	5.1kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-075K1L
1	LED1	Red	Red LED	0805	Bright LED	F3D02R-4A
1	LED2	Green	Green LED	0805	Bright LED	F3D02HG-1A
1	SW1	4mmx 10mm	Push button	SMD	Any	
1	P1	5A	Type-C connector	SMD	Any	
6	J1, J2, J3, J4, J5, J6	2mm	Connector	DIP	Any	
9	TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9	Test point	Test point yellow	DIP	Any	
3	TP10, TP11, TP12	Test point	Test point ground	SMD	Any	
9	GND, INT, NTC1, PG/NTC2, RST, SCL, SDA, STAT/IB, VCC	2.54mm	Row connector	DIP	Any	
8	JP1, JP2, JP3, JP4, JP5, JP6, JP7, JP8	2.54mm	Row connector	DIP	Any	
5	JP2, JP3, JP4, JP6, JP8	2.54mm	Shunt	DIP	Any	
1	U1	MP2721	I²C-controlled, 1-cell, 5A, NVDC switching charger	QFN-22 (2.5mmx 3.5mm)	MPS	MP2721GRH

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PCB LAYOUT

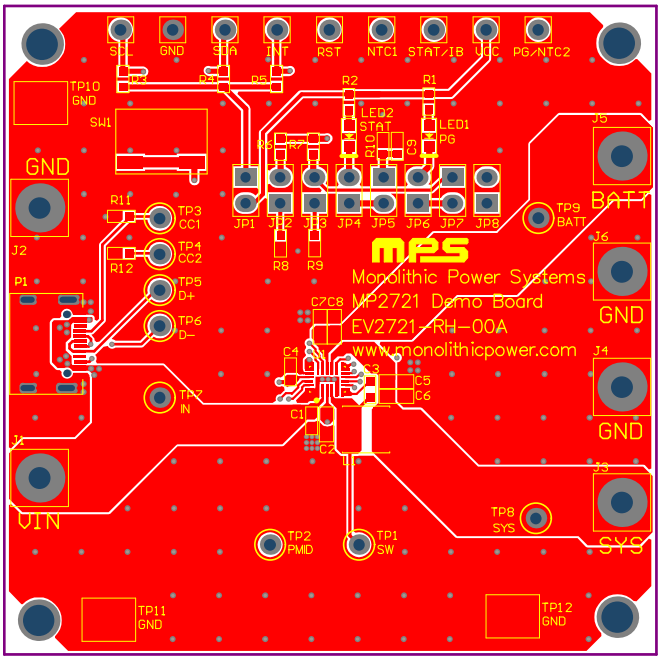


Figure 5: Top Layer

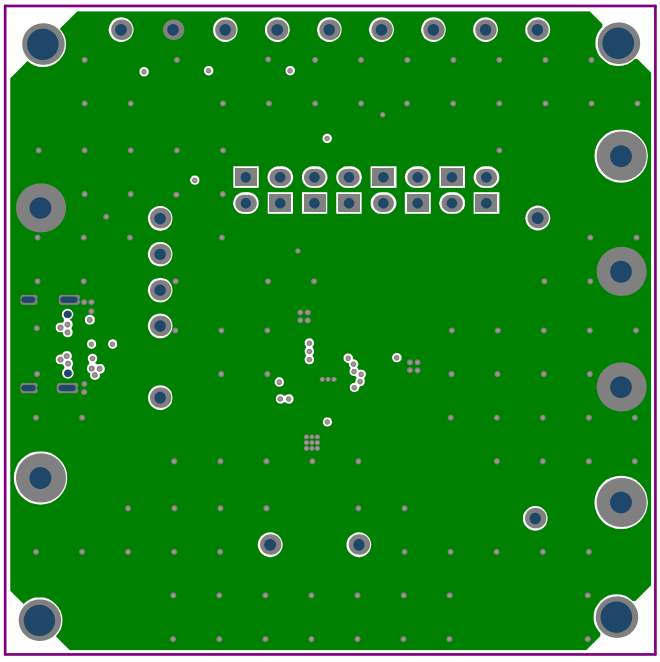


Figure 6: Middle Layer 1

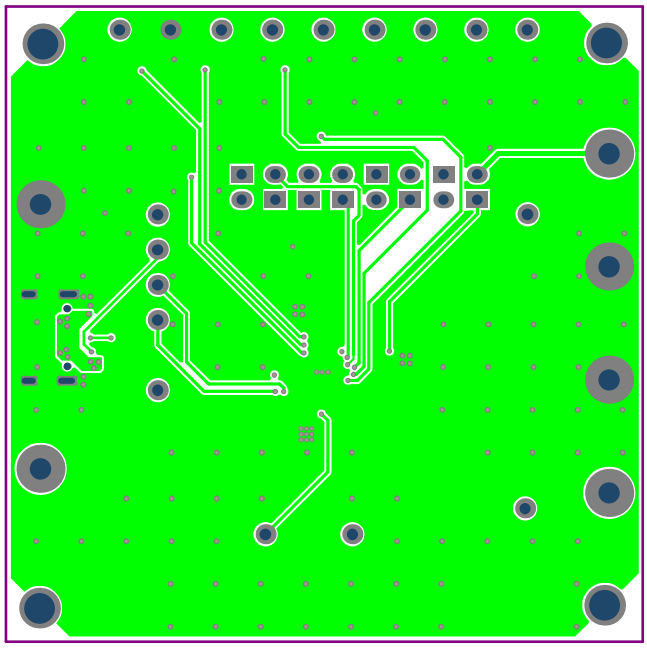


Figure 7: Middle Layer 2

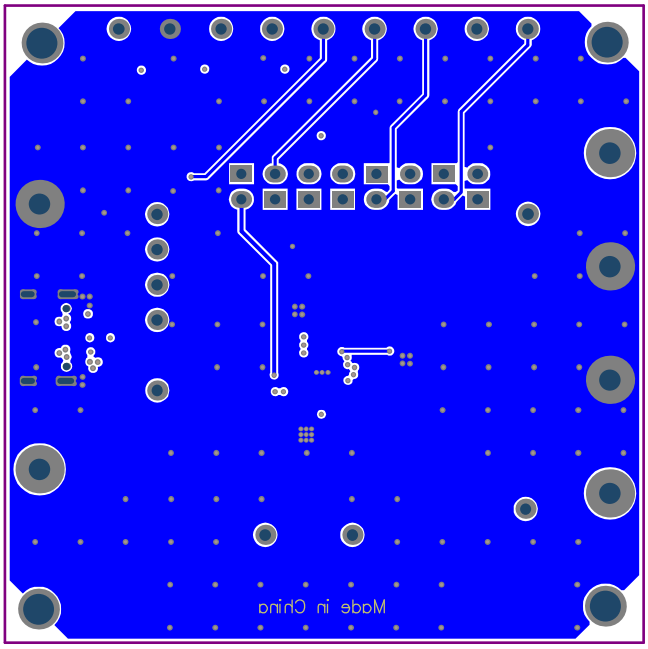


Figure 8: Bottom Layer

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	10/14/2021	Initial Release	-
1.1	2/2/2023	Changed BST capacitor (C3) to 22nF	5–6

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