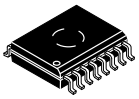
# 5 $kV_{RMS}$, 4.5-A/9-A Isolated Dual Channel Gate Driver

# NCP51563



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SOIC−16 WB LESS PINS 12 & 13
CASE 752AJ

The NCP51563 are isolated dual−channel gate drivers with 4.5−A/9−A source and sink peak current respectively. They are designed for fast switching to drive power MOSFETs, and SiC MOSFET power switches. The NCP51563 offers short and matched propagation delays.

Two independent and 5 $kV_{RMS}$ internal galvanic isolation from input to each output and internal functional isolation between the two output drivers allows a working voltage of up to 1850 $V_{DC}$. This driver can be used in any possible configurations of two low side, two high−side switches or a half−bridge driver with programmable dead time.

An ENA/DIS pin shutdowns both outputs simultaneously when set low or high for ENABLE or DISABLE mode respectively.

The NCP51563 offers other important protection functions such as independent under−voltage lockout for both gate drivers and a Dead Time adjustment function.

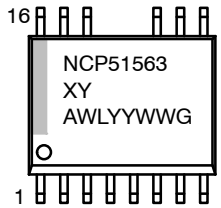
### Features

- Flexible: Dual Low−Side, Dual High−Side or Half−Bridge Gate Driver
- 4.5−A Peak Source, 9−A Peak Sink Output Current Capability
- Independent UVLO Protections for Both Output Drivers
- Output Supply Voltage from 6.5 V to 30 V with 5−V and 8−V for MOSFET, 13−V and 17−V UVLO for SiC, Thresholds
- Common Mode Transient Immunity CMTI > 200 V/ns
- Propagation Delay Typical 36 ns with
  - 5 ns Max Delay Matching per Channel
  - 5 ns Max Pulse−Width Distortion
- User Programmable Input Logic
  - Single or Dual−input Modes via ANB
  - ENABLE or DISABLE Mode
- User Programmable Dead−Time
- Isolation & Safety
  - 5 $kV_{RMS}$ Isolation for 1 Minute (per UL1577 Requirements)
  - 8000 $V_{PK}$ Reinforced Isolation Voltage (per VDE0884−11 Requirements)
  - CQC Certification per GB4943.1−2011
  - SGS FIMO Certification per IEC 62386−1
- These are Pb−Free Devices

### Typical Applications

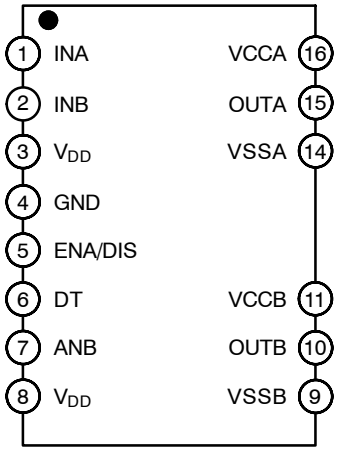
- Motor Drives
- Isolated Converters in DC−DC and AC−DC Power Supply
- Server, Telecom, and Industrial Infrastructures
- UPS and Solar Inverters

### MARKING DIAGRAM




| | |
|---|---|
| NCP51563 | = Specific Device Code |
| X | = A or B or C or D for UVLO Option |
| Y | = A or B for ENABLE/DISABLE |
| A | = Assembly Location |
| WL | = Wafer Lot |
| YY | = Year |
| WW | = Work Week |
| G | = Pb−Free Package |

### PIN CONNECTIONS




### ORDERING INFORMATION

See detailed ordering and shipping information on page 30 of this data sheet.

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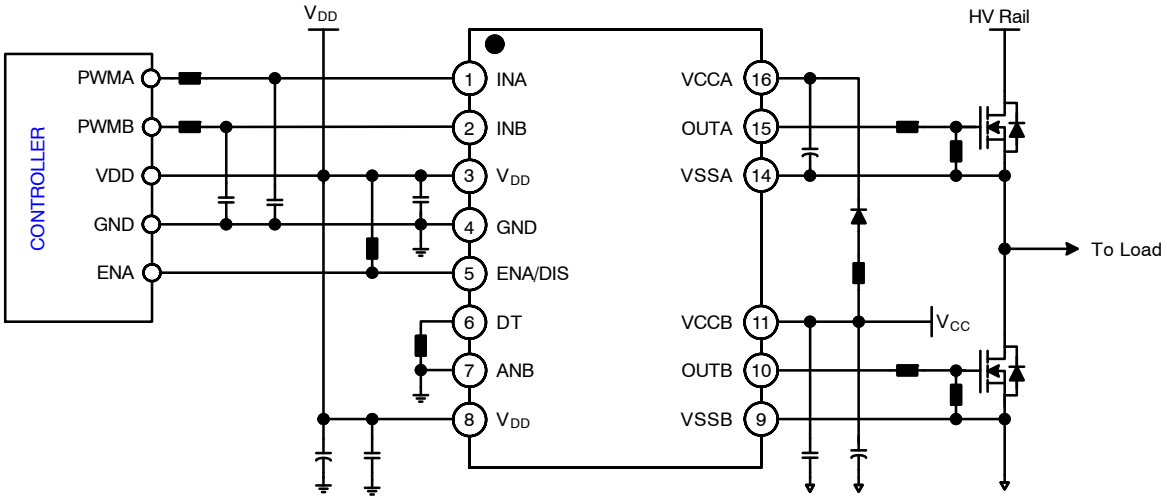
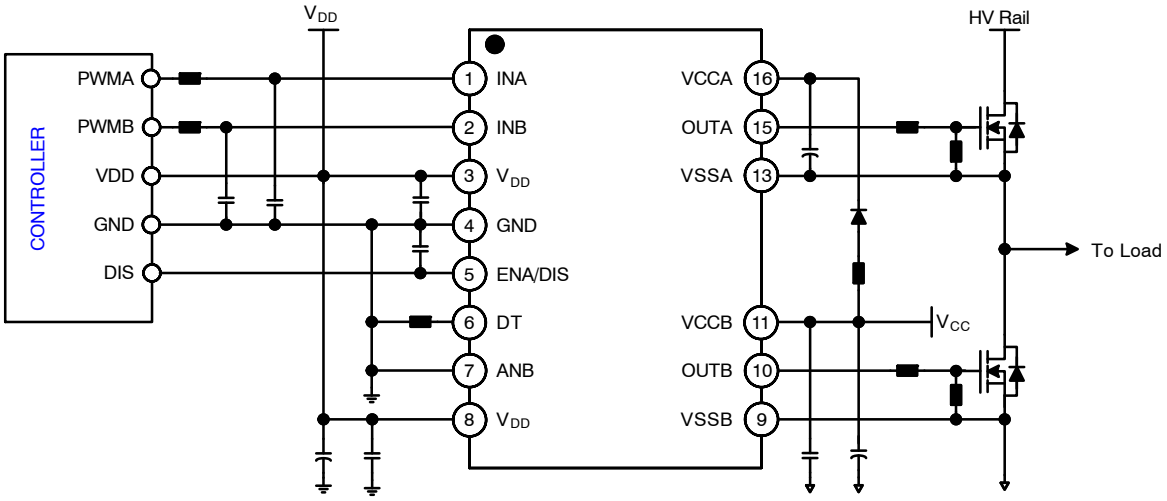
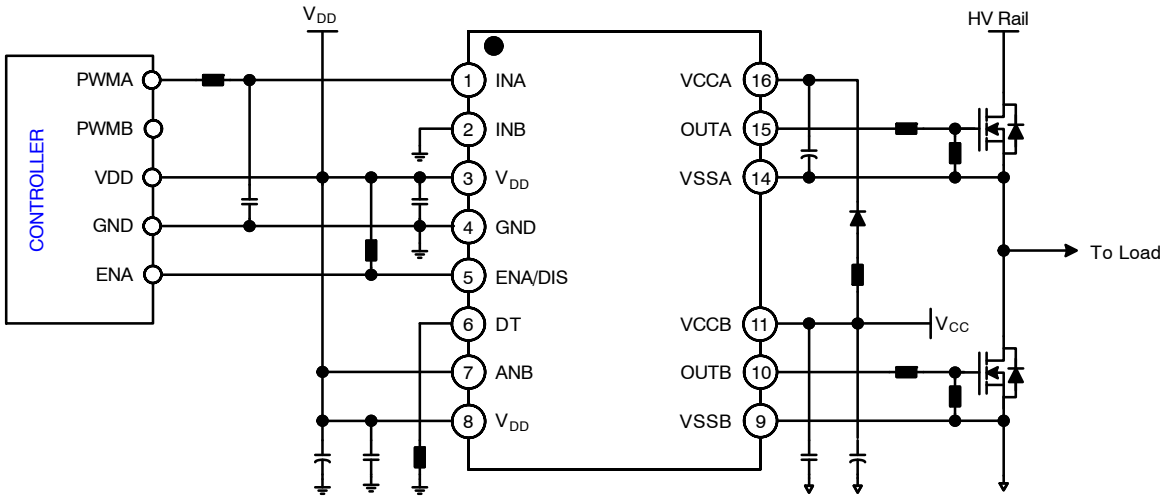
## TYPICAL APPLICATION CIRCUIT




(a) High and Low Side MOSFET Gate Drive for ENABLE Version




(b) High and Low Side MOSFET Gate Drive for DISABLE Version




(c) High and Low Side MOSFET Gate Drive with PWM Controller for ENABLE Version

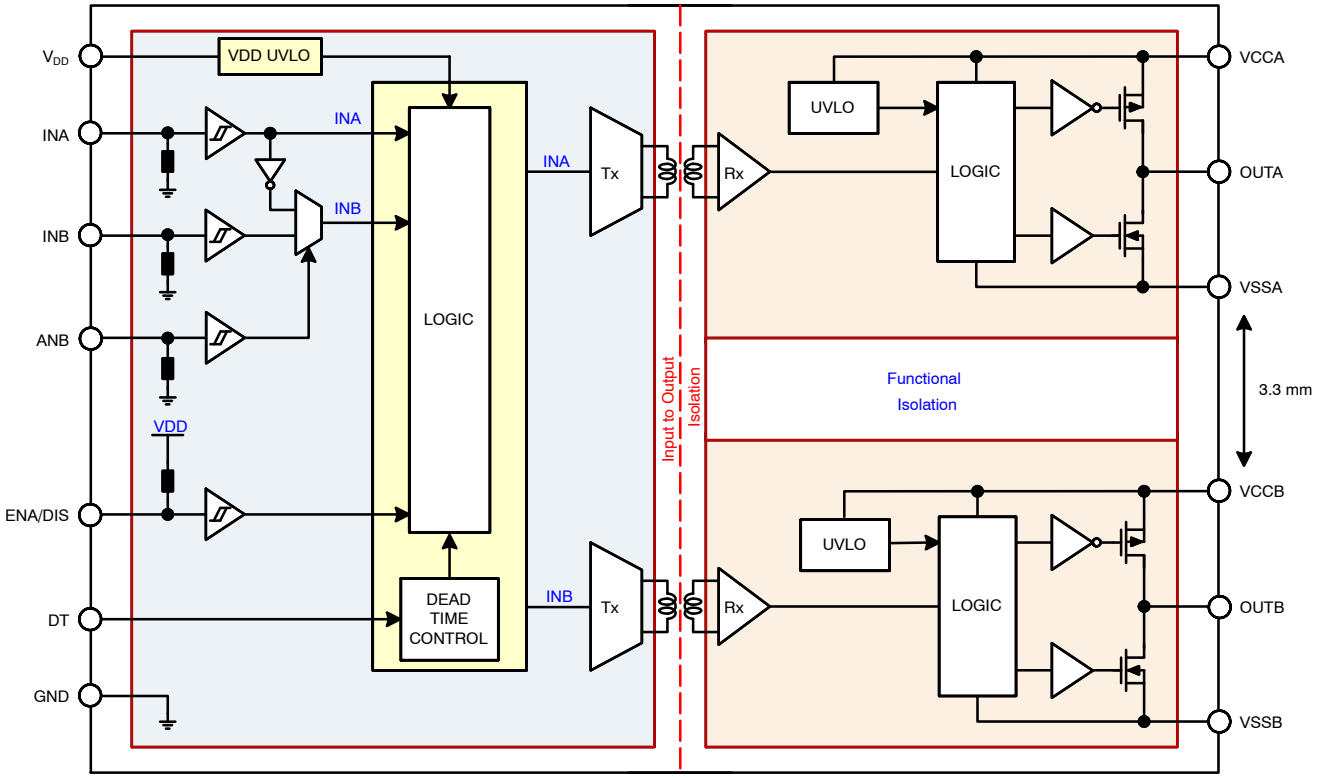
**Figure 1. Typical Application Schematic**

## FUNCTIONAL TABLE

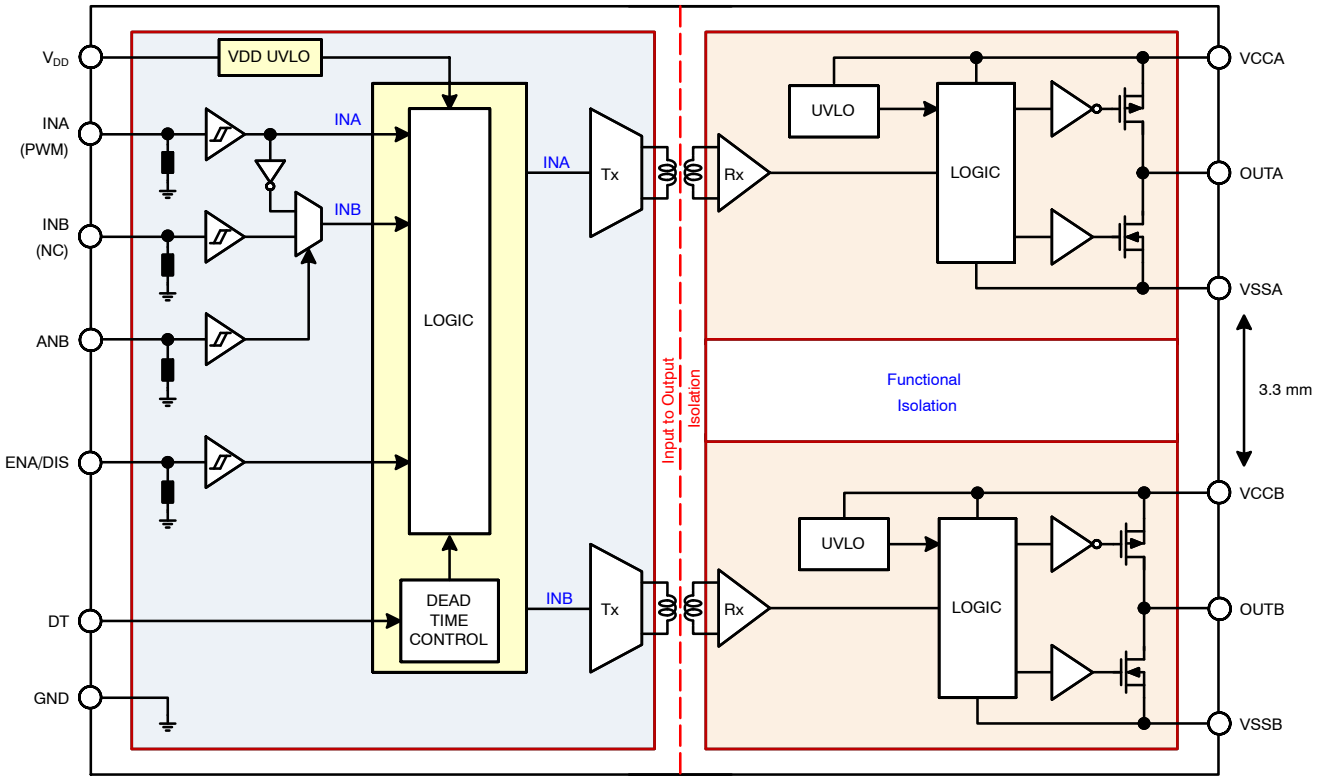
| INPUT | | | | | UVLO | | | GATE DRIVE OUTPUT | |
|---|---|---|---|---|---|---|---|---|---|
| ENA/DIS (Note 3) | | | | | | Output Side | | | |
| ENABLE | DISABLE | ANB | INA | INB | Input Side ($V_{DD}$) | Channel A ($V_{CCA}$) | Channel B ($V_{CCB}$) | OUTA | OUTB |
| X | X | X | X | X | Active | X | X | L | L |
| X | X | X | X | X | X | Active | Active | L | L |
| H | L | L | X | L | Inactive | Active | Inactive | L | L |
| H | L | L | X | H | Inactive | Active | Inactive | L | H |
| H | L | L | L | X | Inactive | Inactive | Active | L | L |
| H | L | L | H | X | Inactive | Inactive | Active | H | L |
| L | H | L | X | X | Inactive | Inactive | Inactive | L | L |
| H | L | L | L | L | Inactive | Inactive | Inactive | L | L |
| H | L | L | L | H | Inactive | Inactive | Inactive | L | H |
| H | L | L | H | H | Inactive | Inactive | Inactive | L (Note 5) | L (Note 5) |
| | | | | | Inactive | Inactive | Inactive | H (Note 6) | H (Note 6) |
| H | L | H | L | X | Inactive | Active | Inactive | L | H |
| H | L | H | H | X | Inactive | Active | Inactive | L | L |
| H | L | H | L | X | Inactive | Inactive | Active | L | L |
| H | L | H | H | X | Inactive | Inactive | Active | H | L |
| L | H | H | X | X | Inactive | Inactive | Inactive | L | L |
| H | L | H | L | X | Inactive | Inactive | Inactive | L | H |
| H | L | H | H | X | Inactive | Inactive | Inactive | H | L |

1. “L” means that LOW, “H” means that HIGH and X: Any Status
2. Inactive means that $V_{DD}$, $V_{CCA}$, and $V_{CCB}$ are above UVLO threshold voltage (Normal operation)
   Active means that UVLO disables the gate driver output stage.
3. Disables both gate drive output when the ENA/DIS pin is LOW in ENABLE version, which is default is HIGH, if this pin is open.
   Enables both gate drive output when the ENA/DIS pin is LOW in DISABLE version, which is default is LOW, if this pin is open.
4. When the ANB pin is HIGH, OUTA and OUTB are complementary outputs from PWM input signal on the INA pin regardless the INB signal.
5. DT pin is left open or programmed with $R_{DT}$.
6. DT pin pulled to $V_{DD}$.

## FUNCTIONAL BLOCK DIAGRAM




(a) For Only ENABLE (NCP51563xA) Version




(b) For Only DISABLE (NCP51563xB) Version

**Figure 2. Simplified Block Diagram**

## PIN CONNECTIONS

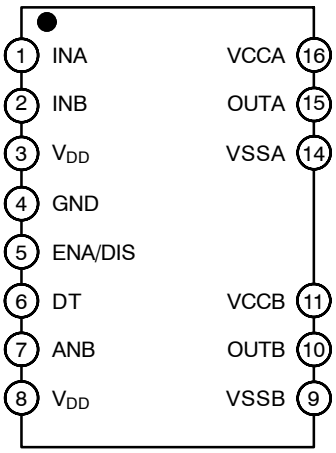



**Figure 3. Pin Connections – SOIC–16 WB (Top View)**

### PIN FUNCTION DESCRIPTION

| Pin No. | Pin Name | I/O | Description |
|---|---|---|---|
| 1 | INA | Input | Logic Input for Channel A with internal pull–down resistor to GND |
| 2 | INB | Input | Logic Input for Channel B with internal pull–down resistor to GND. |
| 3, 8 | $V_{DD}$ | Power | Input–side Supply Voltage.<br>It is recommended to place a bypass capacitor from $V_{DD}$ to GND. |
| 4 | GND | Power | Ground Input–side. (all signals on input–side are referenced to this pin) |
| 5 | ENA/DIS | Input | Logic Input High Enables Both Output Channels with Internal pull–up resistor for an ENABLE version. Conversely, Logic Input High disables Both Output Channels with Internal pull–down resistor for the DISABLE version. |
| 6 | DT | Input | Input for programmable Dead–Time<br>It provides three kind of operating modes according to the DT pin voltage as below.<br>*Mode–A*: Cross–conduction both channel outputs is not allowed even though dead–time is less than maximum 20 ns when the DT pin is floating.<br>*Mode–B*: Dead–time is adjusted according to an external resistance ($R_{DT}$).<br>$t_{DT}$ (in ns) = 10 x $R_{DT}$ (in kΩ)<br>Recommended dead–time resistor ($R_{DT}$) values are between 1 kΩ and 300 kΩ.<br>*MODE–C*: Cross–conduction both channel outputs is allowed when the DT pin pulled to $V_{DD}$. |
| 7 | ANB | Input | Logic Input to change the input signal configuration with internal pull*down resistor to GND. OUTA and OUTB work as complementary outputs from INA PWM input signal regardless of the INB signal when the ANB pin is high. It is recommended to tie this pin to GND or floating (not recommended) if the ANB pin is not used to achieve better noise immunity.<br>The ANB pin has a typical 3.3 μs internal filter to improve noise immunity but we recommend to tie to GND, if the ANB pin is not used. |
| 9 | VSSB | Power | Ground for Channel B |
| 10 | OUTB | Output | Output for Channel B |
| 11 | $V_{CCB}$ | Power | Supply Voltage for Output Channel B.<br>It is recommended to place a bypass capacitor from $V_{CCB}$ to VSSB. |
| 14 | VSSA | Power | Ground for Channel A |
| 15 | OUTA | Output | Output of Channel A |
| 16 | $V_{CCA}$ | Power | Supply Voltage for Output Channel A.<br>It is recommended to place a bypass capacitor from $V_{CCA}$ to VSSA. |

**SAFETY AND INSULATION RATINGS**

| Symbol | Parameter | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | Installation Classifications per DIN VDE 0110/1.89 Table 1 Rated Mains Voltage | <150 $V_{RMS}$ | – | I–IV | – | |
| | | <300 $V_{RMS}$ | – | I–IV | – | |
| | | <450 $V_{RMS}$ | – | I–IV | – | |
| | | <600 $V_{RMS}$ | – | I–IV | – | |
| | | <1000 $V_{RMS}$ | – | I–III | – | |
| CTI | Comparative Tracking Index (DIN IEC 112/VDE 0303 Part 1) | | 600 | – | – | |
| | Climatic Classification | | – | 40/125/21 | – | |
| | Pollution Degree (DIN VDE 0110/1.89) | | – | 2 | – | |
| $V_{PR}$ | Input−to−Output Test Voltage, Method b, $V_{IORM}$ x 1.875 = $V_{PR}$, 100% Production Test with $t_m$ = 1 s, Partial Discharge < 5 pC | | 2250 | – | – | $V_{PK}$ |
| $V_{IORM}$ | Maximum Repetitive Peak Isolation Voltage | | 1200 | – | – | $V_{PK}$ |
| $V_{IOWM}$ | Maximum Working Isolation Voltage | | 1200 | – | – | $V_{DC}$ |
| $V_{IOTM}$ | Maximum Transient Isolation Voltage | | 8000 | – | – | $V_{PK}$ |
| $E_{CR}$ | External Creepage | | 8.0 | – | – | mm |
| $E_{CL}$ | External Clearance | | 8.0 | – | – | mm |
| DTI | Insulation Thickness | | 17.3 | – | – | μm |
| $R_{IO}$ | Insulation Resistance at $T_S$, $V_{IO}$ = 500 V | | $10^9$ | – | – | Ω |

**UL1577**

| | | | | | | |
|---|---|---|---|---|---|---|
| VISO | Withstand Isolation Voltage | $V_{TEST}$ = $V_{ISO}$ = 5000 $V_{RMS}$, t = 60 s (Qualification), $V_{TEST}$ = 1.2 x $V_{ISO}$ = 6000 $V_{RMS}$, t = 1 s (100% Production) | 5000 | – | – | $V_{RMS}$ |

## SAFETY LIMITING VALUE

| Symbol | Parameter | | Side | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $P_S$ | Safety Supply Power | Maximum Values in Failure; Input Power | $P_{S,INPUT}$ | – | – | 88 | mW |
| | | Maximum Values in Failure; Output Power | $P_{S,OUT}$ | – | – | 1412 | |
| | | Maximum Values in Failure; Total Power | $P_{S,TOTAL}$ | – | – | 1500 | |
| $T_S$ | Safety Temperature | Maximum Values in Failure; Case Temperature | | – | – | 150 | °C |

## MAXIMUM RATINGS

| Symbol | | Parameter | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ to GND | | Power Supply Voltage – Input Side (Note 8) | −0.3 | 5.5 | V |
| $V_{CCA}$ – VSSA, $V_{CCB}$ – VSSB | | Power Supply Voltage – Driver Side (Note 9) | −0.3 | 33 | V |
| OUTA to VSSA, OUTB to VSSB | | Driver Output Voltage (Note 9) | −0.3 | $V_{CCA}$ + 0.3, $V_{CCB}$ + 0.3 | V |
| OUTA to VSSA, OUTB to VSSB, Transient for 200 ns (Note 10) | | | −2 | $V_{CCA}$ + 0.3, $V_{CCB}$ + 0.3 | V |
| INA, INB, and ANB | | Input Signal Voltages (Note 8) | −0.3 | 20 | V |
| INA, INB Transient for 50 ns (Note 10) | | | −5 | 20 | V |
| ENA/DIS | | Input Signal Voltages (Note 8) | −0.3 | 5.5 | V |
| ENA/DIS Transient for 50 ns (Note 10) | | | −5 | 5.5 | V |
| DT | | Dead Time Control (Note 8) | −0.3 | $V_{DD}$ + 0.3 | V |
| VSSA−VSSB, VSSB−VSSA | | Channel to Channel Voltage | 1850 | | V |
| $T_J$ | | Junction Temperature | −40 | +150 | °C |
| $T_S$ | | Storage Temperature | −65 | +150 | °C |
| Electrostatic Discharge Capability | HBM (Note 11) | Human Body Model | – | ±2 | kV |
| | CDM (Note 11) | Charged Device Model | – | ±1 | kV |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

7. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.
8. All voltage values are given with respect to GND pin.
9. All voltage values are given with respect to VSSA or VSSB pin.
10. This parameter verified by design and bench test, not tested in production.
11. This device series incorporates ESD protection and is tested by the following methods:
    ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
    ESD Charged Device Model tested per AEC−Q100−011 (EIA/JESD22−C101)
    Latch up Current Maximum Rating: ≤100 mA per JEDEC standard: JESD78F.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Rating | | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ | Power Supply Voltage – Input Side | | 3.0 | 5.0 | V |
| $V_{CCA}$, $V_{CCB}$ | Power Supply Voltage – Driver Side | 5–V UVLO Version | 6.5 | 30 | V |
| | | 8–V UVLO Version | 9.5 | 30 | V |
| | | 13–V UVLO Version | 14.5 | 30 | V |
| | | 17–V UVLO Version | 18.5 | 30 | V |
| $V_{IN}$ | Logic Input Voltage at Pins INA, INB, and ANB | | 0 | 18 | V |
| $V_{ENA/DIS}$ | Logic Input Voltage at Pin ENA/DIS | | 0 | 5.0 | V |
| $T_A$ | Ambient Temperature | | –40 | +125 | °C |
| $T_J$ | Junction Temperature | | –40 | +125 | °C |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

## THERMAL CHARACTERISTICS

| Symbol | Rating | Condition | Value | Unit |
|---|---|---|---|---|
| $R_{\theta JA}$ | *Thermal Characteristics*, (Note 13) Thermal Resistance Junction–Air 16–SOIC–WB | 100 $mm^2$, 1 oz Copper, 1 Surface Layer (1S0P) | 120 | °C/W |
| | | 100 $mm^2$, 2 oz Copper, 1 Surface Layer (1S0P) | 81 | |
| $R_{qJC}$ | Thermal Resistance Junction–case | 100 $mm^2$, 1 oz Copper, 1 Surface Layer (1S0P) | 38 | °C/W |
| $\psi_{JT}$ | Thermal Resistance Junction–to–top | | 18 | °C/W |
| $\psi_{JB}$ | Thermal Resistance Junction–to–board | | 55 | °C/W |
| $P_D$ | *Power Dissipation* (Note 13) 16–SOIC–WB | 100 $mm^2$, 1 oz Copper, 1 Surface Layer (1S0P) | 0.8 | W |
| | | 100 $mm^2$, 2 oz Copper, 1 Surface Layer (1S0P) | 1.5 | |

12. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.
13. JEDEC standard: JESD51–2, and JESD51–3.

## ISOLATION CHARACTERISTICS

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{ISO,INPUT\ TO\ OUTPUT}$ | Input to Output Isolation Voltage | $T_A$ = 25°C, Relative Humidity < 50%, t = 1.0 minute, $I_{I-O}$ 10 A, 50 Hz (Note 14, 15, 16) | 5000 | – | – | $V_{RMS}$ |
| $V_{ISO,OUTA\ TO\ OUTB}$ | OUTA to OUTB Isolation Voltage | Impulse Test > 10 ms (Note 14, 15) | 1850 | – | – | $V_{DC}$ |
| $R_{ISO}$ | Isolation Resistance | $V_{I_O}$ = 500 V (Note 14) | $10^{11}$ | – | – | Ω |

14. Device is considered a two–terminal device: pins 1 to 8 are shorted together and pins 9 to 16 are shorted together for input to output isolation test, and pins 9 to 11 are shorted together and pins 14 to 16 are shorted together for between channel isolation test.
15. 5,000 $V_{RMS}$ for 1–minute duration is equivalent to 6,000 $V_{RMS}$ for 1–second duration for input to output isolation test, and Impulse Test > 10 ms; sample tested for between channel isolation test.
16. The input–output isolation voltage is a dielectric voltage rating per UL1577. It should not be regarded as an input–output continuous voltage rating. For the continuous working voltage rating, refer to equipment–level safety specification or DIN VDE V 0884–11 Safety and Insulation Ratings Table.

**ELECTRICAL CHARACTERISTICS** ($V_{DD}$ = 5 V, $V_{CCA}$ = $V_{CCB}$ = 12 V, or 20 V (Note 18) and VSSA = VSSB, for typical values $T_J$ = $T_A$ = 25°C, for min/max values $T_J$ = −40°C to +125°C, unless otherwise specified. (Note 17))

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **PRIMARY POWER SUPPLY SECTION ($V_{DD}$)** | | | | | | |
| $I_{QVDD}$ | $V_{DD}$ Quiescent Current | $V_{INA}$ = $V_{INB}$ = 0 V, $V_{ENABLE}$ = $V_{DD}$ or V $V_{DISABLE}$ = 0 V | 500 | 780 | 1000 | μA |
| | | $V_{INA}$ = $V_{INB}$ = 5 V, $V_{ENABLE}$ = 0 V or $V_{DISABLE}$ = $V_{DD}$ | 500 | 820 | 1000 | μA |
| | | $V_{INA}$ = $V_{INB}$ = 5 V, $V_{ENABLE}$ = $V_{DD}$ or $V_{DISABLE}$ = 0 V | 7 | 12 | 16 | mA |
| $I_{VDD}$ | $V_{DD}$ Operating Current | $f_{IN}$ = 500 kHz, 50% duty cycle, $C_{OUT}$ = 100 pF | 5.0 | 7.15 | 9.0 | mA |
| $V_{DDUV+}$ | $V_{DD}$ Supply Under−Voltage Positive−Going Threshold | $V_{DD}$ = Sweep | 2.7 | 2.8 | 2.9 | V |
| $V_{DDUV-}$ | $V_{DD}$ Supply Under−Voltage Negative−Going Threshold | $V_{DD}$ = Sweep | 2.6 | 2.7 | 2.8 | V |
| $V_{DDHYS}$ | $V_{DD}$ Supply Under−Voltage Lockout Hysteresis | $V_{DD}$ = Sweep | – | 0.1 | – | V |
| **SECONDARY POWER SUPPLY SECTION ($V_{CCA}$ AND $V_{CCB}$)** | | | | | | |
| $I_{QVCCA}$ $I_{QVCCB}$ | $V_{CCA}$ and $V_{CCB}$ Quiescent Current | $V_{INA}$ = $V_{INB}$ = 0 V, per channel | 200 | 280 | 500 | μA |
| | | $V_{INA}$ = $V_{INB}$ = 5 V, per channel | 300 | 410 | 600 | μA |
| $I_{VCCA}$ $I_{VCCB}$ | $V_{CCA}$ and $V_{CCB}$ Operating Current | Current per channel ($f_{IN}$ = 500 kHz, 50% duty cycle), $C_{OUT}$ = 100 pF | 2.0 | 3.0 | 5.5 | mA |
| **VCCA AND VCCB UVLO THRESHOLD (5−V UVLO VERSION)** | | | | | | |
| $V_{CCAUV+}$ $V_{CCBUV+}$ | $V_{CCA}$ and $V_{CCB}$ Supply Under−Voltage Positive−Going Threshold | | 5.7 | 6.0 | 6.3 | V |
| $V_{CCAUV-}$ $V_{CCBUV-}$ | $V_{CCA}$ and $V_{CCB}$ Supply Under−Voltage Negative−Going Threshold | | 5.4 | 5.7 | 6.0 | V |
| $V_{CCHYS}$ | Under−Voltage Lockout Hysteresis | | – | 0.3 | – | V |
| $t_{UVFLT}$ | Under−Voltage Debounce Time (Note 18) | | – | – | 10 | μs |
| **VCCA AND VCCB UVLO THRESHOLD (8−V UVLO VERSION)** | | | | | | |
| $V_{CCAUV+}$ $V_{CCBUV+}$ | $V_{CCA}$ and $V_{CCB}$ Supply Under−Voltage Positive−Going Threshold | | 8.3 | 8.7 | 9.2 | V |
| $V_{CCAUV-}$ $V_{CCBUV-}$ | $V_{CCA}$ and $V_{CCB}$ Supply Under−Voltage Negative−Going Threshold | | 7.8 | 8.2 | 8.7 | V |
| $V_{CCHYS}$ | Under−Voltage Lockout Hysteresis | | – | 0.5 | – | V |
| $t_{UVFLT}$ | Under−Voltage Debounce Time (Note 18) | | – | – | 10 | μs |
| **VCCA AND VCCB UVLO THRESHOLD (13−V UVLO VERSION)** | | | | | | |
| $V_{CCAUV+}$ $V_{CCBUV+}$ | $V_{CCA}$ and $V_{CCB}$ Supply Under−Voltage Positive−Going Threshold | | 12 | 13 | 14 | V |
| $V_{CCAUV-}$ $V_{CCBUV-}$ | $V_{CCA}$ and $V_{CCB}$ Supply Under−Voltage Negative−Going Threshold | | 11 | 12 | 13 | V |
| $V_{CCHYS}$ | Under−Voltage Lockout Hysteresis | | – | 1 | – | V |
| $t_{UVFLT}$ | Under−Voltage Debounce Time (Note 18) | | – | – | 10 | μs |

**ELECTRICAL CHARACTERISTICS** ($V_{DD}$ = 5 V, $V_{CCA}$ = $V_{CCB}$ = 12 V, or 20 V (Note 18) and VSSA = VSSB, for typical values $T_J$ = $T_A$ = 25°C, for min/max values $T_J$ = −40°C to +125°C, unless otherwise specified. (Note 17)) (continued)

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **VCCA AND VCCB UVLO THRESHOLD (17−V UVLO VERSION)** | | | | | | |
| $V_{CCAUV+}$ $V_{CCBUV+}$ | $V_{CCA}$ and $V_{CCB}$ Supply Under−Voltage Positive−Going Threshold | | 16 | 17 | 18 | V |
| $V_{CCAUV-}$ $V_{CCBUV-}$ | $V_{CCA}$ and $V_{CCB}$ Supply Under−Voltage Negative−Going Threshold | | 15 | 16 | 17 | V |
| $V_{CCHYS}$ | Under−Voltage Lockout Hysteresis | | – | 1 | – | V |
| $t_{UVFLT}$ | Under−Voltage Debounce Time (Note 18) | | – | – | 10 | μs |
| **LOGIC INPUT SECTION (INA, INB, AND ANB)** | | | | | | |
| $V_{INH}$ | High Level Input Voltage | | 1.4 | 1.6 | 1.8 | V |
| $V_{INL}$ | Low Level Input Voltage | | 0.9 | 1.1 | 1.3 | V |
| $V_{INHYS}$ | Input Logic Hysteresis | | – | 0.5 | – | V |
| $I_{IN+}$ | High Level Logic Input Bias Current | $V_{IN}$ = 5 V | 20 | 25 | 33 | μA |
| $I_{IN-}$ | Low Level Logic Input Bias Current | $V_{IN}$ = 0 V | – | – | 1.0 | μA |
| **LOGIC INPUT SECTION (FOR ONLY ENABLE VERSION)** | | | | | | |
| $V_{ENAH}$ | Enable High Voltage | | 1.4 | 1.6 | 1.8 | V |
| $V_{ENAL}$ | Enable Low Voltage | | 0.9 | 1.1 | 1.3 | V |
| $V_{ENAHYS}$ | Enable Logic Hysteresis | | – | 0.5 | – | V |
| **LOGIC INPUT SECTION (FOR ONLY DISABLE VERSION)** | | | | | | |
| $V_{DISH}$ | Disable High Voltage | | 1.4 | 1.6 | 1.8 | V |
| $V_{DISL}$ | Disable Low Voltage | | 0.9 | 1.1 | 1.3 | V |
| $V_{DISHYS}$ | Disable Logic Hysteresis | | – | 0.5 | – | V |
| **DEAD−TIME AND OVERLAP SECTION** | | | | | | |
| $t_{DT,MIN}$ | Minimum Dead−Time | DT pin is left open | 0 | 10 | 29 | ns |
| $t_{DT}$ | Dead−Time | $R_{DT}$ = 20 kΩ | 145 | 200 | 245 | ns |
| | | $R_{DT}$ = 100 kΩ | 800 | 1000 | 1200 | ns |
| $\Delta t_{DT}$ | Dead−Time Mismatch between OUTB → OUTA and OUTA → OUTB | $R_{DT}$ = 20 kΩ | −30 | – | 30 | ns |
| | | $R_{DT}$ = 100 kΩ | −150 | – | 150 | ns |
| $V_{DT,SHORT}$ | DT Threshold Voltage for OUTA & OUTB Overlap | | 0.85 x $V_{DD}$ | 0.9 x $V_{DD}$ | 0.95 x $V_{DD}$ | V |
| **GATE DRIVE SECTION** | | | | | | |
| $I_{OUTA+}$, $I_{OUTB+}$ | OUTA and OUTB Source Peak Current (Note 18) | $V_{INA}$ = $V_{INB}$ = 5 V, PW ≤ 5 μs $V_{CCA}$ = $V_{CCB}$ = 12 V | 2.6 | 4.5 | – | A |
| $I_{OUTA-}$, $I_{OUTB-}$ | OUTA and OUTB Sink Peak Current (Note 18) | $V_{INA}$ = $V_{INB}$ = 0 V, PW 3 5 μs $V_{CCA}$ = $V_{CCB}$ = 12 V | 7.0 | 9.0 | – | A |
| $R_{OH}$ | Output Resistance at High State | $I_{OUTH}$ = 100 mA | – | 1.4 | 2.7 | Ω |
| $R_{OL}$ | Output Resistance at Low State | $I_{OUTL}$ = 100 mA | – | 0.5 | 1.0 | Ω |
| $V_{OHA}$, $V_{OHB}$ | High Level Output Voltage ($V_{CCX}$ − $V_{OUTX}$) | $I_{OUT}$ = 100 mA | – | – | 270 | mV |
| $V_{OLA}$, $V_{OLB}$ | Low Level Output Voltage ($V_{OUTX}$ − $V_{SSX}$) | $I_{OUT}$ = 100 mA | – | – | 100 | mV |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

17. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at $T_J$ = $T_A$ = 25°C.
18. $V_{CCA}$ = $V_{CCB}$ = 12 V is used for the test condition of 5−V and 8−V UVLO, $V_{CCA}$ = $V_{CCB}$ = 20 V is used for 13−V and 17−V UVLO.
19. These parameters are verified by bench test only and not tested in production.

**DYNAMIC ELECTRICAL CHARACTERISTICS** ($V_{DD}$ = 5 V, $V_{CCA}$ = $V_{CCB}$ = 12 V, or 20 V (Note 21) and VSSA = VSSB, for typical values $T_J$ = $T_A$ = 25°C, for min/max values $T_J$ = −40°C to +125°C, unless otherwise specified. (Note 20))

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{PDON}$ | Turn−On Propagation Delay from INx to OUTx | $V_{CCA}$ = $V_{CCB}$ = 12 V, $C_{LOAD}$ = 0 nF | 22 | 36 | 55 | ns |
| | | $V_{CCA}$ = $V_{CCB}$ = 20 V, $C_{LOAD}$ = 0 nF | 25 | 39 | 58 | ns |
| $t_{PDOFF}$ | Turn−Off Propagation Delay from INx to OUTx | $V_{CCA}$ = $V_{CCB}$ = 12 V, $C_{LOAD}$ = 0 nF | 22 | 36 | 55 | ns |
| | | $V_{CCA}$ = $V_{CCB}$ = 20 V, $C_{LOAD}$ = 0 nF | 25 | 39 | 58 | ns |
| $t_{PWD}$ | Pulse Width Distortion ($t_{PDON}$ − $t_{PDOFF}$) | | −5 | – | 5 | ns |
| $t_{DM}$ | Propagation Delay Mismatching between Channels | $f_{IN}$ = 100 kHz | −5 | – | 5 | ns |
| $t_R$ | Turn−On Rise Time | $V_{CCA}$ = $V_{CCB}$ = 12 V, $C_{LOAD}$ = 1.8 nF | – | 9 | 16 | ns |
| | | $V_{CCA}$ = $V_{CCB}$ = 20 V, $C_{LOAD}$ = 1.8 nF | – | 11 | 19 | ns |
| $t_F$ | Turn−Off Fall Time | $V_{CCA}$ = $V_{CCB}$ = 12 V, $C_{LOAD}$ = 1.8 nF | – | 8 | 16 | ns |
| | | $V_{CCA}$ = $V_{CCB}$ = 20 V, $C_{LOAD}$ = 1.8 nF | – | 10 | 19 | ns |
| $T_{ENABLE,OUT}$, $T_{DISABLE,OUT}$ | ENABLE or DISABLE to OUTx Turn−On/Off Propagation Delay | $V_{CCA}$ = $V_{CCB}$ = 12 V | 22 | 36 | 55 | ns |
| | | $V_{CCA}$ = $V_{CCB}$ = 20 V | 25 | 39 | 58 | ns |
| $t_{PW}$ | Minimum Input Pulse Width that Change Output State | $C_{LOAD}$ = 0 nF | – | 15 | 30 | ns |
| $T_{FLT,ANB}$ | Glitch Filter on the ANB Pin | | 2.0 | 3.3 | 4.5 | μs |
| CMTI | Common Mode Transient Immunity (Note 22) | Slew rate of GND versus VSSA and VSSB. INA and INB both are tied to $V_{DD}$ or GND. $V_{CM}$ = 1500 V | 200 | – | – | V/ns |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

20. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at $T_J$ = $T_A$ = 25°C.
21. $V_{CCA}$ = $V_{CCB}$ = 12 V is used for the test condition of 5−V and 8−V UVLO, $V_{CCA}$ = $V_{CCB}$ = 20 V is used for 13−V and 17−V UVLO.
22. These parameters are verified by bench test only and not tested in production.

## INSULATION CHARACTERISTICS CURVES

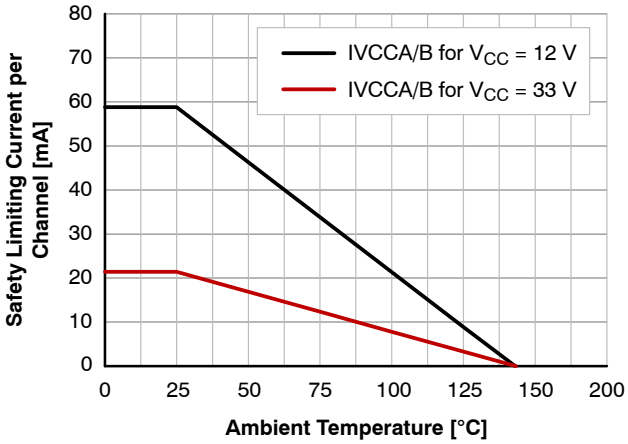



**Figure 4. Thermal Derating Curve for Safety−Related Limiting Current (Current in Each Channel with Both Channels Running Simultaneously)**

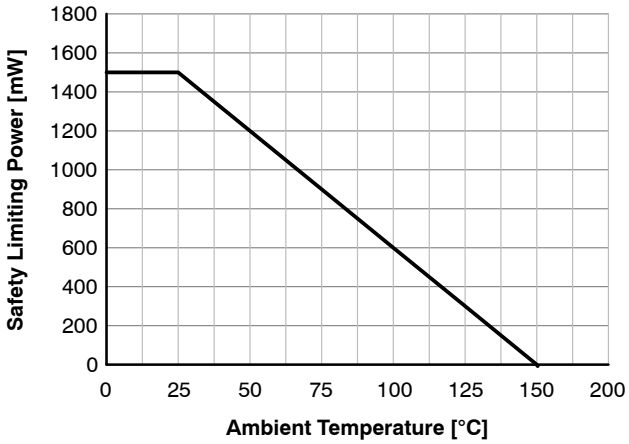



**Figure 5. Thermal Derating Curve for Safety−Related Limiting Power**

## TYPICAL CHARACTERISTICS

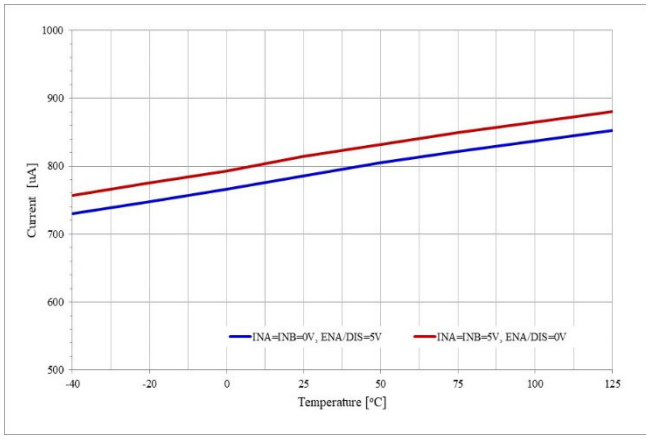



**Figure 6. Quiescent $V_{DD}$ Supply Current vs. Temperature ($V_{DD}$ = 5 V, INA = INB = 0 V, ENA/DIS = 5 V or , INA = INB = 5 V, ENA/DIS = 0 V and No Load)**

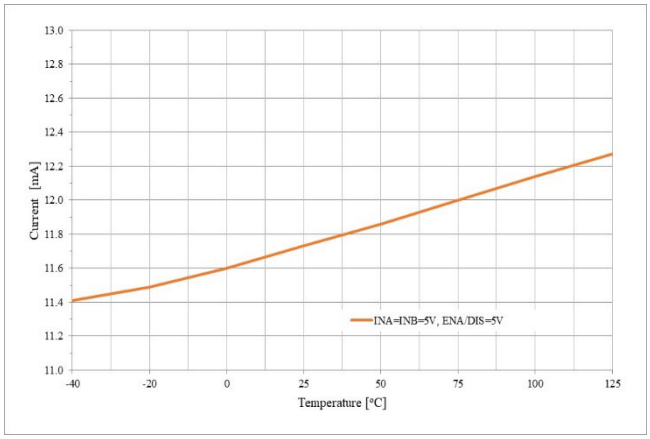



**Figure 7. Quiescent $V_{DD}$ Supply Current vs. Temperature ($V_{DD}$ = 5 V, INA = INB = ENA/DIS = 5 V and No Load)**

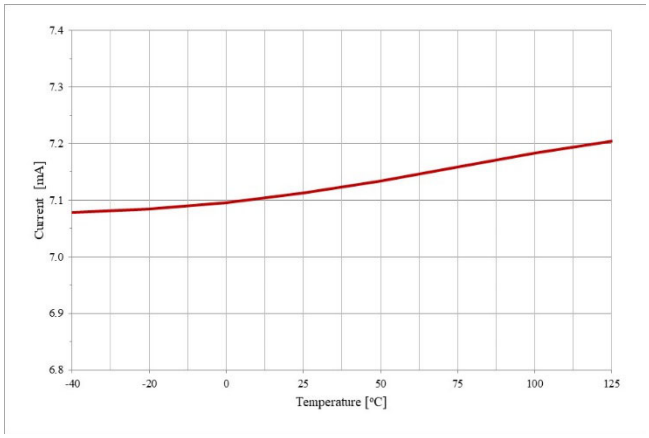



**Figure 8. $V_{DD}$ Operating Current vs. Temperature ($V_{DD}$ = 5 V, No Load, and Switching Frequency = 500 kHz)**

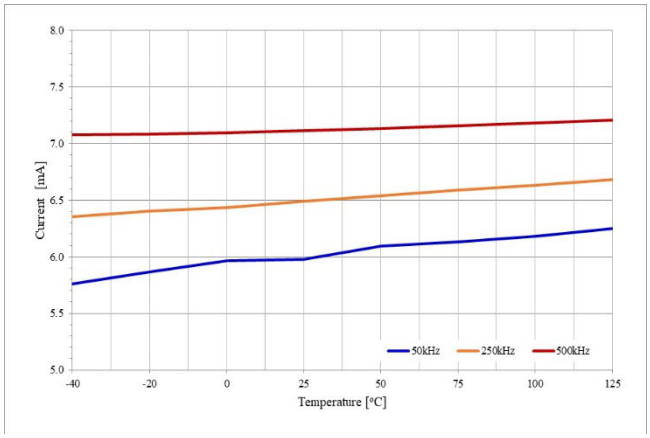



**Figure 9. $V_{DD}$ Operating Current vs. Temperature ($V_{DD}$ = 5 V, No Load, and Different Switching Frequency)**

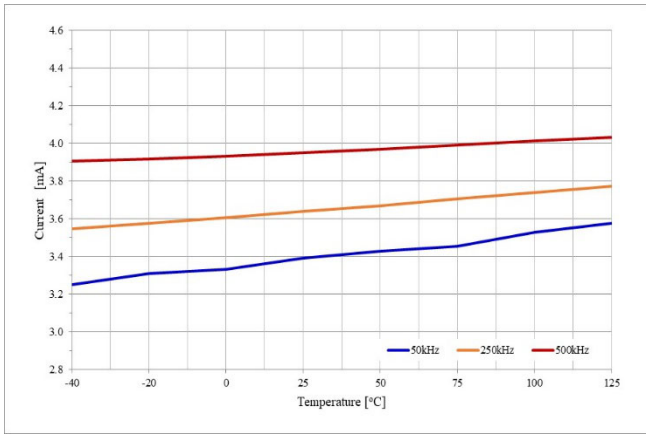



**Figure 10. Per Channel $V_{DD}$ Operating Current vs. Temperature ($V_{DD}$ = 5 V, No Load, and Different Switching Frequency**

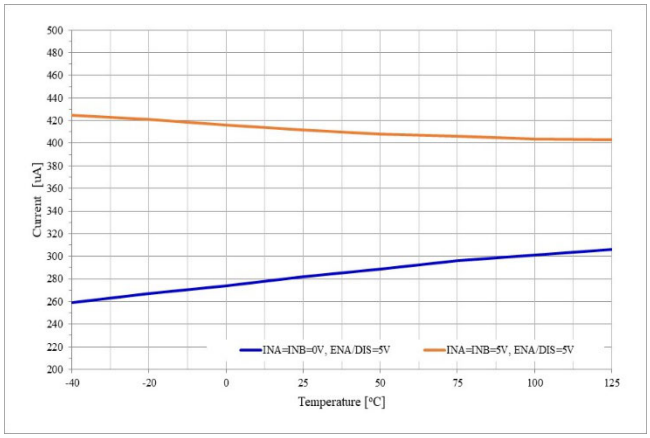



**Figure 11. Per Channel Quiescent $V_{CC}$ Supply Current vs. Temperature (INA = INB = 0 V or 5 V, ENA/DIS = 5 V and No Load)**

## TYPICAL CHARACTERISTICS (CONTINUED)

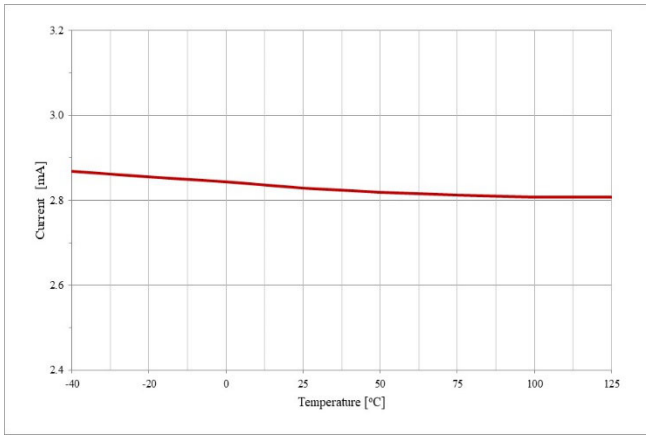



**Figure 12. Per Channel $V_{CC}$ Operating Current vs. Temperature (No Load and Switching Frequency = 500 kHz**

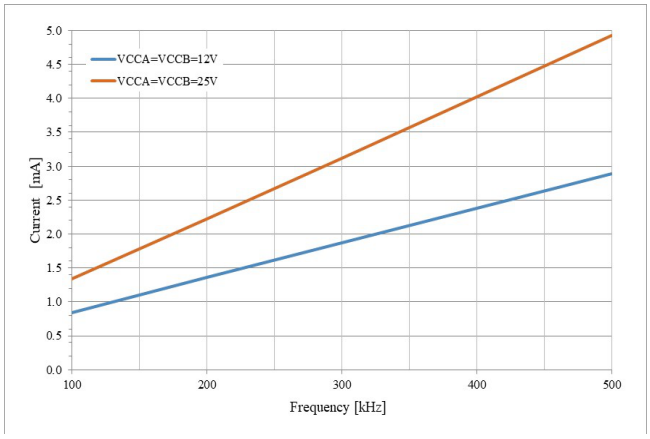



**Figure 13. Per Channel Operating Current vs. Frequency (No Load, $V_{CCA}$ = $V_{CCB}$ = 12 V, or 25 V)**

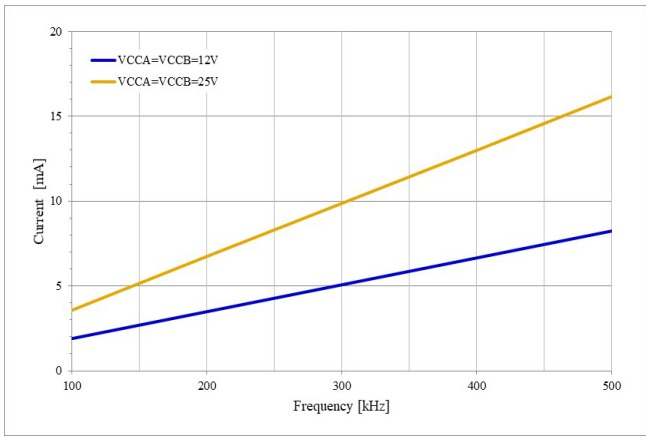



**Figure 14. Per Channel Operating Current vs. Frequency ($C_{LOAD}$ = 1 nF, $V_{CCA}$ = $V_{CCB}$ = 12 V, or 25 V)**

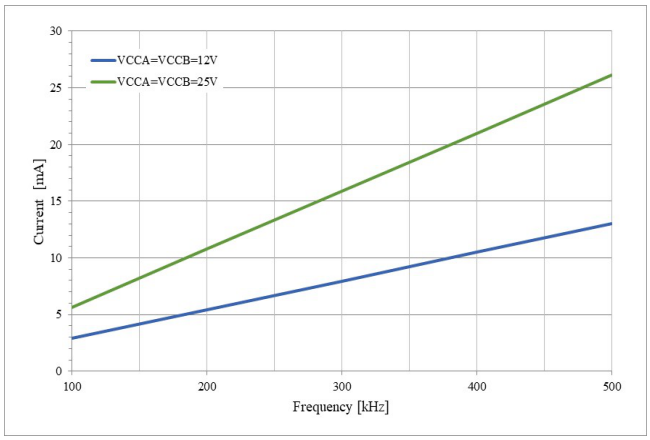



**Figure 15. Per Channel Operating Current vs. Frequency ($C_{LOAD}$ = 1.8 nF, $V_{CCA}$ = $V_{CCB}$ = 12 V, or 25 V)**

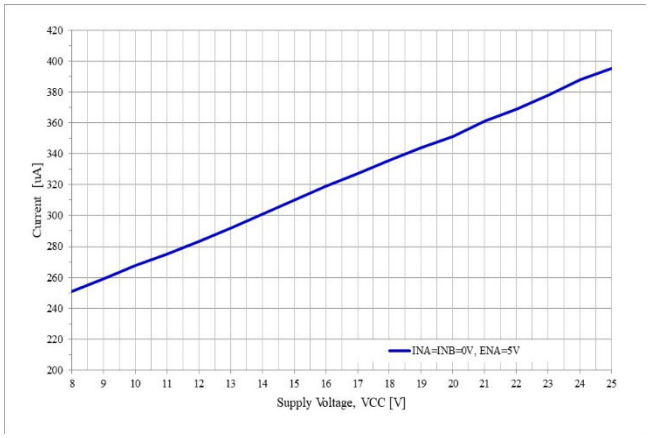



**Figure 16. Per Channel $V_{CC}$ Quiescent Current vs. $V_{CC}$ Supply Voltage (INA = INB = 0 V, ENA = 5 V)**

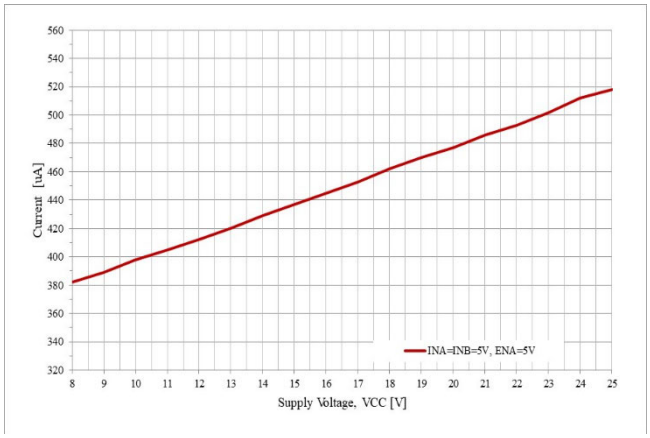



**Figure 17. Per Channel $V_{CC}$ Quiescent Current vs. $V_{CC}$ Supply Voltage (INA = INB = 5 V, ENA = 5 V)**

## TYPICAL CHARACTERISTICS (CONTINUED)

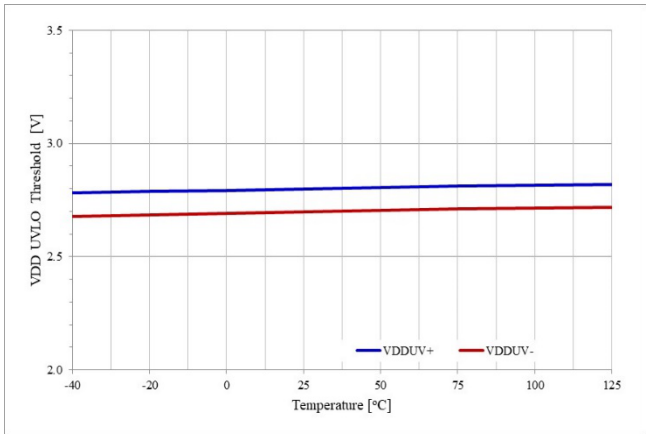



Figure 18. $V_{DD}$ UVLO Threshold vs. Temperature

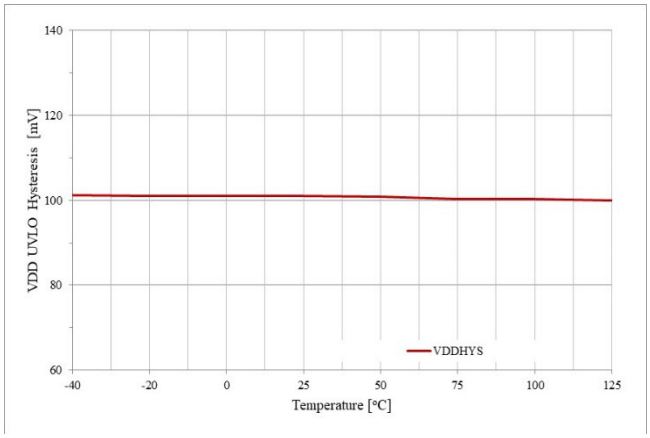



Figure 19. $V_{DD}$ UVLO Hysteresis vs. Temperature

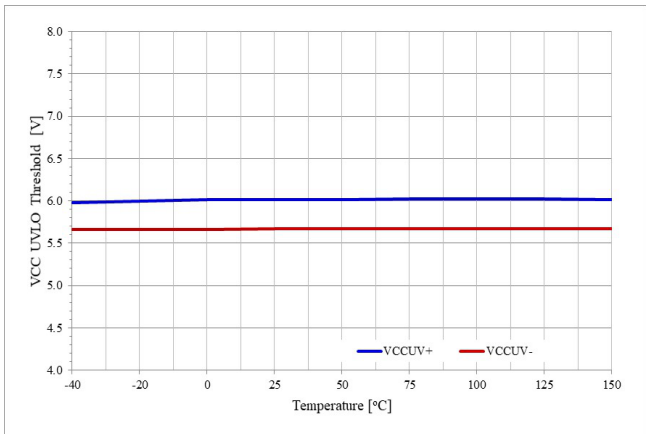



Figure 20. $V_{CC}$ 5−V UVLO Threshold vs. Temperature

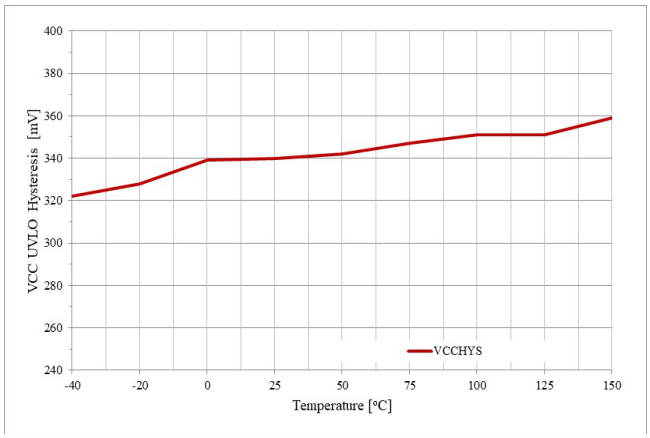



Figure 21. $V_{CC}$ 5−V UVLO Hysteresis vs. Temperature

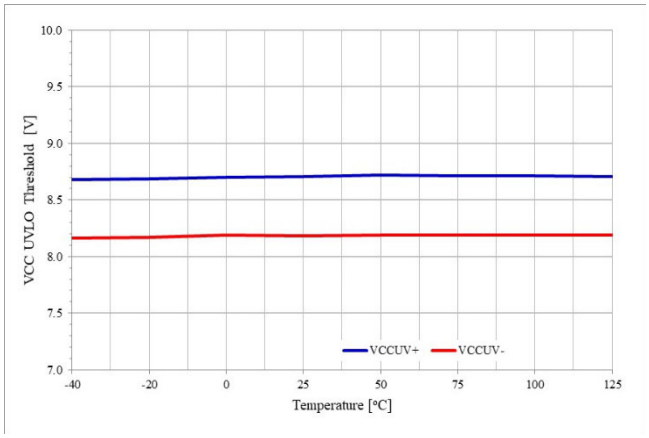



Figure 22. $V_{CC}$ 8−V UVLO Threshold vs. Temperature

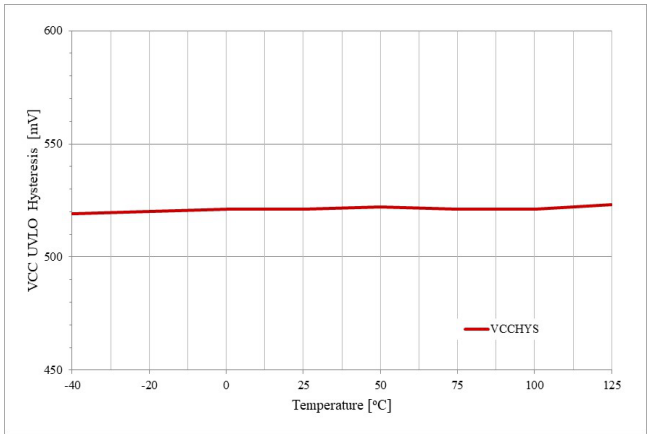



Figure 23. $V_{CC}$ 8−V UVLO Hysteresis vs. Temperature

## TYPICAL CHARACTERISTICS (CONTINUED)

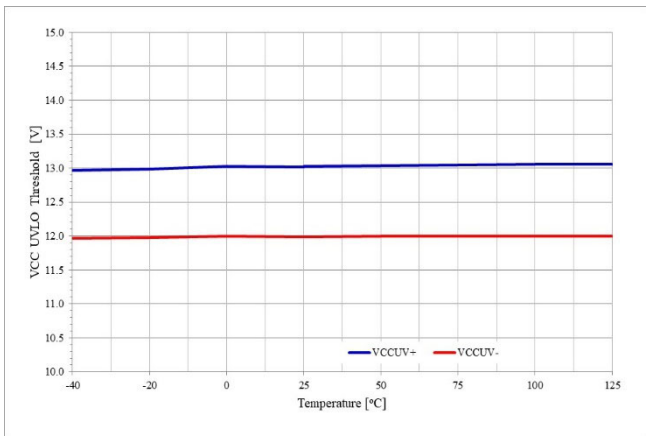



Figure 24. $V_{CC}$ 13−V UVLO Threshold vs. Temperature

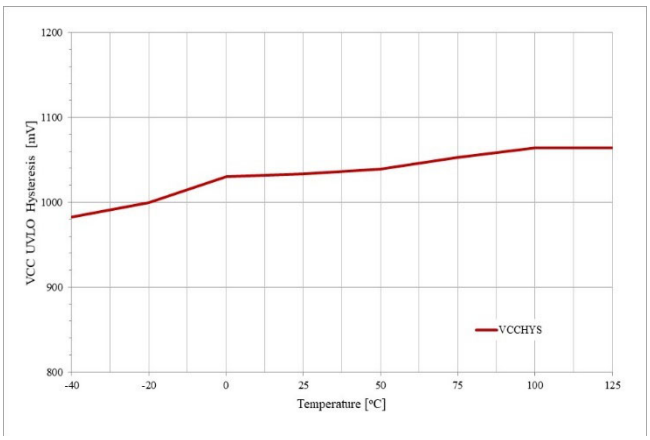



Figure 25. $V_{CC}$ 13−V UVLO Hysteresis vs. Temperature

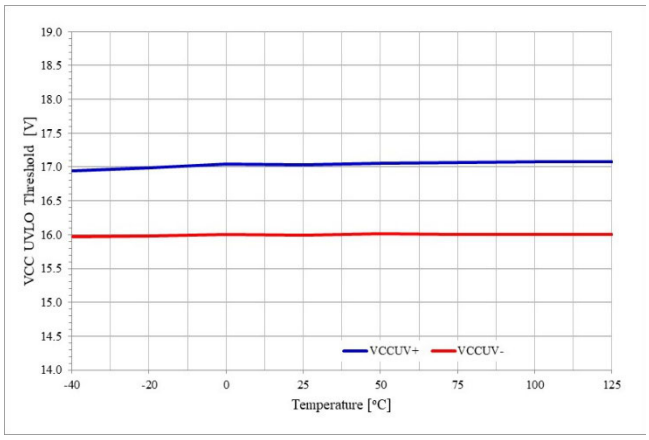



Figure 26. $V_{CC}$ 17−V UVLO Threshold vs. Temperature

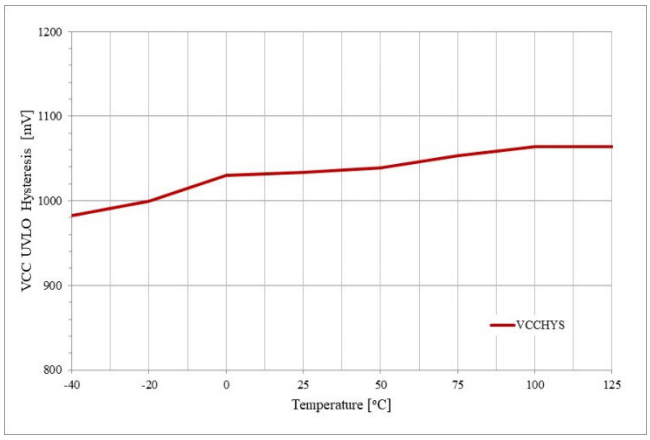



Figure 27. $V_{CC}$ 17−V UVLO Hysteresis vs. Temperature

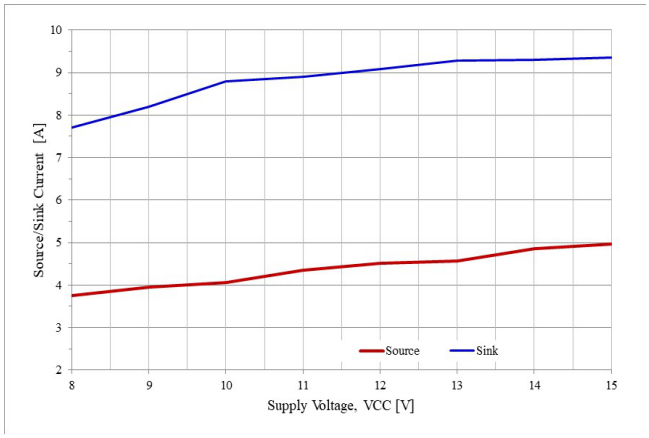



Figure 28. Output Current vs. $V_{CC}$ Supply Voltage

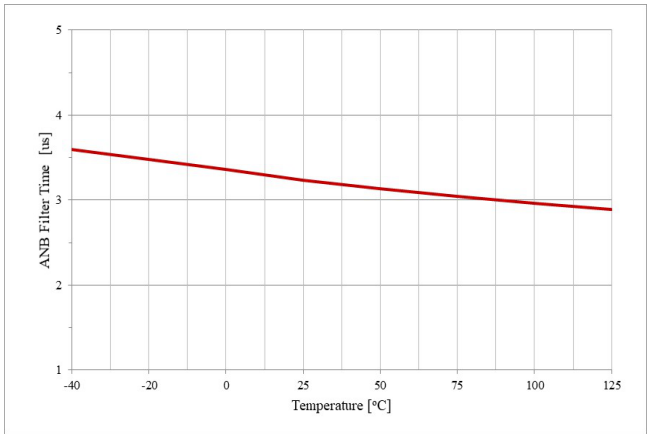



Figure 29. ANB Filer Time vs. Temperature

## TYPICAL CHARACTERISTICS (CONTINUED)

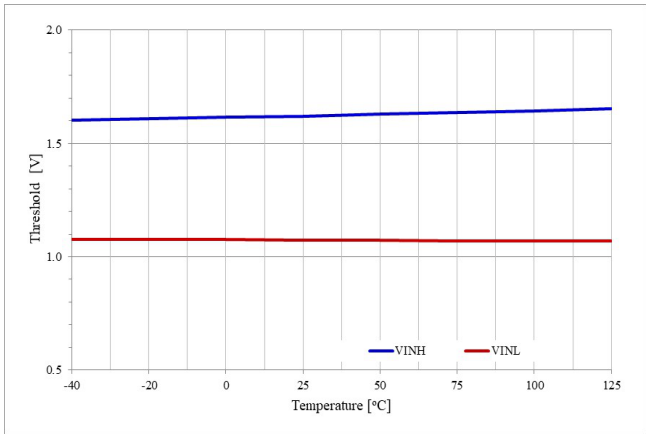



**Figure 30. Input Logic Threshold vs. Temperature (INA, INB, and ANB)**

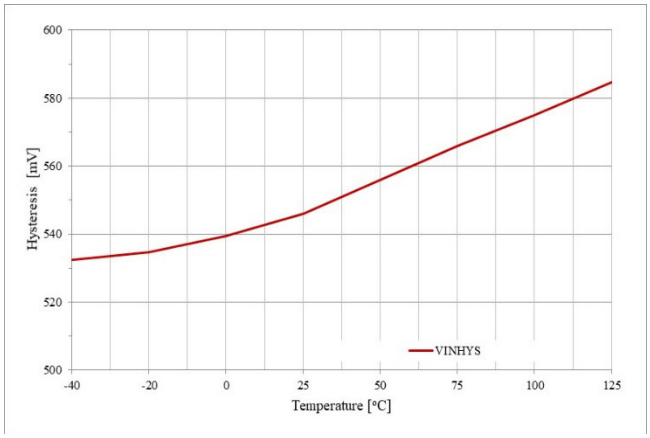



**Figure 31. Input Logic Hysteresis vs. Temperature (INA, INB, and ANB)**

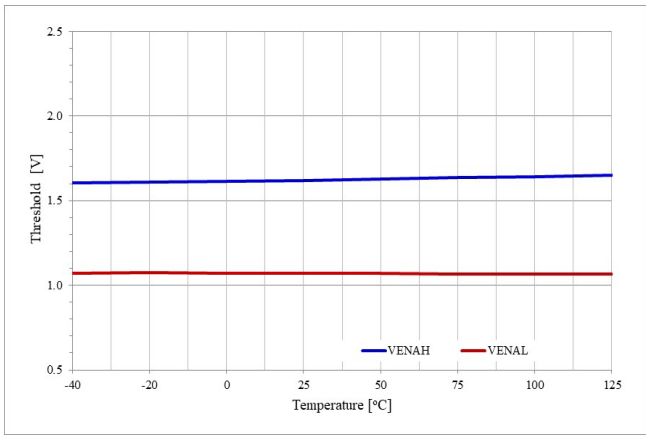



**Figure 32. ENA/DIS Threshold vs. Temperature (ENABLE, and DISABLE)**

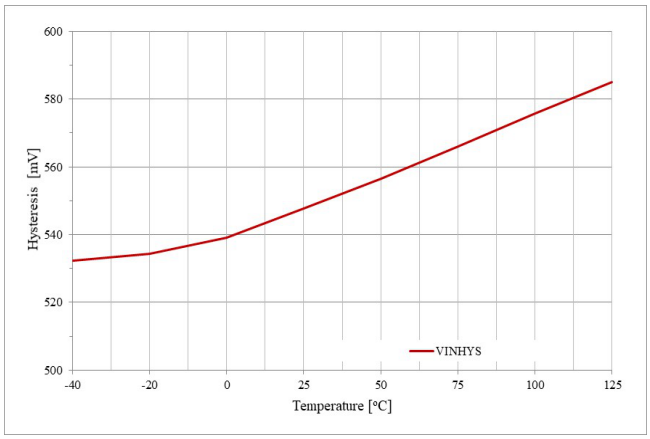



**Figure 33. ENA/DIS Hysteresis vs. Temperature (ENABLE, and DISABLE)**

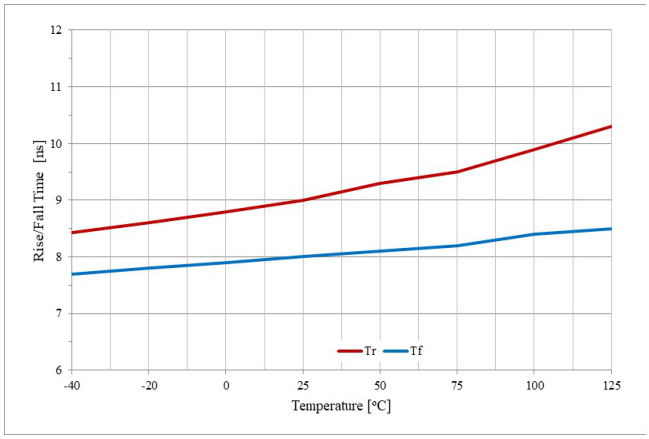



**Figure 34. Rise/Fall Time vs. Temperature ($C_{LOAD}$ = 1.8 nF)**

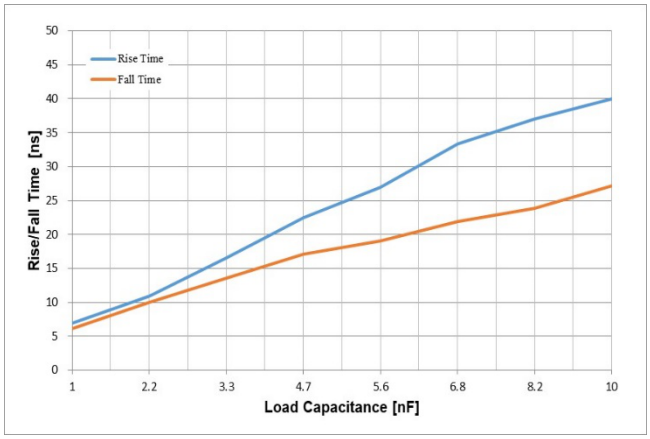



**Figure 35. Rise/Fall Time vs. Temperature ($V_{CCA}$ = $V_{CCB}$ = 12 V, and Different Load)**

## TYPICAL CHARACTERISTICS (CONTINUED)

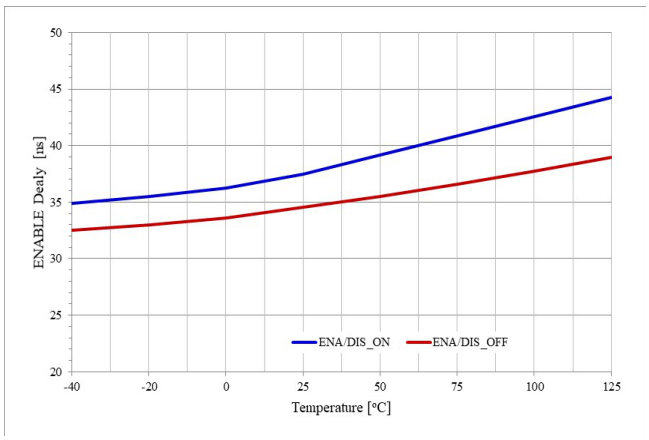



Figure 36. ENA/DIS Delay Time vs. Temperature

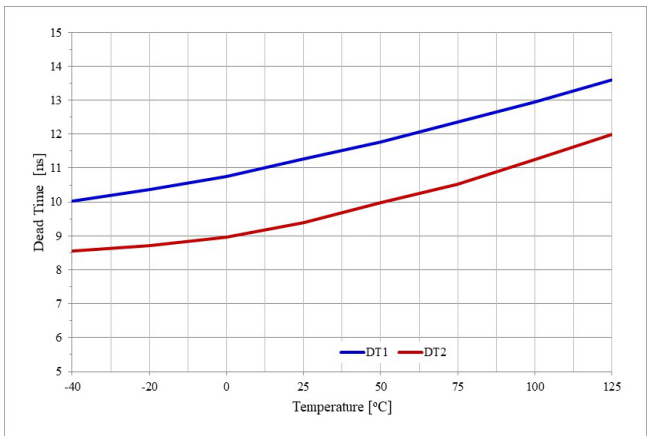



Figure 37. Dead Time vs. Temperature ($R_{DT}$ = Open)

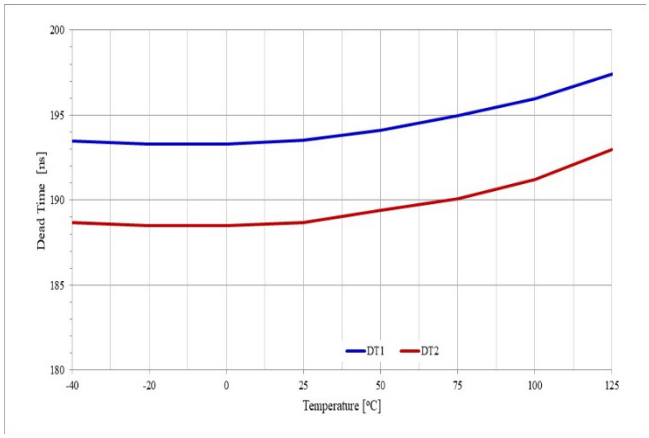



Figure 38. Dead Time vs. Temperature ($R_{DT}$ = 20 kΩ)

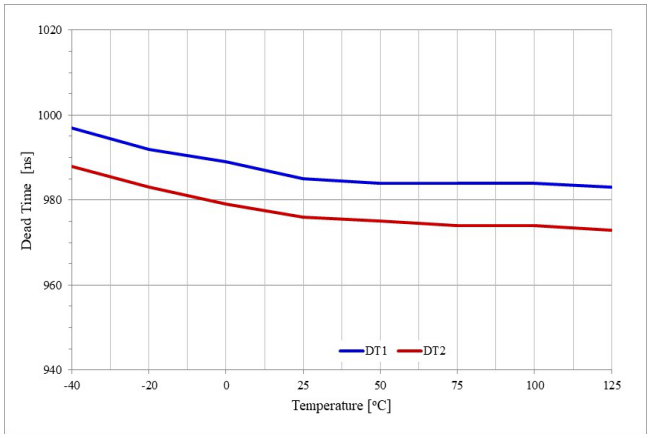



Figure 39. Dead Time vs. Temperature ($R_{DT}$ = 100 kΩ)

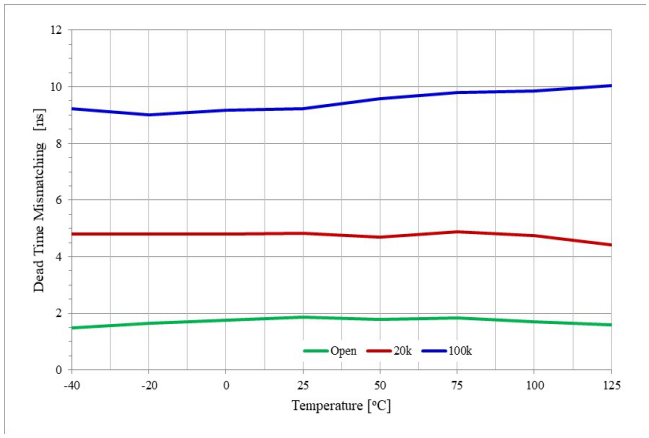



Figure 40. Dead Time Mismatching vs. Temperature

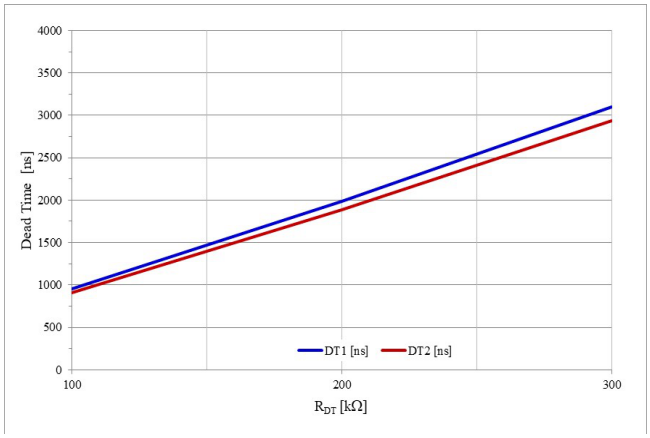



Figure 41. Dead Time vs. $R_{DT}$

## TYPICAL CHARACTERISTICS (CONTINUED)

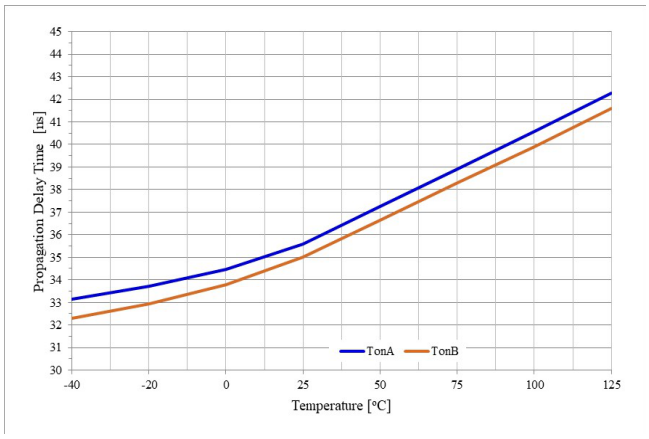



Figure 42. Turn−on Propagation Delay vs. Temperature

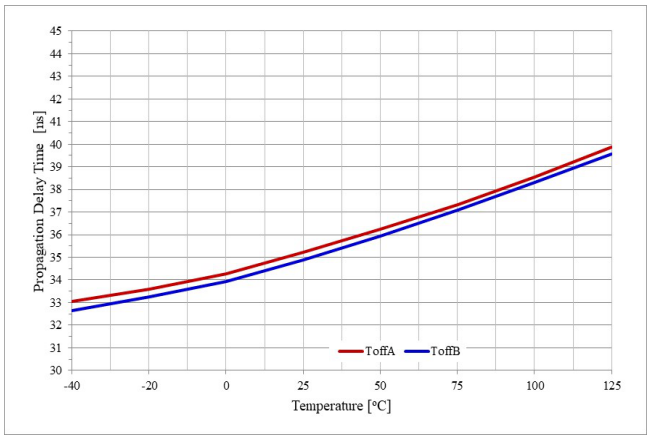



Figure 43. Turn−off Propagation Delay vs. Temperature

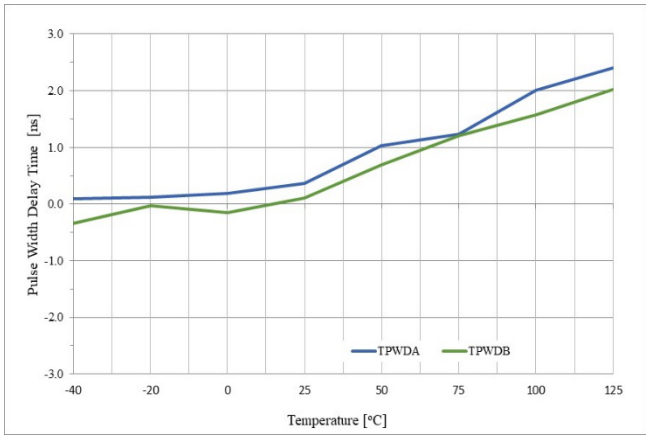



Figure 44. Pulse Width Distortion vs. Temperature

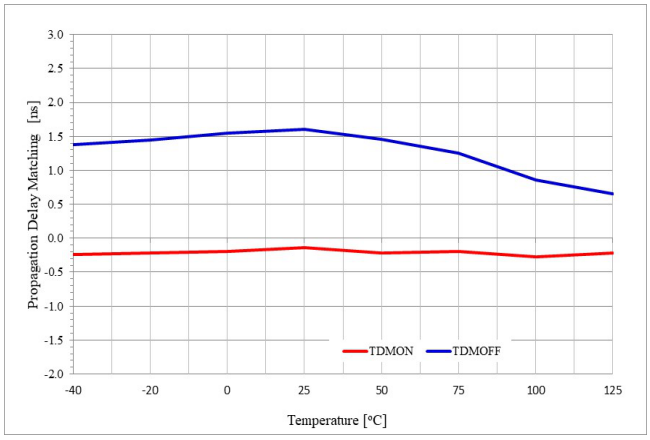



Figure 45. Propagation Delay Matching vs. Temperature

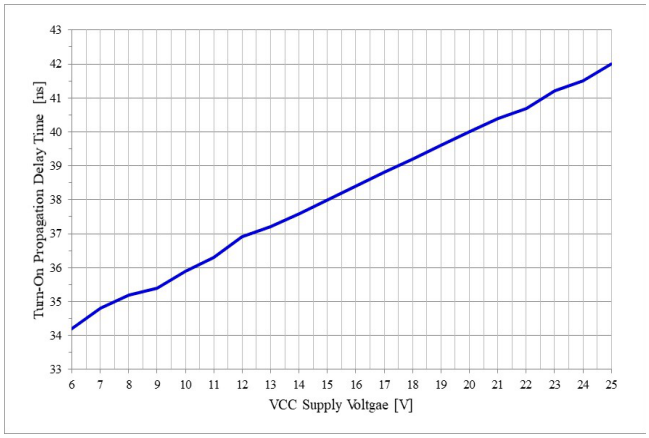



Figure 46. Turn−on Propagation Delay vs. $V_{CC}$ Supply Voltage

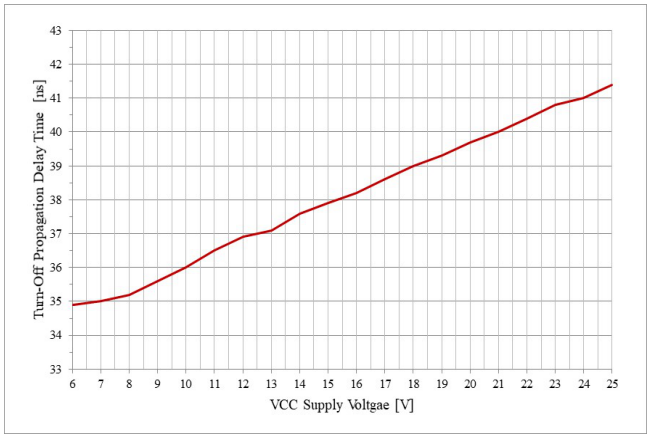



Figure 47. Turn−off Propagation Delay vs. $V_{CC}$ Supply Voltage

## PARAMETER MEASUREMENT DEFINITION

### Switching Time Definitions

Figure 48 shows the switching time definitions of the turn−on ($t_{PDON}$) and turn−off ($t_{PDOFF}$) propagation delay time among the driver's two input signals INA, INB and two output signals OUTA, OUTB. The typical values of the propagation delay ($t_{PDON}$, $T_{PDOFF}$), pulse width distortion ($t_{PWD}$) and delay matching between channels times are specified in the electrical characteristics table.

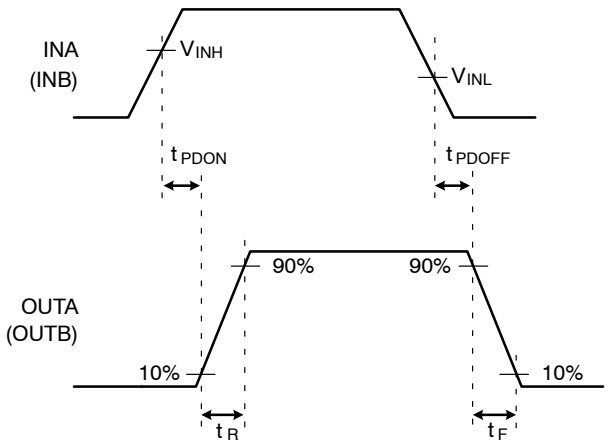



**Figure 48. Switching Time Definitions**

### Enable and Disable Function

Figure 49 shows the response time according to an ENABLE or the DISABLE operating modes. If the ENA/DIS pin voltage goes to LOW state, i.e. $V_{ENA} \leq 1.1$ V shuts down both outputs simultaneously and Pull the ENA/DIS pin HIGH (or left open), i.e. $V_{ENA} \geq 1.6$ V to operate normally in an ENABLE mode as shown in Figure 49 (a). Conversely, if the ENA/DIS pin voltage goes to HIGH state, i.e. $V_{DIS} \geq 1.6$ V shuts down both outputs simultaneously and Pull the ENA/DIS pin LOW (or left open), i.e. $V_{DIS} \leq 1.1$ V operate normally in the DISABLE mode as shown in Figure 49 (b).

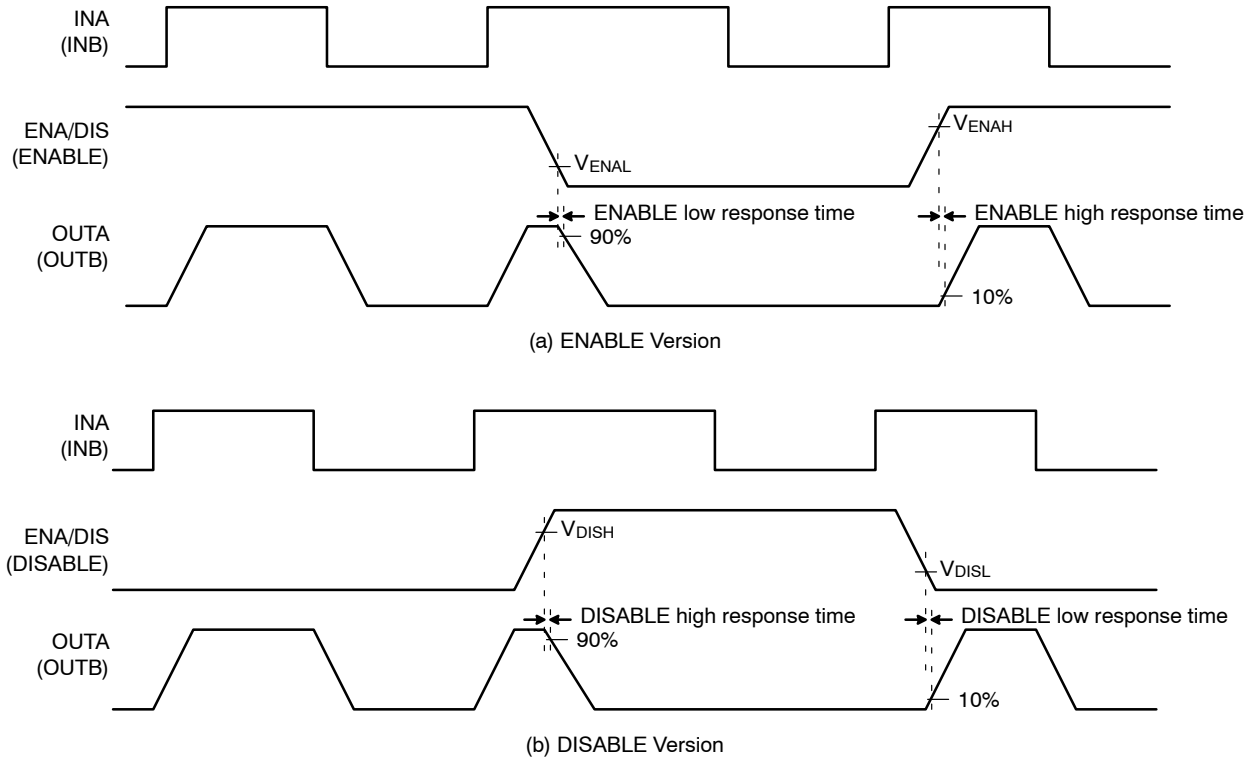



**Figure 49. Timing Chart of Enable and Disable Function**

**Programmable Dead−Time**

Dead time is automatically inserted whenever the dead time of the external two input signals (between INA and INB signals) is shorter than internal setting dead times (DT1 and DT2). Otherwise, if the external input signal dead times are larger than internal dead− time, the dead time is not modified by the gate driver and internal dead−time definition as shown in Figure 50.

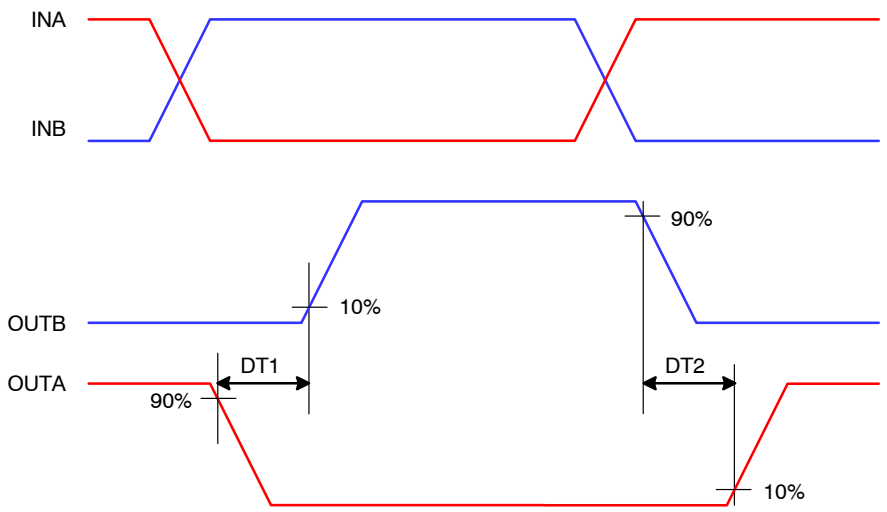



**Figure 50. Internal Dead−Time Definitions**

Figure 51 shows the definition of internal dead time and shoot−through prevention when input signals applied at same time.

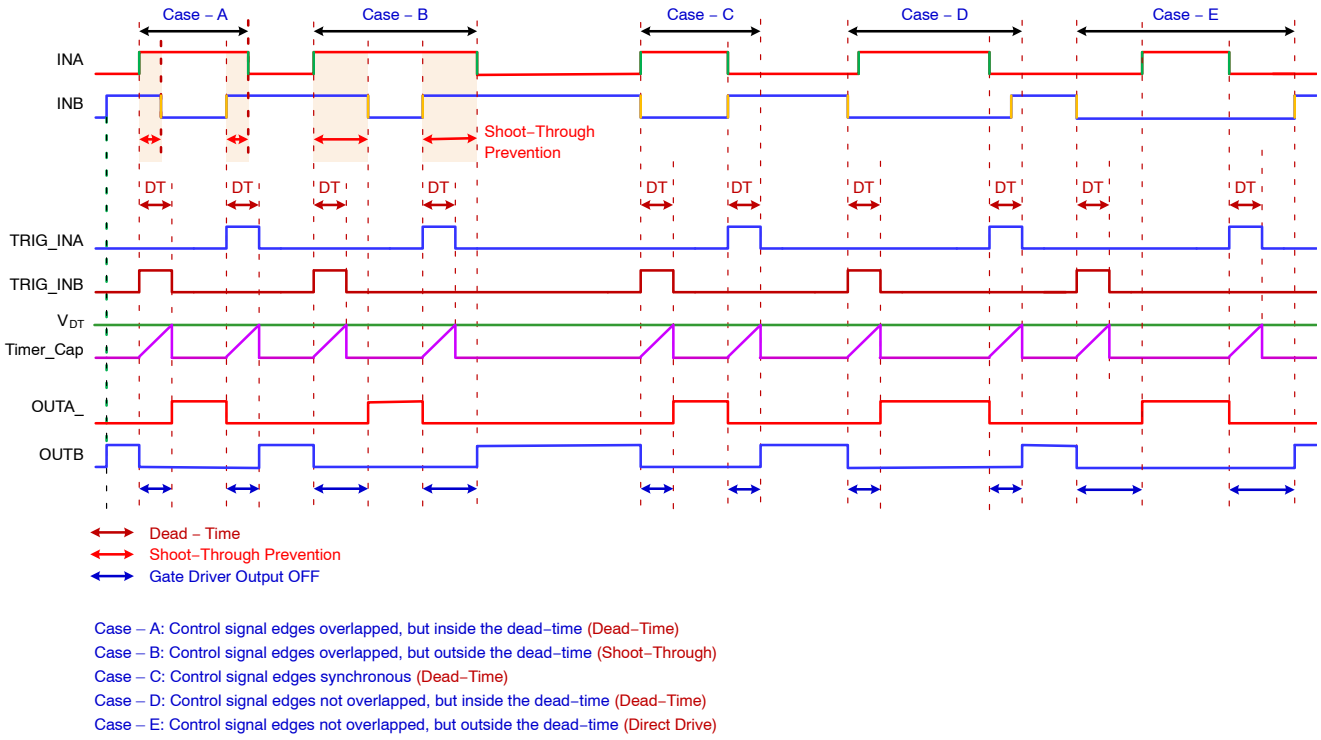



**Figure 51. Internal Dead−Time Definitions**

### Input to Output Operation Definitions

The NCP51563 provides important protection functions such as independent under−voltage lockout for both gate driver; enable or disable function and dead−time control function. Figure 52 shows an overall input to output timing diagram when shutdown mode via ENA/DIS pin in the *CASE−A*, and Under−Voltage Lockout protection on the primary− and secondary−sides power supplies events in the *CASE−B*. The gate driver output (OUTA and OUTB) were turn−off when cross−conduction event at the dead time control mode in the *CASE−C*.

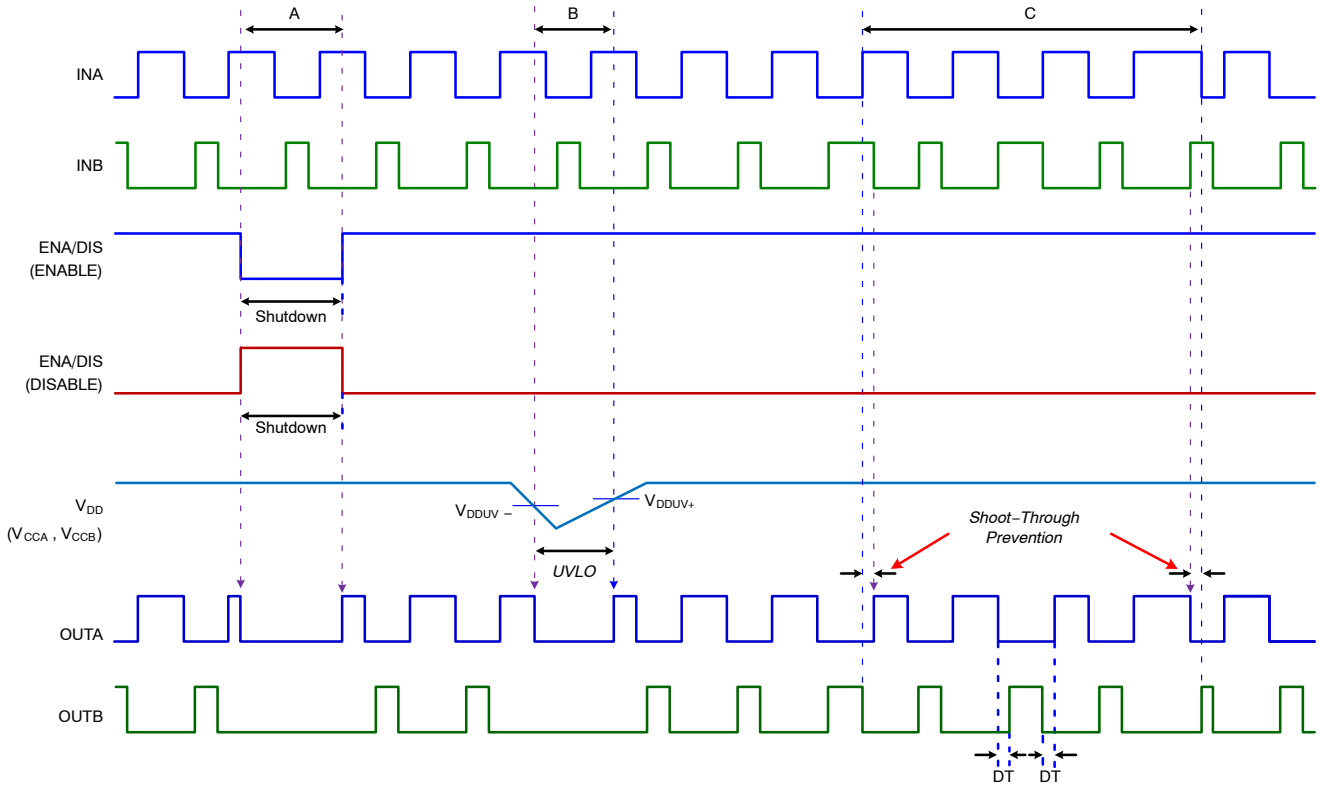



**Figure 52. Overall Operating Waveforms Definitions at the Dead−Time Control Mode**

### Input and Output Logic Table

Table 1 shows an input to output logic table according to the dead time control modes and an enable or disable operation mode.

**Table 1. INPUT AND OUTPUT LOGIC TABLE**

| INPUT | | | | OUTPUT | | |
|---|---|---|---|---|---|---|
| | | ENA/DIS | | | | |
| INA | INB | ENABLE | DISABLE | OUTA | OUTB | NOTE |
| L | L | H or Left open | L or Left open | L | L | Programmable dead time control with $R_{DT}$. |
| L | H | H or Left open | L or Left open | L | H | |
| H | L | H or Left open | L or Left open | H | L | |
| H | H | H or Left open | L or Left open | L | L | DT pin is left open Or programmed with $R_{DT}$. |
| H | H | H or Left open | L or Left open | H | H | DT pin pulled to $V_{DD}$. |
| Left open | Left open | H or Left open | L or Left open | L | L | |
| X | X | L | H | L | L | |

23. “X” means L, H or left open.

### Input Signal Configuration

The NCP51563 allows to set the input signal configuration through the ANB pin for user convenience. There are four operating modes that allow to change the configuration of the input to output channels (e.g. single input – dual output, or dual input – dual output), and select the shutdown function (e.g. Disable or Enable mode) as below Table 2. Unused input pins (e.g. INA, INB, and ANB) should be tied to GND to achieve better noise immunity.

In addition, the ANB pin has an internal filter time typically 3.3 μs to achieve the noise immunity.

**Table 2. INPUT SIGNAL CONFIGURATION LOGIC TABLE**

| Mode | Functional Input Pin | | | | Input Configuration |
|---|---|---|---|---|---|
| | INA | INB | ANB | ENA/DIS | |
| 1 | INA | INB | L | DISABLE | Dual−Input, Dual−Output with disable mode (ENA/DIS = LOW) |
| 2 | INA | X | H | DISABLE | Single−Input (INA), Dual−Output with disable mode(ENA/DIS = LOW) |
| 3 | INA | INB | L | ENABLE | Dual−Input, Dual−Output with enable mode (ENA/DIS = HIGH) |
| 4 | INA | X | H | ENABLE | Single−Input (INA), Dual−Output with enable mode (ENA/DIS = HIGH) |

Figure 53 shows an operating timing chart of input to output and shutdown function according to the ANB and ENA/DIS pins setting. The ENA/DIS and ANB pins are only functional when $V_{DD}$ stays above the specified UVLO threshold. It is recommended to tie these pins to Ground if the ENA/DIS and ANB pins are not used to achieve better noise immunity, and it is recommended to bypass using a 1 nF low ESR/ESL capacitor close to these pins for the DISABLE (e.g. NCP51563xB) mode.

When it is not possible to connect ANB to GND then external pull−down resistor few ten kΩ (e.g. 10~47 kΩ) is recommended to prevent unwanted ANB activation by external interference as despite its internal 3.3 μs filter.

The OUTA and OUTB works as complementary outputs from PWM input signal on the INA pin regardless the INB signal when the ANB pin is HIGH.

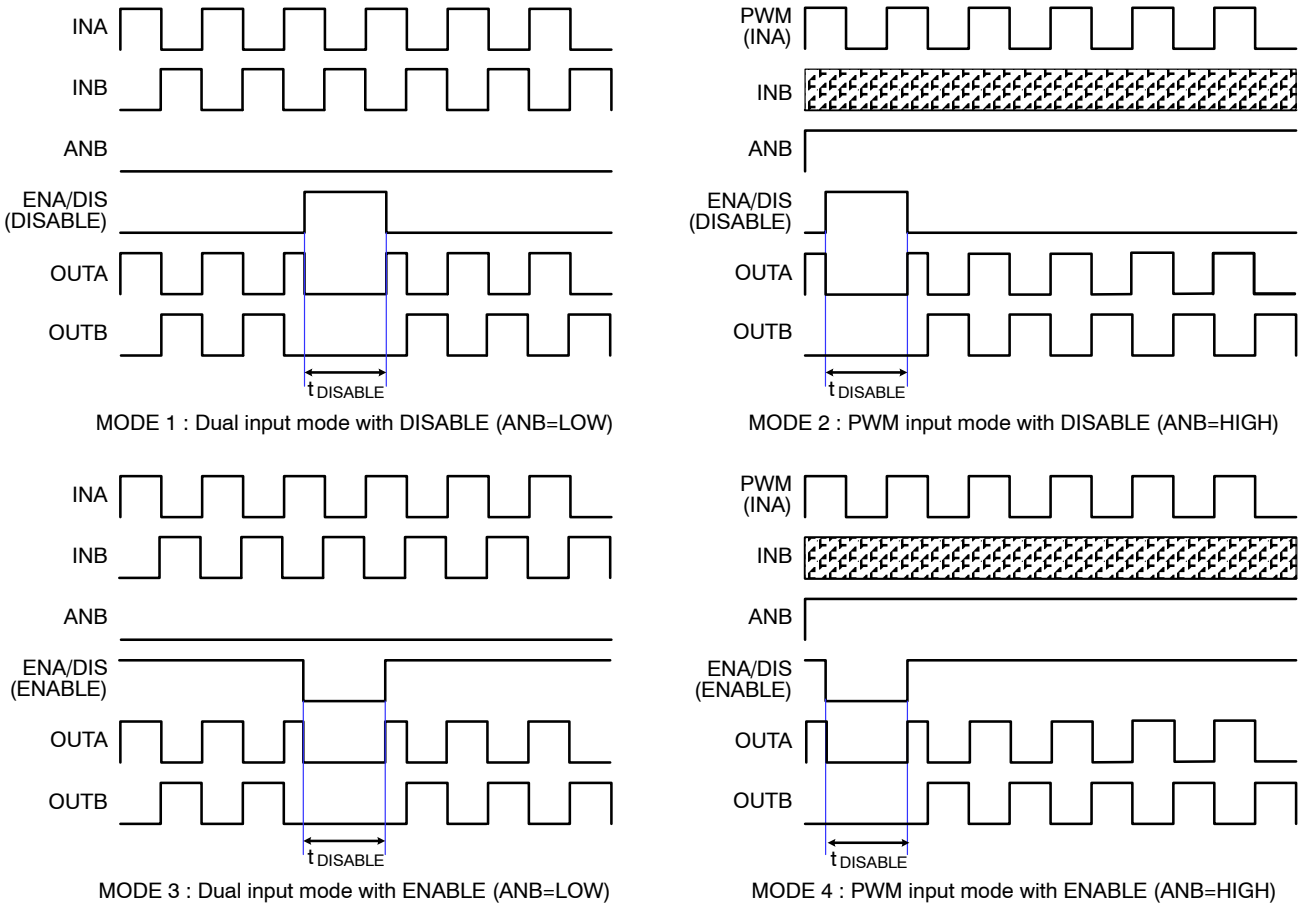



**Figure 53. Timing Chart of ENABLE and DISABLE Modes**

## PROTECTION FUNCTION

The NCP51563 provides the protection features include enable or disable function, Cross Conduction Protection, and Under−Voltage Lockout (UVLO) of power supplies on primary−side ($V_{DD}$), and secondary−side both channels ($V_{CCA}$, and $V_{CCB}$).

### Under−Voltage Lockout Protection $V_{DD}$ and $V_{CCx}$

The NCP51561 provides the Under−Voltage Lockout (UVLO) protection function for $V_{DD}$ in primary−side and both gate drive output for $V_{CCA}$ and $V_{CCB}$ in secondary−side as shown in Figure 54.

The gate driver is running when the $V_{DD}$ supply voltage is greater than the specified under−voltage lockout threshold voltage (e.g. typically 2.8 V) and ENA/DIS pin is HIGH or LOW states for an ENABLE (e.g. NCP51561xA) or the DISABLE (e.g. NCP51561xB) mode respectively.

In addition, both gate output drivers have independent under voltage lockout protection (UVLO) function and each channel supply voltages in secondary−side (e.g. $V_{CCA}$, and $V_{CCB}$) need to be greater than specified UVLO threshold level in secondary−side to let the output operate per input signal. The typical $V_{CCx}$ UVLO threshold voltage levels for each option are per below Table 3.

**Table 3. $V_{CCX}$ UVLO OPTION TABLE**

| Option | $V_{CC}$ UVLO Level | Unit |
|---|---|---|
| 5−V | 6.0 | V |
| 8−V | 8.7 | V |
| 13−V | 13 | V |
| 17−V | 17 | V |

UVLO protection has an hysteresis to provide immunity to short $V_{CC}$ drops that can occur.

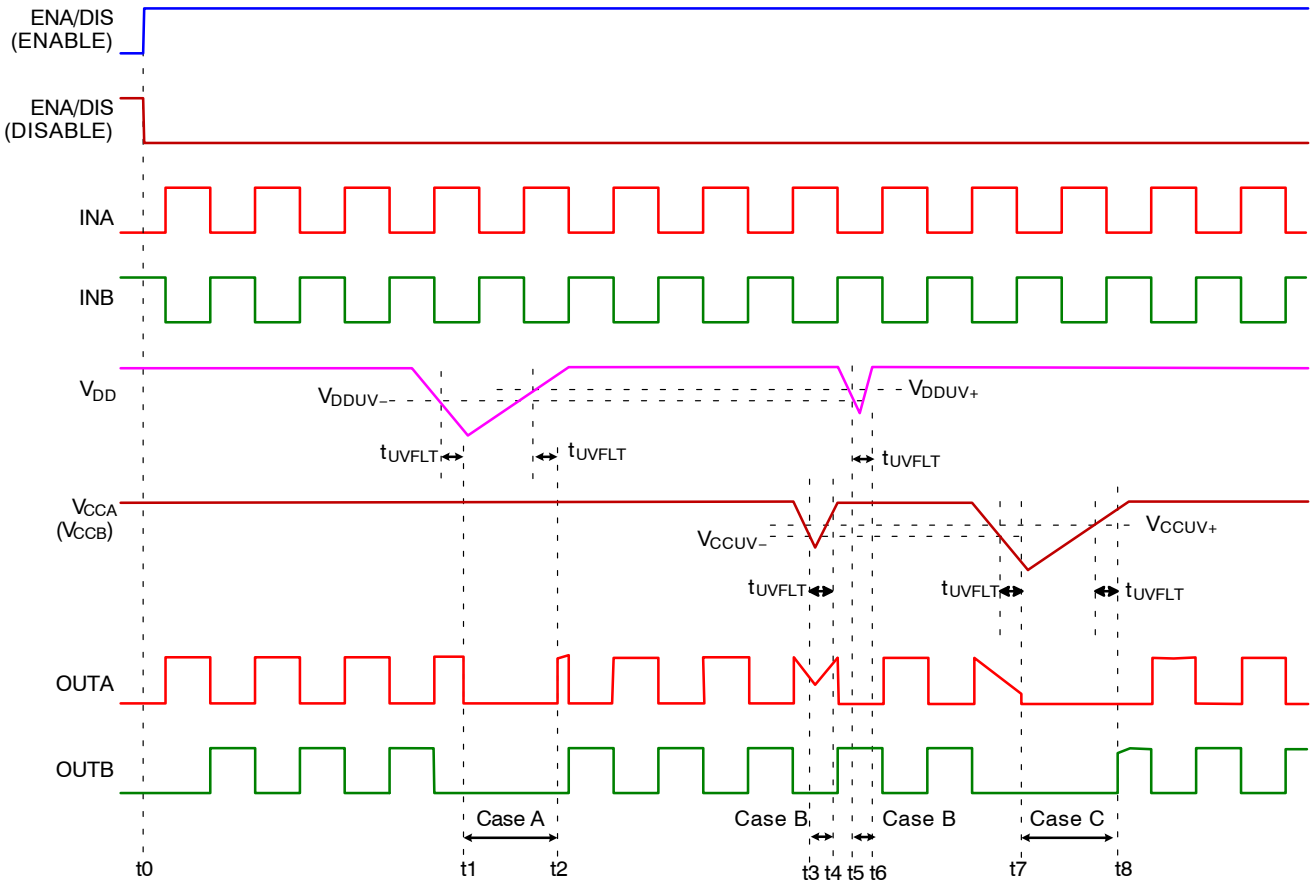
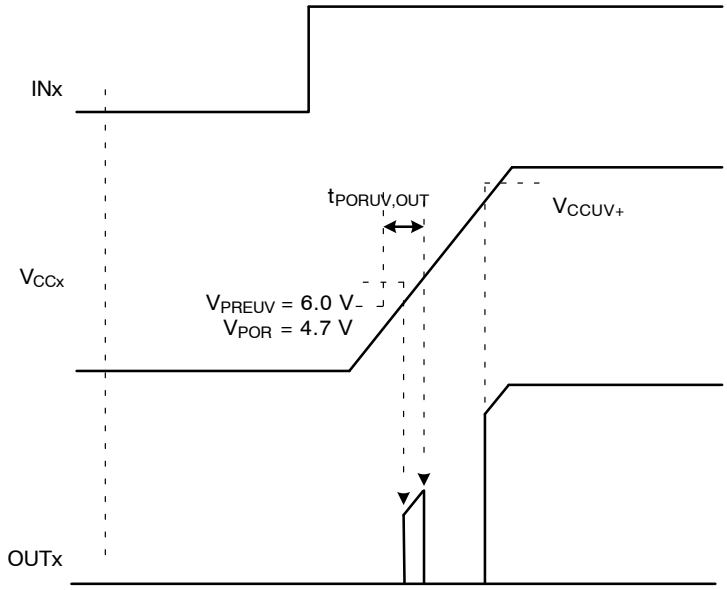



**Figure 54. Timing Chart Under−Voltage Lockout Protection**

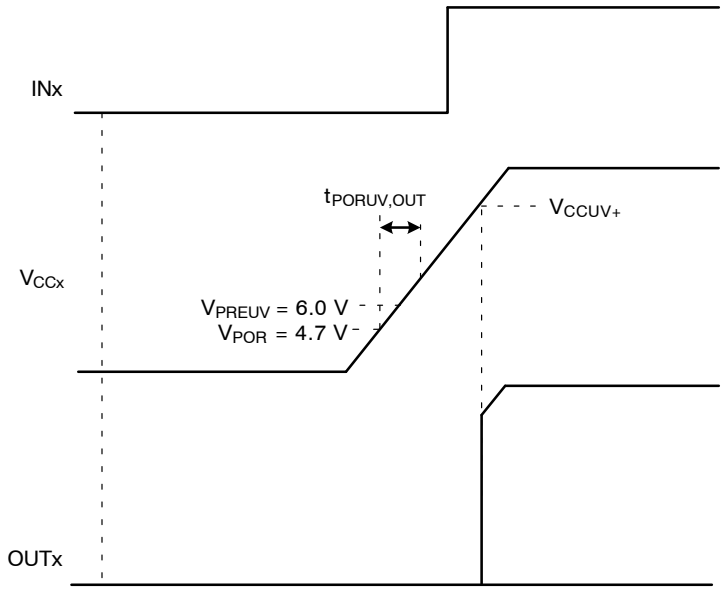
### $V_{CCX}$ Power−Up and $IN_X$ Signal

To provide a variety of Under−Voltage Lockout (UVLO) thresholds NCP51563 has a power−up delay time during initial $V_{CCX}$ start−up or after POR event.

In case $IN_X$ pins are active when $V_{CCX}$ is above 4.7 V, outputs would occur until settling time has elapsed as shown in Figure 55 (A). If $IN_X$ are only active after settling time has expired, outputs won't be active until $V_{CCX}$ cross NCP51561 specific $V_{CCUV+}$ as shown in Figure 55 (B).




A. Power up with PWM signals during Preset




B. Power up without PWM signals during Preset

**Figure 55. $V_{CCX}$ Power−up**

### Cross−Conduction Prevention and Allowed Overlapped Operation

The cross conduction prevents both high− and low−side switches from conducting at the same time when the dead time (DT) control mode is in half−bridge type, as shown in Figure 56.

For full topologies flexibility, cross conduction can be allowed both high− and low−side switches conduct at the same time when the DT pin is pulled to $V_{DD}$ for example, as shown in Figure 57.

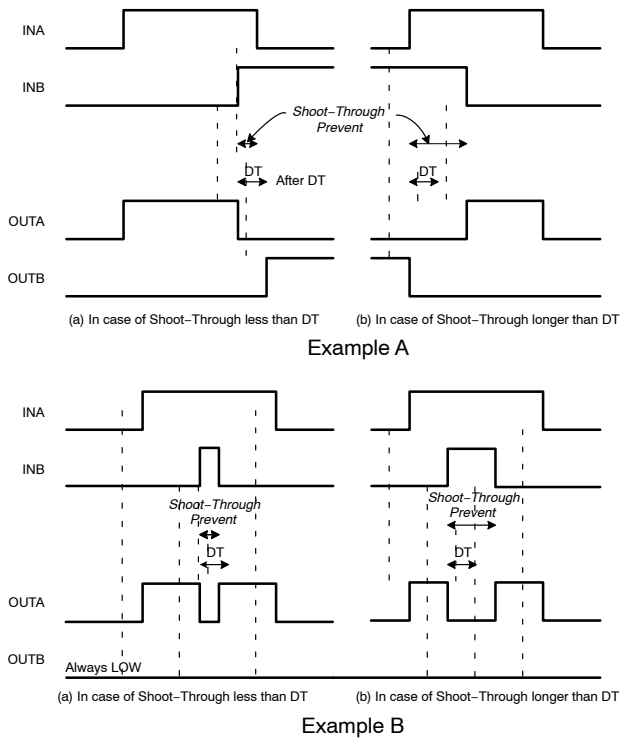



**Figure 56. Concept of Shoot−Through Prevention**

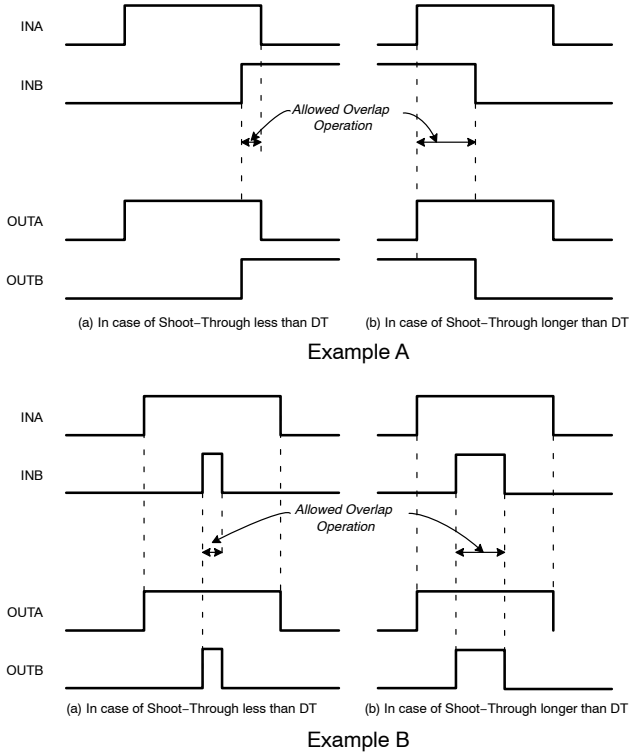



**Figure 57. Concept of Allowed the Shoot−Through**

### Programmable Dead Time Control

Cross−conduction between both driver outputs (OUTA, and OUTB) is not allowed with minimum dead time ($t_{DTMIN}$) typically 10 ns when the DT pin is open in the *MODE−A*. External resistance ($R_{DT}$) controls dead time when the DT pin resistor between 1 kΩ and 300 kΩ in the *MODE−B*. Overlap is not allowed when the dead time (DT) control mode is activated.

The dead time (DT) between both outputs is set according to: DT (in ns) = 10 x $R_{DT}$ (in kΩ).

Overlap is allowed for both outputs when the DT pin is pulled to $V_{DD}$ in the *MODE−C*, as shown in Figure 58.

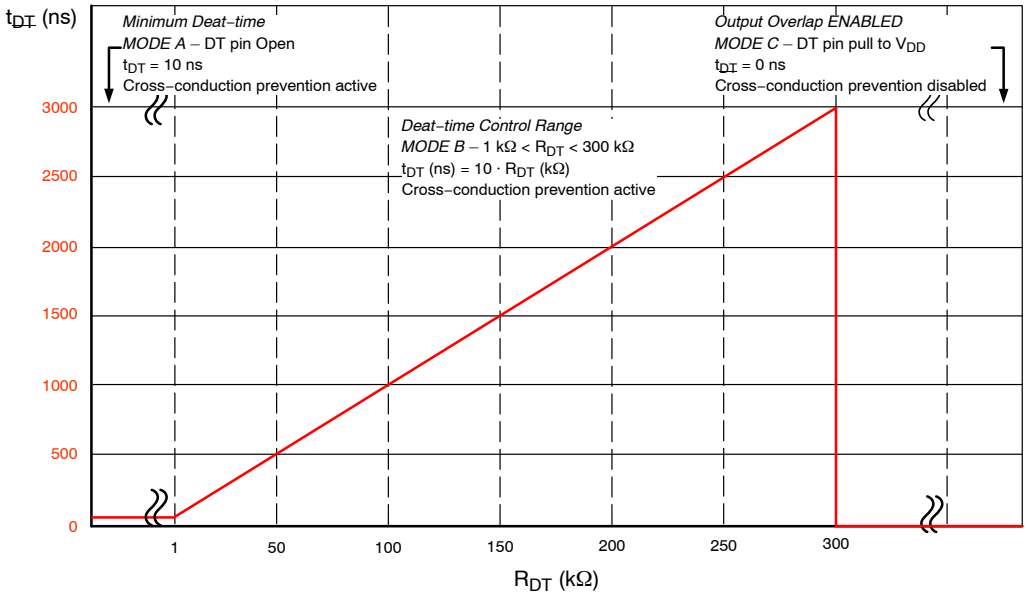



**Figure 58. Timing Chart of Dead−Time Mode Control**

### Common Mode Transient Immunity Testing

Figure 59 is a simplified diagram of the Common Mode Transient Immunity (CMTI) testing configuration.

CMTI is the maximum sustainable common−mode voltage slew rate while maintaining the correct output.

CMTI applies to both rising and falling common−mode voltage edges. CMTI is tested with the transient generator connected between GND and $V_{SSA}$ and $V_{SSB}$. ($V_{CM}$ = 1500 V).

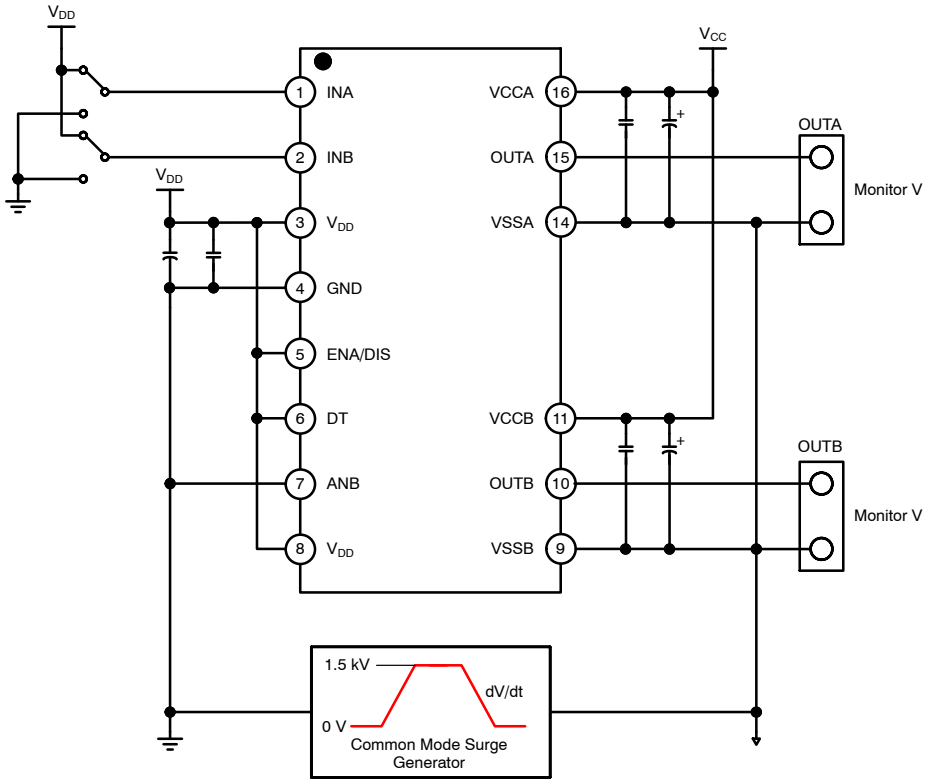



**Figure 59. Common Mode Transient Immunity Test Circuit**

## APPLICATION INFORMATION

This section provides application guidelines when using the NCP51563.

### Power Supply Recommendations

It is important to remember that during the Turn−On of switch the output current to the gate is drawn from the $V_{CCA}$ and $V_{CCB}$ supply pins. The $V_{CCA}$ and $V_{CCB}$ pins should be bypassed with a capacitor with a value of at least ten times the gate capacitance, and no less than 100 nF and located as close to the device as possible for the purpose of decoupling. A low ESR, ceramic surface mount capacitor is necessary. We recommend using 2 capacitors; a 100 nF ceramic surface−mount capacitor which can be very close to the pins of the device, and another surface−mount capacitor of few microfarads added in parallel.

In addition, it is recommended to provide various $V_{CCX}$ Under−Voltage Lockout voltage options (e.g. 8−V, or 13−V), the $V_{CCX}$ rising time from 5−V to 6−V should be at least 16 μs or above at initial start−up.

### Input Stage

The input signal pins (INA, INB, ANB, and ENA/DIS) of the NCP51563 are based on the TTL compatible input−threshold logic that is independent of the $V_{DD}$ supply voltage. The logic level compatible input provides a typically high and low threshold of 1.6 V and 1.1 V respectively. The input signal pins impedance of the NCP51563 is 200 kΩ typically and the INA, INB, and ANB pins are pulled to GND pin and ENA/DIS pin is pulled to $V_{DD}$ pin for an ENABLE version as shown in Figure 60. Conversely, ENA/DIS pin pulled to GND pin for the DISABLE version. It is recommended that ENA/DIS pin should be tie to $V_{DD}$ or GND pins for ENABLE and DISABLE versions respectively if the ENA/DIS pin is not used to achieve better noise immunity because the ENA/DIS pin is quite responsive, as far as propagation delay and other switching parameters are concerned.

An RC filter is recommended to be added on the input signal pins to reduce the impact of system noise and ground bounce, the time constant of the RC filter. Such a filter should use an $R_{IN}$ in the range of 0 Ω to 100 Ω and a $C_{IN}$ between 10 pF and 100 pF. In the example, an $R_{IN}$ = 51 Ω and a $C_{IN}$ = 33 pF are selected, with a corner frequency of approximately 100 MHz. When selecting these components, it is important to pay attention to the trade−off between good noise immunity and propagation delay.

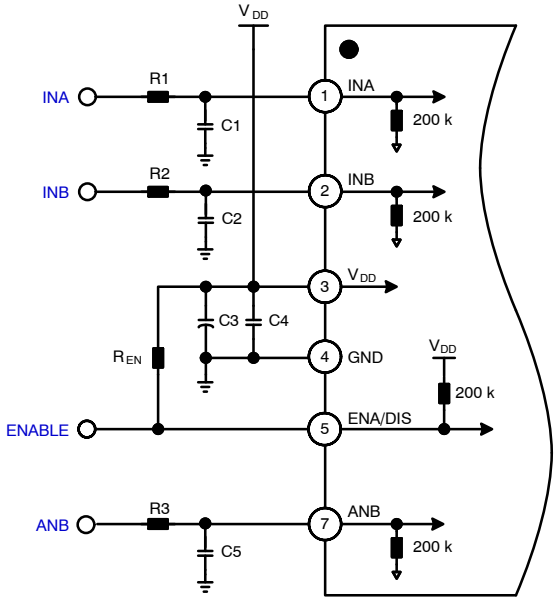



**Figure 60. Schematic of Input Stage**

### Output Stage

The output driver stage of the NCP51563 features a pull up structure and a pull down structure.

The pull up structure of the NCP51563 consists of a PMOS stage ensuring to pull all the way to the $V_{CC}$ rail. The pull down structure of the NCP51563 consists of a NMOS device as shown in Figure 61.

The output impedance of the pull up and pull down switches shall be able to provide about +4.5 A and −9 A peak currents typical at 25°C and the minimum sink and source peak currents at −40°C are −7 A sink and +2.6 A source.

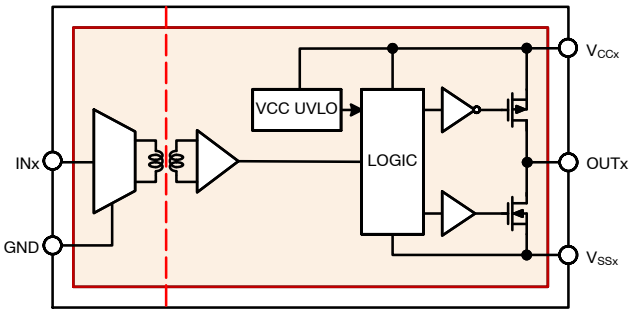



**Figure 61. Schematic of Output Stage**

### Consideration of Driving Current Capability

Peak source and sink currents ($I_{SOURCE}$, and $I_{SINK}$) capability should be larger than average current ($I_{G,AV}$) as shown in Figure 62.

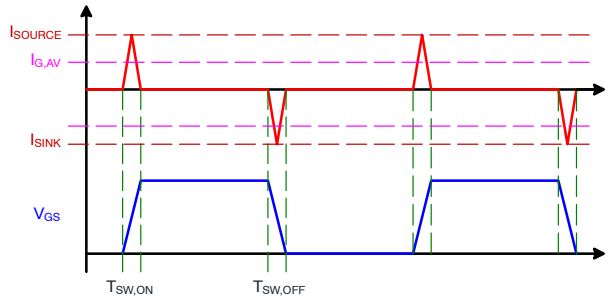



**Figure 62. Definition of Current Driving Capability**

The approximate maximum gate charge $Q_G$ that can be switched in the indicated time for each driver current rating may be calculate: Needed driver current ratings depend on what gate charge $Q_G$ must be moved in what switching time $t_{SW-ON/OFF}$ because average gate current during switching is $I_G$.

$$I_{G.AV} = \frac{Q_G}{t_{SW,ON/OFF}} \quad \text{(eq. 1)}$$

The approximate gate driver source and sink peak currents can be calculated as below equations.

*At turn−on (Sourcing current)*

$$I_{SOURCE} \geq 1.5 \times \frac{Q_G}{t_{SW,ON}} \quad \text{(eq. 2)}$$

*At turn−off (Sinking current)*

$$I_{SINK} \geq 1.5 \times \frac{Q_G}{t_{SW,OFF}} \quad \text{(eq. 3)}$$

where, $Q_G$ = Gate charge at $V_{GS} = V_{CC}$
$t_{SW,\ ON/OFF}$ = Switch On / Off time
1.5 = empirically determined factor
(Influenced by $I_{G,AV}$ vs. $I_{DRV}$, and circuit parasitic)

### Consideration of Gate Resistor

The gate resistor is also sized to reduce ringing voltage by parasitic inductances and capacitances. However, it limits the current capability of the gate driver output. The limited current capability value induced by turn−on and off gate resistors can be obtained with below equation.

$$I_{SOURCE} = \frac{V_{CC} - V_{OH}}{R_{G,ON}}$$

$$I_{SINK} = \frac{V_{CC} - V_{OL}}{R_{G,OFF}} \quad \text{(eq. 4)}$$

where:
$I_{SOURCE}$: Source peak current
$I_{SINK}$: Sink peak current.
$V_{OH}$: High level output voltage drop
$V_{OL}$: Low level output voltage drop

### Application Circuits with Output Stage Negative Bias

SiC MOSFET unique operating characteristics need to be carefully considered to fully benefits from SiC characteristics. The gate driver needs to be capable of providing +20 V and −2 V to −5 V negative bias with minimum output impedance and high current capability.

When parasitic inductances are introduced by non−ideal PCB layout and long package leads (e.g. TO−220 and TO−247 type packages), there could be ringing in the gate−source drive voltage of the power transistor during high di/dt and dv/dt switching. If the ringing is over the threshold voltage, there is the risk of unintended turn−on and even shoot−through. Applying a negative bias on the gate drive is a popular way to keep such ringing below the threshold. Negative voltage can improve the noise tolerance of SiC MOSFET to suppress turning it unintentionally. The negative gate−source voltage makes the capacitance of Cgd becoming lower, which can reduce the ringing voltage.

Below are a few examples of implementing negative gate drive bias. The first example with negative bias with two isolated−bias power supplies as shown in Figure 63.

Power supply VHx determines the positive drive output voltage and VLx determines the negative turn−off voltage for each channels. This solution requires more power supplies than the conventional bootstrapped power supply example; however, it provides more flexibility when setting the positive, VHx, and negative, VLx, rail voltages.

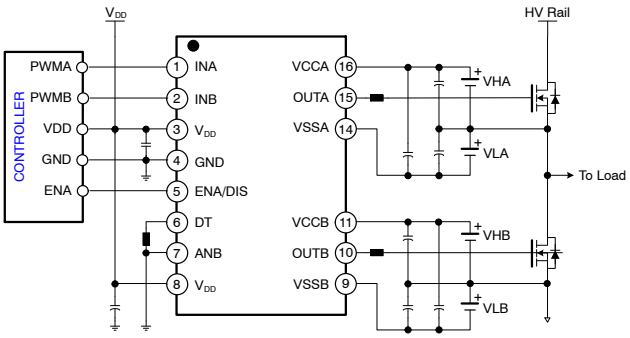



**Figure 63. Negative Bias with Two Isolated−Bias Power Supplies**

Figure 64 shows another example with negative bias turn−off on the gate driver using a Zener diode on an isolated power supply. The negative bias set by the voltage of Zener diode.

For example, if the isolated power supply, VHx for each channels, the turn−off voltage will be –5.1 V and turn−on voltage will be 20 V − 5.1 V ≈ 15 V.

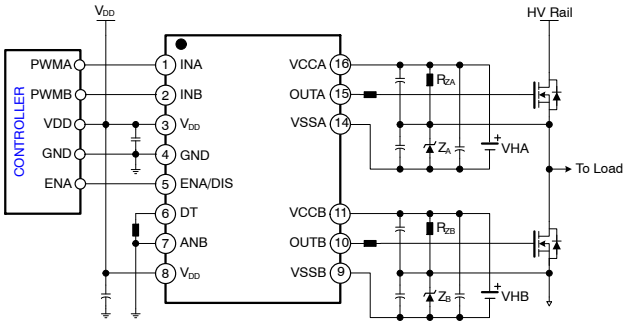



**Figure 64. Negative Bias with Zener Diode on Single Isolated−Bias Power Supply**

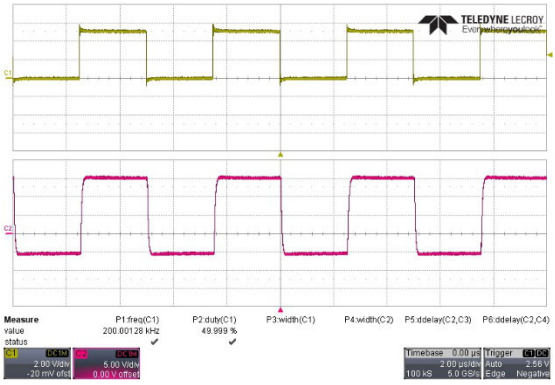
Moreover, this configuration could easily be changed negative bias by a using different Zener diode with the same 20 V isolated power supply. This configuration needs two isolated power supplies for a half−bridge configuration, but this scheme is very simple.

However, it has the disadvantage of having a steady state power consumption from $R_{Zx}$. Therefore, one should be careful in selecting the $R_{Zx}$ values. It is recommended that $R_{Zx}$ allow the minimal current flow to stabilize the Zener clamping voltage (e.g. $I_Z$: 5 mA~10 mA).

Typical recommended values are in the few kohm range (e.g. 1 kΩ~4.7 kΩ) of SiC MOSFETs application.

### Experimental Results

Figure 65 show the experimental results of the negative bias with Zener diode on single isolated power supply of the NCP51563 for SiC MOSFET gate drive application. The examples were design to have a +15 V and −5.1 V drive power supply referenced to the device source by using the 20 V isolated power supply.




CH1: INPUT [2 V/div], and CH2: OUTPUT [5 V/div]

**Figure 65. Experimental Waveforms of Negative Bias with Zener Diode on Single Isolated Power Supply**

## PCB LAYOUT GUIDELINE

To improve the switching characteristics and efficiency of design, the following should be considered before beginning a PCB layout.

*Component Placement*

- Keep the input/output traces as short as possible. Minimize influence of the parasitic inductance and capacitance on the layout. (To maintain low signal−path inductance, avoid using via.)
- Placement and routing for supply bypass capacitors for $V_{DD}$ and $V_{CCx}$, and gate resistors need to be located as close as possible to the gate driver.
- The gate driver should be located switching device as close as possible to decrease the trace inductance and avoid output ringing.

*Grounding Consideration*

- Have a solid ground plane underneath the high−speed signal layer.
- Have a solid ground plane next to $V_{SSA}$ and $V_{SSB}$ pins with multiple $V_{SSA}$ and $V_{SSB}$ vias to reduce the parasitic inductance and minimize the ringing on the output signals.

*High−Voltage ($V_{ISO}$) Consideration*

- To ensure isolation performance between the primary and secondary side, any PCB traces or copper should be not place under the driver device as shown in Figure 66. A PCB cutout is recommended in order to prevent contamination that may impair the isolation performance of NCP51563.

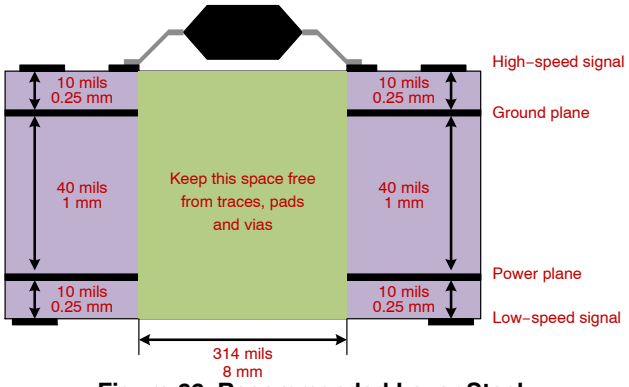
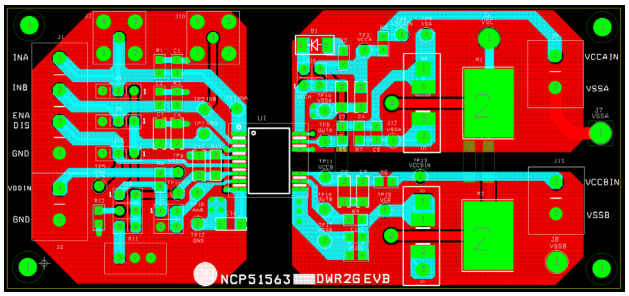
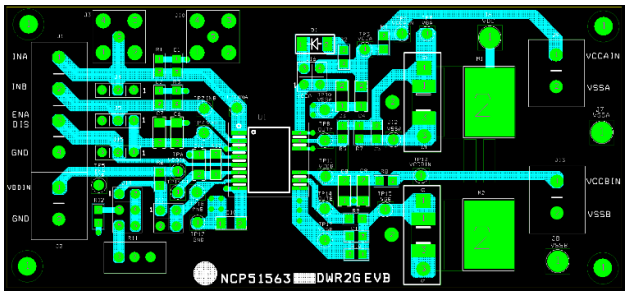



**Figure 66. Recommended Layer Stack**

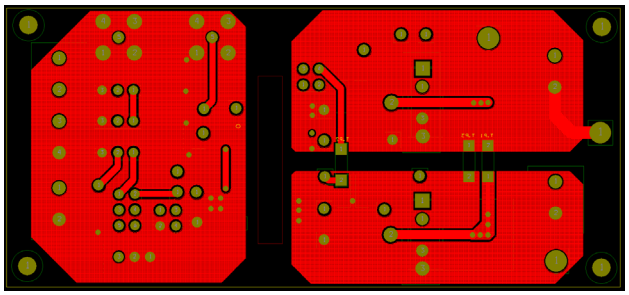
Figure 67 shows the printed circuit board layout of NCP51563 evaluation board.




(a) Top & Bottom View




(b) Top View



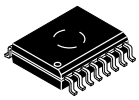
(c) Bottom View

**Figure 67. Printed Circuit Board**

## ORDERING INFORMATION

| Device | Description | Package | UVLO | ENA/DIS | Shipping† |
|---|---|---|---|---|---|
| NCP51563AADWR2G* | High current dual isolated MOS driver | SOIC−16 WB (Pb−Free) | 5 V | ENABLE | 1000 / Tape & Reel |
| NCP51563ABDWR2G* | | SOIC−16 WB (Pb−Free) | 5 V | DISABLE | 1000 / Tape & Reel |
| NCP51563BADWR2G* | | SOIC−16 WB (Pb−Free) | 8 V | ENABLE | 1000 / Tape & Reel |
| NCP51563BBDWR2G | | SOIC−16 WB (Pb−Free) | 8 V | DISABLE | 1000 / Tape & Reel |
| NCP51563CADWR2G | | SOIC−16 WB (Pb−Free) | 13 V | ENABLE | 1000 / Tape & Reel |
| NCP51563CBDWR2G* | | SOIC−16 WB (Pb−Free) | 13 V | DISABLE | 1000 / Tape & Reel |
| NCP51563DADWR2G* | | SOIC−16 WB (Pb−Free) | 17 V | ENABLE | 1000 / Tape & Reel |
| NCP51563DBDWR2G* | | SOIC−16 WB (Pb−Free) | 17 V | DISABLE | 1000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*Option on demand



1

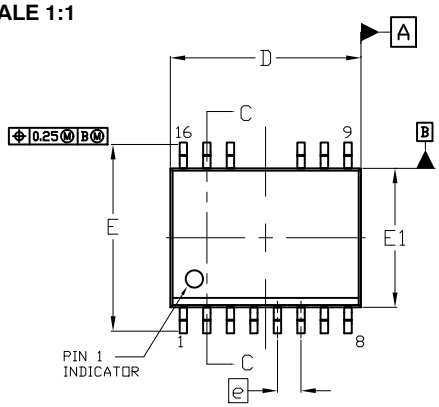
**SCALE 1:1**

## SOIC−16 WB LESS PINS 12 & 13

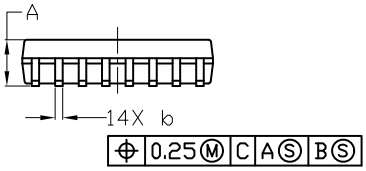
CASE 752AJ
ISSUE O

DATE 17 FEB 2021

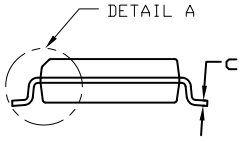
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.15 IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.15 mm PER SIDE.
5. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONS D AND E1 ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
6. DATUMS A AND B ARE TO BE DETERMINED AT DATUM H.
7. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 TO 0.25 FROM THE LEAD TIP.
8. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.




TOP VIEW

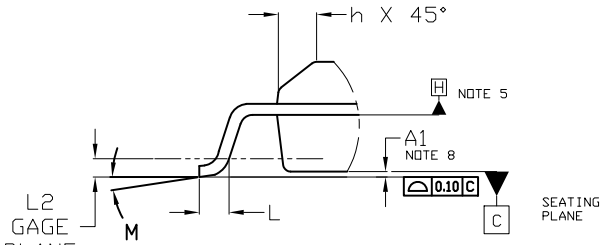



SIDE VIEW

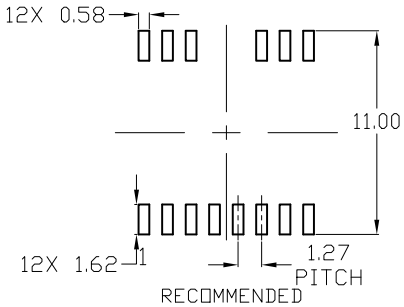



SECTION C-C

| DIM | MILLIMETERS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | 2.35 | 2.50 | 2.65 |
| A1 | 0.10 | 0.18 | 0.25 |
| b | 0.35 | 0.42 | 0.49 |
| c | 0.25 REF | | |
| D | 10.15 | 10.30 | 10.45 |
| E | 10.05 | 10.30 | 10.55 |
| E1 | 7.40 | 7.50 | 7.60 |
| e | 1.27 BSC | | |
| h | 0.25 | --- | 0.75 |
| L | 0.50 | --- | 0.90 |
| L2 | 0.25 REF | | |
| M | 0° | --- | 7° |



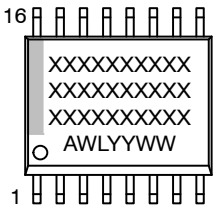

DETAIL A




RECOMMENDED
MOUNTING FOOTPRINT

* For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

### GENERIC
### MARKING DIAGRAM*




XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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