High Performance, Low Power, 169 MHz ISM Band, Radio Transceiver IC

Data Sheet **ADF7030**

FEATURES

- RF frequency range: 169.4 MHz to 169.6 MHz
- Modulation: 2 Gaussian frequency key shifting (GFSK), 4GFSK
- Data rates
  - 2GFSK: 2.4 kbps and 4.8 kbps
  - 4GFSK: 6.4 kbps (transmitter only)
- Low power consumption
  - 1 nA sleep current
- Receiver (Rx) performance
  - 97 dB blocking at ±10 MHz offset
  - 93 dB blocking at ±2 MHz offset
  - 66 dB adjacent channel rejection
  - −122.8 dBm sensitivity at BER = 0.1%
- Transmitter (Tx) performance
  - 2 power amplifier (PA) outputs
  - −20 dBm to +17 dBm output power range
  - 0.1 dB output power step resolution
  - Very low output power variation vs. temperature and supply
  - 61 mA Tx current at 17 dBm
- Accurate digital received signal strength indication (RSSI)
- Fast settling automatic frequency control (AFC) algorithm for very short preambles
- Autonomous automatic gain control (AGC) algorithm
- On-chip ARM Cortex-M0 processor performs the following functions:
  - Radio control
  - Radio calibration
  - Packet management
- Host microprocessor interface
  - Easy to use programming interface (SPI)
  - Configurable output and input interrupts
- Suitable for systems targeting compliance with ETSI EN 300 220
- 6 mm × 6 mm, 40-lead, standard lead LFCSP

APPLICATIONS

- Wireless M-Bus Mode N (EN 13757-4)
- Smart metering
- Social alarms
- Active tag asset tracking

GENERAL DESCRIPTION

The ADF7030 is a low power, high performance, integrated radio transceiver supporting narrow-band operation in the 169.4 MHz to 169.6 MHz ISM band. The ADF7030 supports transmit and receive operation at 2.4 kbps and 4.8 kbps using 2GFSK modulation and transmit operation at 6.4 kbps using 4GFSK modulation.

The ADF7030 features an on-chip ARM® Cortex®-M0 processor that performs radio control and calibration, as well as packet management.

FUNCTIONAL BLOCK DIAGRAM

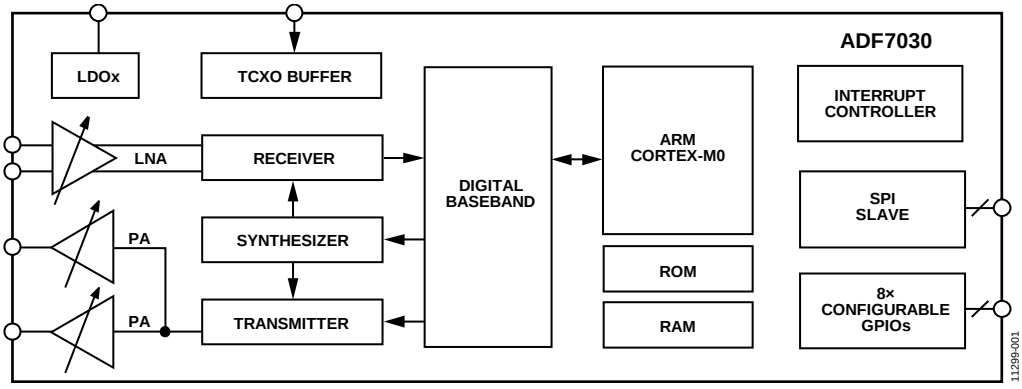

Figure 1.

Rev. 0 Document Feedback

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REVISION HISTORY

7/15—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = VBAT1 = VBAT2 = VBAT3 = VBAT4 = VBAT5 = VBAT6 = 2.2 V to 3.6 V, exposed pad (EPAD) = 0 V (ground), T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical specifications are at V_{DD} = 3 V, T_A = 25°C, unless otherwise noted. All VBATx pins must be tied together.

GENERAL SPECIFICATIONS

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
TEMPERATURE RANGE, T_A	−40		+85	°C	
VOLTAGE SUPPLY					All VBATx pins must be tied together
Maximum Output Power					
13 dBm	2.2		3.6	V	
17 dBm	2.8		3.6	V	
RF FREQUENCY					
Frequency Range	169.4		169.6	MHz	
Channel Frequency Resolution		1		Hz	
REFERENCE INPUT					DC-coupled external TCXO into HFXTALN pin, clipped sine wave
Frequency		26		MHz	
Peak-to-Peak Voltage Level	0.8		1.8	V	
Voltage Level with Respect to Ground	−0.1		+1.9	V	
Duty Cycle	40		60	%	
DATA RATE					
2GFSK		2.4		kbps	
2GFSK		4.8		kbps	
4GFSK		6.4		kbps	Tx only
FREQUENCY DEVIATION					
2GFSK		2.4		kHz	
4GFSK		3.2		kHz	Tx only
GAUSSIAN FILTER BANDWIDTH TIME (BT) PRODUCT		0.5			

TRANSMITTER SPECIFICATIONS

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER AMPLIFIERS (PAs)					
PA1					
Transmit Power					
Maximum		13		dBm	
Minimum		−20		dBm	
Transmit Power Step Resolution		0.1		dB	
Transmit Power Variation vs. Temperature					From −40°C to +85°C
13 dBm		±0.15		dB	
−10 dBm		±0.3		dB	
Transmit Power Variation vs. V_{DD}					From V_{DD} = 2.2 V to V_{DD} = 3.6 V
13 dBm		±0.1		dB	
−10 dBm		±0.1		dB	
Transmit Power Accuracy					
13 dBm		±0.3		dB	
−10 dBm		±0.9		dB	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
PA2					
Transmit Power					
Maximum					The maximum output power level achievable on PA2 depends on the programmable PA LDO setting
2.8 V ≤ V_{DD} ≤ 3.6 V		17		dBm	
2.2 V ≤ V_{DD} ≤ 3.6 V		13		dBm	
Minimum		−20		dBm	
Step Resolution		0.1		dB	
Transmit Power Variation vs. Temperature		±0.1		dB	From −40°C to +85°C, transmit power = 17 dBm
Transmit Power Variation vs. V_{DD}		±0.1		dB	From V_{DD} = 3.0 V to V_{DD} = 3.6 V, transmit power = 17 dBm
Transmit Power Accuracy		±0.25		dB	Transmit power = 17 dBm
ADJACENT CHANNEL POWER (ACP)					Measured according to ETSI EN 300 220-1 V2.4.1; 12.5 kHz channel spacing; spectrum analyzer settings: measurement bandwidth (BW) = 8.5 kHz, resolution bandwidth (RBW) = 100 Hz, video bandwidth (VBW) = 300 Hz
2.4 kbps					2GFSK, frequency deviation = 2.4 kHz, PA1, output power = 13 dBm
Adjacent Channel		−81		dBc	
Alternate Channel		−81		dBc	
4.8 kbps					2GFSK, frequency deviation = 2.4 kHz, PA2, output power = 17 dBm
Adjacent Channel		−59		dBc	
Alternate Channel		−77		dBc	
6.4 kbps					4GFSK, frequency deviation = 3.2 kHz, PA1, output power = 13 dBm
Adjacent Channel		−68		dBc	
Alternate Channel		−79		dBc	
OCCUPIED BANDWIDTH					Occupied bandwidth is the bandwidth containing 99% of the total integrated power; spectrum analyzer settings: measurement BW = 8.5 kHz, RBW = 100 Hz, VBW = 300 Hz
2.4 kbps		6.3		kHz	2GFSK, frequency deviation = 2.4 kHz, PA1, output power = 13 dBm
4.8 kbps		7.8		kHz	2GFSK, frequency deviation = 2.4 kHz, PA2, output power = 17 dBm
6.4 kbps		8.1		kHz	4GFSK, frequency deviation = 3.2 kHz, PA1, output power = 13 dBm
MAXIMUM SPURIOUS EMISSIONS (EXCLUDING HARMONICS)					Measured according to ETSI EN 300 220-1 V2.4.1 on the ADF7030 evaluation board; transmitting continuous PN9 data on PA1 at 13 dBm
47 MHz to 74 MHz		−84		dBc	
74 MHz to 87.5 MHz		<−87		dBc	
87.5 MHz to 118 MHz		−87		dBc	
118 MHz to 168.5 MHz		−79		dBc	
168.5 MHz to 170.5 MHz		−69		dBc	Excluding frequency range $f_{CHANNEL}$ ± 31.25 kHz
170.5 MHz to 174 MHz		−80		dBc	
174 MHz to 230 MHz		−84		dBc	
230 MHz to 470 MHz		−82		dBc	
470 MHz to 862 MHz		−84		dBc	
862 MHz to 1 GHz		<−87		dBc	
1 GHz to 4 GHz		<−87		dBc	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
MAXIMUM HARMONIC EMISSIONS					Measured conductively at antenna input, according to ETSI EN 300 220-1 V2.4.1 on the ADF7030 evaluation board; transmitting continuous PN9 data
17 dBm Output Power					PA2
Second Harmonic		−74		dBc	
Third Harmonic		−86		dBc	
Fourth Harmonic		−90		dBc	
All Other Harmonics		<−90		dBc	
13 dBm Output Power					PA1
Second Harmonic		−73		dBc	
Third Harmonic		−82		dBc	
Fourth Harmonic		−90		dBc	
All Other Harmonics		<−90		dBc	
OPTIMUM PA LOAD IMPEDANCE					
PA1		47 + j10		Ω	
PA2		38 + j10		Ω	

RECEIVER SPECIFICATIONS

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SENSITIVITY, BIT ERROR ATE (BER)					At BER = 0.1%, AFC disabled, 2GFSK frequency deviation = 2.4 kHz
2.4 kbps		−122.8		dBm	
4.8 kbps		−121.4		dBm	
SENSITIVITY, PACKET ERROR RATE (PER)					At PER = 5%, preamble length = 2 bytes, sync word = 0xF672, payload length = 24 bytes, data rate error tolerance = ±400 ppm, RF frequency error range = ±2 kHz, AFC enabled, 2GFSK frequency deviation = 2.4 kHz
2.4 kbps		−121.2		dBm	
4.8 kbps		−119.5		dBm	
CHANNEL SELECTIVITY AND BLOCKING					
BER-Based Test Method					Desired signal 3 dB above the input sensitivity level (BER = 0.1%), carrier wave (CW) interferer power level increased until BER = 0.1%, image calibrated, 12.5 kHz channel spacing, 2GFSK frequency deviation = 2.4 kHz
2.4 kbps					
Adjacent Channel (±12.5 kHz)		66		dB	
Alternate Channel (±25 kHz)		70		dB	
±2 MHz		93		dB	
±10 MHz		97		dB	
4.8 kbps					
Adjacent Channel (±12.5 kHz)		63		dB	
Alternate Channel (±25 kHz)		69		dB	
±2 MHz		93		dB	
±10 MHz		96		dB	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
PER-Based Test Method					Desired signal 3 dB above the input sensitivity level (PER = 5%), CW interferer power level increased until PER = 5%, image calibrated, AFC enabled, preamble length = 2 bytes, sync word = 0xF672, payload length = 24 bytes, 12.5 kHz channel spacing, 2GFSK frequency deviation = 2.4 kHz
2.4 kbps					
Adjacent Channel (±12.5 kHz)		62		dB	
Alternate Channel (±25 kHz)		70		dB	
±2 MHz		93		dB	
±10 MHz		96		dB	
4.8 kbps					
Adjacent Channel (±12.5 kHz)		55		dB	
Alternate Channel (±25 kHz)		69		dB	
±2 MHz		91		dB	
±10 MHz		95		dB	
ETSI EN 300 220-1 V2.4.1 Test Method					Measured as per EN 300 220-1 V2.4.1, image calibrated, AFC disabled, 12.5 kHz channel spacing, 2GFSK frequency deviation = 2.4 kHz
2.4 kbps					Wanted signal level = −106.7 dBm (3 dB above the reference sensitivity level), receiver bandwidth = 8.7 kHz
±2 MHz		−18		dBm	
±10 MHz		−14		dBm	
4.8 kbps					Wanted signal level = −105.8 dBm (3 dB above the reference sensitivity level), receiver bandwidth = 10.6 kHz
±2 MHz		−18		dBm	
±10 MHz		−14		dBm	
CO-CHANNEL REJECTION					
PER-Based Test Method					Desired signal 3 dB above the input sensitivity level (PER = 5%), CW interferer power level increased until PER = 5%, AFC enabled, preamble length = 2 bytes, sync word = 0xF672, payload length = 24 bytes, 2GFSK frequency deviation = 2.4 kHz
2.4 kbps		−10		dB	
4.8 kbps		−10		dB	
BER-Based Test Method					Desired signal 3 dB above the input sensitivity level (BER = 0.1%), CW interferer power level increased until BER = 0.1%, AFC disabled, 2GFSK frequency deviation = 2.4 kHz
2.4 kbps		−8		dB	
4.8 kbps		−9		dB	
IMAGE REJECTION		55		dB	Desired signal 3 dB above the input sensitivity level (PER = 5%), CW interferer power level increased until PER = 5%, AFC enabled, preamble length = 2 bytes, sync word = 0xF672, payload length = 24 bytes, 2GFSK frequency deviation = 2.4 kHz
RECEIVER LINEARITY					Measured at maximum receiver gain
Input Third-Order Intercept (IP3)		−8.5		dBm	Receiver channel frequency = 169.43125 MHz, $f_{SOURCE1}$ = 171.35 MHz, $f_{SOURCE2}$ = 173.26875 MHz
Input Second-Order Intercept (IP2)		53		dBm	Receiver channel frequency = 169.53125 MHz, $f_{SOURCE1}$ = 171.55 MHz, $f_{SOURCE2}$ = 171.63125 MHz
1 dB Compression Point (P1dB)		−18.7		dBm	Receiver channel frequency = 169.43125 MHz, $f_{SOURCE1}$ = 171.43125 MHz

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
RSSI					
Resolution		0.25		dB	
Absolute Accuracy		±2		dB	RSSI range = −110 dBm to −12 dBm with one point calibration at −70 dBm and result averaged over 20 RSSI measurements
MAXIMUM RF INPUT LEVEL		10		dBm	
DIFFERNTIAL LNA INPUT IMPEDANCE		78 + j17.7		Ω	
Rx SPURIOUS EMISSIONS					Measured conductively at antenna input, according to ETSI EN 300 220-1 V2.4.1 on the ADF7030 evaluation board
<1 GHz		<−63		dBm	
1 GHz to 4 GHz		−50		dBm	

CURRENT CONSUMPTION SPECIFICATIONS

Table 4.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
TRANSMIT CURRENT CONSUMPTION					In the PHY_TX state
10 dBm		35.5		mA	PA1
13 dBm		44		mA	PA1
17 dBm		61		mA	PA2
RECEIVE CURRENT CONSUMPTION		26		mA	In the PHY_RX state, waiting for preamble
LOW POWER MODE					
Deep Sleep		1		nA	No memory retained

DIGITAL INPUT/OUTPUT SPECIFICATIONS

Table 5.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
LOGIC INPUTS						
Input Voltage						
High	V_{INH}	$0.7 \times V_{DD}$			V	
Low	V_{INL}			$0.2 \times V_{DD}$	V	
Input Capacitance	C_{IN}		3.6		pF	
LOGIC OUTPUTS						
Output Voltage						
High	V_{OH}	$V_{DD} - 0.4$			V	I_{OH} = 500 µA
Low	V_{OL}			0.4	V	I_{OL} = 500 µA

DIGITAL TIMING SPECIFICATIONS

V_{DD} = VBAT1 = VBAT2 = VBAT3 = VBAT4 = VBAT5 = VBAT6 = 2.2 V to 3.6 V. EPAD = 0 V (ground), $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.

Table 6. SPI Interface Timing

Parameter	Description	Min	Typ	Max	Unit
t_1	Falling edge to MISO setup time			15	ns
t_2	$\overline{CS}$ low to SCLK setup time	40			ns
t_3	SCLK high time	40			ns
t_4	SCLK low time	40			ns
t_5	SCLK period	80			ns
t_6	SCLK falling edge to MISO delay			10	ns
t_7	MOSI to SCLK rising edge setup time	5			ns
t_8	MOSI to SCLK rising edge hold time	5			ns
t_9	SCLK falling edge to $\overline{CS}$ hold time	40			ns
t_{10}	$\overline{CS}$ high time	80			ns
t_{11}	$\overline{CS}$ low to MISO high wake-up time		92		µs
t_{12}	MISO high to SCLK setup time	SCLK low time			µs

Timing Diagrams

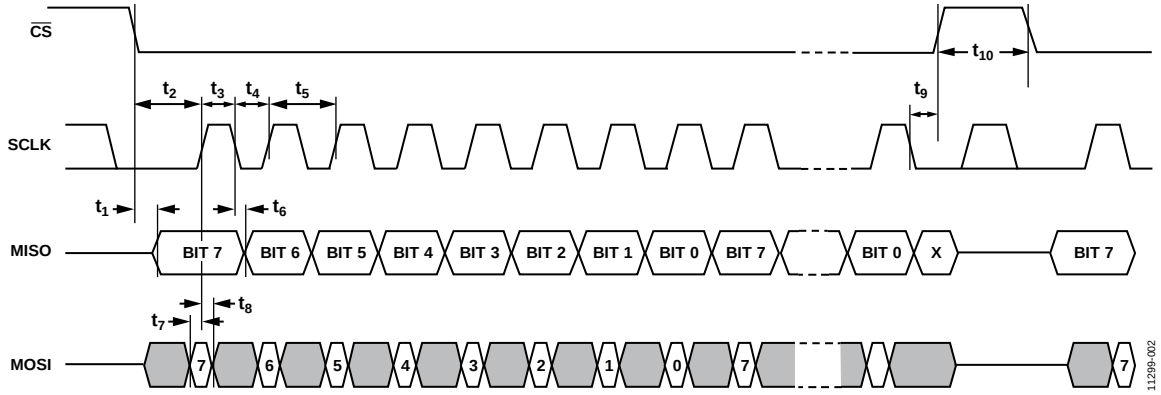

Figure 2. SPI Interface Timing

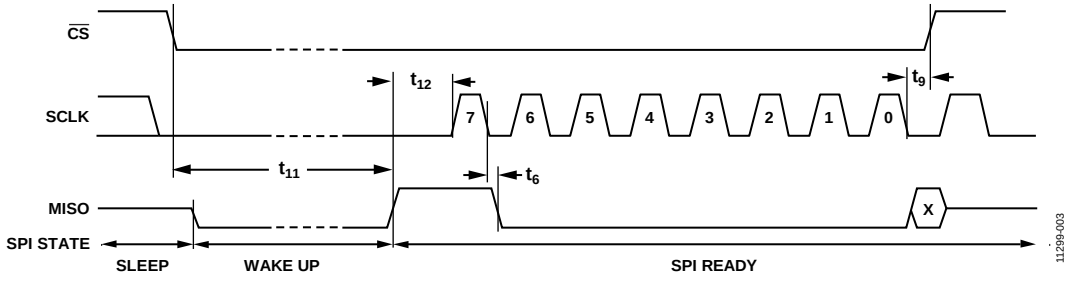

Figure 3. PHY_SLEEP to SPI Ready State Timing

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted. All VBATx pins must be tied together. The LNAIN1 and LNAIN2 inputs must be ac-coupled.

Table 7.

Parameter	Rating
Supply Pins	
VBAT1, VBAT2, VBAT3, VBAT4, VBAT5, VBAT6 to Ground	−0.3 V to +3.9 V
LNAIN1, LNAIN2	−0.3 V to +1.98 V
PAOUT1, PAOUT2	−0.3 V to +3.9 V
HFXTALP, HFXTALN	−0.3 V to +1.98 V
CLF	−0.3 V to +1.98 V
CREG1, CREG2, CREG4, CREG5, CREG6, CREG7	−0.3 V to +1.98 V
CREG3	−0.3 V to +3.9 V
Digital Inputs/Outputs, GPIOx	−0.3 V to +3.9 V
MOSI, MISO, SCLK, $\overline{CS}$, $\overline{RST}$	−0.3 V to +3.9 V
Industrial Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +125°C
Maximum Junction Temperature	150°C
θ_{JA} Thermal Impedance	26°C/W
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature	40 sec

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Connect the exposed pad of the device to ground.

This device is a high performance, RF integrated circuit with an ESD rating of <2 kV; it is ESD sensitive. Take proper precautions for handling and assembly.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

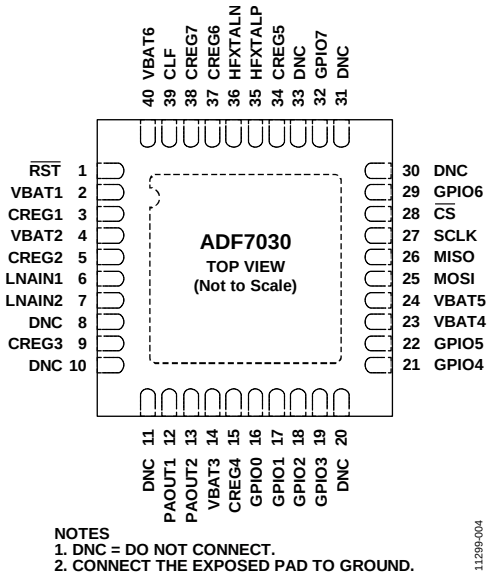

Figure 4. Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$\overline{\text{RST}}$	External Reset, Active Low.
2	VBAT1	Power Supply Pin 1 to the Internal Regulators.
3	CREG1	Regulator Output 1. Place a 220 nF capacitor between this pin and ground for regulator stability and noise rejection. Also, place a 1.2 nF capacitor between this pin and the CLF pin.
4	VBAT2	Power Supply Pin 2 to the Internal Regulators.
5	CREG2	Regulator Output 2. Place a 220 nF capacitor between this pin and ground for regulator stability and noise rejection.
6	LNAIN1	LNA Input 1.
7	LNAIN2	LNA Input 2.
8	DNC	Do Not Connect. Do not connect to this pin.
9	CREG3	Regulator Output 3. Connect to the PA choke inductor to provide bias to the PA. Place a 220 nF capacitor between this pin and ground for regulator stability and noise rejection.
10	DNC	Do Not Connect. Do not connect to this pin.
11	DNC	Do Not Connect. Do not connect to this pin.
12	PAOUT1	Single-Ended PA1 Output.
13	PAOUT2	Single-Ended PA2 Output.
14	VBAT3	Power Supply Pin 3 to the Internal Regulators.
15	CREG4	Regulator Output 4. Place a 220 nF capacitor between this pin and ground for regulator stability and noise rejection.
16	GPIO0	Digital General-Purpose Input/Output (GPIO) Pin 0.
17	GPIO1	Digital GPIO Pin 1.
18	GPIO2	Digital GPIO Pin 2.
19	GPIO3	Digital GPIO Pin 3.
20	DNC	Do Not Connect. Do not connect to this pin.
21	GPIO4	Digital GPIO Pin 4.
22	GPIO5	Digital GPIO Pin 5.
23	VBAT4	Power Supply Pin 4 to the Internal Regulators.
24	VBAT5	Power Supply Pin 5 to the Internal Regulators.
25	MOSI	Serial Port Master Out/Slave In.
26	MISO	Serial Port Master In/Slave Out.
27	SCLK	Serial Port Clock.
28	$\overline{\text{CS}}$	Chip Select (Active Low). A pull-up resistor of 100 kΩ to V_{DD} is recommended to prevent the host processor from inadvertently waking the ADF7030 from sleep.

Pin No.	Mnemonic	Description
29	GPIO6	Digital GPIO Pin 6
30	DNC	Do Not Connect. Do not connect to this pin.
31	DNC	Do Not Connect. Do not connect to this pin.
32	GPIO7	Digital GPIO Pin 7.
33	DNC	Do Not Connect. Do not connect to this pin.
34	CREG5	Regulator Output 5. Place a 220 nF capacitor between this pin and ground for regulator stability and noise rejection.
35	HFXTALP	Do Not Connect. Do not connect to this pin.
36	HFXTALN	Reference Input. Connect this pin to an external 26 MHz reference (typically a TCXO).
37	CREG6	Regulator Output 6. Place a 220 nF capacitor between this pin and ground for regulator stability and noise rejection.
38	CREG7	Regulator Output 7. Place a 220 nF capacitor between this pin and ground for regulator stability and noise rejection.
39	CLF	External Loop Filter Capacitor to CREG1. Place a 1.2 nF capacitor between this pin and the CREG1 pin.
40	VBAT6	Power Supply Pin 6 to the Internal Regulators.
	EPAD	Exposed Pad. Connect the exposed pad to ground.

TYPICAL PERFORMANCE CHARACTERISTICS

RECEIVER

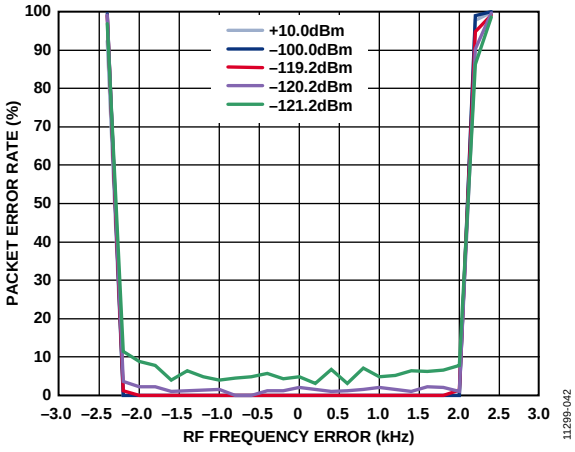

Figure 5. Packet Error Rate vs. RF Frequency Error and RF Input Power, Data Rate = 2.4 kbps, AFC Enabled, V_{DD} = 3.0 V, T_A = 25°C

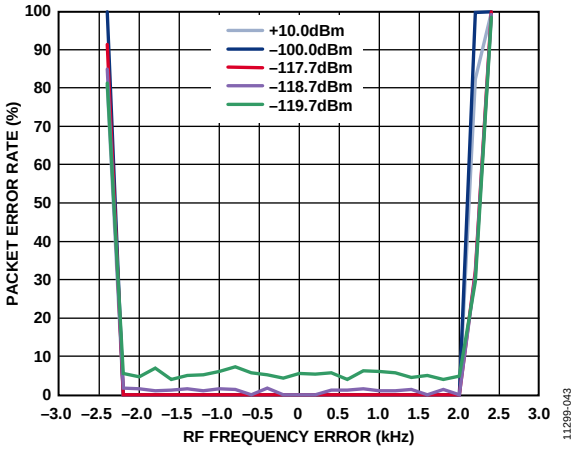

Figure 6. Packet Error Rate vs. RF Frequency Error and RF Input Power, Data Rate = 4.8 kbps, AFC Enabled, V_{DD} = 3.0 V, T_A = 25°C

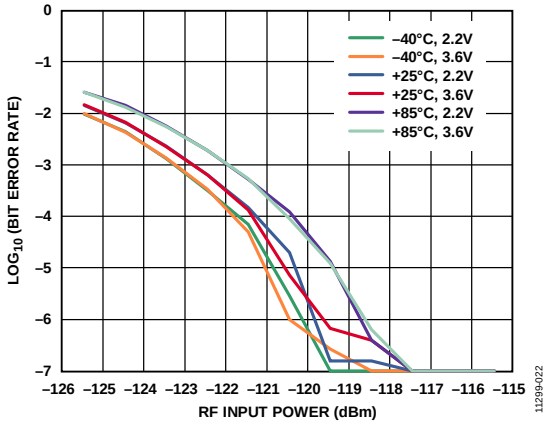

Figure 7. Log_{10} (Bit Error Rate) vs. RF Input Power, Temperature, and V_{DD}, Data Rate = 2.4 kbps, AFC Disabled

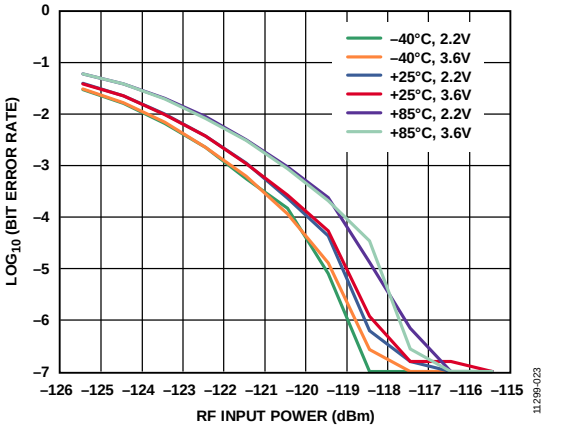

Figure 8. Log_{10} (Bit Error Rate) vs. RF Input Power, Temperature, and V_{DD}, Data Rate = 4.8 kbps, AFC Disabled

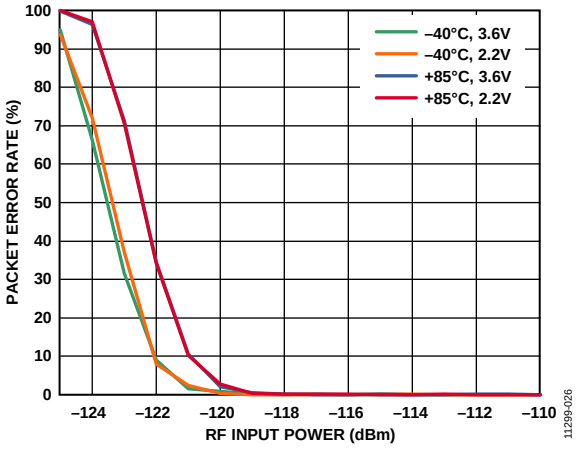

Figure 9. Packet Error Rate vs. RF Input Power, Temperature, and V_{DD}, Data Rate = 2.4 kbps

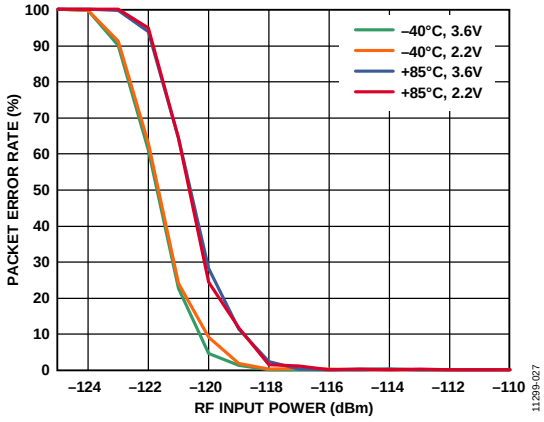

Figure 10. Packet Error Rate vs. RF Input Power, Temperature, and V_{DD}, Data Rate = 4.8 kbps

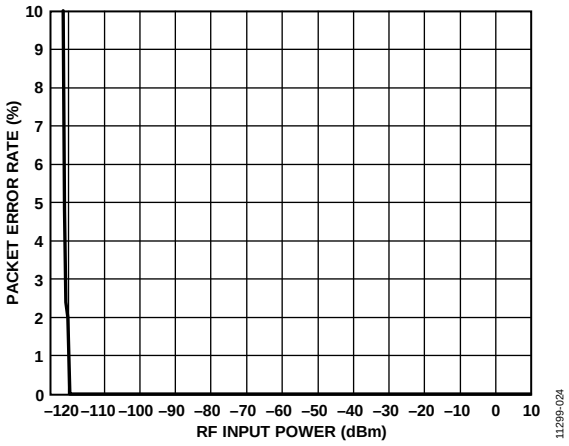

Figure 11. Packet Error Rate vs. RF Input Power, Data Rate = 2.4 kbps, V_{DD} = 3.0 V, T_A = 25°C

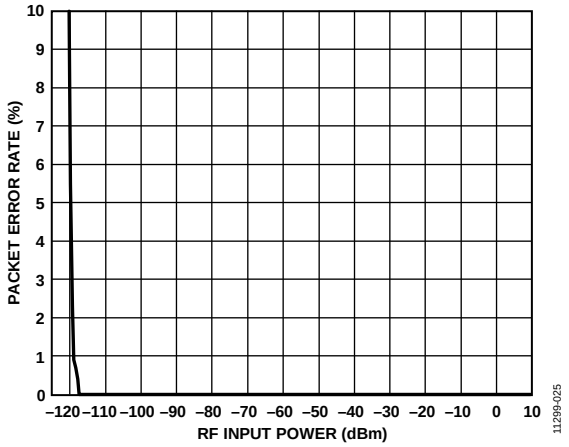

Figure 12. Packet Error Rate vs. RF Input Power, Data Rate = 4.8 kbps, V_{DD} = 3.0 V, T_A = 25°C

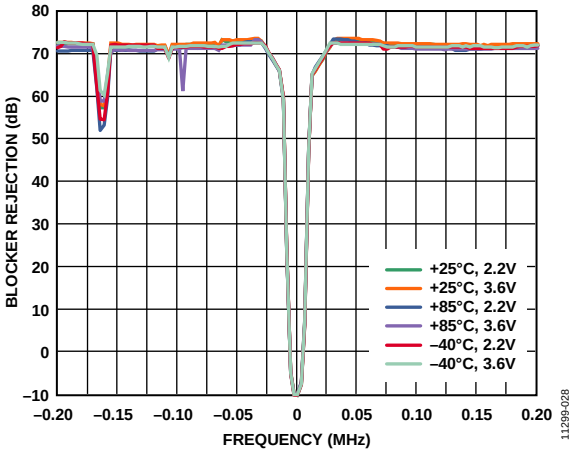

Figure 13. Receiver Close-In Blocking vs. Temperature and V_{DD}, Data Rate = 2.4 kbps, CW Interferer, Wanted Signal 3 dB Above the Sensitivity Level of PER = 5%, PER-Based Test

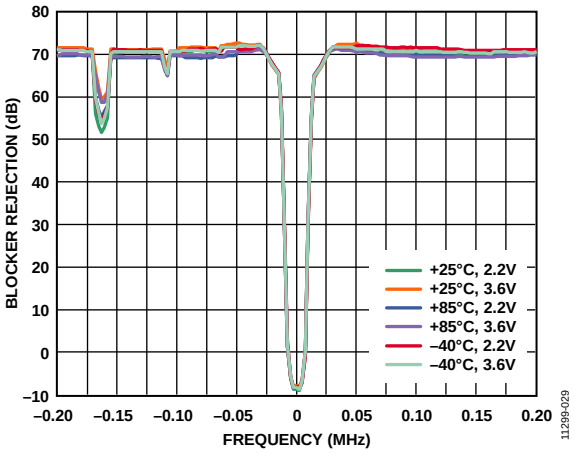

Figure 14. Receiver Close-In Blocking vs. Temperature and V_{DD}, Data Rate = 4.8 kbps, CW Interferer, Wanted Signal 3 dB Above the Sensitivity Level of PER = 5%, PER-Based Test

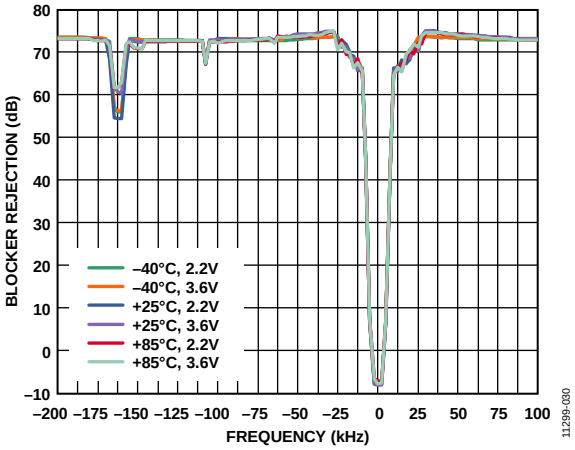

Figure 15. Receiver Close-In Blocking vs. Temperature and V_{DD}, Data Rate = 2.4 kbps, CW Interferer, Wanted Signal 3 dB Above the Sensitivity Level of BER = 0.1%, BER-Based Test

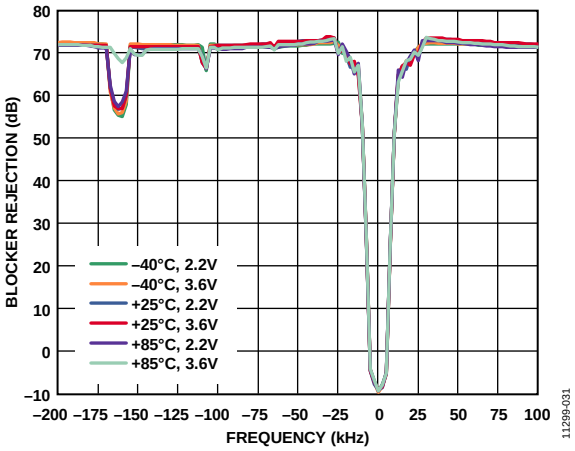

Figure 16. Receiver Close-In Blocking vs. Temperature and V_{DD}, Data Rate = 4.8 kbps, CW Interferer, Wanted Signal 3 dB Above the Sensitivity Level of BER = 0.1%, BER-Based Test

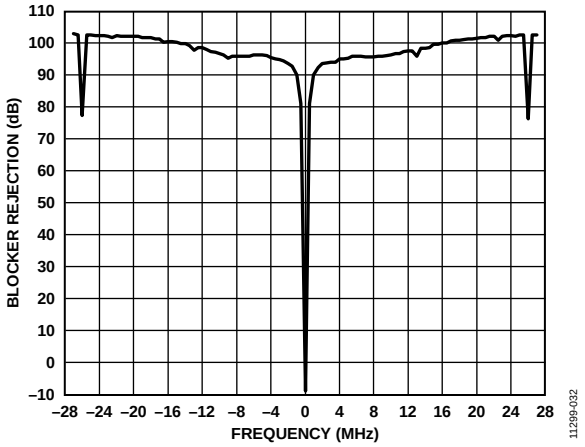

Figure 17. Receiver Wideband Blocking, T_A = 25°C, V_{DD} = 3.6 V, Data Rate = 2.4 kbps, CW Interferer, Wanted Signal 3 dB Above the Sensitivity Level of PER = 5%, PER-Based Test

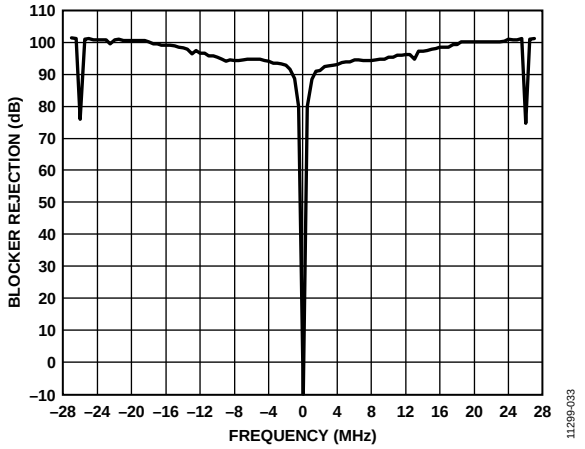

Figure 18. Receiver Wideband Blocking, T_A = 25°C, V_{DD} = 3.0 V, Data Rate = 4.8 kbps, CW Interferer, Wanted Signal 3 dB Above the Sensitivity Level of PER = 5%, PER-Based Test

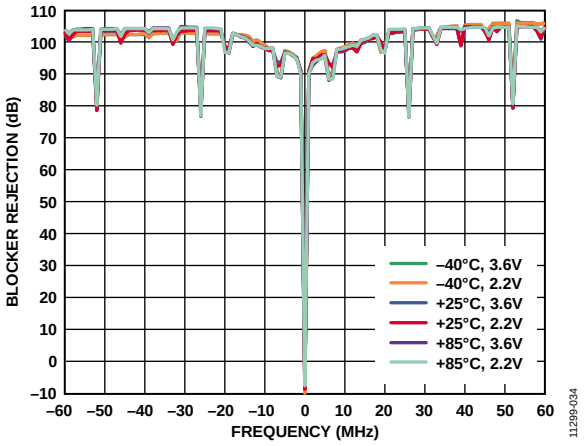

Figure 19. Receiver Wideband Blocking vs. Temperature and V_{DD}, Data Rate = 2.4 kbps, CW Interferer, Wanted Signal 3 dB Above the Sensitivity Level of BER = 0.1%, BER-Based Test

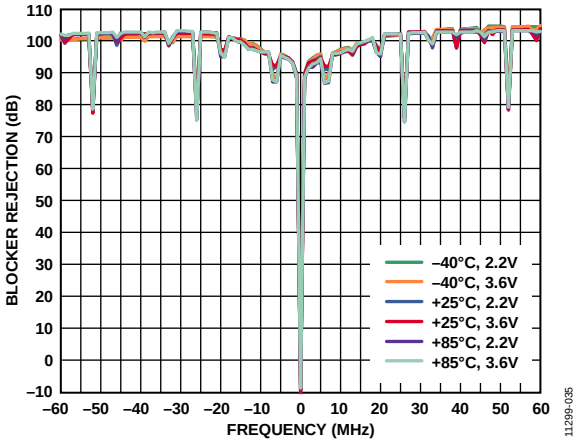

Figure 20. Receiver Wideband Blocking vs. Temperature and V_{DD}, Data Rate = 4.8 kbps, CW Interferer, Wanted Signal 3 dB Above the Sensitivity Level of BER = 0.1%, BER-Based Test

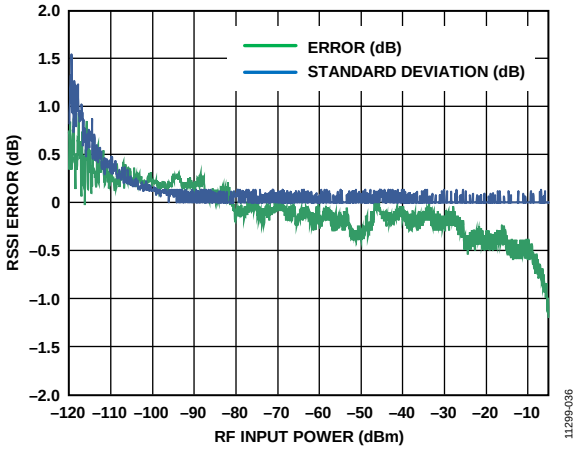

Figure 21. RSSI Error vs. RF Input Power with One-Point Calibration at –70 dBm, V_{DD} = 2.2 V, T_A = 25°C (Error is Based on the Mean of 20 RSSI Measurements)

TRANSMITTER

PA_COARSE is a programmable value that provides a coarse adjustment of the PA output power. This value can be programmed in the range of 1 to 6 for PA1, and from 1 to 10 for PA2. PA_FINE is a programmable value that provides a fine adjustment of the PA output power. This value can be programmed in the range of 2 to 127 for both PA1 and PA2. PA_MICRO is a programmable value that provides a microadjustment (typically <0.1 dB) of the PA output power. This value can be programmed in the range of 1 to 31 for both PA1 and PA2.

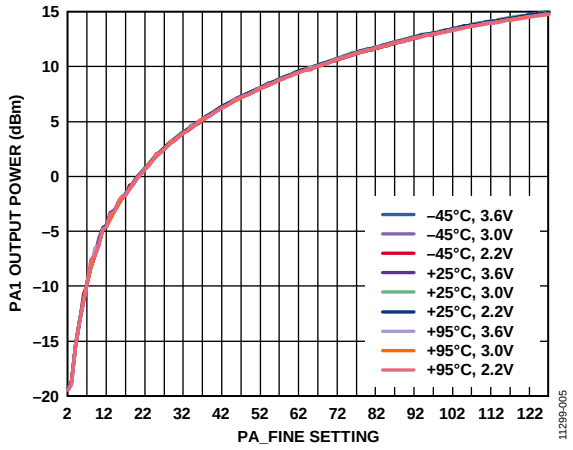

Figure 22. PA1 Output Power vs. PA_FINE Setting, Temperature, and V_{DD} with PA_COARSE = 6, Maximum Recommended Temperature = 85°C, Minimum Recommended Temperature = −40°C; −45°C and +95°C Operation Only Shown for Robustness

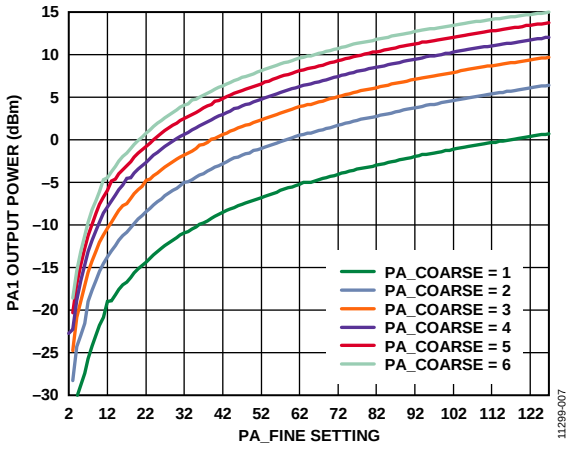

Figure 24. PA1 Output Power vs. PA_FINE Setting and PA_COARSE Setting, V_{DD} =3.0 V, T_A = 25°C

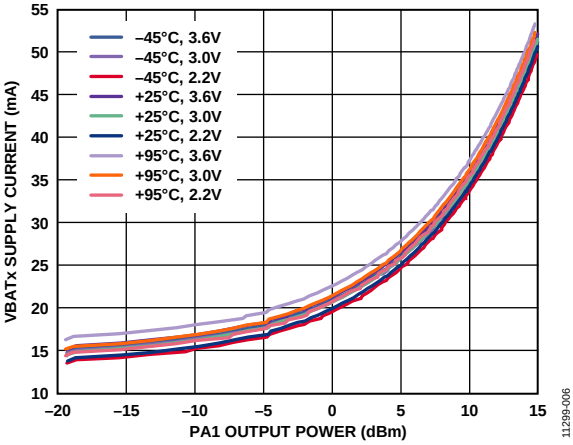

Figure 23. VBATx Supply Current vs. PA1 Output Power, Temperature, and V_{DD} with PA_COARSE = 6, Maximum Recommended Temperature = 85°C, Minimum Recommended Temperature = −40°C; −45°C and +95°C Operation Only Shown for Robustness

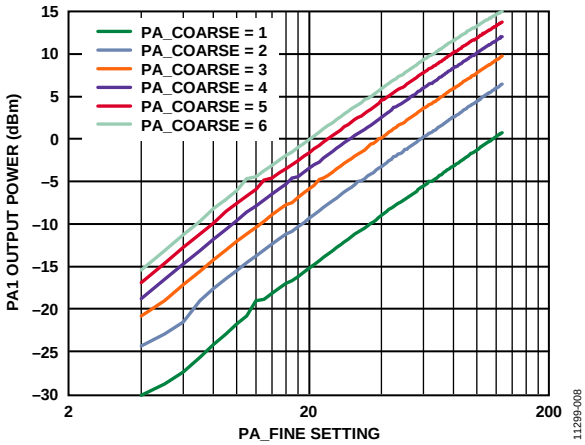

Figure 25. PA1 Output Power vs. PA_FINE Setting and PA_COARSE Setting with PA_FINE on a Logarithmic Scale, V_{DD} = 3.0 V, T_A = 25°C

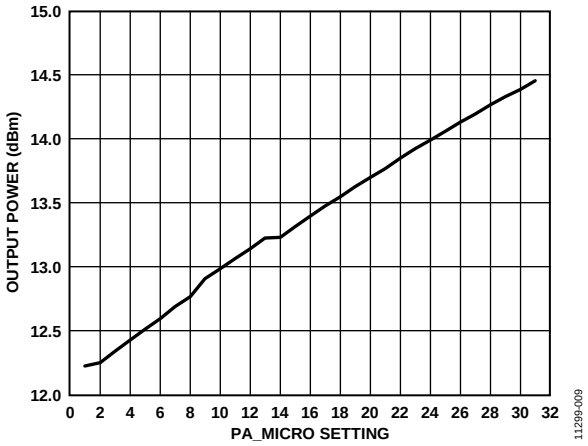

Figure 26. Microadjustment of the PA1 Output Power Using a PA_MICRO Setting Around 13 dBm with PA_COARSE = 6 and PA_FINE = 100, V_{DD} = 3.0 V, T_A = 25°C

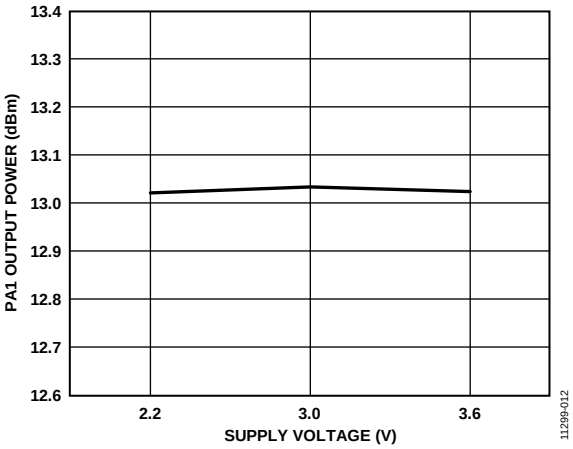

Figure 29. PA1 Output Power vs. Supply Voltage (V_{DD}), PA_COARSE = 6, PA_FINE = 97, PA_MICRO = 16, T_A = 25°C

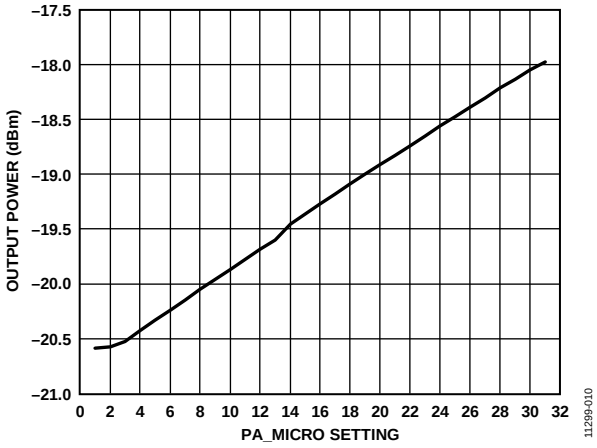

Figure 27. Microadjustment of the PA1 Output Power Using a PA_MICRO Setting Around −20 dBm with PA_COARSE = 6 and PA_FINE = 2, V_{DD} = 3.0 V, T_A = 25°C

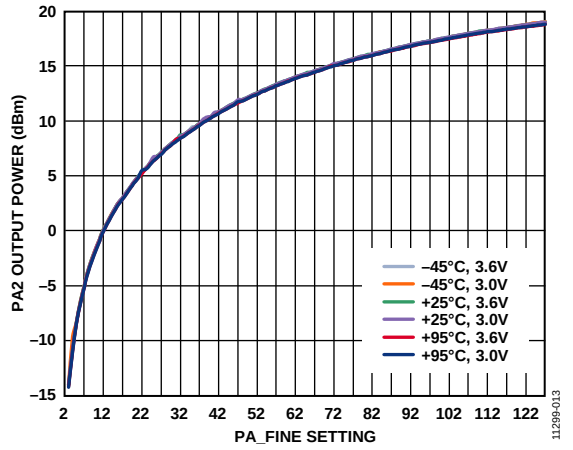

Figure 30. PA2 Output Power vs. PA_FINE Setting, Temperature, and V_{DD}, PA_COARSE = 6, Maximum Recommended Temperature = 85°C, Minimum Recommended Temperature = −40°C; −45°C and +95°C Operation Only Shown for Robustness

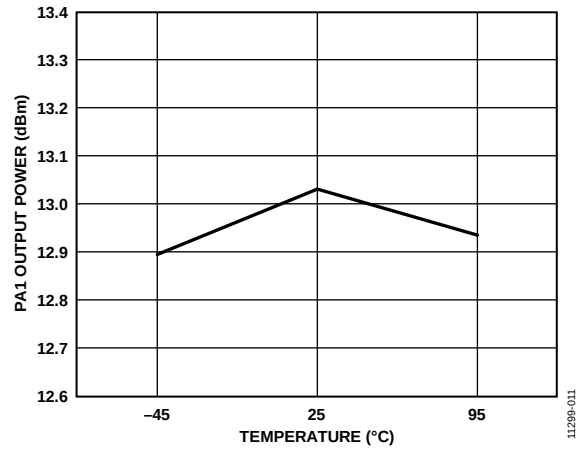

Figure 28. PA1 Output Power vs. Temperature, PA_COARSE = 6, PA_FINE = 97, PA_MICRO = 16, Maximum Recommended Temperature = 85°C, Minimum Recommended Temperature = −40°C; −45°C and +95°C Operation Only Shown for Robustness

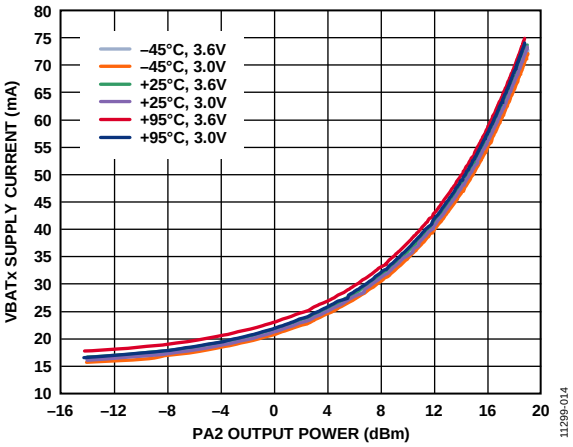

Figure 31. VBATx Supply Current vs. PA2 Output Power, Temperature, and V_{DD}, PA_COARSE = 10, Maximum Recommended Temperature = 85°C, Minimum Recommended Temperature = −40°C; −45°C and +95°C Operation Only Shown for Robustness

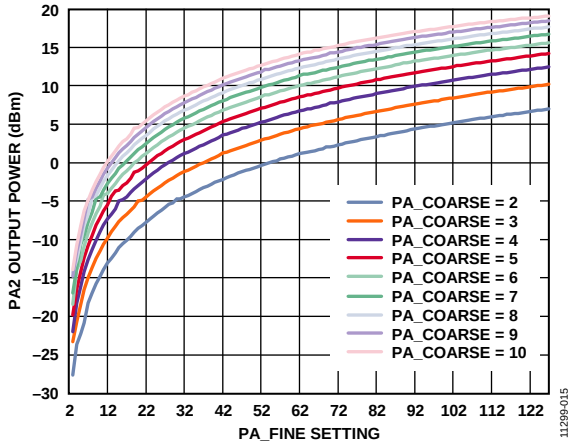

Figure 32. PA2 Output Power vs. PA_FINE Setting and PA_COARSE Setting, V_{DD} = 3.0 V, T_A = 25°C

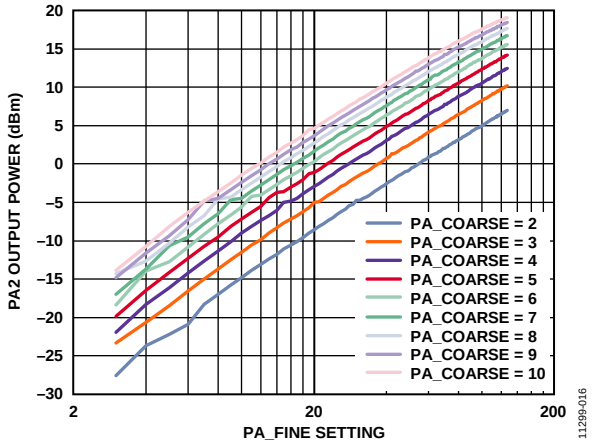

Figure 33. PA2 Output Power vs. PA_FINE Setting and PA_COARSE Setting with PA_FINE on a Logarithmic Scale, V_{DD} = 3.0 V, T_A = 25°C

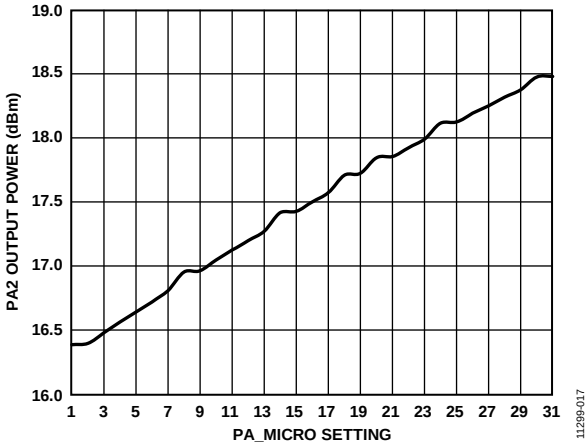

Figure 34. Microadjustment of the PA2 Output Power Using a PA_MICRO Setting Around 17 dBm, PA_COARSE = 10, PA_FINE = 100, V_{DD} = 3.0 V, T_A = 25°C

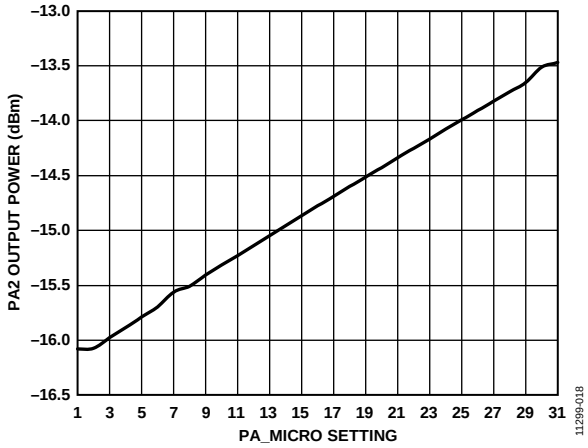

Figure 35. Microadjustment of the PA2 Output Power Using a PA_MICRO Setting Around −15 dBm, PA_COARSE = 10, PA_FINE = 2, V_{DD} = 3.0 V, T_A = 25°C

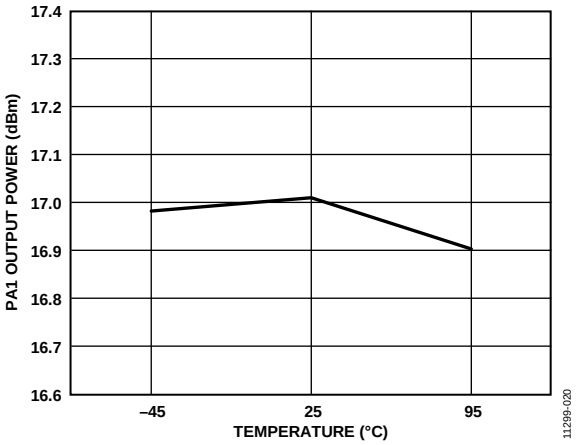

Figure 36. PA1 Output Power vs. Temperature, PA_COARSE = 10, PA_FINE = 93, and PA_MICRO = 16; Maximum Recommended Temperature = 85°C, Minimum Recommended Temperature = −40°C; −45°C and +95°C Operation Only Shown for Robustness

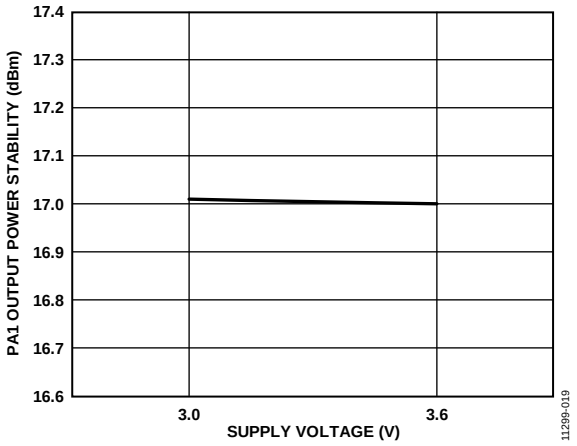

Figure 37. PA2 Output Power Stability vs. Supply Voltage (V_{DD}), PA_COARSE = 10, PA_FINE = 93, and PA_MICRO = 16, T_A = 25°C

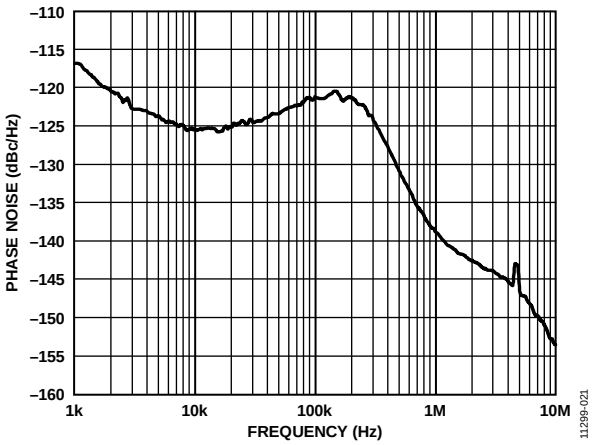

Figure 38. Transmit Phase Noise, V_{DD} = 3 V, T_A = 25°C, RF Frequency = 169.43125 MHz

THEORY OF OPERATION

HOST INTERFACE

Physical Interface

The ADF7030 provides a host interface (HIF) that consists of a 4-wire standard SPI, a hardware reset pin ($\overline{RST}$), and GPIOs. The ADF7030 always acts as a slave to the host processor. The host processor uses the SPI interface to perform the following operations on the ADF7030:

- Reads and writes to the ADF7030 memory.
- Configures and controls the ADF7030 radio.
- Receives and transmits packets over the air.

Host Interface Protocol

The ADF7030 implements a very simple protocol over the SPI interface. Using this protocol, the host processor can perform a number of operations as described in the following sections.

Memory Access

The memory access commands allow the host processor to read from and write to the internal memory of the ADF7030. Typically, the host uses these commands to update the configuration of the ADF7030 and to write packets for transmission or read received packets.

Radio Commands

There are two types of radio commands: a state machine radio command and a special radio command. A state machine command triggers a change of radio state as described in Table 9. A special radio command generates specific actions, such as to perform a system reset or to disable IRs as described in Table 10.

Table 9. State Machine Radio Commands

Command	Description
CMD_PHY_OFF	Performs a transition of the device into the PHY_OFF state
CMD_PHY_ON	Performs a transition of the device into the PHY_ON state
CMD_PHY_RX	Performs a transition of the device into the PHY_RX state
CMD_PHY_TX	Performs a transition of the device into the PHY_TX state
CMD_CONFIG_DEV	Configures the ADF7030 based on the radio profile
CMD_GET_RSSI	Performs an RSSI measurement
CMD_RAM_LOAD_INIT	Prepares the program RAM for a firmware module download
CMD_DO_CAL	Executes selected calibration routines

Table 10. Special Radio Commands

Command	Description
CMD_SYSTEM_RESET	Performs a system reset of the ADF7030
CMD_RAM_LOAD_DONE	Configures the ADF7030 to use a downloaded firmware module by restarting the ADF7030
CMD_IRQ1_DIS_IRQ0_DIS	Disables IRQ_IN0 and IRQ_IN1 in triggering preloaded radio commands
CMD_IRQ1_DIS_IRQ0_EN	Disables IRQ_IN1 and enables IRQ_IN0 in triggering preloaded radio commands
CMD_IRQ1_EN_IRQ0_DIS	Enables IRQ_IN1 and disables IRQ_IN0 in triggering preloaded radio commands
CMD_IRQ1_EN_IRQ0_EN	Enables IRQ_IN1 and IRQ_IN0 in triggering preloaded radio commands

Status Byte

The status byte of the ADF7030 (STATUS) is returned at specific times over the MISO during an SPI transaction. The status byte is described in Table 11.

Table 11. Status Byte Description

Bit	Name	Description
7	SPI_READY	0: SPI is not ready for access 1: SPI is ready for access
6	IRQ_STATUS	0: no pending interrupt condition 1: pending interrupt condition
5	CMD_READY	0: the ADF7030 is not ready to receive a radio command 1: the ADF7030 is ready to receive a radio command
4	Reserved	Reserved
3	ERR	0: no error 1: error (for example, an unsupported destination state or an internal error)
[2:1]	TRANSITION_STATUS	0: transition in progress 1: executing in a state 2: idle in a state
0	Reserved	Reserved

RADIO STATE MACHINE

TheADF7030 operates as a simple state machine. The host processor can transition the ADF7030 between states by issuing single-byte commands over the SPI interface. The ADF7030 processor handles the sequencing of various radio circuits and critical timing functions, thereby simplifying radio operation and easing the burden on the host processor.

The ADF7030 has eight states designated as PHY_SLEEP, PHY_OFF, PHY_ON, PHY_RX, PHY_TX, MEASURE_RSSI, RAM_LOAD_INIT, and CALIBRATING, described in Table 12.

Table 12. ADF7030 Radio States

State	Description
PHY_SLEEP	In this state, the ADF7030 is in a deep sleep state with no configuration memory retained.
PHY_OFF	In this state, the ADF7030 executes using its own internal oscillator clock. The host loads the firmware module from this state. The host configures the radio from this state.
PHY_ON	In this state, the external reference clock source is enabled. After entering this state, the ADF7030 is ready for the transmission and reception of packets.
PHY_RX	In this state, the ADF7030 can receive and process an incoming packet.
PHY_TX	In this state, the ADF7030 transmits the programmed packet data.
MEASURE_RSSI	In this state, the ADF7030 continuously measures the RSSI level in the selected channel and stores this value in dBm for access by the host. The ADF7030 remains in this state until commanded to move back to PHY_ON.
RAM_LOAD_INIT	In this state, the host can write a firmware module to the ADF7030 RAM memory.
CALIBRATING	In this state, the ADF7030 executes a receive radio calibration.

Firmware Modules

The host must download firmware modules to the ADF7030 RAM to enable certain aspects of the radio state machine. There are three firmware modules: transmit, receive, and calibrate. These modules are described in Table 13.

Table 13. ADF7030 Firmware Modules

Firmware Module	Functionality
RAM_CODE_VX_XXT.DAT	This module is the transmit firmware module and supports all radio states, except PHY_RX, CALIBRATING, and MEASURE_RSSI. VX_XX refers to the version number.
RAM_CODE_VX_XXR.DAT	This module is the receive firmware module and supports all radio states, except PHY_TX and CALIBRATING. VX_XX refers to the version number.
RAM_CODE_VX_XXC.DAT	This module is the calibrate firmware module and supports all radio states, except PHY_TX, PHY_RX, and MEASURE_RSSI. VX_XX refers to the version number.

PACKET HANDLING

The ADF7030 includes comprehensive transmit and receive packet management capabilities and can be configured for use with a wide variety of packet-based radio protocols.

The ADF7030 can be programmed to transmit and receive variable and fixed length packets. The packet data to be transmitted must be written by the host processor into the ADF7030 internal memory. Received packet data is available from the ADF7030 internal memory.

There are 256 bytes of dedicated RAM available to store, transmit, and receive packets. In transmit mode, a preamble, sync word, and cyclic redundancy check (CRC) can be added by the ADF7030 to the payload data stored in the RAM. In receive mode, the ADF7030 can qualify received packets based on preamble detection, sync word detection, or CRC validation. On reception of a valid packet, the received payload data is loaded to packet memory.

To transmit or receive a packet, the host processor must first configure the ADF7030. Then, the host processor issues the commands to place the ADF7030 into the PHY_RX state or the PHY_TX state. After either state is entered, the ADF7030 automatically starts transmitting or receiving a packet.

The host can track the progress of the transmission or reception of a packet by monitoring the interrupt signals coming from the ADF7030. There are two independent logical interrupts from the ADF7030, and events can be configured to trigger one or both of these logical interrupts.

The ADF7030 provides two frames in its radio profile that give flexibility in choosing what packet formats to use in the transmit and receive operations. A frame can be configured to use one of several packet formats; it is also possible to switch between these formats before entering the PHY_TX state or the PHY_RX state.

SUPPORTED RADIO CONFIGURATIONS

To eliminate many of the RF related design challenges users typically face, Analog Devices, Inc., provides a set of optimized radio profile configurations for the ADF7030.

The configurations ensure that the RF communication layer operates seamlessly, thereby allowing the user to concentrate on the protocol and system level design. Three radio configurations are supported in total, described in Table 14.

Table 14. Supported Radio Configurations

Radio Profile	Operation Supported	Data Rate (kbps)	Modulation	Frequency Deviation (kHz)	Receiver Bandwidth (kHz)	Channel Spacing (kHz)	Receiver Frequency Tolerance (kHz)
ADF7030_USECASE_0	Tx and Rx	2.4	2GFSK	2.4	8.7	12.5	±2
ADF7030_USECASE_2	Tx and Rx	4.8	2GFSK	2.4	10.6	12.5	±2
ADF7030_USECASE_9	Tx only	6.4	4GFSK	3.2	Not applicable	Not applicable	Not applicable

APPLICATIONS INFORMATION

TYPICAL APPLICATION CIRCUIT

Typical application circuits for the ADF7030 are shown in Figure 39 and Figure 40. All external components required for operation of the device are shown. The bottom of the LFCSP package has an exposed pad that must be soldered to ground on the printed circuit board (PCB).

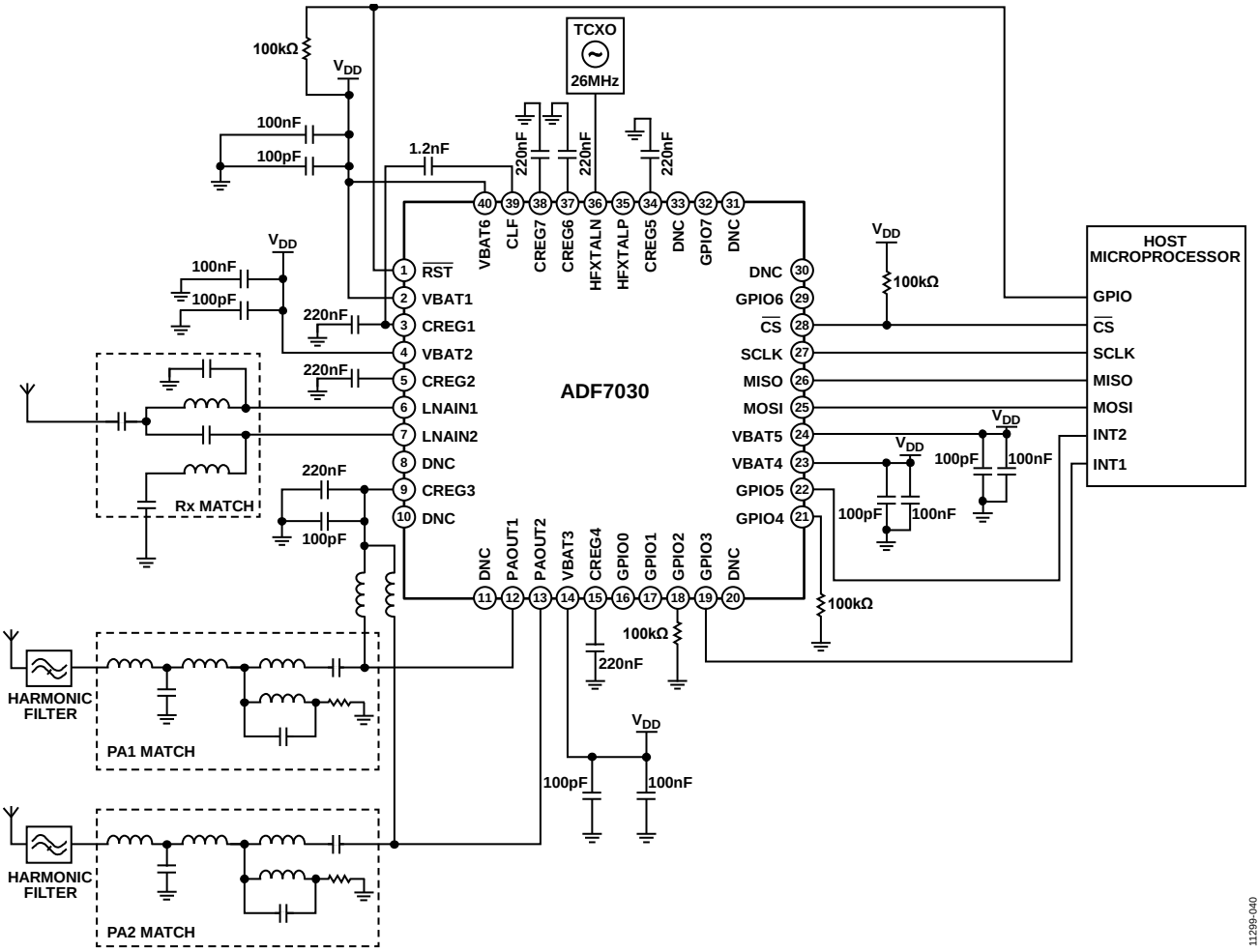

Figure 39. Application Circuit with Both PAs and LNA Matched, Without External PA or Tx/Rx Switch

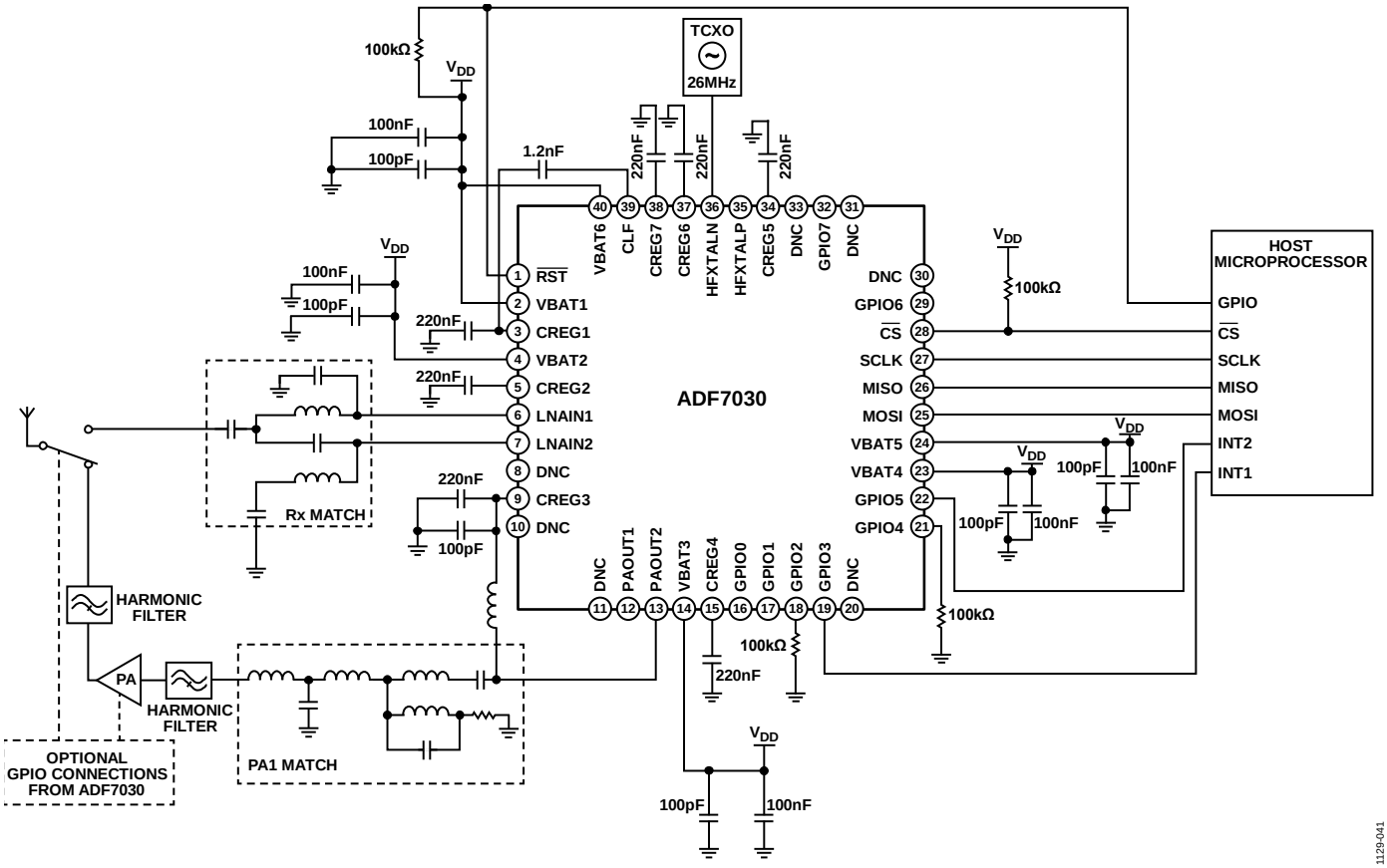

Figure 40. Application Circuit with Tx/Rx Switch and External PA

OUTLINE DIMENSIONS

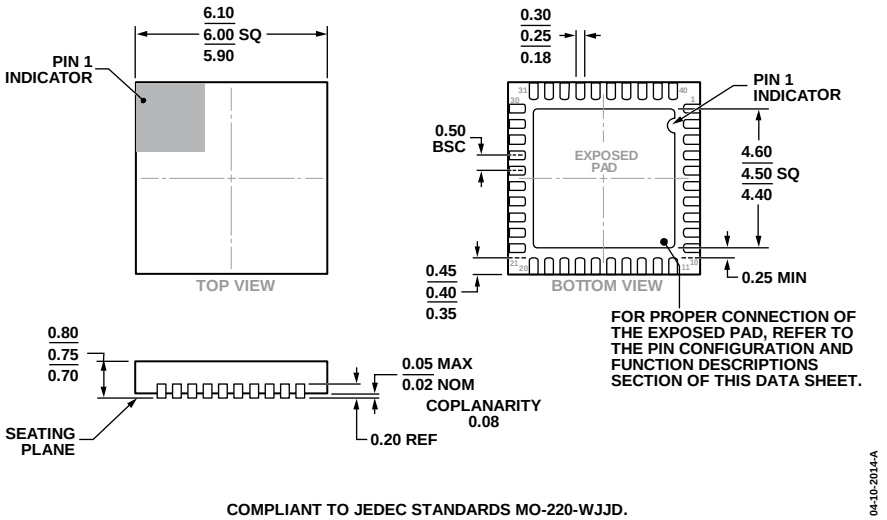

Figure 41. 40-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
6 mm × 6 mm Body, Very Very Thin Quad
(CP-40-17)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADF7030BCPZN	−40°C to +85°C	40-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-40-17
ADF7030BCPZN-RL	−40°C to +85°C	40-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-40-17
EVAl-ADF7030DB7Z		Evaluation Board (RF Daughter Board)	
EVAL-ADF7XXXMB4Z		Evaluation Board (Motherboard)	

[1] Z = RoHS Compliant Part.