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NTE4007 & NTE4007T Integrated Circuit CMOS, Dual Complementary Pair Plus Inverter

Description:

The NTE4007 (14-Lead DIP) and NTE4007T (SOIC-14) are multipurpose devices consisting of three N-Channel and three P-Channel enhancement mode devices packaged to provide access to each device. These versatile parts are useful in inverter circuits, pulse-shapers, linear amplifiers, high input impedance amplifiers, threshold detectors, transmission gating, and functional gating.

Features:

- Diode Protection on All Inputs
- Supply Voltage Range: 3Vdc to 18Vdc
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range

Absolute Maximum Ratings: (Voltages referenced to V_{SS} , Note 1)

DC Supply Voltage, V_{DD}	-0.5 to +18.0V
Input Voltage (DC or Transient), V_{in}	-0.5 to V_{DD} to +0.5V
Output Voltage (DC or Transient), V_{out}	-0.5 to V_{DD} to +0.5V
Input Current (DC or Transient, Per Pin), I_{in}	± 10 mA
Output Current (DC or Transient, Per Pin), I_{out}	± 10 mA
Power Dissipation (Per Package), P_D	500mW
Temperature Derating (from +65° to +125°C)	-7.0mW/°C
Ambient Temperature Range, T_A	-55° to +125°C
Storage Temperature Range, T_{stg}	-65° to +150°C
Lead Temperature (During Soldering, 8sec max), T_L	+260°C

Note 1. Stresses exceeding Absolute Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Electrical Characteristics: (Voltages referenced to V_{SS} , Note 2)

Parameter	Symbol	V_{DD} Vdc	-55°C		+25°C			+125°C		Unit
			Min	Max	Min	Typ	Max	Min	Max	
Output Voltage “0” Level $V_{in} = V_{DD}$ or 0 “1” Level $V_{in} = 0$ or V_{DD}	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
		10	–	0.05	–	0	0.05	–	0.05	Vdc
		15	–	0.05	–	0	0.05	–	0.05	Vdc
	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
		10	9.95	–	9.95	10	–	9.95	–	Vdc
		15	14.95	–	14.95	15	–	14.95	–	Vdc
Input Voltage “0” Level ($V_O = 4.5Vdc$) ($V_O = 9.0Vdc$) ($V_O = 13.5Vdc$) “1” Level ($V_O = 0.5Vdc$) ($V_O = 1.0Vdc$) ($V_O = 1.5Vdc$)	V_{IL}	5.0	–	1.0	–	2.25	1.0	–	1.0	Vdc
		10	–	2.0	–	4.50	2.0	–	2.0	Vdc
		15	–	2.5	–	6.75	2.5	–	2.5	Vdc
	V_{IH}	5.0	4.0	–	4.0	2.75	–	4.0	–	Vdc
		10	8.0	–	8.0	5.50	–	8.0	–	Vdc
		15	12.5	–	12.5	8.25	–	12.5	–	Vdc
Output Drive Current Source ($V_{OH} = 2.5Vdc$) ($V_{OH} = 4.6Vdc$) ($V_{OH} = 9.5Vdc$) ($V_{OH} = 13.5Vdc$) Sink ($V_{OL} = 0.4Vdc$) ($V_{OL} = 0.5Vdc$) ($V_{OL} = 1.5Vdc$)	I_{OH}	5.0	–3.0	–	–2.4	–5.0	–	–1.7	–	mAdc
		5.0	–0.64	–	–0.51	–1.0	–	–0.36	–	mAdc
		10	–1.6	–	–1.3	–2.5	–	–0.9	–	mAdc
		15	–4.2	–	–3.4	–10	–	–2.4	–	mAdc
	I_{OL}	5.0	0.64	–	0.51	1.0	–	0.36	–	mAdc
		10	1.6	–	1.3	2.5	–	0.9	–	mAdc
		15	4.2	–	3.4	10	–	2.4	–	mAdc
		15	–	±0.1	–	±0.00001	±0.1	–	±0.1	μAdc
Input Capacitance ($V_{IN} = 0$)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (Per Package)	I_{DD}	5.0	–	0.25	–	0.0005	0.25	–	7.5	μAdc
		10	–	0.5	–	0.0010	0.5	–	15	μAdc
		15	–	1.0	–	0.0015	1.0	–	30	μAdc
Total Supply Current (Dynamic plus Quiescent, Per Gate, $C_L = 50pF$, Note 3, Note 4)	I_T	5.0	$I_T = (0.7\mu A/kHz) f + I_{DD}/6$							μAdc
		10	$I_T = (1.4\mu A/kHz) f + I_{DD}/6$							μAdc
		15	$I_T = (2.2\mu A/kHz) f + I_{DD}/6$							μAdc

Note 2. Data labeled “Typ” is not to be used for design purposes but is intended as an indication of the device’s potential performance.

Note 3. The formulas given are for the typical characteristics only at +25°C.

Note 4. To calculate total supply current at loads other than 50pF:

$$I_T(C_L) = I_T(50pF) + (C_L - 50) V_{fk}$$

where: I_T is in μA (per package), C_L in pF, $V = (V_{DD} - V_{SS})$ in volts, f in kHz is input frequency, and $k = 0.003$.

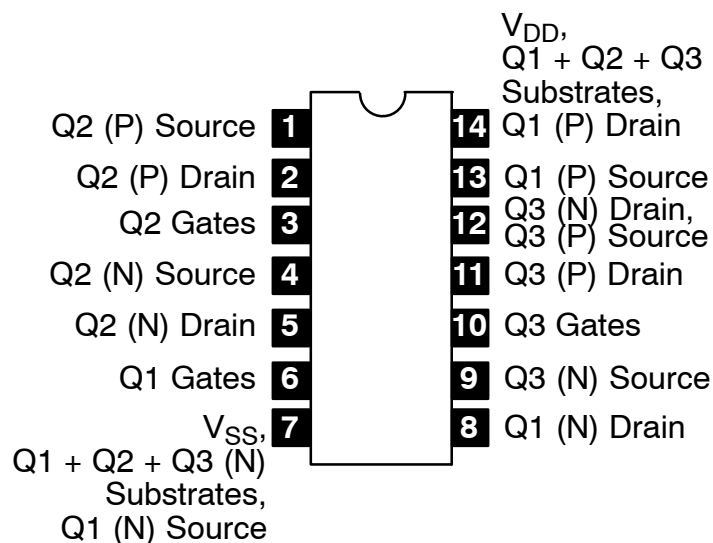
Switching Characteristics: ($C_L = 50\text{pF}$, $T_A = +25^\circ\text{C}$, Note 2, Note 5)

Parameter	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise Time $t_{TLH} = (1.2\text{ns/pf}) C_L + 30\text{ns}$ $t_{TLH} = (0.5\text{ns/pf}) C_L + 20\text{ns}$ $t_{TLH} = (0.4\text{ns/pf}) C_L + 15\text{ns}$	t_{TLH}	5.0	–	90	180	ns
		10	–	45	90	ns
		15	–	35	70	ns
Output Fall Time $t_{THL} = (1.2\text{ns/pf}) C_L + 15\text{ns}$ $t_{THL} = (0.5\text{ns/pf}) C_L + 15\text{ns}$ $t_{THL} = (0.4\text{ns/pf}) C_L + 10\text{ns}$	t_{THL}	5.0	–	75	150	ns
		10	–	40	80	ns
		15	–	30	60	ns
Turn-Off Delay Time $t_{PLH} = (1.5\text{ns/pf}) C_L + 35\text{ns}$ $t_{PLH} = (0.2\text{ns/pf}) C_L + 20\text{ns}$ $t_{PLH} = (0.15\text{ns/pf}) C_L + 17.5\text{ns}$	t_{PLH}	5.0	–	60	125	ns
		10	–	30	75	ns
		15	–	25	55	ns
Turn-On Delay Time $t_{PHL} = (1.0\text{ns/pf}) C_L + 10\text{ns}$ $t_{PHL} = (0.3\text{ns/pf}) C_L + 15\text{ns}$ $t_{PHL} = (0.2\text{ns/pf}) C_L + 15\text{ns}$	t_{PHL}	5.0	–	60	125	ns
		10	–	30	75	ns
		15	–	25	55	ns

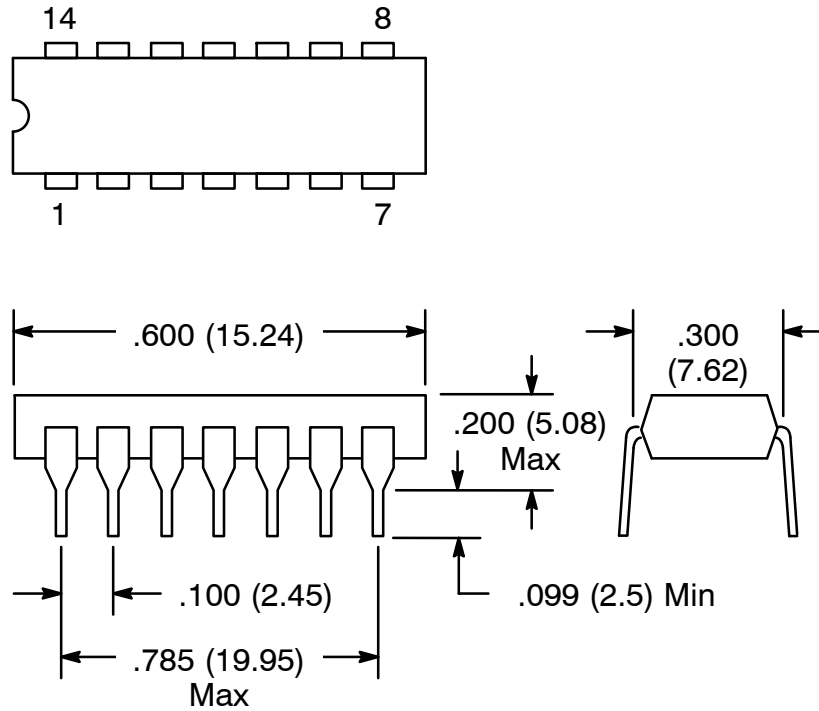
Note 2. Data labeled “Typ” is not to be used for design purposes but is intended as an indication of the device’s potential performance.

Note 5. The formulas given are for the typical characteristics only. Switching specifications are for devices connected as an inverter.

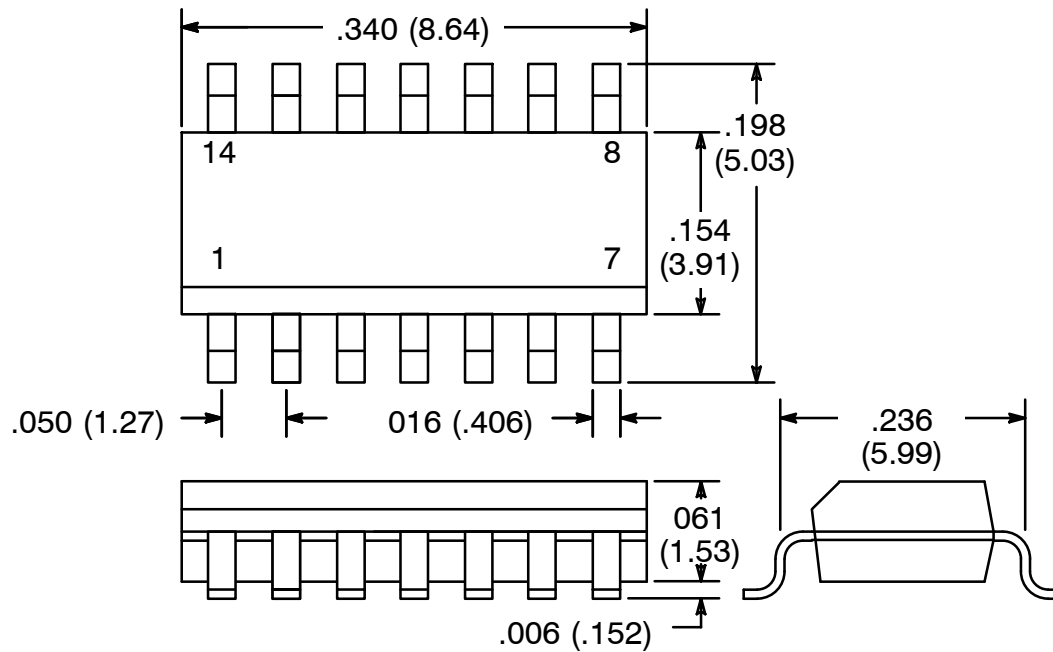
Pin Connection Diagram



NTE4007



NTE4007T



NOTE: Pin1 on Beveled Edge