

NTB6412AN, NTP6412AN, NVB6412AN

N-Channel Power MOSFET 100 V, 58 A, 18.2 mΩ

Features

- Low $R_{DS(on)}$
- High Current Capability
- 100% Avalanche Tested
- NVB Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ Unless otherwise specified)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V _{DSS}	100	V
Gate-to-Source Voltage – Continuous			V _{GS}	± 20	V
Continuous Drain Current R _{θJC}	Steady State	T _C = 25°C	I _D	58	A
		T _C = 100°C		41	
Power Dissipation R _{θJC}	Steady State	T _C = 25°C	P _D	167	W
Pulsed Drain Current	t _p = 10 μs		I _{DM}	240	A
Operating Junction and Storage Temperature Range			T _J , T _{stg}	–55 to +175	°C
Source Current (Body Diode)			I _S	58	A
Single Pulse Drain-to-Source Avalanche Energy (V _{DD} = 50 Vdc, V _{GS} = 10 Vdc, I _{L(pk)} = 44.7 A, L = 0.3 mH, R _G = 25 Ω)			E _{AS}	300	mJ
Lead Temperature for Soldering Purposes, 1/8" from Case for 10 Seconds			T _L	260	°C

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Case (Drain) Steady State	$R_{\theta JC}$	0.9	$^\circ\text{C/W}$
Junction-to-Ambient (Note 1)	$R_{\theta JA}$	33	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface mounted on FR4 board using 1 sq in pad size, (Cu Area 1.127 sq in [2 oz] including traces).

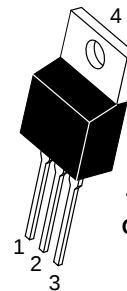
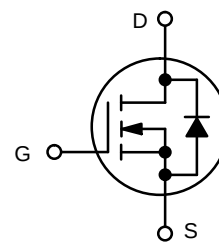


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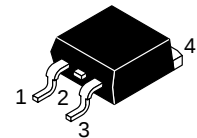
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$V_{(BR)DSS}$	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$ (Note 1)
100 V	18.2 mΩ @ 10 V	58 A

N-Channel

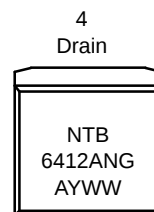
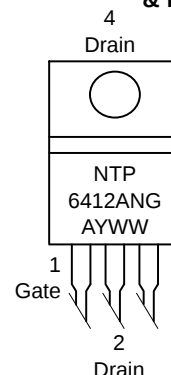


TO-220AB
CASE 221A
STYLE 5



D²PAK
CASE 418B
STYLE 2

MARKING DIAGRAM & PIN ASSIGNMENT



6412AN = Specific Device Code
G = Pb-Free Device
A = Assembly Location
Y = Year
WW = Work Week

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

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ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ Unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	100			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			103		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = 100\text{ V}$	$T_J = 25^\circ\text{C}$		1.0	μA
			$T_J = 125^\circ\text{C}$		100	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA

ON CHARACTERISTICS (Note 2)

Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = 250\text{ }\mu\text{A}$	2.0		4.0	V
Negative Threshold Temperature Coefficient	$V_{GS(th)}/T_J$			9.2		mV/°C
Drain-to-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 58\text{ A}$		16.8	18.2	m Ω
		$V_{GS} = 10\text{ V}, I_D = 20\text{ A}$		15.6	18.2	
Forward Transconductance	g_{FS}	$V_{DS} = 5\text{ V}, I_D = 20\text{ A}$		31		S

CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C_{iss}	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		2700	3500	pF
Output Capacitance	C_{oss}			400	500	
Reverse Transfer Capacitance	C_{rss}			150		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}, V_{DS} = 80\text{ V}, I_D = 58\text{ A}$		73	100	nC
Threshold Gate Charge	$Q_{G(TH)}$			2.5		
Gate-to-Source Charge	Q_{GS}			13.5		
Gate-to-Drain Charge	Q_{GD}			35		
Plateau Voltage	V_{GP}			5.6		V
Gate Resistance	R_G			2.2		Ω

SWITCHING CHARACTERISTICS, $V_{GS} = 10\text{ V}$ (Note 3)

Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = 10\text{ V}, V_{DD} = 80\text{ V}, I_D = 58\text{ A}, R_G = 6.2\text{ }\Omega$		16		ns
Rise Time	t_r			140		
Turn-Off Delay Time	$t_{d(off)}$			70		
Fall Time	t_f			126		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V _{SD}	I _S = 58 A	T _J = 25°C		0.96	1.3	V
			T _J = 125°C		0.89		
Reverse Recovery Time	t _{rr}	V _{GS} = 0 V, I _S = 58 A, dI _{SD} /dt = 100 A/μs			85		ns
Charge Time	t _a				60		
Discharge Time	t _b				25		
Reverse Recovery Charge	Q _{RR}				270		nC

2. Pulse Test: Pulse Width $\leq 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2\%$.

3. Switching characteristics are independent of operating junction temperatures.

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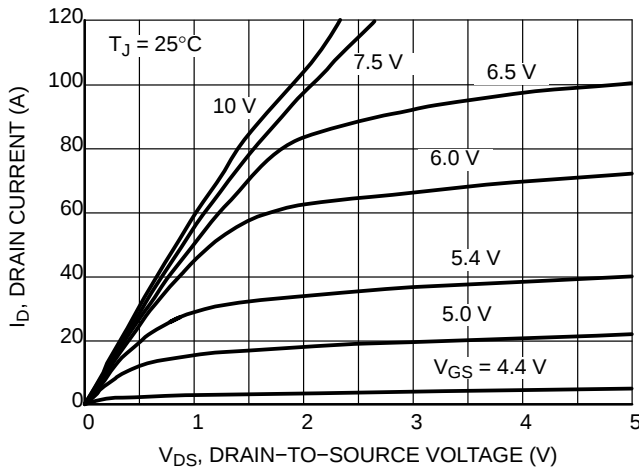


Figure 1. On-Region Characteristics

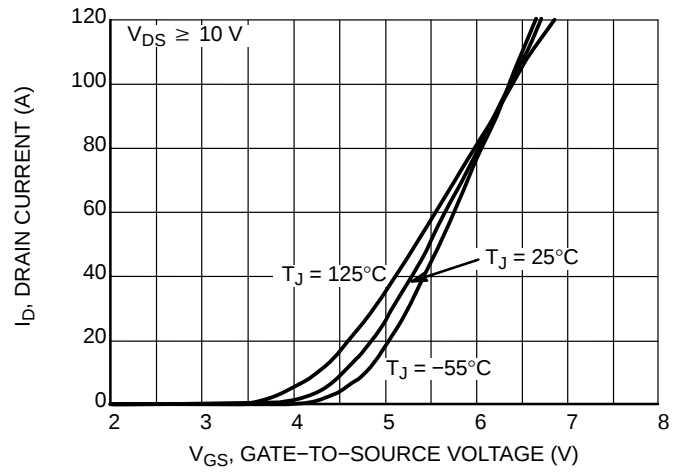


Figure 2. Transfer Characteristics

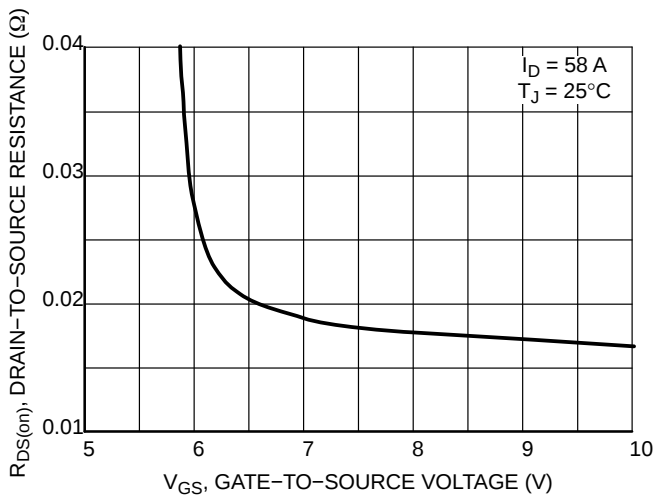


Figure 3. On-Region versus Gate Voltage

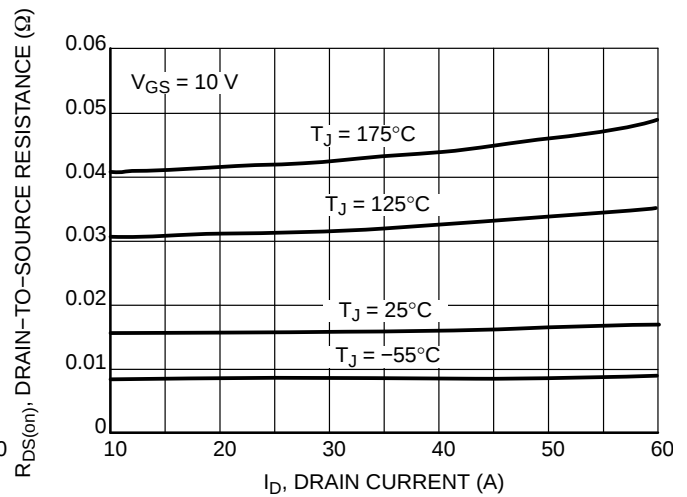


Figure 4. On-Resistance versus Drain Current and Gate Voltage

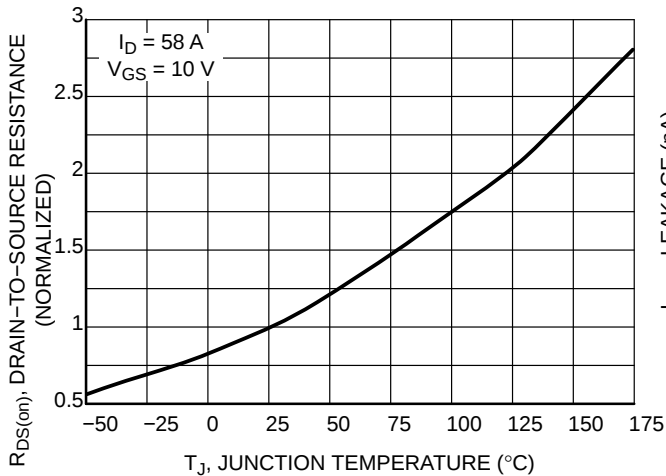


Figure 5. On-Resistance Variation with Temperature

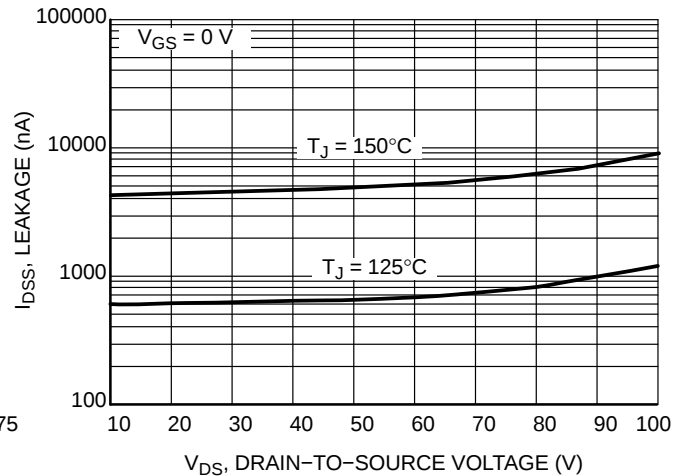


Figure 6. Drain-to-Source Leakage Current versus Voltage

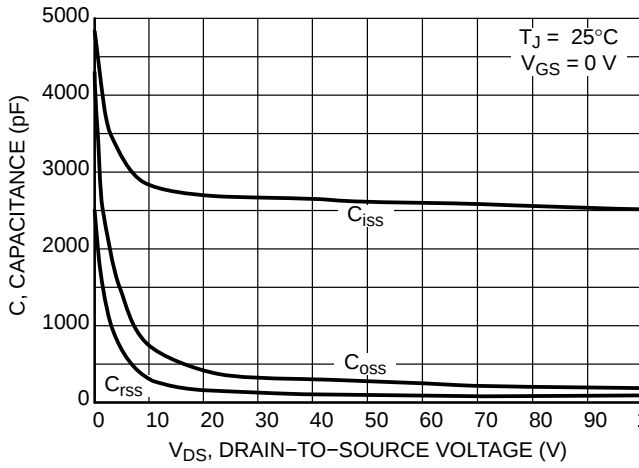


Figure 7. Capacitance Variation

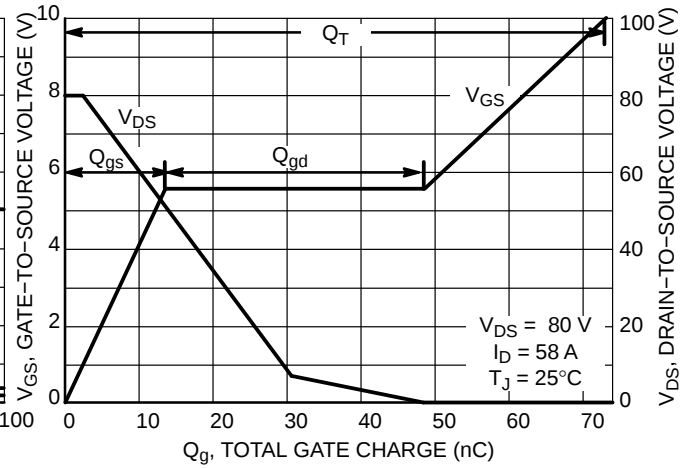


Figure 8. Gate-to-Source Voltage and Drain-to-Source Voltage versus Total Charge

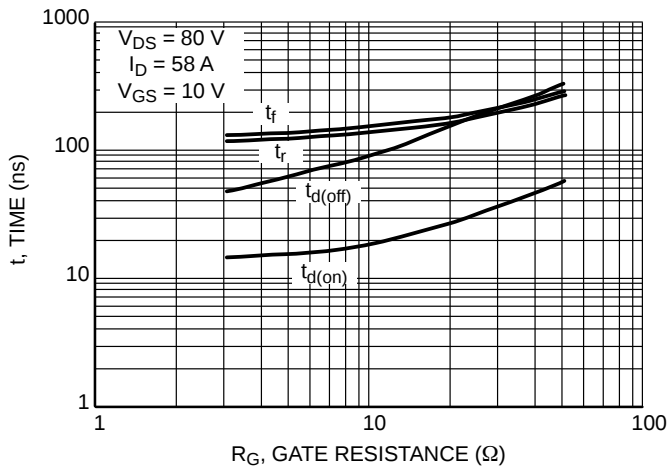


Figure 9. Resistive Switching Time Variation versus Gate Resistance

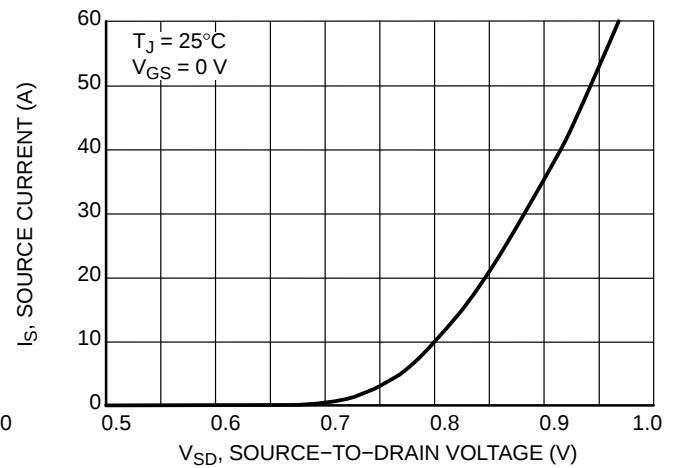


Figure 10. Diode Forward Voltage versus Current

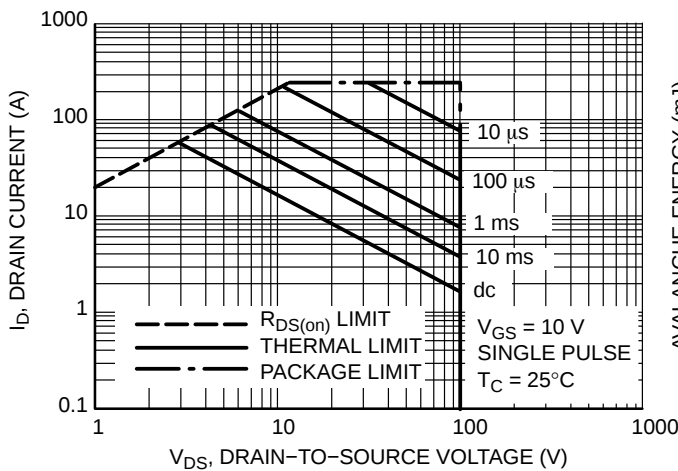


Figure 11. Maximum Rated Forward Biased Safe Operating Area

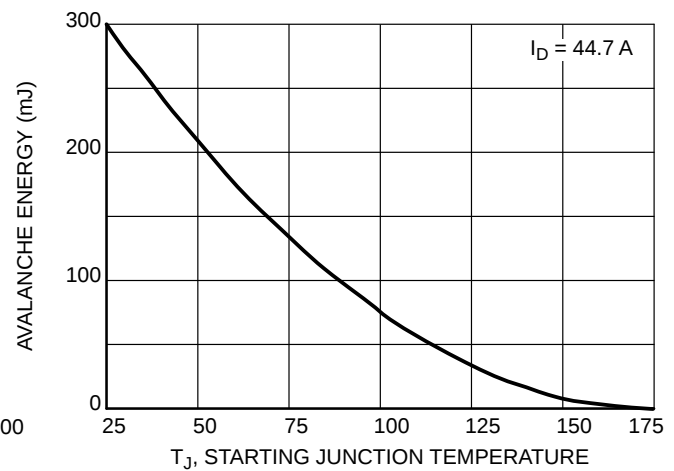


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

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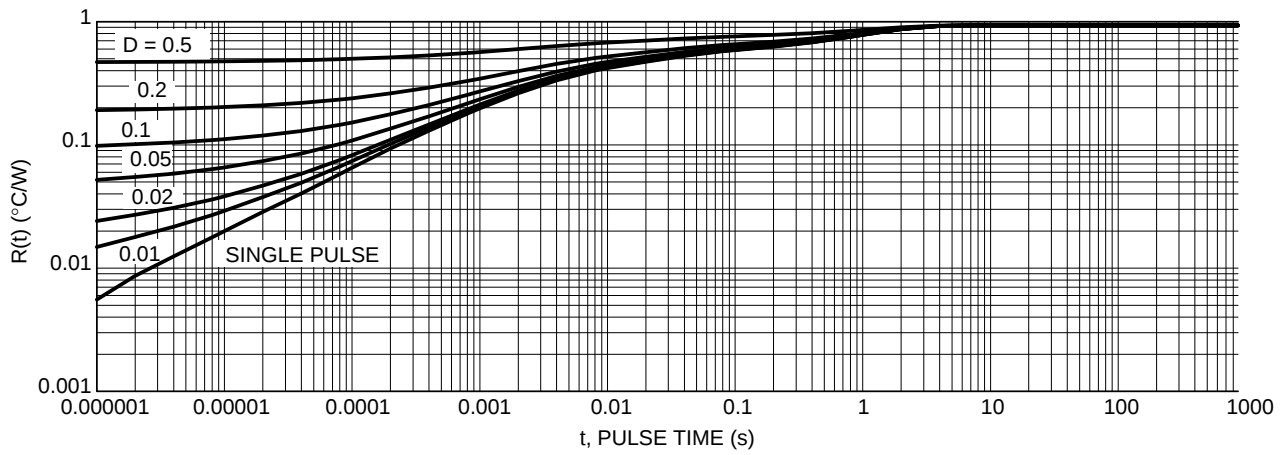


Figure 13. Thermal Response

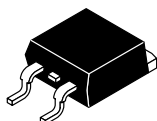
ORDERING INFORMATION

Device	Package	Shipping [†]
NTB6412ANG	D ² PAK (Pb-Free)	50 Units / Rail
NTB6412ANT4G	D ² PAK (Pb-Free)	800 / Tape & Reel
NTP6412ANG	TO-220 (Pb-Free)	50 Units / Rail
NVB6412ANT4G	D ² PAK (Pb-Free)	800 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

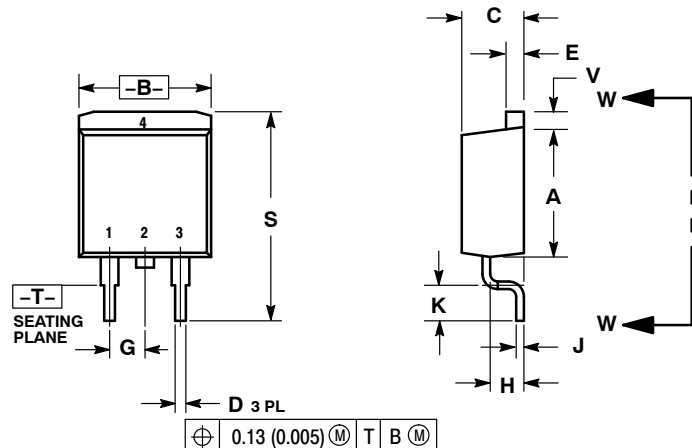
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D²PAK 3
CASE 418B-04
ISSUE L

DATE 17 FEB 2015

SCALE 1:1

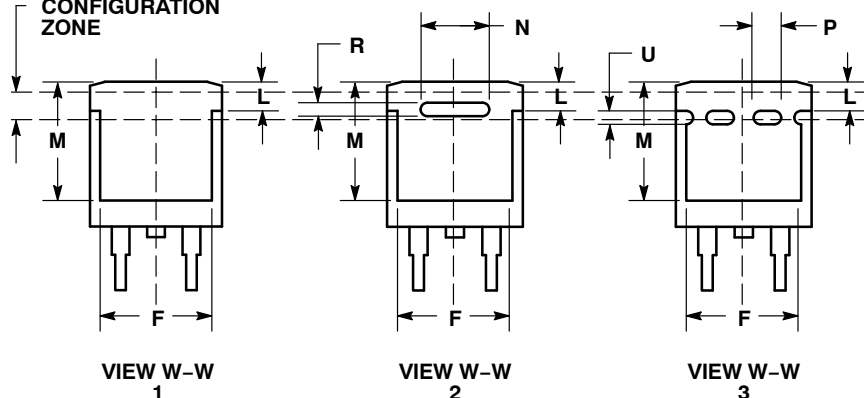


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 418B-01 THRU 418B-03 OBSOLETE, NEW STANDARD 418B-04.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.340	0.380	8.64	9.65
B	0.380	0.405	9.65	10.29
C	0.160	0.190	4.06	4.83
D	0.020	0.035	0.51	0.89
E	0.045	0.055	1.14	1.40
F	0.310	0.350	7.87	8.89
G	0.100	BSC	2.54	BSC
H	0.080	0.110	2.03	2.79
J	0.018	0.025	0.46	0.64
K	0.090	0.110	2.29	2.79
L	0.052	0.072	1.32	1.83
M	0.280	0.320	7.11	8.13
N	0.197	REF	5.00	REF
P	0.079	REF	2.00	REF
R	0.039	REF	0.99	REF
S	0.575	0.625	14.60	15.88
V	0.045	0.055	1.14	1.40

VARIABLE CONFIGURATION ZONE



STYLE 1:

- PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:

- PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:

- PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 4:

- PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 5:

- PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:

- PIN 1. NO CONNECT
2. CATHODE
3. ANODE
4. CATHODE

MARKING INFORMATION AND FOOTPRINT ON PAGE 2

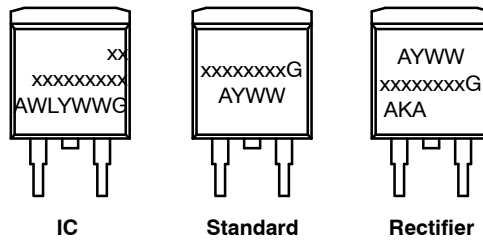
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ISSUE L

DATE 17 FEB 2015

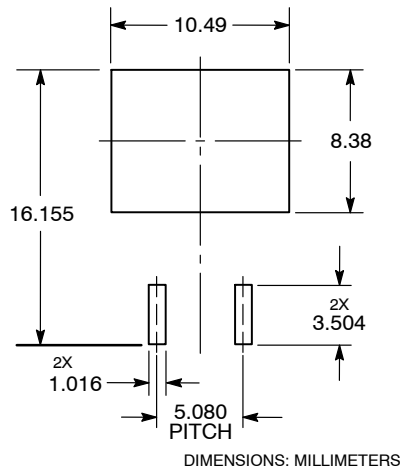
**GENERIC
MARKING DIAGRAM***



xx = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb-Free Package
AKA = Polarity Indicator

*This information is generic. Please refer to device data sheet for actual part marking.
Pb-Free indicator, "G" or microdot "▪", may or may not be present.

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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