

Complementary Power Transistors

For Isolated Package Applications

MJF15030 (NPN), MJF15031 (PNP)

Designed for general-purpose amplifier and switching applications, where the mounting surface of the device is required to be electrically isolated from the heatsink or chassis.

Features

- Electrically Similar to the Popular MJE15030 and MJE15031
- No Isolating Washers Required, Reduced System Cost
- High Current Gain-Bandwidth Product
- UL Recognized, File #E69369, to 3500 V_{RMS} Isolation
- These Devices are Pb-Free and are RoHS Compliant*

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V _{CEO}	150	Vdc
Collector-Base Voltage	V _{CB}	150	Vdc
Emitter-Base Voltage	V _{EB}	5	Vdc
RMS Isolation Voltage (Note 1) (t = 0.3 sec, R.H. ≤ 30%, T _A = 25°C) Per Figure 11	V _{ISOL}	4500	V _{RMS}
Collector Current – Continuous	I _C	8	Adc
Collector Current – Peak	I _{CM}	16	Adc
Base Current	I _B	2	Adc
Total Power Dissipation (Note 2) @ T _C = 25°C Derate above 25°C	P _D	36 0.286	W W/°C
Total Power Dissipation @ T _A = 25°C Derate above 25°C	P _D	2.0 0.016	W W/°C
Operating and Storage Temperature Range	T _J , T _{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

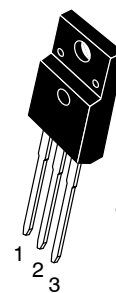
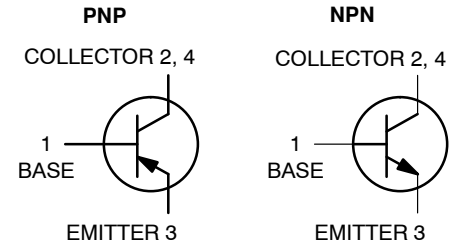
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction-to-Ambient	R _{θJA}	62.5	°C/W
Thermal Resistance, Junction-to-Case (Note 2)	R _{θJC}	3.5	°C/W
Lead Temperature for Soldering Purposes	T _L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- Proper strike and creepage distance must be provided.
- Measurement made with thermocouple contacting the bottom insulated surface (in a location beneath the die), the devices mounted on a heatsink with thermal grease and a mounting torque of ≥ 6 in. lbs.

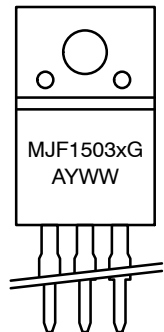
*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

COMPLEMENTARY SILICON POWER TRANSISTORS 8 AMPERES 150 VOLTS, 36 WATTS



TO-220 FULLPACK
CASE 221D
STYLE 2

MARKING DIAGRAM



MJF1503x = Specific Device Code
 x = 0 or 1
 G = Pb-Free Package
 A = Assembly Location
 Y = Year
 WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MJF15030G	TO-220 FULLPACK (Pb-Free)	50 Units/Rail
MJF15031G	TO-220 FULLPACK (Pb-Free)	50 Units/Rail

MJF15030 (NPN), MJF15031 (PNP)

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (Note 3) ($I_C = 10\text{ mAdc}$, $I_B = 0$)	$V_{CEO(sus)}$	150	–	Vdc
Collector Cutoff Current ($V_{CE} = 150\text{ Vdc}$, $I_B = 0$)	I_{CEO}	–	10	μAdc
Collector Cutoff Current ($V_{CB} = 150\text{ Vdc}$, $I_E = 0$)	I_{CBO}	–	10	μAdc
Emitter Cutoff Current ($V_{BE} = 5\text{ Vdc}$, $I_C = 0$)	I_{EBO}	–	10	μAdc
ON CHARACTERISTICS (Note 3)				
DC Current Gain ($I_C = 0.1\text{ Adc}$, $V_{CE} = 2\text{ Vdc}$) ($I_C = 2\text{ Adc}$, $V_{CE} = 2\text{ Vdc}$) ($I_C = 3\text{ Adc}$, $V_{CE} = 2\text{ Vdc}$) ($I_C = 4\text{ Adc}$, $V_{CE} = 2\text{ Vdc}$)	h_{FE}	40 40 40 20	– – – –	–
DC Current Gain Linearity (V_{CE} from 2 V to 20 V, I_C from 0.1 A to 3 A) (NPN to PNP)	h_{FE}	Typ 2 3		
Collector-Emitter Saturation Voltage ($I_C = 1\text{ Adc}$, $I_B = 0.1\text{ Adc}$)	$V_{CE(sat)}$	–	0.5	Vdc
Base-Emitter On Voltage ($I_C = 1\text{ Adc}$, $V_{CE} = 2\text{ Vdc}$)	$V_{BE(on)}$	–	1	Vdc

DYNAMIC CHARACTERISTICS

Current Gain – Bandwidth Product (Note 4) ($I_C = 500\text{ mAdc}$, $V_{CE} = 10\text{ Vdc}$, $f_{test} = 10\text{ MHz}$)	f_T	30	–	MHz
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Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: Pulse Width $\leq 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2\%$.

4. $f_T = |h_{fe}| \cdot f_{test}$.

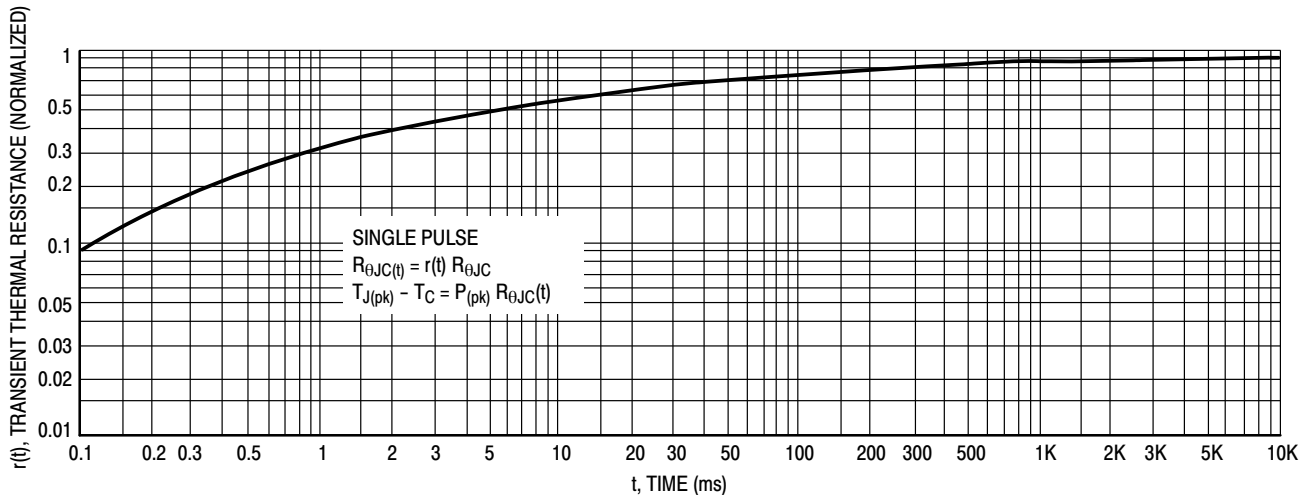


Figure 1. Thermal Response

MJF15030 (NPN), MJF15031 (PNP)

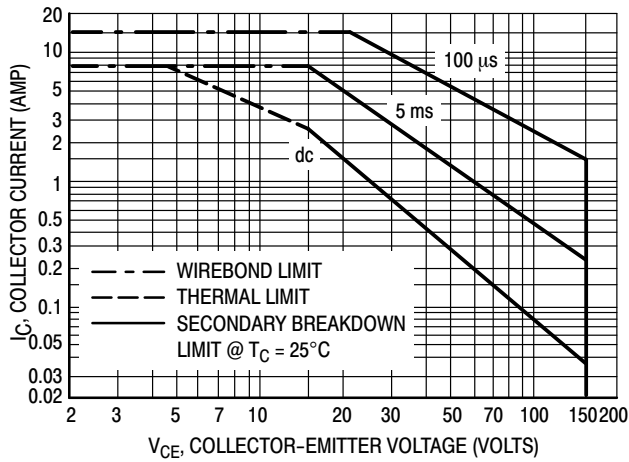


Figure 2. Forward Bias Safe Operating Area

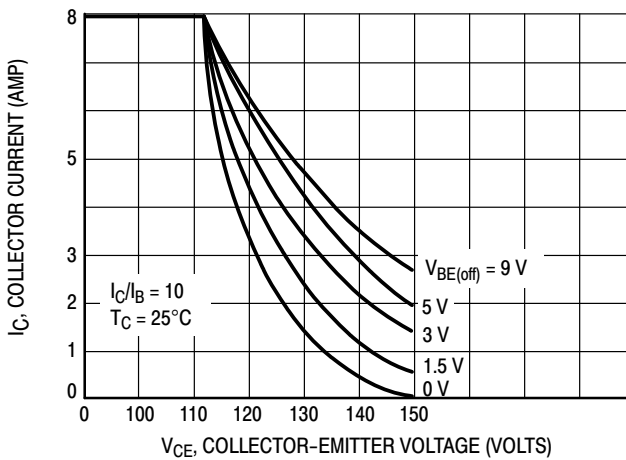


Figure 3. Reverse Bias Switching Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 2 and 3 is based on $T_{J(pk)} = 150^\circ\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150^\circ\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 1. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

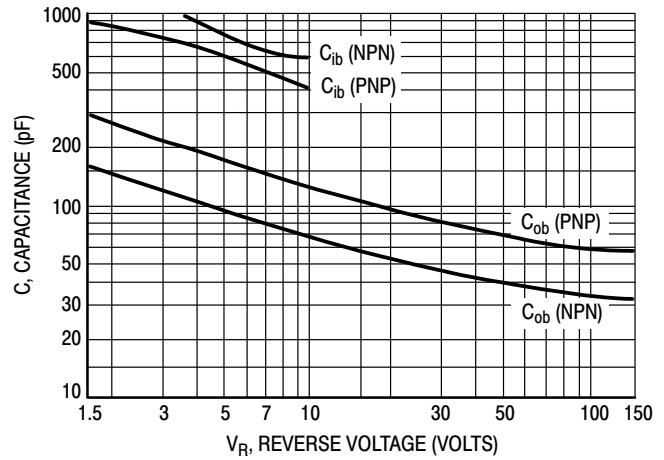


Figure 4. Capacitances

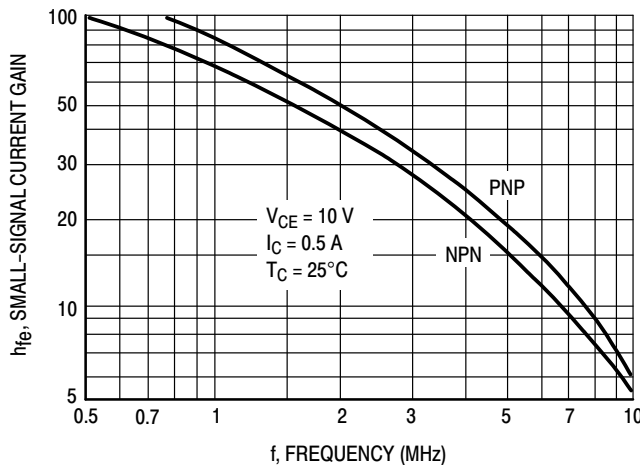


Figure 5. Small-Signal Current Gain

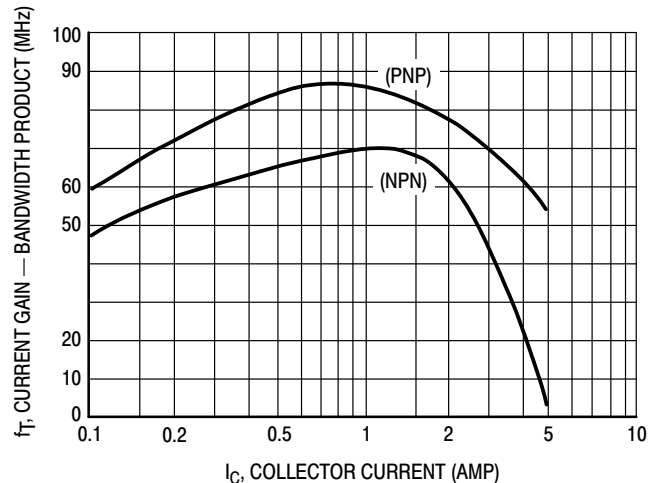


Figure 6. Current Gain — Bandwidth Product

MJF15030 (NPN), MJF15031 (PNP)

DC CURRENT GAIN

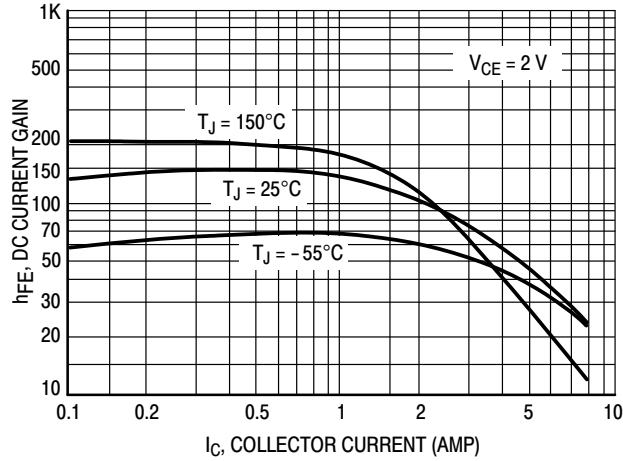


Figure 7a. MJF15030 NPN

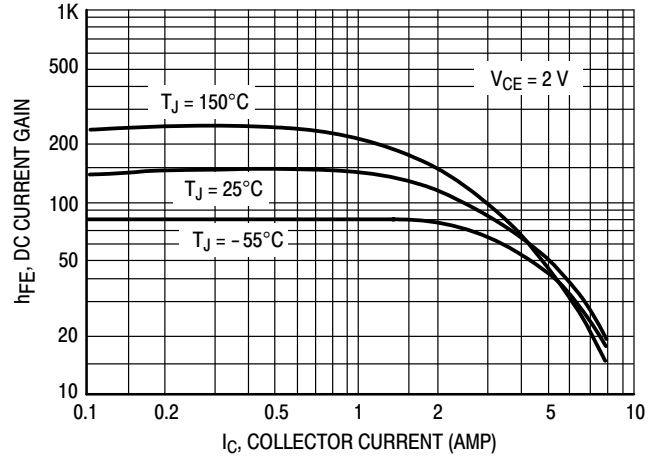


Figure 7b. MJF15031 PNP

“ON” VOLTAGE

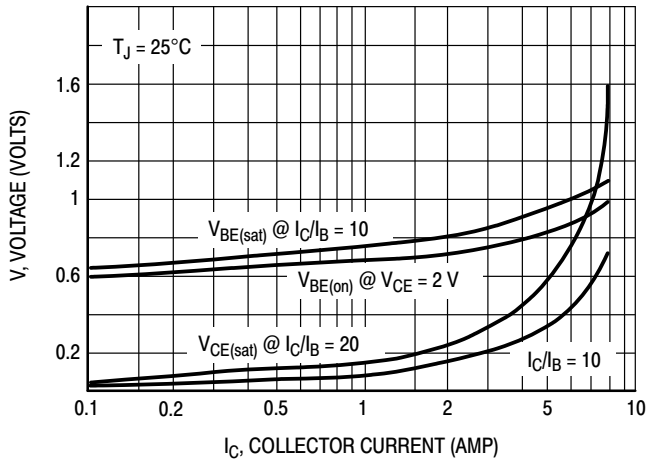


Figure 8a. MJF15030 NPN

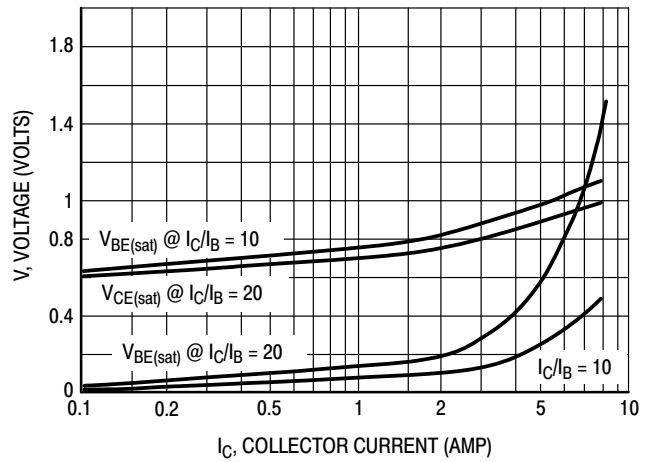


Figure 8b. MJF15031 PNP

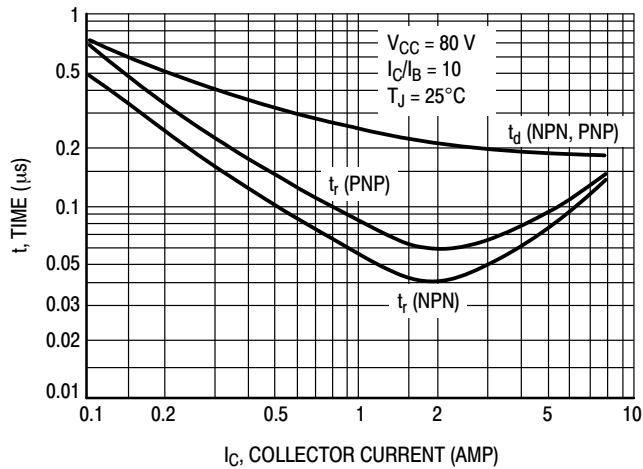


Figure 9. Turn-On Times

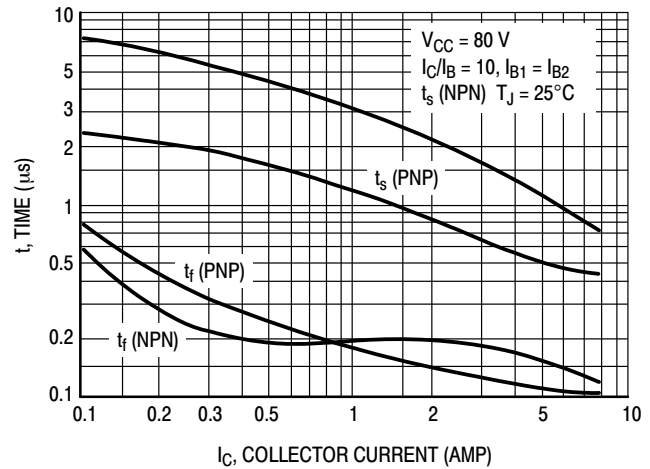


Figure 10. Turn-Off Times

MJF15030 (NPN), MJF15031 (PNP)

TEST CONDITIONS FOR ISOLATION TESTS*

FULLY ISOLATED PACKAGE

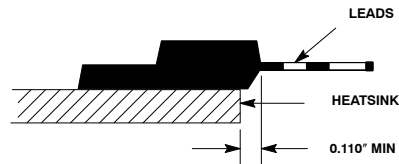


Figure 11. Mounting Position

*Measurement made between leads and heatsink with all leads shorted together.

MOUNTING INFORMATION

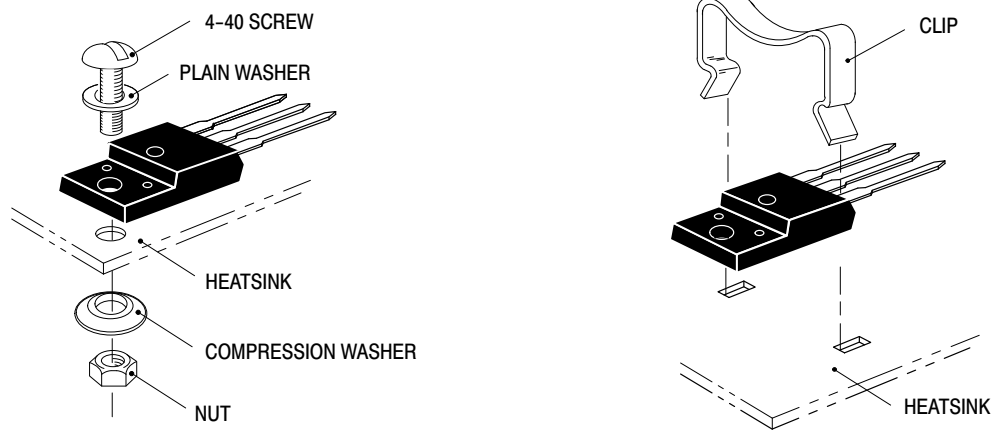


Figure 12. Typical Mounting Techniques*

Laboratory tests on a limited number of samples indicate, when using the screw and compression washer mounting technique, a screw torque of 6 to 8 in · lbs is sufficient to provide maximum power dissipation capability. The compression washer helps to maintain a constant pressure on the package over time and during large temperature excursions.

Destructive laboratory tests show that using a hex head 4–40 screw, without washers, and applying a torque in excess of 20 in · lbs will cause the plastic to crack around the mounting hole, resulting in a loss of isolation capability.

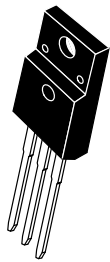
Additional tests on slotted 4–40 screws indicate that the screw slot fails between 15 to 20 in · lbs without adversely affecting the package. However, in order to positively ensure the package integrity of the fully isolated device, **onsemi** does not recommend exceeding 10 in · lbs of mounting torque under any mounting conditions.

**For more information about mounting power semiconductors see Application Note AN1040.

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

ON Semiconductor®

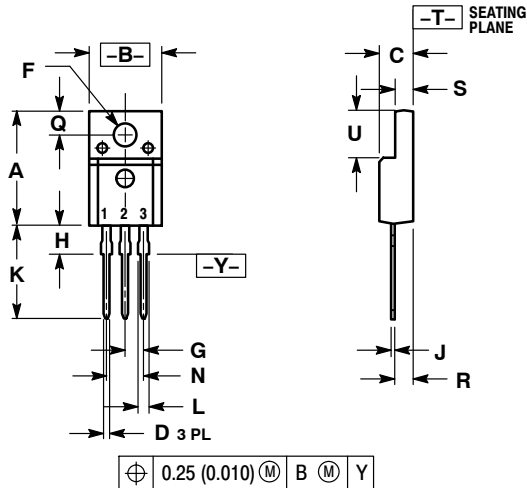
ON



SCALE 1:1

TO-220 FULLPAK CASE 221D-03 ISSUE K

DATE 27 FEB 2009



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH
 3. 221D-01 THRU 221D-02 OBSOLETE, NEW STANDARD 221D-03.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.617	0.635	15.67	16.12
B	0.392	0.419	9.96	10.63
C	0.177	0.193	4.50	4.90
D	0.024	0.039	0.60	1.00
F	0.116	0.129	2.95	3.28
G	0.100 BSC		2.54 BSC	
H	0.118	0.135	3.00	3.43
J	0.018	0.025	0.45	0.63
K	0.503	0.541	12.78	13.73
L	0.048	0.058	1.23	1.47
N	0.200 BSC		5.08 BSC	
Q	0.122	0.138	3.10	3.50
R	0.099	0.117	2.51	2.96
S	0.092	0.113	2.34	2.87
U	0.239	0.271	6.06	6.88

MARKING DIAGRAMS

- STYLE 1:
PIN 1. GATE
2. DRAIN
3. SOURCE
- STYLE 2:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
- STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
- STYLE 4:
PIN 1. CATHODE
2. ANODE
3. CATHODE
- STYLE 5:
PIN 1. CATHODE
2. ANODE
3. GATE
- STYLE 6:
PIN 1. MT 1
2. MT 2
3. GATE



Bipolar



Rectifier

xxxxxx = Specific Device Code
G = Pb-Free Package
A = Assembly Location
Y = Year
WW = Work Week

A = Assembly Location
Y = Year
WW = Work Week
xxxxxx = Device Code
G = Pb-Free Package
AKA = Polarity Designator

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