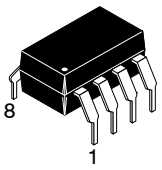
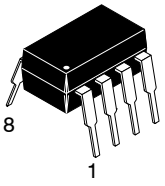
High-Speed 10 MBit/s Logic Gate Optocouplers

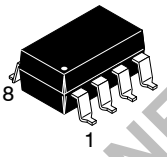
Single-Channel: 6N137, HCPL2601, HCPL2611 Dual-Channel: HCPL2630, HCPL2631



PDIP8 6.6x3.81, 2.54P
CASE 646BW



PDIP8 9.655x6.6, 2.54P
CASE 646CQ



PDIP8 GW
CASE 709AC

Description

The 6N137, HCPL2601, HCPL2611 single−channel and HCPL2630, HCPL2631 dual−channel optocouplers consist of a 850 nm AlGaAS LED, optically coupled to a very high speed integrated photo−detector logic gate with a strobable output. This output features an open collector, thereby permitting wired OR outputs. The coupled parameters are guaranteed over the temperature range of −40°C to +85°C. A maximum input signal of 5 mA will provide a minimum output sink current of 13 mA (fan out of 8).

An internal noise shield provides superior common mode rejection of typically 10 kV/μs. The HCPL2601 and HCPL2631 has a minimum CMR of 5 kV/μs. The HCPL2611 has a minimum CMR of 10 kV/μs.

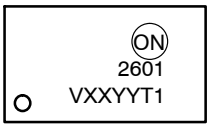
Features

- Very High Speed – 10 MBit/s
- Superior CMR – 10 kV/μs
- Double working voltage – 480 V
- Fan−out of 8 Over −40°C to +85°C
- Logic Gate Output
- Strobable Output
- Wired OR−open Collector
- U.L. Recognized (File # E90700)

Applications

- Ground Loop Elimination
- LSTTL to TTL, LSTTL or 5−volt CMOS
- Line Receiver, Data Transmission
- Data Multiplexing
- Switching Power Supplies
- Pulse Transformer Replacement
- Computer−peripheral Interface

MARKING DIAGRAM



2601	= Device Number
V	= VDE mark (Note: Only Appears on Parts Ordered with VDE Option – See Order Entry Table)
XX	= Two−Digit Year Code, e.g., ‘03’
YY	= Two−Digit Work Week, Ranging from ‘01’ to ‘53’
T1	= Assembly Package Code

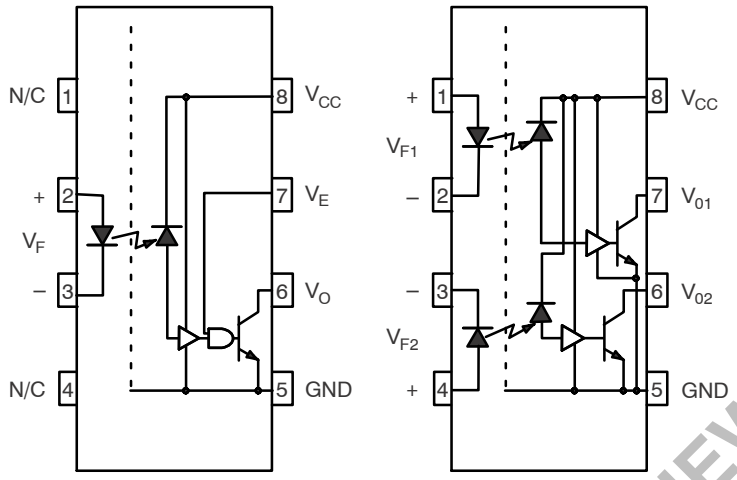
ORDERING INFORMATION

See detailed ordering and shipping information on page 10 of this data sheet.

DEVICE NOT RECOMMENDED FOR NEW DESIGN

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SCHEMATICS



6N137, HCPL2601, HCPL2611 | HCPL2630, HCPL2631

A 0.1 μF bypass capacitor must be connected between pins 8 and 5 (Note 1).

Figure 1. Schematics

TRUTH TABLE (Positive Logic)

Input	Enable	Output
H	H	L
L	H	H
H	L	H
L	L	H
H	NC	L
L	NC	H

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ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Symbol	Parameter		Value	Unit
T_{STG}	Storage Temperature		−55 to +125	°C
T_{OPR}	Operating Temperature		−40 to +85	°C
T_{SOL}	Lead Solder Temperature (for Wave Soldering Only)*		260 for 10 s	°C
EMITTER				
I_F	DC/Average Forward Input Current	Single Channel	50	mA
		Dual Channel (Each Channel)	30	
V_E	Enable Input Voltage Not to Exceed V_{CC} by More than 500 mV	Single Channel	5.5	V
V_R	Reverse Input Voltage	Each Channel	5.0	V
P_I	Power Dissipation	Single Channel	100	mW
		Dual Channel (Each Channel)	45	
DETECTOR				
V_{CC} (1 Minute Max)	Supply Voltage		7.0	V
I_O	Output Current	Single Channel	25	mA
		Dual Channel (Each Channel)	50	mA
V_O	Output Voltage	Each Channel	7.0	V
P_O	Collector Output Power Dissipation	Single Channel	85	mW
		Dual Channel (Each Channel)	60	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
*For peak soldering reflow, please refer to the Reflow Profile on page 9.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
I_{FL}	Input Current, Low Level	0	250	μA
I_{FH}	Input Current, High Level	*6.3	15	mA
V_{CC}	Supply Voltage, Output	4.5	5.5	V
V_{EL}	Enable Voltage, Low Level	0	0.8	V
V_{EH}	Enable Voltage, High Level	2.0	V_{CC}	V
T_A	Low Level Supply Current	−40	+85	°C
N	Fan Out (TTL Load)	−	8	

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.
*6.3 mA is a guard banded value which allows for at least 20% CTR degradation. Initial input current threshold value is 5.0 mA or less.

DEVICE NOT RECOMMENDED FOR NEW DESIGN

ELECTRICAL CHARACTERISTICS (T_A = 0°C to 70°C unless otherwise specified)

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
INDIVIDUAL COMPONENT CHARACTERISTICS							
EMITTER							
V_F	Input Forward Voltage	I_F = 10 mA		–	–	1.8	V
			T_A = 25°C	–	1.4	1.75	
B_{VR}	Input Reverse Breakdown Voltage	I_R = 10 μA		5.0	–	–	V
C_{IN}	Input Capacitance	V_F = 0, f = 1 MHz		–	60	–	pF
$\Delta V_F / \Delta T_A$	Input Diode Temperature Coefficient	I_F = 10 mA		–	−1.4	–	mV/°C
DETECTOR							
I_{CCH}	High Level Supply Current	V_{CC} = 5.5 V, I_F = 0 mA, V_E = 0.5 V	Single Channel	–	7	10	mA
			Dual Channel	–	10	15	
I_{CCL}	Low Level Supply Current	Single Channel	V_{CC} = 5.5 V, I_F = 10 mA	–	9	13	mA
		Dual Channel	V_E = 0.5 V	–	14	21	
I_{EL}	Low Level Enable Current	V_{CC} = 5.5 V, V_E = 0.5 V		–	−0.8	−1.6	mA
I_{EH}	High Level Enable Current	V_{CC} = 5.5 V, V_E = 2.0 V		–	−0.6	−1.6	mA
V_{EH}	High Level Enable Voltage	V_{CC} = 5.5 V, I_F = 10 mA		2.0	–	–	V
V_{EL}	Low Level Enable Voltage	V_{CC} = 5.5 V, I_F = 10 mA (Note 3)		–	–	0.8	V
SWITCHING CHARACTERISTICS (T_A = −40°C to +85°C, V_{CC} = 5 V, I_F = 7.5 mA unless otherwise specified)							
T_{PLH}	Propagation Delay Time to Output HIGH Level	R_L = 350 Ω, C_L = 15 pF (Note 4) (Figure 13)	T_A = 25°C	20	45	75	ns
				–	–	100	
T_{PHL}	Propagation Delay Time to Output LOW Level	T_A = 25°C (Note 5)		25	45	75	ns
		R_L = 350 Ω, C_L = 15 pF (Figure 13)		–	–	100	
$\lvert T_{PHL}-T_{PLH} \rvert$	Pulse Width Distortion	R_L = 350 Ω, C_L = 15 pF (Figure 13)		–	3	35	ns
t_r	Output Rise Time (10−90%)	R_L = 350 Ω, C_L = 15 pF (Note 6) (Figure 13)		–	50	–	ns
t_f	Output Rise Time (90−10%)	R_L = 350 Ω, C_L = 15 pF (Note 7) (Figure 13)		–	12	–	ns
t_{ELH}	Enable Propagation Delay Time to Output HIGH Level	I_F = 7.5 mA, V_{EH} = 3.5 V, R_L = 350 Ω, C_L = 15 pF (Note 8) (Figure 14)		–	20	–	ns
t_{EHL}	Enable Propagation Delay Time to Output LOW Level	I_F = 7.5 mA, V_{EH} = 3.5 V, R_L = 350 Ω, C_L = 15pF (Note 9) (Figure 14)		–	20	–	ns
$\lvert CM_H \rvert$	Common Mode Transient Immunity (at Output HIGH Level)	T_A = 25°C, $\lvert V_{CM} \rvert$ = 50 V (Peak), I_F = 0 mA, V_{OH} (Min.) = 2.0 V, R_L = 350 Ω (Note 10) (Figure 15)	6N137, HCPL2630	–	10,000	–	V/μs
			HCPL2601, HCPL2631	5000	10,000	–	
		$\lvert V_{CM} \rvert$ = 400 V	HCPL2611	10,000	15,000	–	V/μs
$\lvert CM_L \rvert$	Common Mode Transient Immunity (at Output LOW Level)	R_L = 350 Ω, I_F = 7.5 mA, V_{OL} (Max.) = 0.8 V, T_A = 25°C (Note 11) (Figure 15)	6N137, HCPL2630	–	10,000	–	
			HCPL2601, HCPL2631	5000	10,000	–	
		$\lvert V_{CM} \rvert$ = 400 V	HCPL2611	10,000	15,000	–	
TRANSFER CHARACTERISTICS (T_A = −40°C to +85°C unless otherwise specified)							
I_{OH}	HIGH Level Output Current	V_{CC} = 5.5 V, V_O = 5.5 V, I_F = 250 μA, V_E = 2.0V (Note 2)		–	–	100	μA
V_{OL}	LOW Level Output Current	V_{CC} = 5.5 V, I_F = 5 mA, V_E = 2.0 V, I_{CL} = 13 mA (Note 2)		–	.35	0.6	V
I_{FT}	Input Threshold Current	V_{CC} = 5.5 V, V_O = 0.6 V, V_E = 2.0 V, I_{OL} = 13 mA		–	3	5	mA

DEVICE NOT RECOMMENDED FOR NEW DESIGN

ELECTRICAL CHARACTERISTICS (T_A = 0°C to 70°C unless otherwise specified) (continued)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
ISOLATION CHARACTERISTICS (T_A = −40°C to +85°C unless otherwise specified)						
I_{I-O}	Input−Output Insulation Leakage Current	Relative Humidity = 45%, T_A = 25°C, t = 5 s, V_{I-O} = 3000 VDC (Note 12)	–	–	1.0*	μA
V_{ISO}	Withstand Insulation Test Voltage	RH < 50%, T_A = 25°C, $I_{I-O} \le$ 2 μA, t = 1 min. (Note 12)	2500	–	–	V_{RMS}
R_{I-O}	Resistance (Input to Output)	V_{I-O} = 500 V (Note 12)	–	10^{12}	–	Ω
C_{I-O}	Capacitance (Input to Output)	f = 1 MHz (Note 12)	–	0.6	–	pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

*All Typicals at V_{CC} = 5 V, T_A = 25°C

1. The V_{CC} supply to each optoisolator must be bypassed by a 0.1 μF capacitor or larger. This can be either a ceramic or solid tantalum capacitor with good high frequency characteristic and should be connected as close as possible to the package V_{CC} and GND pins of each device.
2. Each channel.
3. Enable Input − No pull up resistor required as the device has an internal pull up resistor.
4. t_{PLH} − Propagation delay is measured from the 3.75 mA level on the HIGH to LOW transition of the input current pulse to the 1.5 V level on the LOW to HIGH transition of the output voltage pulse.
5. t_{PHL} − Propagation delay is measured from the 3.75 mA level on the LOW to HIGH transition of the input current pulse to the 1.5 V level on the HIGH to LOW transition of the output voltage pulse.
6. t_r − Rise time is measured from the 10% to the 90% levels on the LOW to HIGH transition of the output pulse.
7. t_f − Fall time is measured from the 90% to the 10% levels on the HIGH to LOW transition of the output pulse.
8. t_{ELH} − Enable input propagation delay is measured from the 1.5 V level on the HIGH to LOW transition of the input voltage pulse to the 1.5 V level on the LOW to HIGH transition of the output voltage pulse.
9. t_{EHL} − Enable input propagation delay is measured from the 1.5 V level on the LOW to HIGH transition of the input voltage pulse to the 1.5 V level on the HIGH to LOW transition of the output voltage pulse.
10. CM_H − The maximum tolerable rate of rise of the common mode voltage to ensure the output will remain in the HIGH state (i.e., V_{OUT} > 2.0 V). Measured in volts per microsecond (V/μs).
11. CM_L − The maximum tolerable rate of rise of the common mode voltage to ensure the output will remain in the LOW output state (i.e., V_{OUT} < 0.8 V). Measured in volts per microsecond (V/μs).
12. Device considered a two−terminal device: Pins 1, 2, 3 and 4 shorted together, and Pins 5, 6, 7 and 8 shorted together.

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TYPICAL PERFORMANCE CURVES

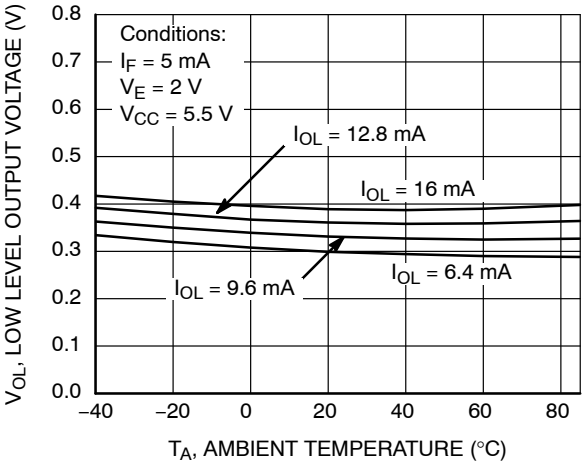


Figure 2. Low Level Output Voltage vs. Ambient Temperature

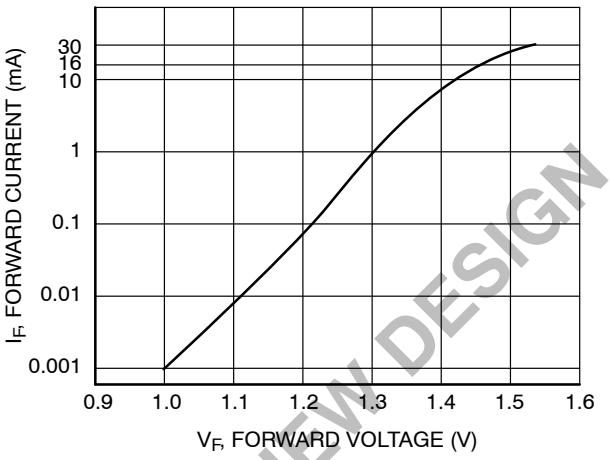


Figure 3. Input Diode Forward Voltage vs. Forward Current

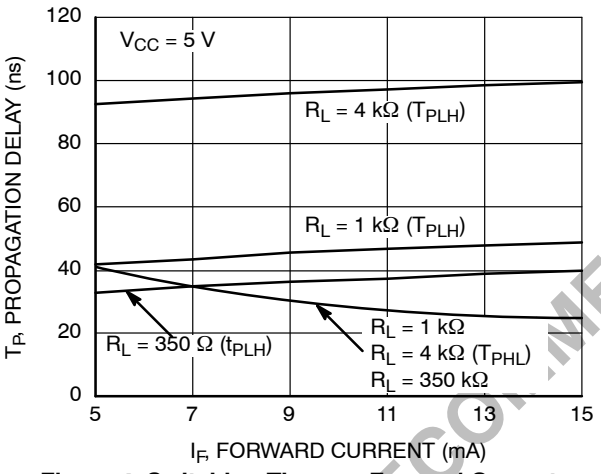


Figure 4. Switching Time vs. Forward Current

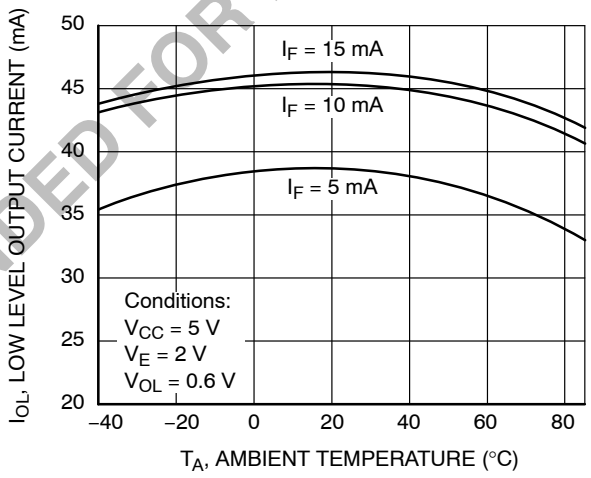


Figure 5. Low Level Output vs. Ambient Temperature

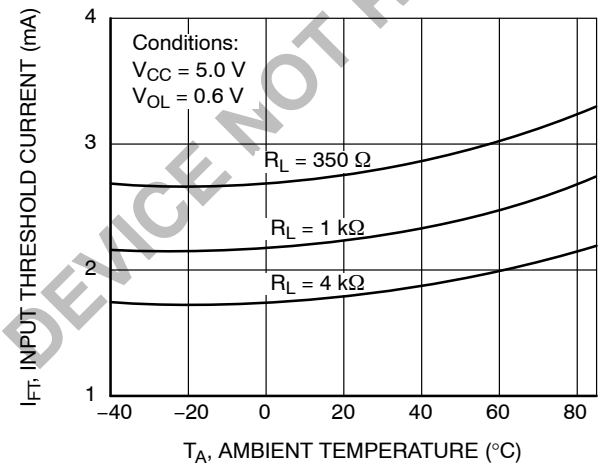


Figure 6. Input Threshold Current vs. Ambient Temperature

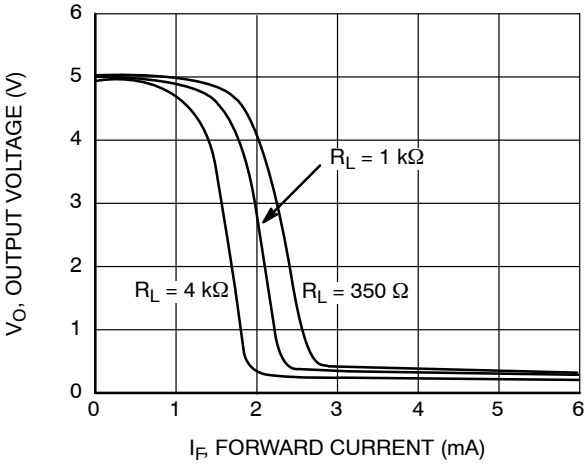


Figure 7. Output Voltage vs. Input Forward Current

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TYPICAL PERFORMANCE CURVES (Continued)

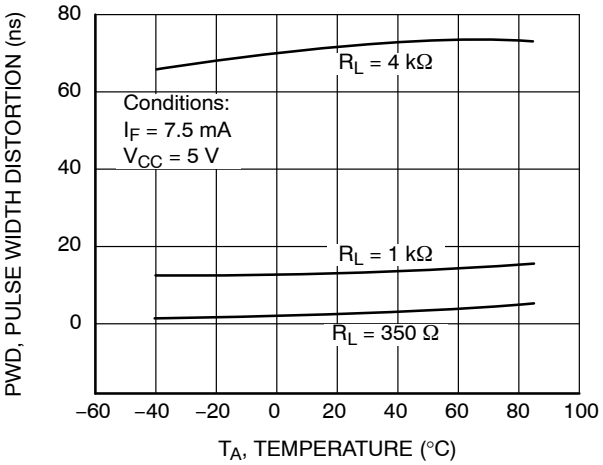


Figure 8. Pulse Width Distortion vs. Temperature

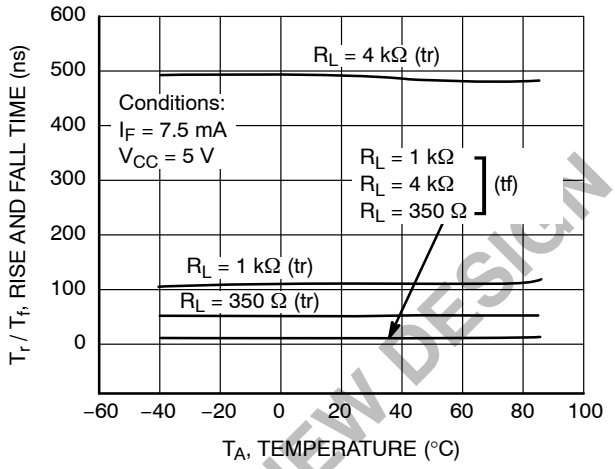


Figure 9. Rise and Fall Time vs. Temperature

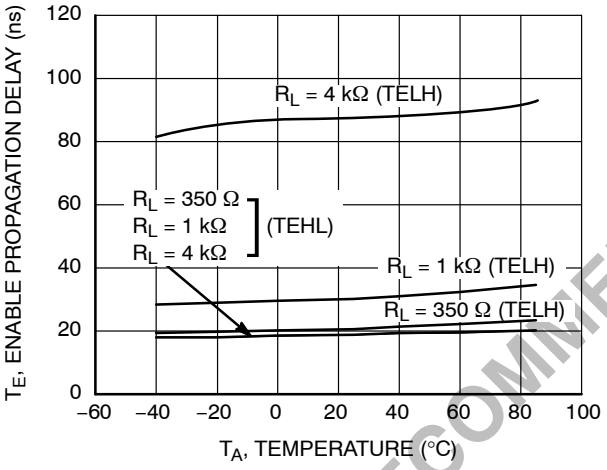


Figure 10. Enable Propagation Delay vs. Temperature

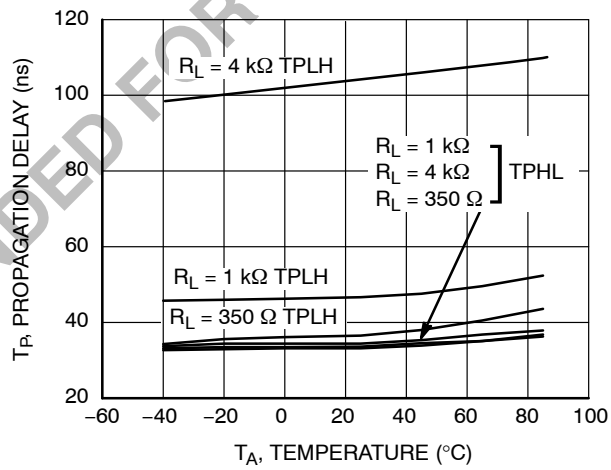


Figure 11. Switching Time vs. Temperature

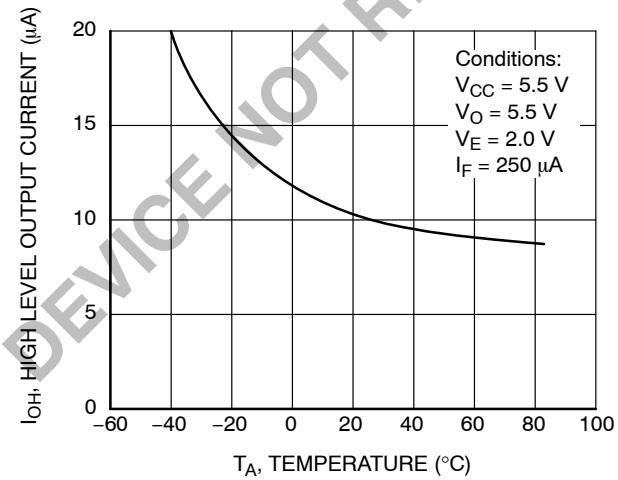


Figure 12. High Level Output Current vs. Temperature

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TEST CIRCUITS

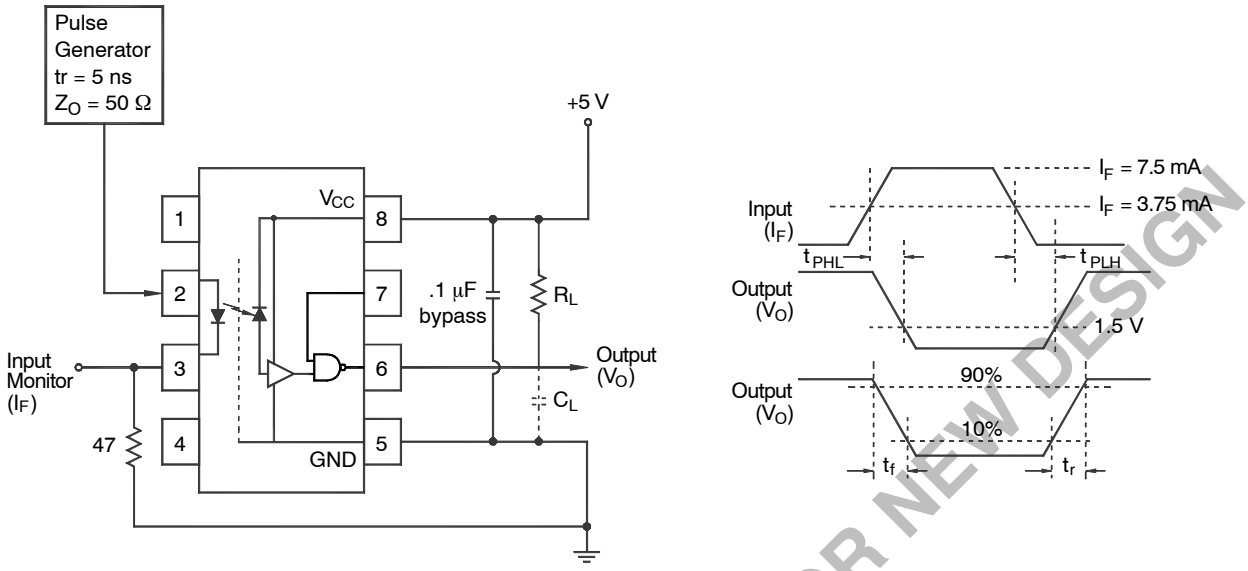


Figure 13. Test Circuit and Waveforms for t_{PLH}, t_{PHL}, t_r and t_f

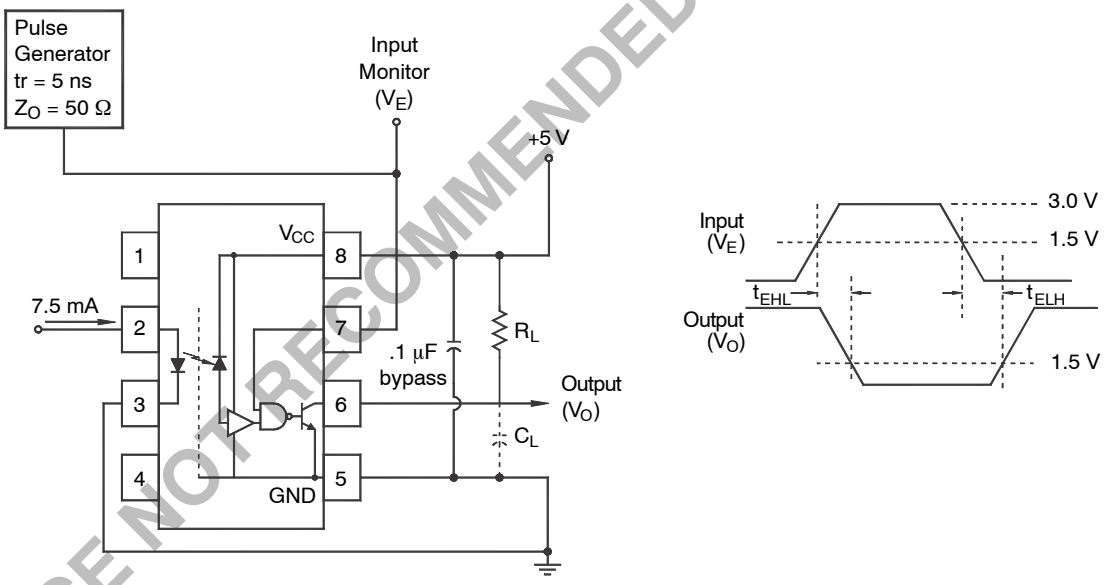


Figure 14. Test Circuit t_{EHL} and t_{ELH}

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TEST CIRCUITS (Continued)

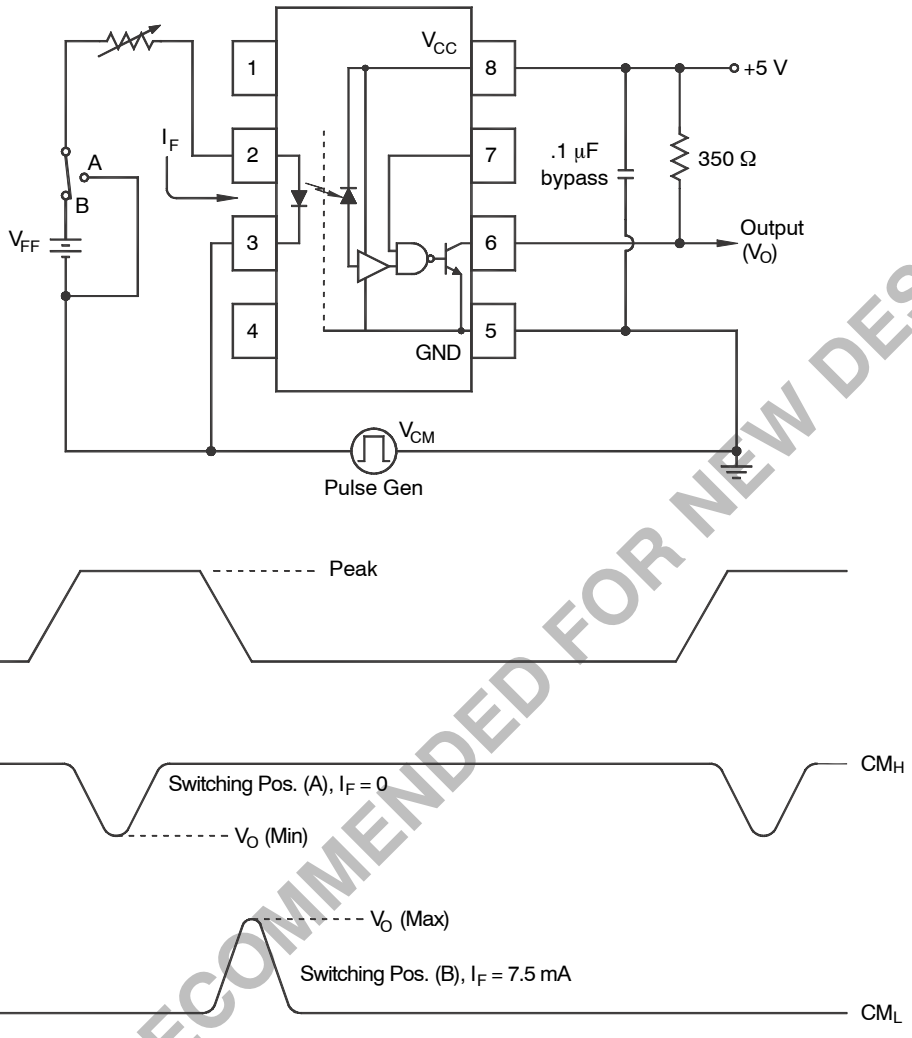
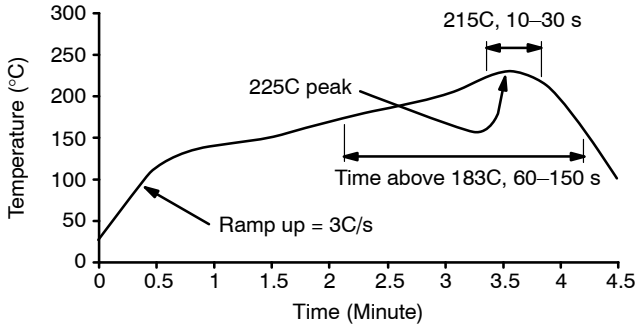


Figure 15. Test Circuit Common Mode Transient Immunity

REFLOW PROFILE



- Peak reflow temperature: 225C (package surface temperature)
- Time of temperature higher than 183C for 60–150 seconds
- One time soldering reflow is recommended

Figure 16. Reflow Profile

DEVICE NOT RECOMMENDED FOR NEW DESIGN

ORDERING INFORMATION

Option	Example Part Number	Description†
S	6N137S	PDIP8 GW, CASE 709AC Surface Mount Lead Bend
SD	6N137SD	PDIP8 GW, CASE 709AC Surface Mount; Tape and Reel
W	6N137W	PDIP8 6.6x3.81, 2.54P, CASE 646BW 0.4” Lead Spacing
V	6N137V	PDIP8 9.655x6.6, 2.54P, CASE 646CQ VDE0884
WV	6N137WV	PDIP8 6.6x3.81, 2.54P, CASE 646BW VDE0884; 0.4” Lead Spacing
SV	6N137SV	PDIP8 GW, CASE 709AC VDE0884; Surface Mount
SDV	6N137SDV	PDIP8 GW, CASE 709AC VDE0884; Surface Mount; Tape and Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

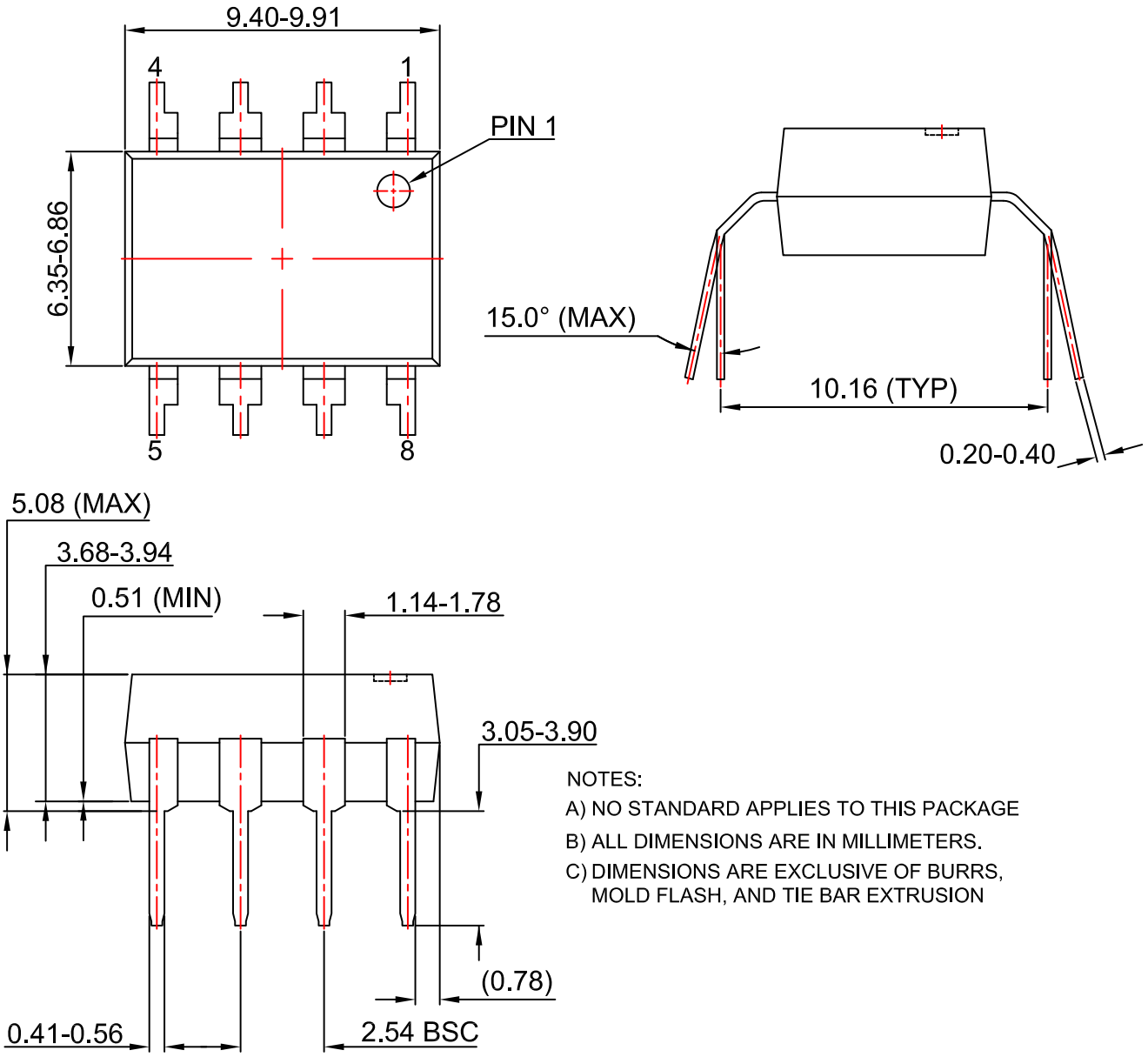
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MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

PDIP8 6.6x3.81, 2.54P
CASE 646BW
ISSUE O

DATE 31 JUL 2016



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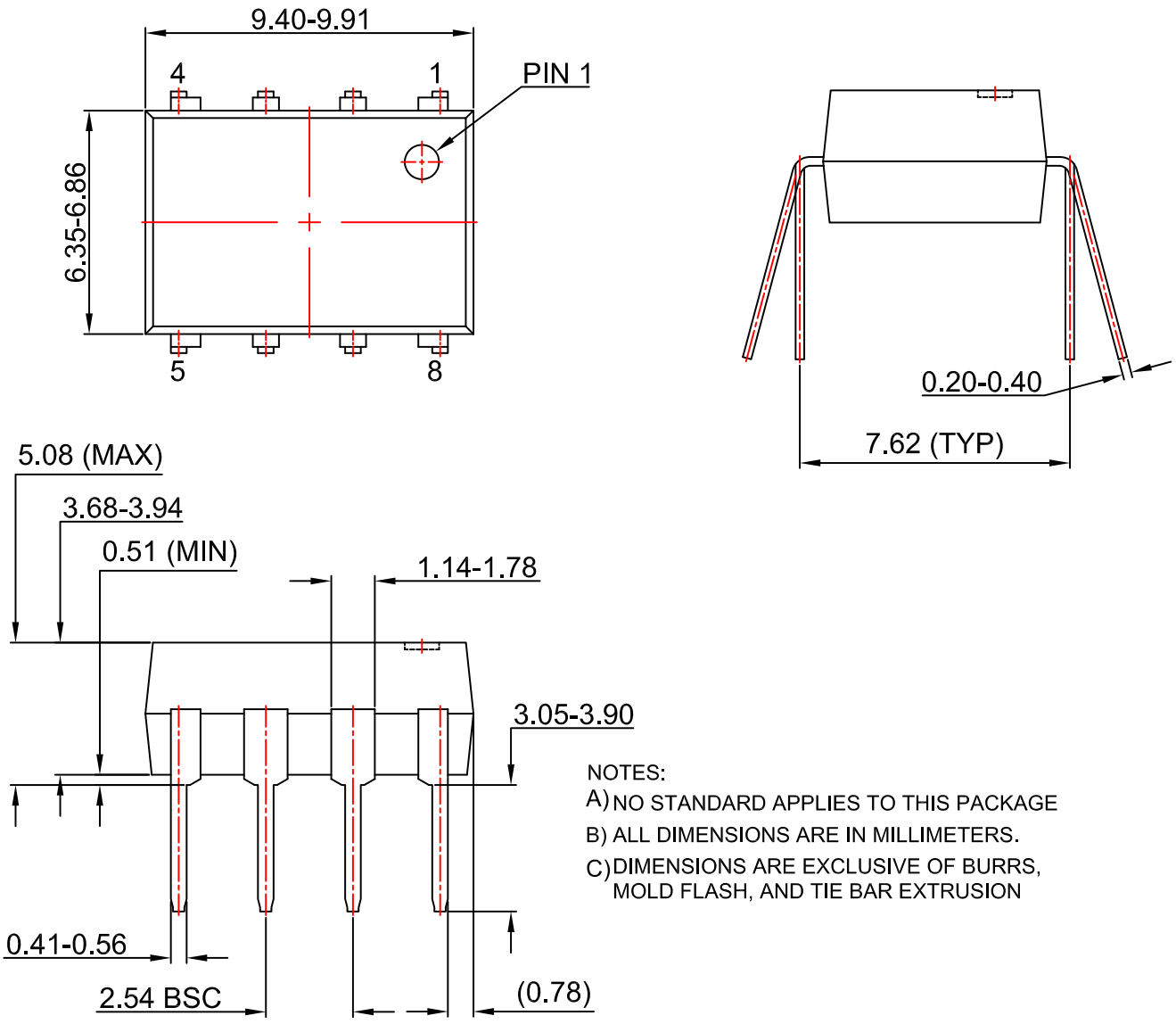
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PDIP8 9.655x6.6, 2.54P
CASE 646CQ
ISSUE O

DATE 18 SEP 2017



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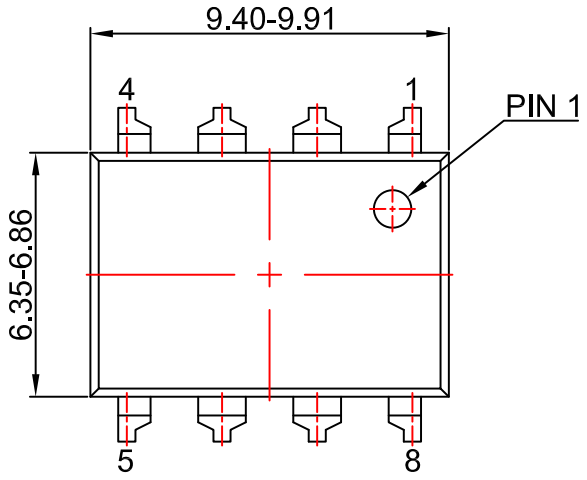
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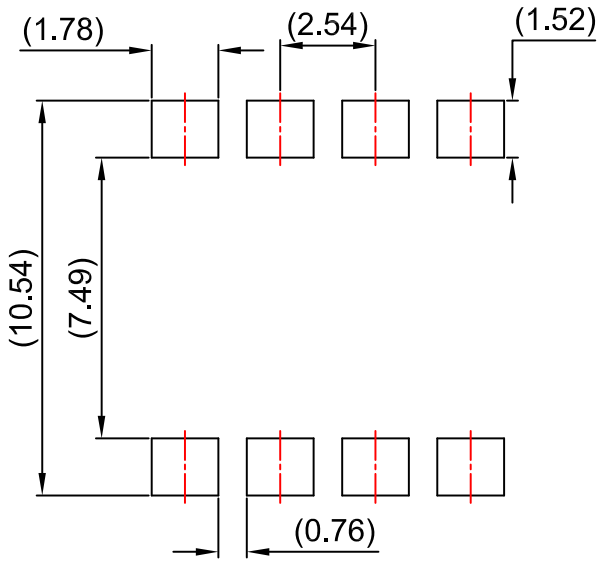
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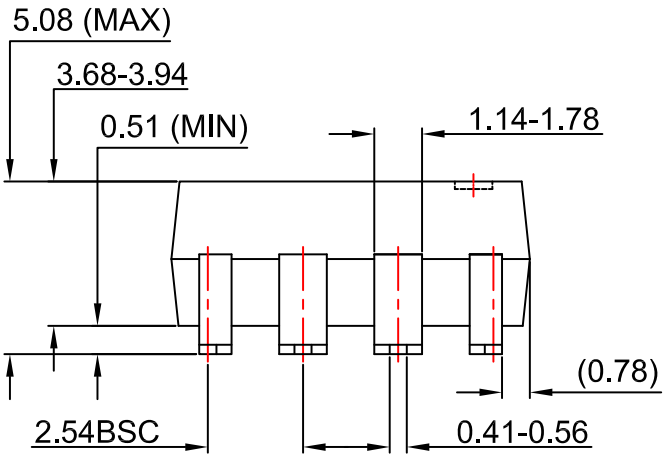
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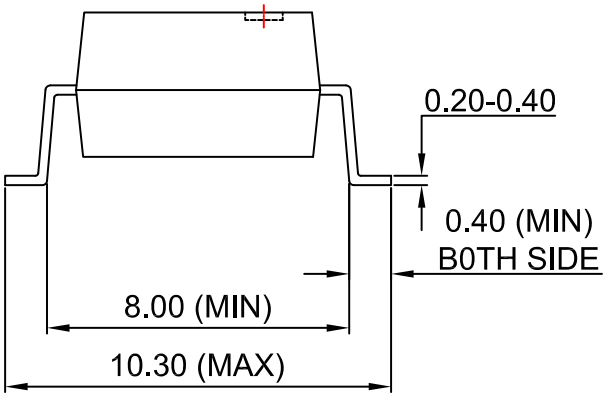
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