# AOZ8300CI-03

## Ultra-Low Capacitance TVS Diode Array

## General Description

The AOZ8300CI-03 is a transient voltage suppressor array designed to protect high speed data lines from ESD and lightning.

This device incorporates eight surge rated, low capacitance steering diodes and a TVS in a single package. During transient conditions, the steering diodes direct the transient to either the positive side of the power supply line or to ground. They AOZ8300CI-03 may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4. The TVS diodes provide effective suppression
of ESD voltages: ±15 kV (air discharge) and ±8 kV (contact discharge).

The AOZ8300CI-03 comes in a Halogen Free and RoHS compliant, SOT-23 package and is rated over a
-40 °C to +85 °C ambient temperature range. Both packages are compatible with lead free and SnPb assembly techniques. The small size, low capacitance, and high ESD protection makes the AOZ8300CI-03 ideal for protecting high speed video and data communication interfaces.

## Features

- ESD protection for high-speed data lines:
  - IEC 61000-4-2, level 4 (ESD) immunity test
  - ±30 kV (air discharge) and ±30 kV (contact discharge)
  - IEC 61000-4-5 (Lightning) 25 A (8/20 µs)
  - IEC 61000-4-4 (EFT) 40 A (5/50 ns)
  - Human Body Model (HBM) ±30 kV
- Protects four I/O lines
- Low clamping voltage

## Applications

- Low-Voltage Differential Signaling (LVDS)
- USB 2.0 power and data line protection
- Video graphics cards
- Monitors and flat panel displays
- Digital Video Interface (DVI)
- 10/100/1000 Ethernet
- Notebook computers

Green Product

## Typical Application

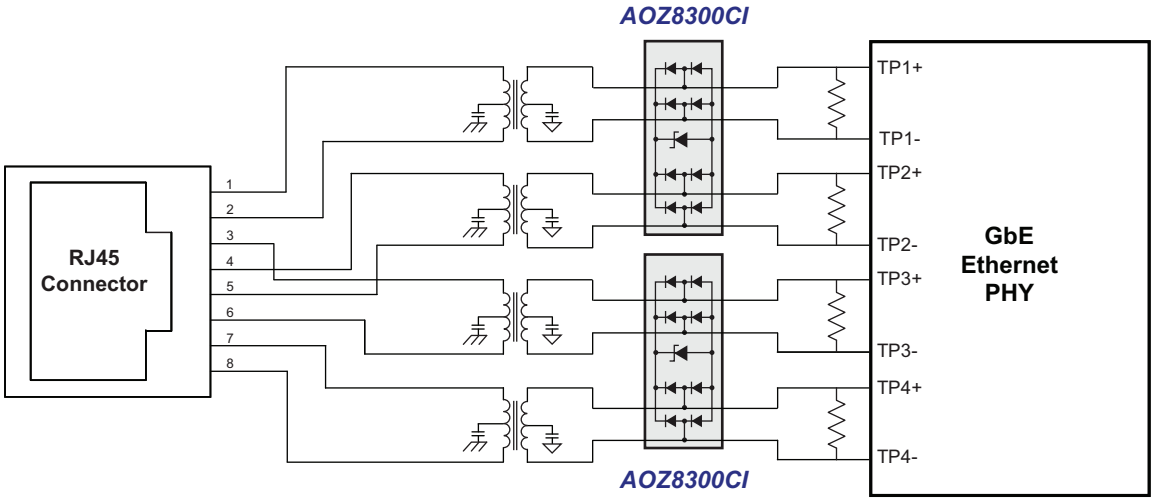


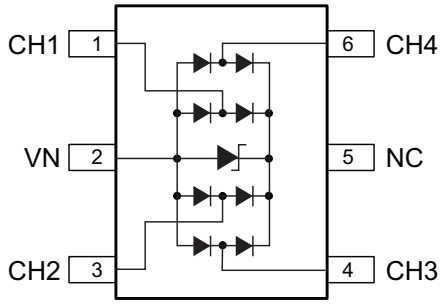

**Figure 1. 10/100/1000 Ethernet Port Connection**

## Ordering Information

| Part Number | Ambient Temperature Range | Package | Environmental |
|---|---|---|---|
| AOZ8300CI-03 | -40 °C to +85 °C | SOT23-6 | Green Product |

AOS Green Products use reduced levels of Halogens, and are also RoHS compliant.
Please visit www.aosmd.com/media/AOSGreenPolicy.pdf for additional information.

## Pin Configuration




**SOT23-6**
**(Top View)**

## Absolute Maximum Ratings

Exceeding the Absolute Maximum ratings may damage the device.

| Parameter | Rating |
|---|---|
| Peak Pulse Current ($I_{PP}$), $t_P$ = 8/20 µs | 25 A |
| Peak Power Dissipation (8 x 20 µs @ 25 °C) | 300 W |
| Storage Temperature ($T_S$) | -65 °C to +150 °C |
| ESD Rating per IEC61000-4-2, Contact(1) | ±30 kV |
| ESD Rating per IEC61000-4-2, Air(1) | ±30 kV |
| ESD Rating per Human Body Model(2) | ±30 kV |

**Notes**:

1. IEC 61000-4-2 discharge with $C_{Discharge}$ = 150 pF, $R_{Discharge}$ = 330 Ω.
2. Human Body Discharge per MIL-STD-883, Method 3015 $C_{Discharge}$ = 100 pF, $R_{Discharge}$ = 1.5 kΩ.

## Maximum Operating Ratings

| Parameter | Rating |
|---|---|
| Junction Temperature ($T_J$) | -40 °C to +125 °C |

## Electrical Characteristics

$T_A$ = 25°C unless otherwise specified.

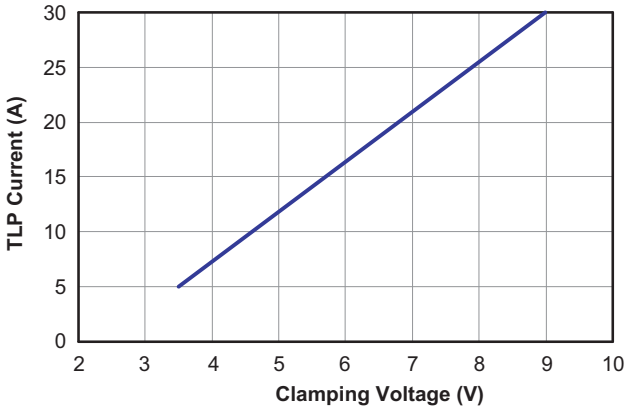
| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $I_R$ | Reverse Leakage Current | $V_{RWM}$ = 2.5 V, between I/O and VIN | | | 0.1 | µA |
| $V_F$ | Diode Forward Voltage | $I_F$ = 15 mA | 0.70 | 0.85 | 1.0 | V |
| $C_j$ | Junction Capacitance | $V_R$ = 0 V, f = 1 MHz, any I/O pin to Ground | | 2.5 | 3.5 | pF |
| $\Delta C_j$ | Channel Input Capacitance Matching | $V_R$ = 0 V, f = 1 MHz, between I/O pins(3) | | | 0.2 | pF |
| $V_{RWM}$ | Reverse Working Voltage | Between I/O and VIN(4) | | | 3.3 | V |
| $V_{BR}$ | Reverse Breakdown Voltage | $I_T$ = 100 µA, between I/O and VIN(5) | 5.0 | | | V |
| $V_{HOLD}$ | Holding Reverse Voltage | Any I/O pin to Ground | | 1.0 | | V |
| $I_{HOLD}$ | Holding Reverse Current | Any I/O pin to Ground | | 10 | | mA |
| $V_{CL}$ | Channel Clamp Voltage<br>Positive Transients<br>Negative Transient | $I_{PP}$ = 5 A, tp = 100 ns, any I/O pin to Ground(3)(6) | | | <br>2.6<br>-2.7 | <br>V<br>V |
| | Channel Clamp Voltage<br>Positive Transients<br>Negative Transient | $I_{PP}$ = 10 A, tp = 100 ns, any I/O pin to Ground(3)(6) | | | <br>3.0<br>-3.3 | <br>V<br>V |
| | Channel Clamp Voltage<br>Positive Transients<br>Negative Transient | $I_{PP}$ = 30 A, tp = 100 ns, any I/O pin to Ground(3)(6) | | | <br>5.0<br>-8.0 | <br>V<br>V |
| | Clamping Voltage(3) (IEC61000-4-5, 8/20µs, I/O Pin-to-Ground) | $I_{PP}$ = 5 A<br>$I_{PP}$ = -5 A | | | 3.9<br>-4.1 | V<br>V |
| | | $I_{PP}$ = 25 A<br>$I_{PP}$ = -25 A | | | 10.5<br>-11.5 | V<br>V |
| $R_{DNY}$ | Dynamic Resistance (100ns Transmission Line Pulse) | $I_{TLP}$ = 1 A to 30 A<br>$I_{TLP}$ = -1 A to -30 A | | 0.15<br>0.17 | | Ω<br>Ω |
| | Dynamic Resistance (IEC61000-4-5, 8/20µs) | $I_{TLP}$ = 2 A to 25 A<br>$I_{TLP}$ = -2 A to -25 A | | 0.35<br>0.40 | | Ω<br>Ω |

**Notes:**

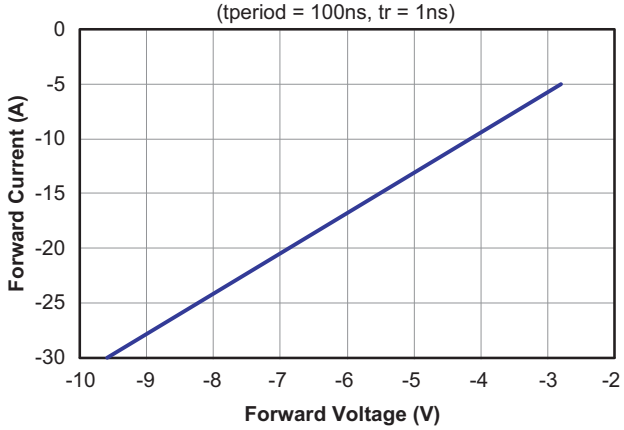
3. These specifications are guaranteed by design.
4. The working peak reverse voltage, $V_{RWM}$, should be equal to or greater than the DC or continuous peak operating voltage level.
5. $V_{BR}$ is measured at the pulse test current $I_T$.
6. Measurements performed using a 100 ns Transmission Line Pulse (TLP) system.

## Typical Performance Characteristics

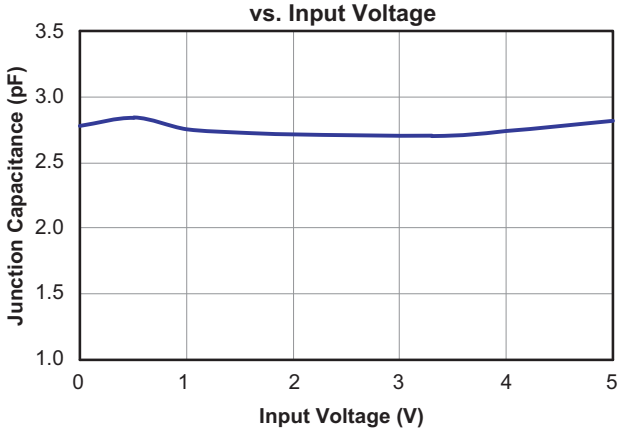
TLP Current vs. Clamping Voltage



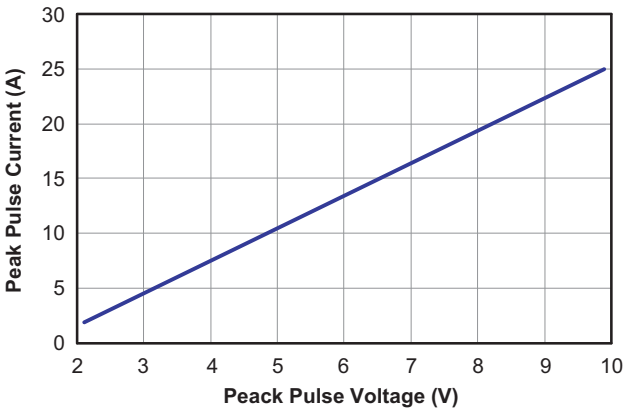

Forward Current vs. Forward Voltage
(tperiod = 100ns, tr = 1ns)



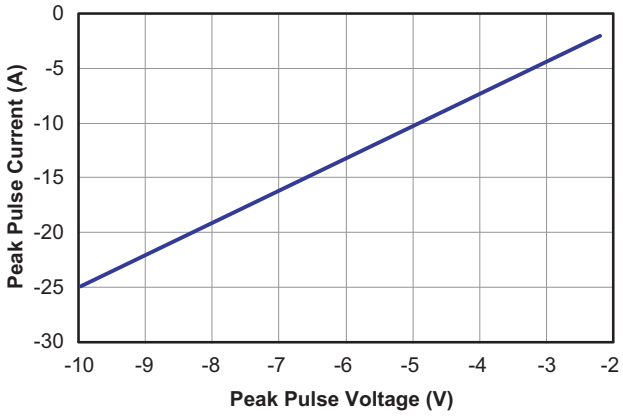

Typical Variation of Junctions Capacitance vs. Input Voltage




IEC61000-4-5 8/20µs Positive Surge




IEC61000-4-5 8/20µs Negative Surge



## Application Information

The AOZ8300CI-03 TVS is design to protect up to four data lines from damaging transient over-voltage by clamping the voltage to a reference. When the transient on a protected data line exceeds the reference voltage, the steering diode is forward bias thereby conducting the harmful ESD transient away from the sensitive circuitry under protection.

### PCB Layout Guidelines

Printed circuit board layout is key to achieving the highest level of surge immunity on power and data lines. The location of the protection devices on the PCB is the most important design consideration. The AOZ8300CI-03 devices should be located as close as possible to the noise source. AOZ8300CI-03 devices should be used on all data and power lines that enter or exit the PCB at the I/O connector.

In most systems, surge pulses occur on data and power lines that enter the PCB through the I/O connector. Placing the AOZ8300CI-03 devices as close as possible to the noise source ensures that a surge voltage will be clamped before the pulse is coupled into adjacent PCB traces. In addition, the PCB should use the shortest possible traces. A short trace length equates to low impedance, which ensures that the surge energy will be dissipated by the AOZ8300CI-03 device. Long signal traces will act as antennas and receive energy from fields that are produced by the ESD pulse. By keeping line lengths as short as possible, the efficiency of the line to act as an antenna for ESD related fields is reduced. Minimize interconnecting line lengths by placing devices with the most interconnects as close together as possible. The protection circuits should shunt the surge voltage to either the reference or chassis ground. Shunting the surge voltage directly to the IC's signal ground may cause ground bounce. The clamping performance of the TVS diodes on a single ground PCB can be improved by minimizing the impedance with relatively short and wide ground traces.

The PCB layout and IC package parasitic inductances can cause significant overshoot to the TVS's clamping voltage. The inductance of the PCB can be reduced by using short trace lengths and multiple layers with separate ground and power planes. One effective method to minimize loop problems is to incorporate a ground plane in the PCB design. The AOZ8300CI-03 ultra-low capacitance TVS is designed to protect four high speed data transmission lines from transient over-voltages by clamping them to a fixed reference. The low inductance and construction minimizes voltage overshoot during high current surges. When the voltage on the protected line exceeds the reference voltage the internal steering diodes are forward biased, conducting the transient current away from the sensitive circuitry.

Good circuit board layout is critical for the suppression of ESD induced transients. The following guidelines are recommended:

1. Place the TVS near the IO terminals or connectors to restrict transient coupling.
2. Fill unused portions of the PCB with ground plane.
3. Minimize the path length between the TVS and the protected line.
4. Minimize all conductive loops including power and ground loops.
5. The ESD transient return path to ground should be kept as short as possible.
6. Never run critical signals near board edges.
7. Use ground planes whenever possible.
8. Avoid running critical signal traces (clocks, resets, etc.) near PCB edges.
9. Separate chassis ground traces from components and signal traces by at least 4mm.
10. Keep the chassis ground trace length-to-width ratio < 5:1 to minimize inductance.
11. Protect all external connections with TVS diodes.

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