MP3426

6A, 35V Boost Converter with Programmable Switching Frequency and UVLO

The Future of Analog IC Technology

DESCRIPTION

The MP3426 is a current-mode step-up converter with a 6A, 90mΩ internal switch that provides a highly efficient regulator with a fast response. The MP3426 features a programmable frequency of up to 2MHz that allows for easy filtering and reduces noise. An external compensation pin gives the user flexibility in setting loop dynamics, and uses small, low-ESR, ceramic output capacitors. Soft-start results in a small inrush current and can be programmed with an external capacitor. The MP3426 operates from an input voltage as low as 3.2V and can generate up to a 35V output.

The MP3426's features include under-voltage lockout, current limiting, and thermal overload protection. The MP3426 is available in a low-profile 14-pin 3mm×4mm QFN package with an exposed pad.

FEATURES

- 6A, 90mΩ, 45V Power MOSFET
- Uses Very Small Capacitors and Inductors
- Wide Input Range: 3.2V to 22V
- Output Voltage as High as 35V
- Programmable f_{sw}: 300kHz to 2MHz
- Programmable UVLO, Soft-Start, UVLO Hysteresis
- Micropower Shutdown <1μA
- Thermal Shutdown 160°C
- Available in 14-Pin 3mm×4mm QFN Package

APPLICATIONS

- Telecom—Power Supplies
- Audio—Microphone and Tuner Bias
- Automotive

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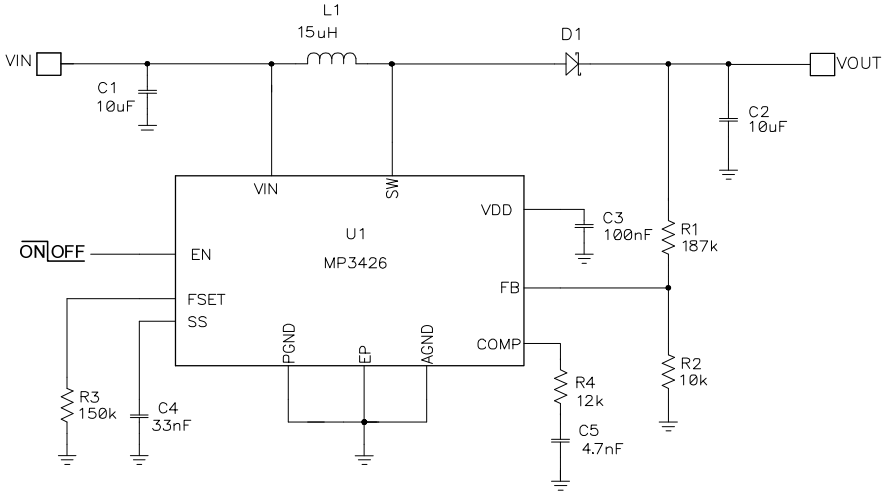
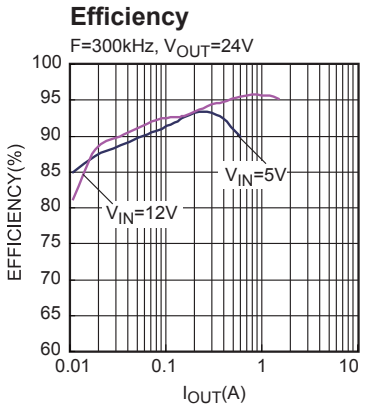
TYPICAL APPLICATION



24V, 1A Output



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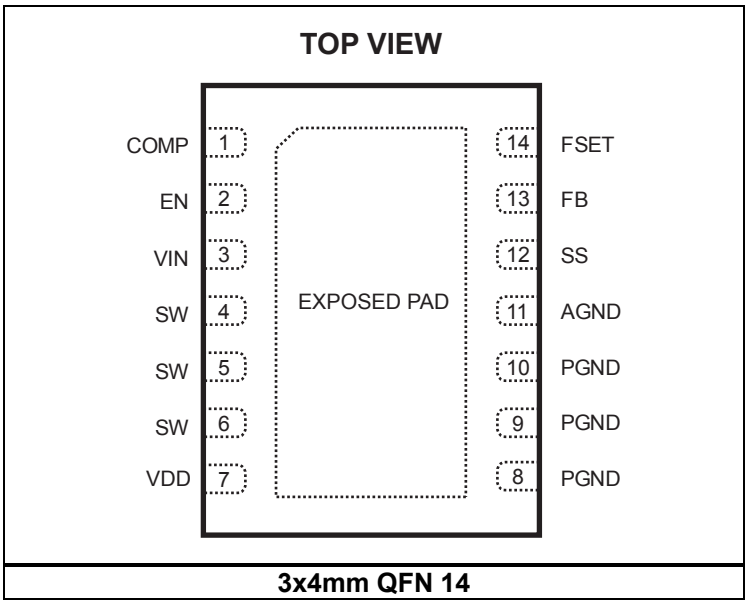
ORDERING INFORMATION

Part Number*	Package	Top Marking	Free Air Temperature (T_A)
MP3426DL	QFN-14(3mmx4mm)	3426	-40°C to 85°C

* For Tape & Reel, add suffix –Z (e.g. MP3426DL–Z);
For RoHS compliant packaging, add suffix –LF (e.g. MP3426DL–LF–Z)

PACKAGE REFERENCE



3x4mm QFN 14

ABSOLUTE MAXIMUM RATINGS (1)

SW .....-0.5V to +45V
IN .....-0.5V to +24V
All Other Pins.....-0.3V to +6.5V
Continuous Power Dissipation (T_A = +25°C) (2)
QFN14 ..... 2.5W
Junction Temperature.....150°C
Lead Temperature .....260°C
Storage Temperature..... -65°C to +150°C

Recommended Operating Conditions (3)

Supply Voltage V_{IN} .....3.2V to 22V
Output Voltage V_{OUT}.....3.2V to 35V
Operating Junction Temp (T_J). - 40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN-14(3mmx4mm) .....50 ..... 12 ... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D(MAX)=(T_J(MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = V_{EN} = 5V, T_A = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Operating Input Voltage	V_{IN}		3.2		22	V
Under-Voltage Lockout		V_{IN} Rising	2.8		3.1	V
Under-Voltage Lockout Hysteresis				250		mV
VDD Voltage Gate Drive Voltage Supply	V_{VDD}	C = 10nF		5.6	5.9	V
Supply Current (Shutdown)		V_{EN} = 0V			1	μA
Supply Current (Quiescent)		V_{FB} = 1.35V		650	900	μA
Switching Frequency		R_{FSET} = 84.5kΩ	450	540	630	kHz
Minimum OFF Time		V_{FB} = 0V		80	150	ns
Minimum ON Time(5)		V_{FB} = 1.35V		100		ns
EN Turn-On Threshold(6)		V_{EN} Rising (switching)	1.45	1.5	1.55	V
EN High Threshold (Micro power)		V_{EN} Rising			1.0	V
EN Low Threshold (Micro power)		V_{EN} Falling	0.5			V
EN Input Bias Current		V_{EN} = 0V, 5V		0.1	1	μA
UVLO Hysteresis Current to EN(6)		1.0 < EN < 1.4		4		μA
Soft-Start Current			4	6	8	μA
FB Voltage			1.200	1.225	1.250	V
FB Input Bias Current			-200	-100		nA
Error Amp. Voltage Gain(5)	A_{VEA}			300		V/V
Error Amp. Transconductance ($\frac{\mu A}{V}$)	G_{EA}			160		μA/V
Error Amp. Output Current				15		μA
GCS : I_{SW}/V_{COMP}	G_{CS}			18		A/V
SW ON Resistance	R_{ON}	I_{SW} = 100mA		90		mΩ
SW Current Limit		Duty Cycle = 0%	6.8	8.5		A
Thermal Shutdown(5)				160		°C

Notes:

5) Guaranteed by design, not tested.

6) Refer to the “APPLICATION INFORMATION-EN UVLO Hysteresis”.

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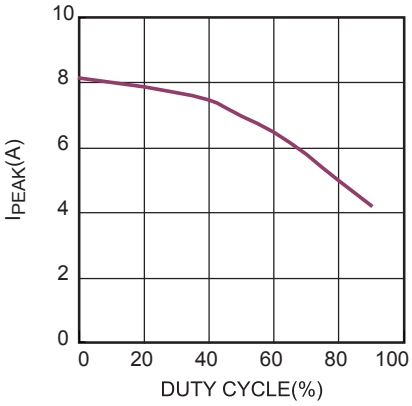
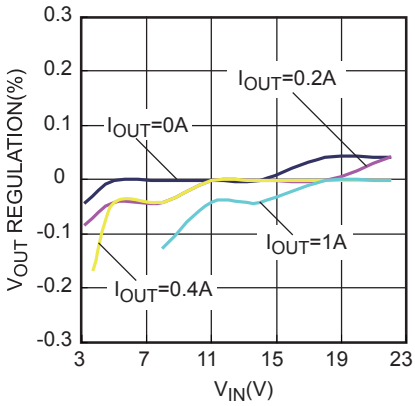
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN}=12V, V_{OUT}=24V, L=15µH, C_{OUT}=4.7µF×2, f_{SW}=300kHz, T_A=+25°C, unless otherwise noted.

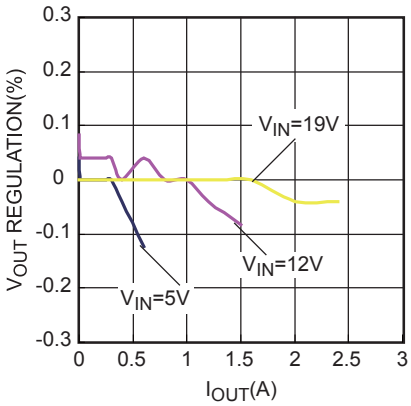
I_{LIMIT} vs. Duty Cycle



Line Regulation

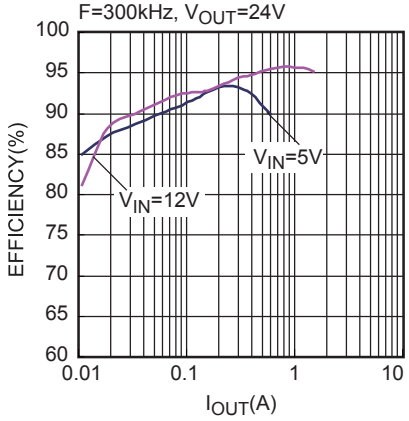


Load Regulation



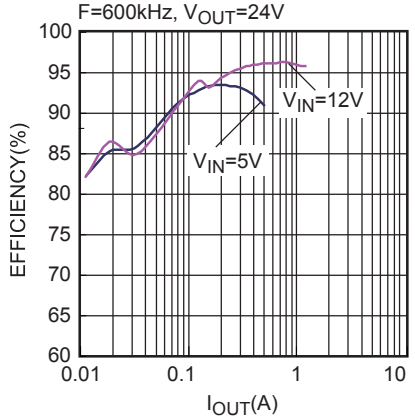
Efficiency

F=300kHz, V_{OUT}=24V



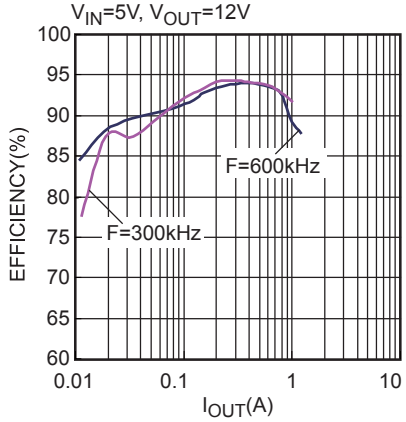
Efficiency

F=600kHz, V_{OUT}=24V



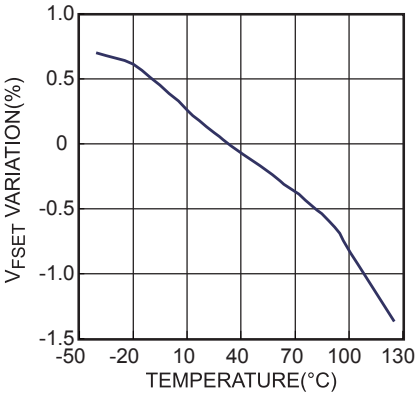
Efficiency

V_{IN}=5V, V_{OUT}=12V

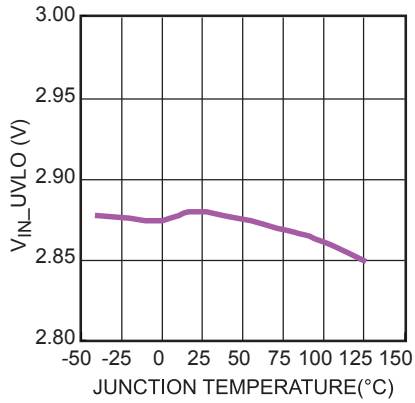


V_{FSET} vs. Temperature

Refer to 0.5V

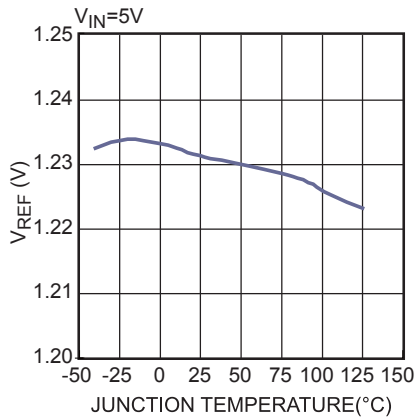


V_{IN} UVLO vs. Junction Temperature



V_{REF} vs. Junction Temperature

V_{IN}=5V



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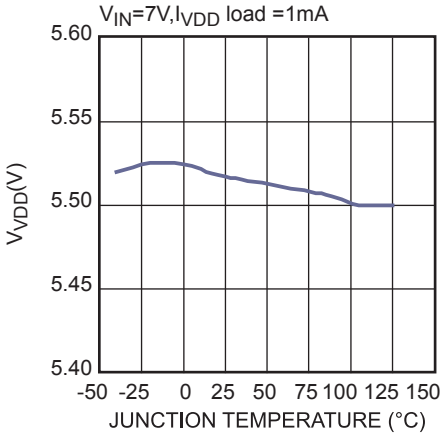
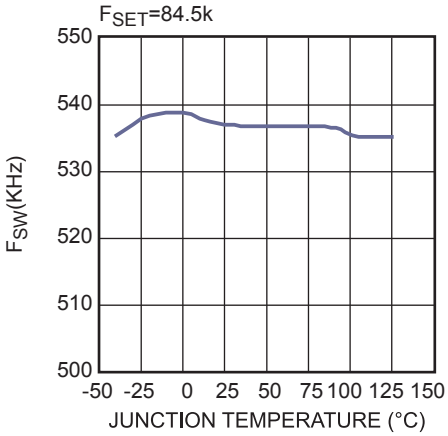
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN}=12V, V_{OUT}=24V, L=15µH, C_{OUT}=4.7µF×2, f_{SW}=300kHz, T_A=+25°C, unless otherwise noted.

V_{DD} vs. Junction Temperature



F_{SW} vs. Junction Temperature



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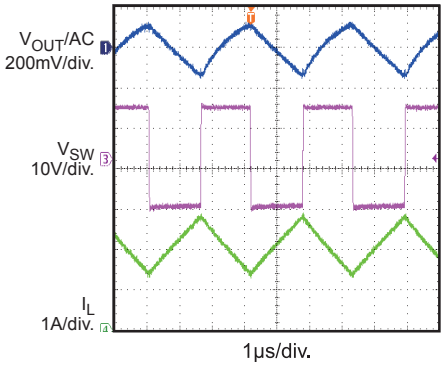
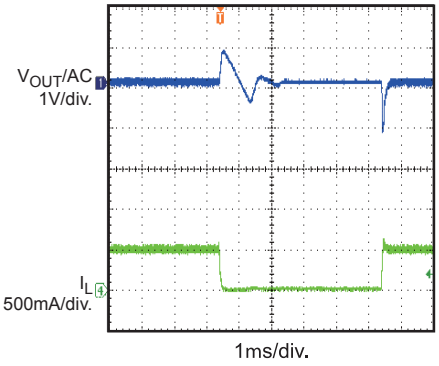
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN}=12V, V_{OUT}=24V, L=15µH, C_{OUT}=4.7µF×2, f_{SW}=300kHz, T_A=+25°C, unless otherwise noted.

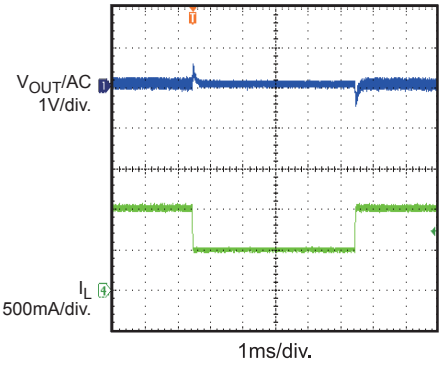
VOUT Ripple
I_{OUT}=1A



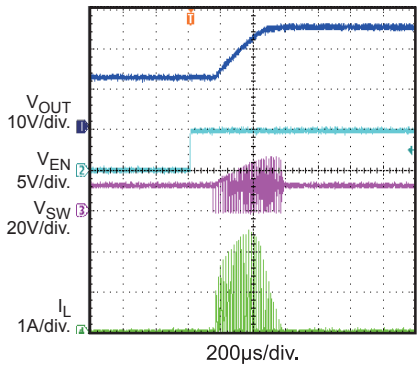
Load Transient Response
I_{OUT}=0->0.5A, 0.1A/µs



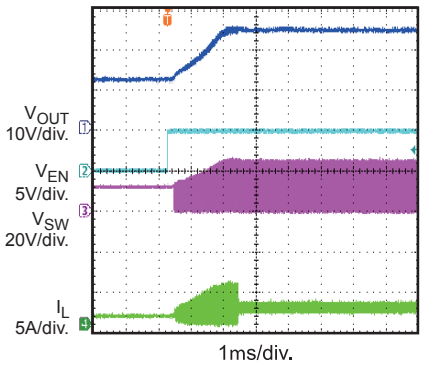
Load Transient Response
I_{OUT}=0.5A->1A, 0.1A/µs



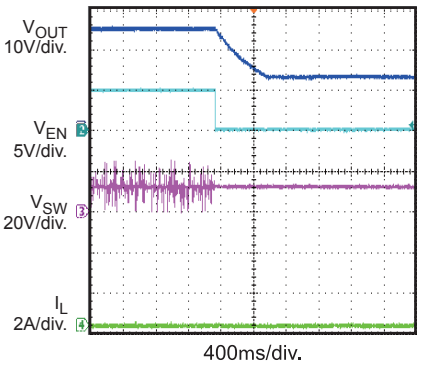
EN Startup
I_{OUT}=0A



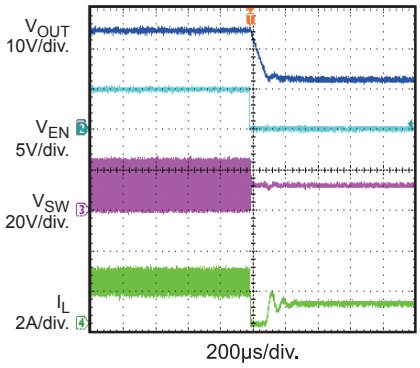
EN Startup
I_{OUT}=1A



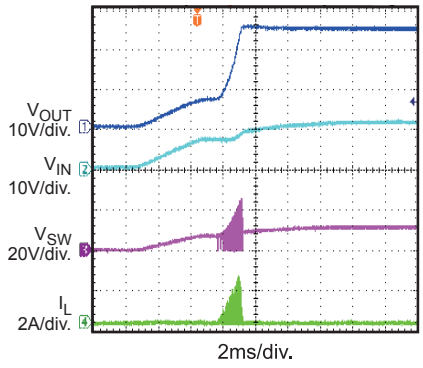
EN Shutodwn
I_{OUT}=0A



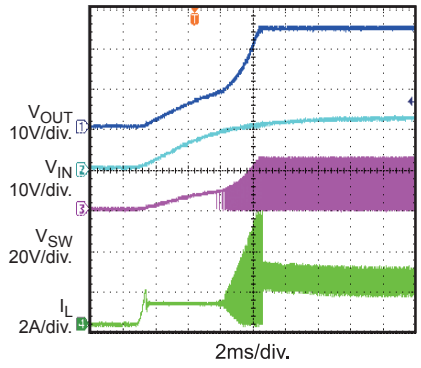
EN Shutdown
I_{OUT}=1A



VIN Startup
I_{OUT}=0A



VIN Startup
I_{OUT}=1A



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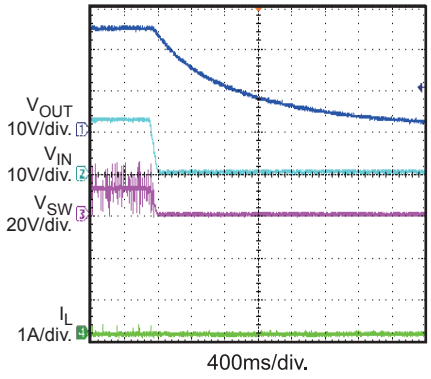
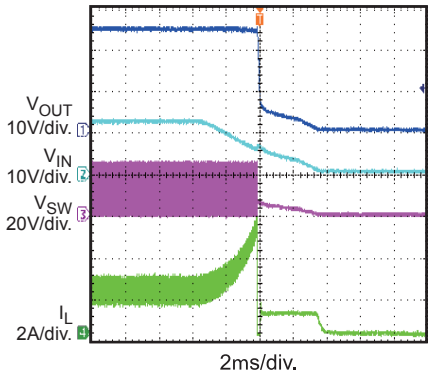
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN}=12V, V_{OUT}=24V, L=15µH, C_{OUT}=4.7µF×2, f_{SW}=300kHz, T_A=+25°C, unless otherwise noted.

VIN SHUTDOWN
I_{OUT}=0A



VIN SHUTDOWN
I_{OUT}=1A



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PIN FUNCTIONS

QFN14 Pin #	Name	Description
1	COMP	Compensation. Connect a capacitor and resistor in series to Analog ground for loop stability.
2	EN	Regulator On/Off Control Input. A high input at EN turns on the converter, and a low input turns it off. When not used, connect EN to the input source (through a 100kΩ pull-up resistor if V_{IN} > 6V) for automatic startup. EN pin can also be used to program VIN UVLO. Do not leave EN floating.
3	VIN	Input Supply. VIN must be locally bypassed.
4, 5, 6	SW	Power Switch Output. SW is the drain of the internal MOSFET switch. Connect to the power inductor and output rectifier.
7	VDD	LDO Output for internal power supply.
8, 9, 10,	PGND	Power Ground.
11	AGND	Analog Ground. Connect to the exposed pad at a single point.
12	SS	Soft-Start. Connect a soft-start capacitor to this pin. The soft-start capacitor charges from a 6μA constant current. Leave disconnected if the soft-start is not used.
13	FB	Feedback Input. Reference voltage is 1.225V. Connect a resistor divider to this pin.
14	FSET	Frequency Set. Connect a resistor from this pin to AGND. FSET pin voltage is internally regulated to 0.5V. The current flowing out of this pin linearly sets the operating frequency.
15	EP	Exposed Pad. The bottom exposed pad is the power ground. For best thermal dissipation, solder the exposed pad to the underlying GND cooper backplane.

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BLOCK DIAGRAM

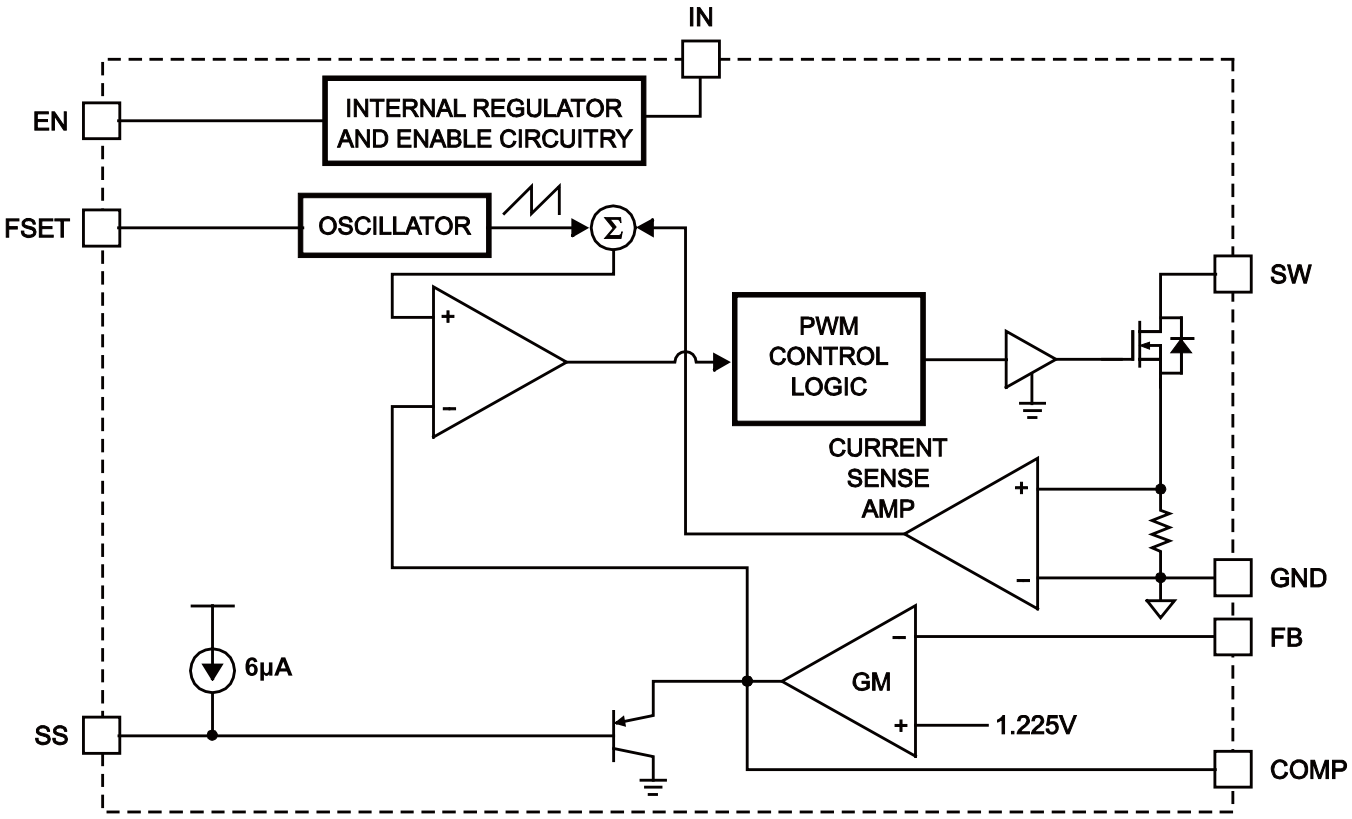

Figure 1: Functional Block Diagram

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APPLICATION INFORMATION

Components referenced below apply to the Typical Application Circuits in Figure 4.

Theory of Operation

The MP3426 uses a constant-frequency, peak-current–mode, boost regulator architecture to regulate the feedback voltage. Refer to the functional block diagram for the MP3426's operating principles.

At the beginning of each cycle, the N-Channel MOSFET switch turns on, causing the inductor current to rise. The current-sense amplifier (CSA) at the switch's source internally converts the switch current to a voltage. This voltage goes to a comparator that compares it to the COMP voltage. The COMP voltage is the output of the error amplifier, which is an amplified version of the difference between the 1.225V reference voltage and V_{FB}.

When V_{CSA} and V_{COMP} are equal, the PWM comparator turns off the switch to force the inductor current through the external rectifier to the output capacitor. This decreases the inductor current. V_{COMP} controls the peak inductor current, which is controlled by the output voltage. The output voltage is regulated by the inductor current to satisfy the load. Current-mode regulation improves the transient response and control-loop stability.

Selecting the Switching Frequency

The switching frequency is set by the FSET resistor (R_{FSET}), where:

$$f_{FSET} = 23 \times (R_{FSET}^{-0.86})$$

Where R_{FSET} is in kΩ and f_{FSET} is in MHz.

EN UVLO Hysteresis

The MP3426 features a programmable UVLO hysteresis. Upon power up a 4μA current sink (I_{SINK}) is applied to the EN pin, requiring a higher V_{IN} to overcome the current sink. That extra voltage on VIN equals

$$(I_{SINK} + I_{R_BOTTOM}) \times R_{TOP} + V_{EN}$$

Once the EN pin reaches about 1.5V (the EN turn-on threshold), the MP3426 starts and the current sink turns off to create the reverse hysteresis for V_{IN} falling. This hysteresis is determined by:

$$UVLO Hysteresis = 4\mu A \times R_{TOP}$$

At the same time V_{IN} startup threshold is determined by its UVLO or:

$$V_{IN} = 1.5 \times \frac{R_{TOP} + R_{BOTTOM}}{R_{BOTTOM}} + UVLO Hysteresis$$

Depending on whichever is higher.V_{IN} in unit V and R_{TOP}/R_{BOTTOM} in MΩ.

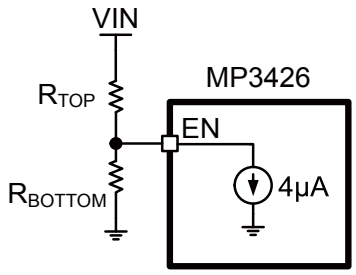

Figure 2: EN Resistor Divider

Table 1: Switching Frequency vs. FSET Resistor Values

R_{FSET} (kΩ)	Freq (MHz)
180	0.26
160	0.29
150	0.31
143	0.32
66.5	0.62
35.7	1.06
25	1.44
18	1.91
16	2.12

Selecting the Soft-Start Capacitor

The MP3426 includes a soft-start timer that limits the COMP voltage during startup to prevent excessive input current. This prevents premature source voltage termination at startup due to input-current overshoot. When power is applied to the MP3426, and EN goes HIGH, a 6μA internal current source charges the external SS capacitor. As the SS capacitor charges, the SS

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voltage rises. When the SS voltage reaches 250mV, the MP3426 starts switching at 1/5 the programmed frequency (frequency fold-back mode). At 800mV the switching frequency rises to the programmed value. The soft-start ends when the SS voltage reaches 2.5V. This limits the inductor current at start-up, forcing the input current to rise slowly to the required current to regulate the output voltage.

The soft-start period is determined by the equation:

$$t_{SS} = \frac{C_{SS} \times 10^{-9} \times 2.5V}{6\mu A}$$

Where C_{SS} (nF) is the soft-start capacitor from SS to GND, and t_{SS} is the soft-start period.

Setting the Output Voltage

V_{OUT} connects to the top of a resistor divider (R2 and R3); the resistor divider's tap connects to the FB pin. The feedback voltage is typically 1.225V. The output voltage is then:

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R2}{R3}\right)$$

Where:

R2 is the top feedback resistor
R3 is the bottom feedback resistor
V_{FB} is the feedback reference voltage (typically 1.225V)

To increase efficiency, use ≥10kΩ bottom feedback resistors.

Selecting the Input Capacitor

The input requires a capacitor to supply the AC ripple current to the inductor, while limiting noise at the input source. Use a low-ESR capacitor with a value >4.7μF to minimize the IC noise. Ceramic capacitors are preferred, but tantalum or low-ESR electrolytic capacitors can also suffice. However since it absorbs the input switching current it requires an adequate ripple current rating. Use a capacitor with an RMS current rating greater than the inductor ripple current.

To ensure stable operation, place the input capacitor as close to the IC as possible. As an alternative, place a small, high-quality ceramic 0.1μF capacitor close to the IC and place the larger capacitor further away. If using the latter technique, use either tantalum- or electrolytic-type capacitors for the larger capacitor. Place all ceramic capacitors close to the MP3426.

Selecting the Output Capacitor

The output capacitor maintains the DC output voltage. For best results, use low-ESR capacitors to minimize the output voltage ripple. The output capacitor's characteristics also affect regulatory control system's stability. For best results, use ceramic, tantalum, or low-ESR electrolytic capacitors. For ceramic capacitors, the capacitance dominates the impedance at the switching frequency, and so the output voltage ripple is mostly independent of the ESR. The output voltage ripple is estimated as

$$V_{RIPPLE} \cong I_{LOAD} \times \frac{1 - \frac{V_{IN}}{V_{OUT}}}{C_{OUT} \times f_{SW}}:$$

Where V_{RIPPLE} is the output ripple voltage, V_{IN} and V_{OUT} are the DC input and output voltages, respectively, I_{LOAD} is the load current, f_{SW} is the switching frequency, and C_{OUT} is the value of the output capacitor.

For tantalum or low-ESR electrolytic capacitors, the ESR dominates the impedance at the switching frequency, and so the output ripple is:

$$V_{RIPPLE} \cong I_{LOAD} \times \frac{1 - \frac{V_{IN}}{V_{OUT}}}{C_{OUT} \times f_{SW}} + \frac{I_{LOAD} \times R_{ESR} \times V_{OUT}}{V_{IN}}$$

Where R_{ESR} is the equivalent series resistance of the output capacitors.

Choose an output capacitor that satisfies the output ripple and load transient requirements of the design. A 4.7μF-to-22μF ceramic capacitor is suitable for most applications.

Selecting the Inductor

The inductor forces the output voltage higher than the input voltage. A larger inductor value results in less ripple current and reduces the peak inductor current; this reduces the stress on the internal N-channel switch. However, a larger-value inductor is physically larger, has a higher series resistance, and/or lower saturation current.

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A good rule of thumb is to allow the peak-to-peak ripple current to equal 30% to 50% of the maximum input current. Make sure that the peak inductor current is less than 75% of the current limit during duty-cycle operation to prevent regulator losses due to the current limit. Also make sure that the inductor does not saturate under the worst-case load transient and startup conditions. Calculate the required inductance value using the following equations:

$$L = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{V_{OUT} \times f_{SW} \times \Delta I}$$

$$I_{IN(max)} = \frac{V_{OUT} \times I_{LOAD(MAX)}}{V_{IN} \times \eta}$$

Where:

I_{LOAD}(max) = maximum load current
ΔI = peak-to-peak inductor ripple current
ΔI = (30% to 50%) × $I_{IN\ (MAX)}$
η = efficiency.

Selecting the Diode

The output rectifier diode supplies current to the inductor when the internal MOSFET is off. Use a Schottky diode to reduce losses due to the diode forward voltage and recovery time. The diode should be rated for a reverse voltage equal to or greater than the expected output voltage. The average current rating must exceed the maximum expected load current, and the peak current rating must exceed the peak inductor current.

Compensation

The output of the transconductance error amplifier (COMP) compensates the regulation control system. The system uses two poles and one zero to stabilize the control loop. The poles are f_{P1} (set by the output capacitor C_{OUT} and the load resistance) and f_{P2} (start from origin), the zero is f_{Z1} (set by the compensation capacitor C_{COMP} and the compensation resistor R_{COMP}). These are determined by the equations:

$$f_{P1} = \frac{1}{2 \times \Pi \times R_{LOAD} \times C_{OUT}} (Hz)$$

$$f_{P2} = \frac{G_{EA}}{2 \times \Pi \times A_{VEA} \times C_{COMP}} (Hz)$$

$$f_{Z1} = \frac{1}{2 \times \Pi \times R_{COMP} \times C_{COMP}} (Hz)$$

Where R_{LOAD} is the load resistance, G_{EA} is the error amplifier transconductance, and A_{VEA} is the error amplifier voltage gain.

The DC loop gain is

$$A_{VDC} = \frac{A_{VEA} \times V_{IN} \times R_{LOAD} \times V_{FB} \times G_{CS}}{0.5 \times V_{OUT}^2} (V/V)$$

Where G_{CS} is the compensation voltage/inductor current gain, and the V_{FB} is the feedback regulation threshold.

There is also a right-half-plane zero (f_{RHPZ}) that exists in continuous conduction mode (the inductor current does not drop to zero for each cycle). The f_{RHPZ} is:

$$f_{RHPZ} = \frac{R_{LOAD}}{2 \times \Pi \times L} \times \left(\frac{V_{IN}}{V_{OUT}} \right)^2 (Hz)$$

Table 2 lists a few compensation component combinations for different input voltages, output voltages and capacitances for the most-frequently–used output ceramic capacitors. Ceramic capacitors generally have extremely low ESR, and therefore do not require the second compensation capacitor (from COMP to GND).

For faster control loop and better transient response, select C_{COMP} (C7) from Table 2: Recommended Component Values. Then gradually increase the R_{COMP} (R6) value and check the load step response to find a value that minimizes any output voltage ringing or overshoot at the load step edge. Finally, check the compensator design by calculating the DC loop gain and the crossover frequency. The crossover frequency where the loop gain drops to 0dB (a gain of 1) can be obtained visually by placing a -20dB/decade slope at each pole, and a +20dB/decade slope at each zero. The crossover frequency should be at least one decade below the f_{RHPZ} at the maximum output load current to obtain a high-enough phase margin for stability.

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Table 2: Recommended Component Values

V_{IN} (V)	V_{OUT} (V)	C_{OUT} (µF)	R_{COMP} (kΩ)	C_{COMP} (nF)	Switching Frequency (kHz)	Inductor (µH)
3.2	12	4.7	10	6.8	600	8.2
3.2	12	10	15	6.8	600	8.2
3.2	12	22	30	6.8	600	8.2
5	12	10	12	4.9	600	6.8
5	12	22	25	4.9	600	6.8
5	18	4.7	12	4.9	600	10
5	18	10	25	4.9	600	10
5	18	22	50	4.9	600	10
12	24	4.7	10	6.8	600	10
12	24	10	20	6.8	600	10
12	24	22	40	6.8	600	10

Layout Considerations

High frequency switching regulators require very careful layout for stable operation and low noise. Place all components as close to the IC as possible. Keep the path between L1, D1, and C_{OUT} extremely short to minimize noise and ringing. Place C_{IN} close to the VIN pin to maximize decoupling. Keep all feedback components close to the FB pin to prevent noise injection on the FB pin trace. Tie the C_{IN} and C_{OUT} ground returns close to the GND pin. Figure 3 shows the recommended component placement for the MP3426.

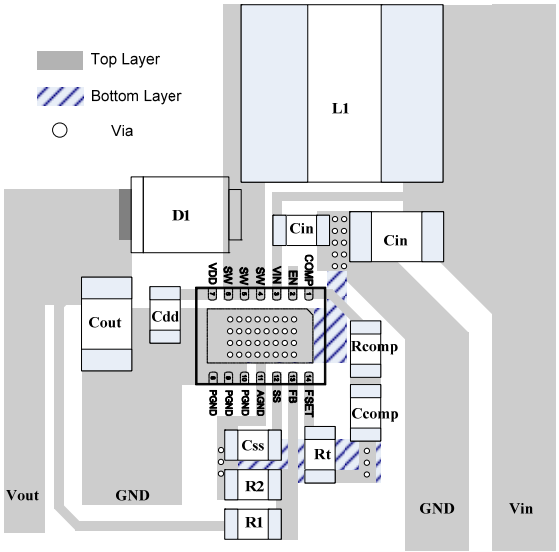

Figure 3: Recommended PCB Layout

Design example

Below is a design example following the application guidelines for the following specifications:

Table 3: Design Example

V_{IN}	8V-22V
V_{OUT}	24V
f_{SW}	300kHz

The typical application circuit for VOUT = 24V on page 14 shows the detailed application schematic, and is the basis for the typical performance and circuit waveforms. For more detailed device applications, please refer to the schematic in Figure 5.

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TYPICAL APPLICATION CIRCUIT

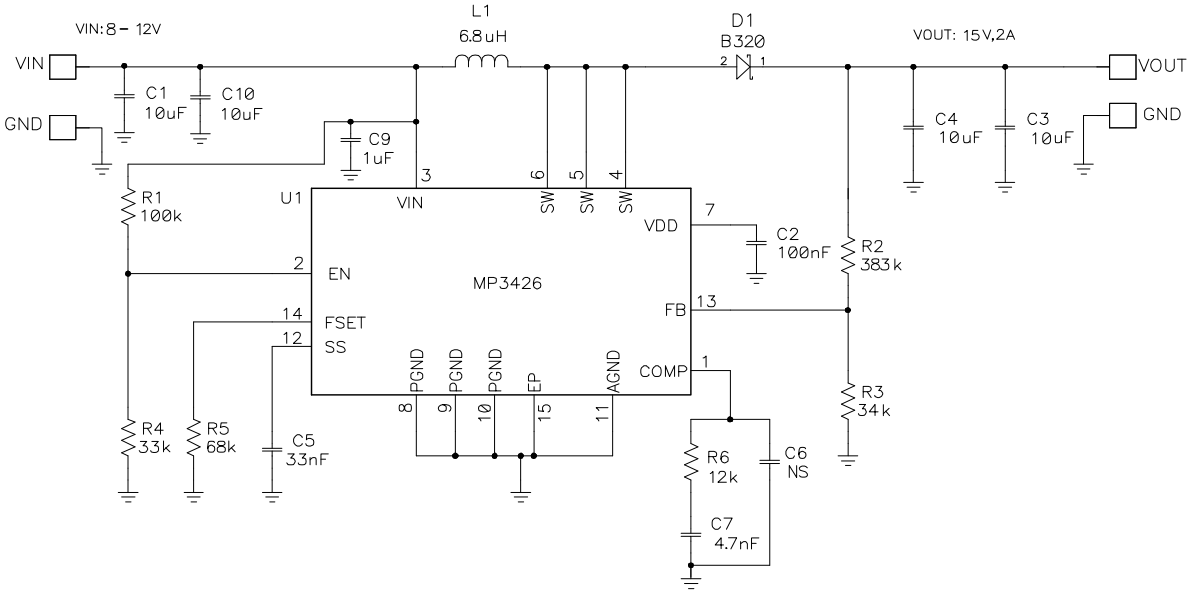

Figure 4: Typical Application Schematic—15V Output

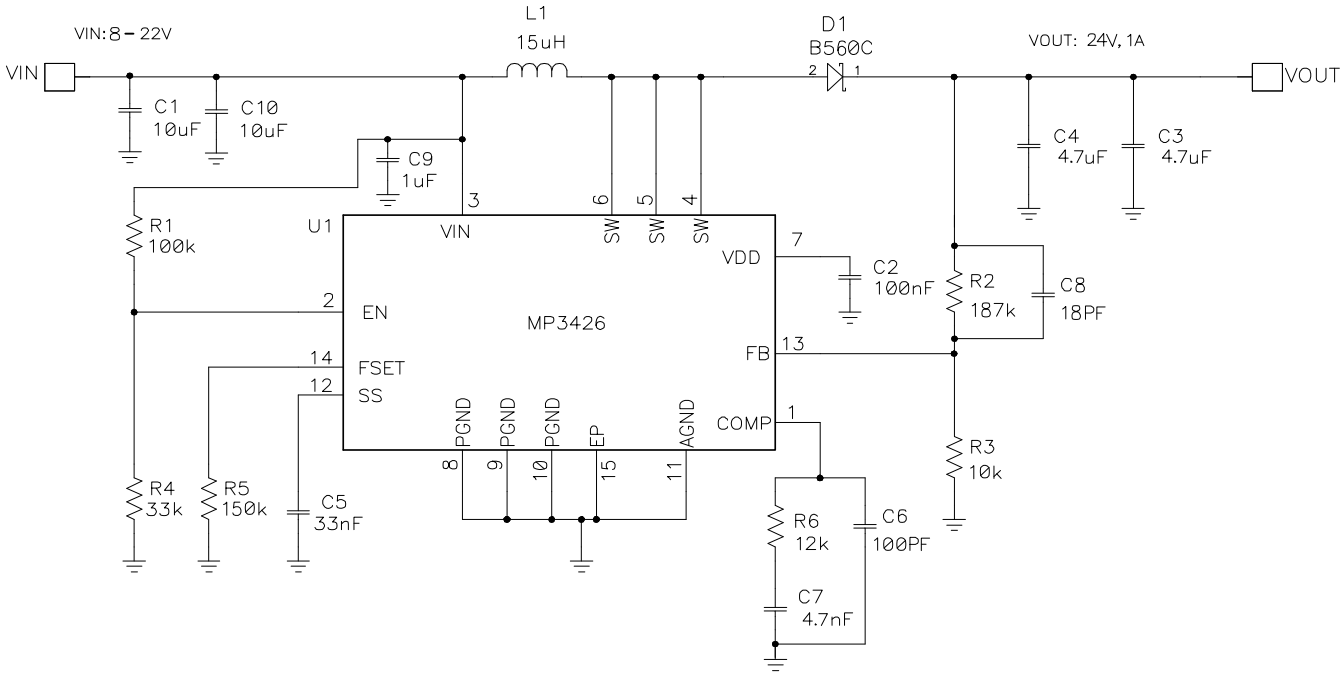

Figure 5: Typical Application Schematic—24V Output

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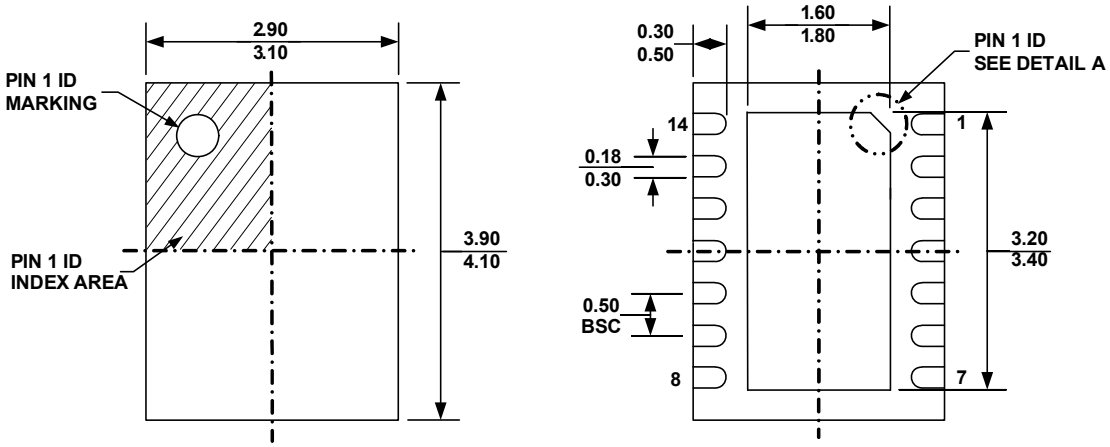
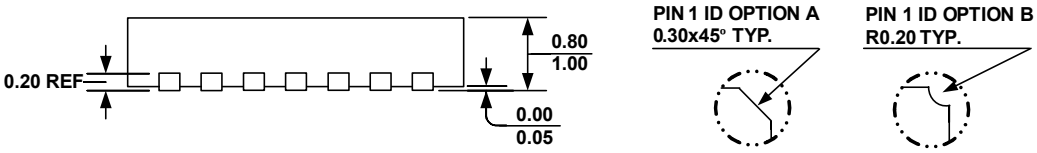
PACKAGE INFORMATION

QFN-14(3mmX4mm)



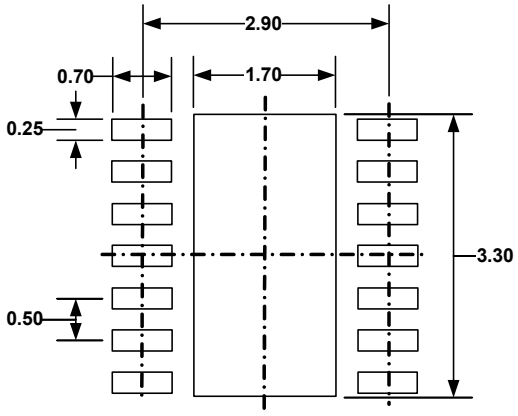
TOP VIEW

BOTTOM VIEW



SIDE VIEW

DETAIL A



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH
3) LEAD COPLANARITY SHALL BE0.10 MILLIMETER MAX
4) DRAWING CONFORMS TO JEDEC MO-229, VARIATION VEED-5.
5) DRAWING IS NOT TO SCALE

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