EEPROM Serial 1-Mb I²C - Automotive Grade 1 in Wettable Flank UDFN8 Package

NV24M01MUW

ON Semiconductor®

www.onsemi.com



UDFN−8
(Wettable Flank)
MUW3 SUFFIX
CASE 517DH

Description

The NV24M01MUW is a EEPROM Serial 1−Mb I²C − Automotive Grade 1, internally organized as 131,072 words of 8 bits each.

It features a 256−byte page write buffer and supports the Standard (100 kHz), Fast (400 kHz) and Fast−Plus (1 MHz) I²C protocol.

Write operations can be inhibited by taking the WP pin High (this protects the entire memory).

External address pins make it possible to address up to four NV24M01MUW devices on the same bus.

On−Chip ECC (Error Correction Code) makes the device suitable for high reliability applications.

Features

- Automotive AEC−Q100 Grade 1 (−40°C to +125°C) Qualified
- 1.8 V to 5.5 V Supply Voltage Range
- 256−Byte Page Write Buffer
- Hardware Write Protection for Entire Memory
- Schmitt Triggers and Noise Suppression Filters on I²C Bus Inputs (SCL and SDA)
- Low Power CMOS Technology
- 1,000,000 Program/Erase Cycles
- 100 Year Data Retention
- Industrial and Extended Temperature Range
- 8−pad UDFN Wettable Flank Package
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

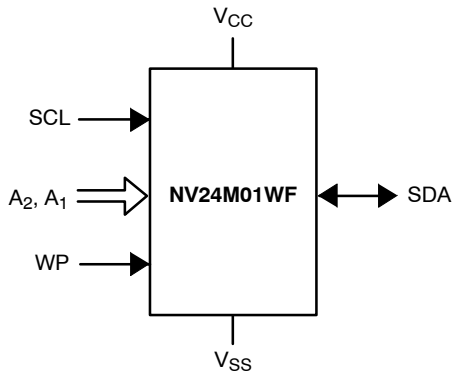


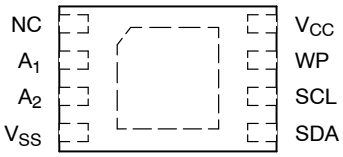
Figure 1. Functional Symbol

MARKING DIAGRAM



CAW	= Specific Device Code
A	= Assembly Location
WL	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

PIN CONFIGURATION



UDFN−8

PIN FUNCTION

Pin Name	Function
A_1, A_2	Device Address
SDA	Serial Data
SCL	Serial Clock
WP	Write Protect
V_{CC}	Power Supply
V_{SS}	Ground

ORDERING INFORMATION

See detailed ordering and shipping information on page 9 of this data sheet.

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Table 1. ABSOLUTE MAXIMUM RATINGS

Parameters	Ratings	Units
Storage Temperature	−65 to +150	°C
Voltage on any Pin with Respect to Ground (Note 1)	−0.5 to +6.5	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The DC input voltage on any pin should not be lower than −0.5 V or higher than V_{CC} + 0.5 V. During transitions, the voltage on any pin may undershoot to no less than −1.5 V or overshoot to no more than V_{CC} + 1.5 V, for periods of less than 20 ns.

Table 2. RELIABILITY CHARACTERISTICS (Note 2)

Symbol	Parameter	Min	Units
N_{END} (Notes 3, 4)	Endurance	1,000,000	Program/Erase Cycles
T_{DR}	Data Retention	100	Years

2. These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC−Q100 and JEDEC test methods.
3. Test Condition: Page Mode, V_{CC} = 5 V, 25°C.
4. The device uses ECC (Error Correction Code) logic with 6 ECC bits to correct one bit error in 4 data bytes. Therefore, when a single byte has to be written, 4 bytes (including the ECC bits) are re-programmed. It is recommended to write by multiple of 4 bytes in order to benefit from the maximum number of write cycles.

Table 3. DC OPERATING CHARACTERISTICS

V_{CC} = 1.8 V to 5.5 V, T_A = −40°C to +125°C, unless otherwise specified.

Symbol	Parameter	Test Conditions		Min	Max	Units
I_{CCR}	Read Current	Read, f_{SCL} = 1 MHz			1	mA
I_{CCW}	Write Current				8.0	mA
I_{SB}	Standby Current	All I/O Pins at GND or V_{CC}	T_A = −40°C to +85°C		2	μA
			T_A = −40°C to +125°C		5	
I_L	I/O Pin Leakage	Pin at GND or V_{CC}	T_A = −40°C to +85°C		1	μA
			T_A = −40°C to +125°C		2	
V_{IL1}	Input Low Voltage	2.5 V ≤ V_{CC} ≤ 5.5 V		−0.5	0.3 V_{CC}	V
V_{IL2}	Input Low Voltage	1.8 V ≤ V_{CC} < 2.5 V		−0.5	0.2 V_{CC}	V
V_{IH1}	Input High Voltage	2.5 V ≤ V_{CC} ≤ 5.5 V		0.7 V_{CC}	V_{CC} + 0.5	V
V_{IH2}	Input High Voltage	1.8 V ≤ V_{CC} < 2.5 V		0.8 V_{CC}	V_{CC} + 0.5	V
V_{OL1}	Output Low Voltage	V_{CC} ≥ 2.5 V, I_{OL} = 3.0 mA			0.4	V
V_{OL2}	Output Low Voltage	V_{CC} < 2.5 V, I_{OL} = 1.0 mA			0.2	V

Table 4. PIN IMPEDANCE CHARACTERISTICS
V_{CC} = 1.8 V to 5.5 V, T_A = −40°C to +125°C, unless otherwise specified.

Symbol	Parameter	Conditions	Max	Units
C_{IN} (Note 5)	SDA I/O Pin Capacitance	V_{IN} = 0 V	8	pF
C_{IN} (Note 5)	Input Capacitance (other pins)	V_{IN} = 0 V	6	pF
I_{WP}, I_A (Note 6)	WP Input Current, Address Input Current (A_1, A_2)	$V_{IN} < V_{IH}$, V_{CC} = 5.5 V	75	μA
		$V_{IN} < V_{IH}$, V_{CC} = 3.3 V	50	
		$V_{IN} < V_{IH}$, V_{CC} = 1.8 V	25	
		$V_{IN} > V_{IH}$	2	

5. These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC−Q100 and JEDEC test methods.
6. When not driven, the WP, A_1, A_2 pins are pulled down to GND internally. For improved noise immunity, the internal pull−down is relatively strong; therefore the external driver must be able to supply the pull−down current when attempting to drive the input HIGH. To conserve power, as the input level exceeds the trip point of the CMOS input buffer (~ 0.5 x V_{CC}), the strong pull−down reverts to a weak current source.

Table 5. AC CHARACTERISTICS (Note 7)
V_{CC} = 1.8 V to 5.5 V, T_A = −40°C to +125°C, unless otherwise specified.

Symbol	Parameter	Fast V_{CC} = 1.8 V – 5.5 V		Fast−Plus V_{CC} = 2.5 V – 5.5 V		Units
		Min	Max	Min	Max	
F_{SCL}	Clock Frequency		400		1,000	kHz
$t_{HD:STA}$	START Condition Hold Time	0.6		0.25		μs
t_{LOW}	Low Period of SCL Clock	1.3		0.45		μs
t_{HIGH}	High Period of SCL Clock	0.6		0.40		μs
$t_{SU:STA}$	START Condition Setup Time	0.6		0.25		μs
$t_{HD:DAT}$	Data In Hold Time	0		0		μs
$t_{SU:DAT}$	Data In Setup Time	100		50		ns
t_R (Note 8)	SDA and SCL Rise Time		300		100	ns
t_F (Note 8)	SDA and SCL Fall Time		300		100	ns
$t_{SU:STO}$	STOP Condition Setup Time	0.6		0.25		μs
t_{BUF}	Bus Free Time Between STOP and START	1.3		0.5		μs
t_{AA}	SCL Low to Data Out Valid		0.9		0.40	μs
t_{DH}	Data Out Hold Time	50		50		ns
T_i (Note 8)	Noise Pulse Filtered at SCL and SDA Inputs		50		50	ns
$t_{SU:WP}$	WP Setup Time	0		0		μs
$t_{HD:WP}$	WP Hold Time	2.5		1		μs
t_{WR}	Write Cycle Time		5		5	ms
t_{PU} (Notes 8, 9)	Power-up to Ready Mode		0.1		0.1	ms

7. Test conditions according to “A.C. Test Conditions” table.
8. Tested initially and after a design or process change that affects this parameter.
9. t_{PU} is the delay between the time V_{CC} is stable and the device is ready to accept commands.

Table 6. AC TEST CONDITIONS

Input Levels	0.2 x V_{CC} to 0.8 x V_{CC} (VCC < 2.5 V) and 0.3 x Vcc to 0.7 x Vcc (VCC ≥ 2.5 V)
Input Rise and Fall Times	≤ 50 ns
Output Reference Levels	0.5 x V_{CC}
Output Load	Current Source: I_L = 3 mA (V_{CC} ≥ 2.5 V); I_L = 1 mA (V_{CC} < 2.5 V); C_L = 100 pF

Power-On Reset (POR)

The NV24M01 incorporates Power−On Reset (POR) circuitry which protects the internal logic against powering up in the wrong state.

The device will power up into Standby mode after V_{CC} exceeds the POR trigger level and will power down into Reset mode when V_{CC} drops below the POR trigger level.

This bi−directional POR behavior protects the device against brown−out failure, following a temporary loss of power.

Pin Description

SCL: The Serial Clock input pin accepts the Serial Clock signal generated by the Master.

SDA: The Serial Data I/O pin receives input data and transmits data stored in EEPROM. In transmit mode, this pin is open drain. Data is acquired on the positive edge, and is delivered on the negative edge of SCL.

A_1 and A_2: The Address pins accept the device address. These pins have on−chip pull−down resistors.

WP: The Write Protect input pin inhibits all write operations, when pulled HIGH. This pin has an on−chip pull−down resistor.

Functional Description

The NV24M01 supports the Inter−Integrated Circuit (I^2C) Bus data transmission protocol, which defines a device that sends data to the bus as a transmitter and a device receiving data as a receiver. Data flow is controlled by a Master device, which generates the serial clock and all START and STOP conditions. The NV24M01 acts as a Slave device. Master and Slave alternate as either transmitter or receiver. Up to 4 devices may be connected to the bus as determined by the device address inputs A_1 and A_2.

I^2C Bus Protocol

The I^2C bus consists of two ‘wires’, SCL and SDA. The two wires are connected to the V_{CC} supply via pull−up resistors. Master and Slave devices connect to the 2−wire bus via their respective SCL and SDA pins. The transmitting device pulls down the SDA line to ‘transmit’ a ‘0’ and releases it to ‘transmit’ a ‘1’.

Data transfer may be initiated only when the bus is not busy (see A.C. Characteristics).

During data transfer, the SDA line must remain stable while the SCL line is HIGH. An SDA transition while SCL is HIGH will be interpreted as a START or STOP condition (Figure 2).

START

The START condition precedes all commands. It consists of a HIGH to LOW transition on SDA while SCL is HIGH. The START acts as a ‘wake−up’ call to all receivers. Absent a START, a Slave will not respond to commands.

STOP

The STOP condition completes all commands. It consists of a LOW to HIGH transition on SDA while SCL is HIGH. The STOP starts the internal Write cycle (when following a Write command) or sends the Slave into standby mode (when following a Read command).

Device Addressing

The Master initiates data transfer by creating a START condition on the bus. The Master then broadcasts an 8−bit serial Slave address. The first 4 bits of the Slave address are set to 1010, for normal Read/Write operations (Figure 3). The next 2 bits, A2, A1, select one of 4 possible memory devices connected on a single I^2C bus. The A2 and A1 bits must match the state of the external address pins. The seventh bit, a16 is the most significant internal address bit. The last bit, R/$\overline{W}$, specifies whether a Read (1) or Write (0) operation is to be performed. To select an internal memory location (data byte) a 17−bit address word is required: a16 bit from the Slave address byte followed by two address bytes.

Acknowledge

After processing the Slave address, the Slave responds with an acknowledge (ACK) by pulling down the SDA line during the 9th clock cycle (Figure 4). The Slave will also acknowledge the byte address and every data byte presented in Write mode. In Read mode the Slave shifts out a data byte, and then releases the SDA line during the 9th clock cycle. If the Master acknowledges the data, then the Slave continues transmitting. The Master terminates the session by not acknowledging the last data byte (NoACK) and by sending a STOP to the Slave. Bus timing is illustrated in Figure 5.

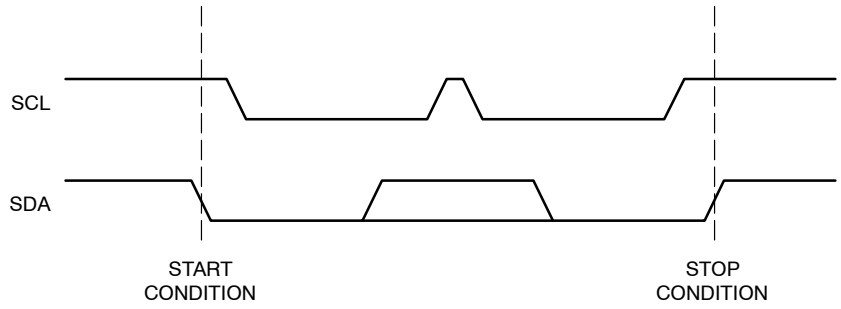


Figure 2. Start/Stop Timing

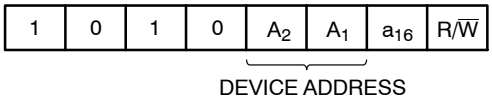


Figure 3. Slave Address Bits

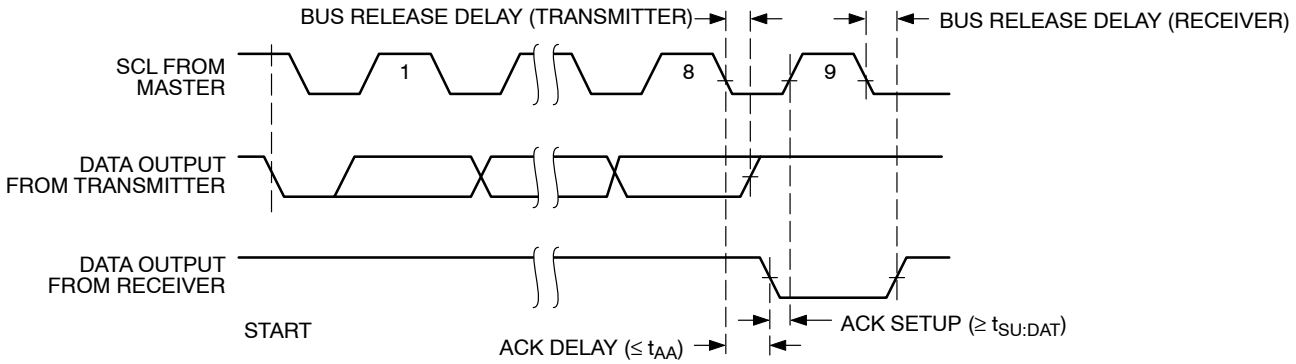


Figure 4. Acknowledge Timing

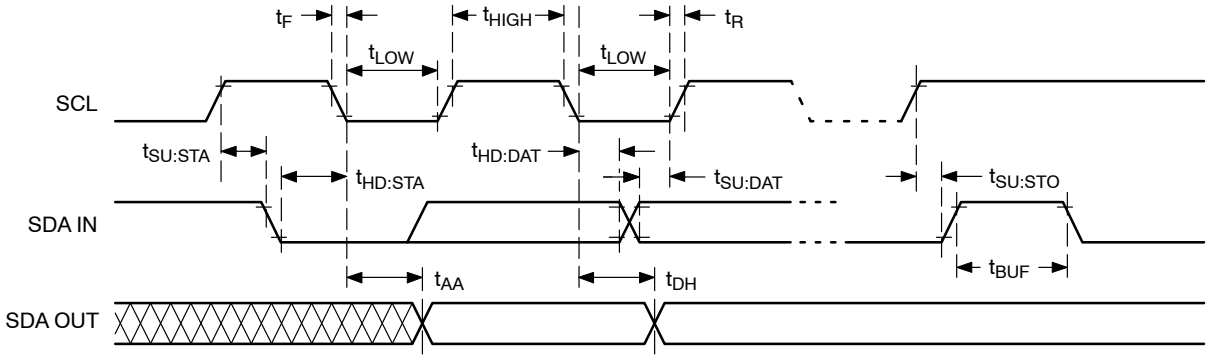


Figure 5. Bus Timing

WRITE OPERATIONS

Byte Write

In Byte Write mode the Master sends a START, followed by Slave address, two byte address and data to be written (Figure 6). The Slave acknowledges all 4 bytes, and the Master then follows up with a STOP, which in turn starts the internal Write operation (Figure 7). During internal Write, the Slave will not acknowledge any Read or Write request from the Master.

Page Write

The NV24M01 contains 131,072 bytes of data, arranged in 512 pages of 256 bytes each. The most significant 9 bits of the address word (a16 from the Slave Address byte and most significant Address byte) identify the page and the last 8 bits identify the byte within the page. The 17−bit address word (a16 from the Slave Address byte followed by two address bytes) points to the first byte to be written. Up to 256 bytes can be written in one Write cycle (Figure 8).

The internal byte address counter is automatically incremented after each data byte is loaded. If the Master transmits more than 256 data bytes, then earlier bytes will be overwritten by later bytes in a ‘wrap−around’ fashion (within the selected page). The internal Write cycle starts immediately following the STOP.

Acknowledge Polling

Acknowledge polling can be used to determine if the NV24M01 is busy writing or is ready to accept commands. Polling is implemented by interrogating the device with a ‘Selective Read’ command (see READ OPERATIONS).

The NV24M01 will not acknowledge the Slave address, as long as internal Write is in progress.

Hardware Write Protection

With the WP pin held HIGH, the entire memory is protected against Write operations. If the WP pin is left floating or is grounded, it has no impact on the operation of the NV24M01. The state of the WP pin is strobed on the last falling edge of SCL immediately preceding the first data byte (Figure 9). If the WP pin is HIGH during the strobe interval, the NV24M01 will not acknowledge the data byte and the Write request will be rejected.

Delivery State

The NV24M01 is shipped erased, i.e., all bytes are FFh.

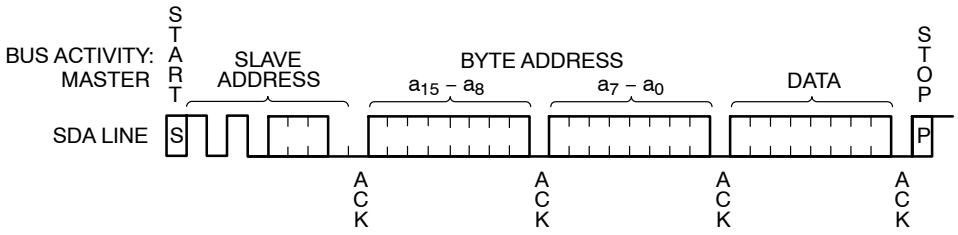


Figure 6. Byte Write Timing

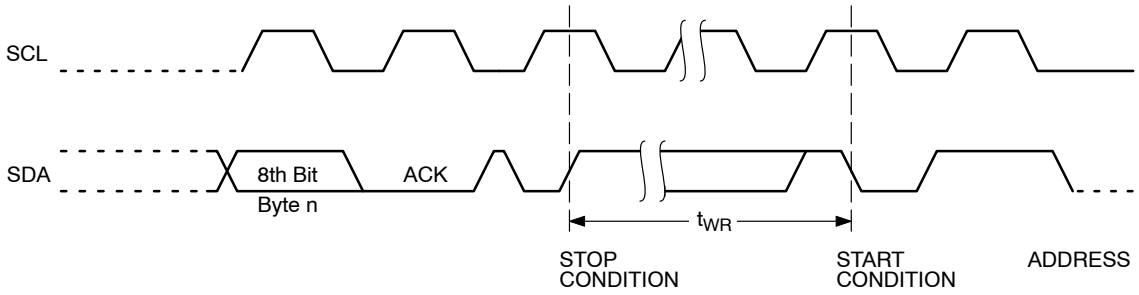


Figure 7. Write Cycle Timing

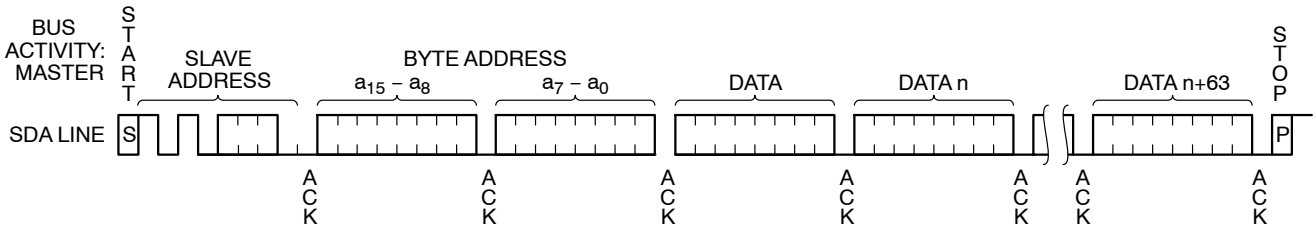


Figure 8. Page Write Timing

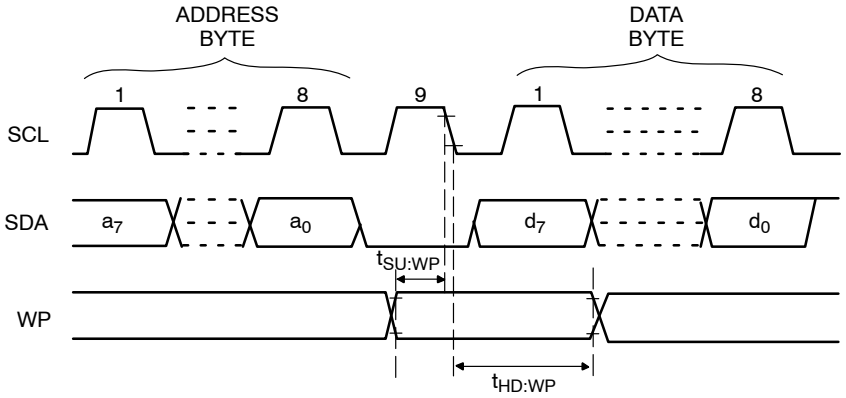


Figure 9. WP Timing

READ OPERATIONS

Immediate Address Read

In standby mode, the NV24M01 internal address counter points to the data byte immediately following the last byte accessed by a previous operation. If that ‘previous’ byte was the last byte in memory, then the address counter will point to the 1st memory byte, etc.

When, following a START, the NV24M01 is presented with a Slave address containing a ‘1’ in the R/$\overline{W}$ bit position (Figure 10), it will acknowledge (ACK) in the 9th clock cycle, and will then transmit data being pointed at by the internal address counter. The Master can stop further transmission by issuing a NoACK, followed by a STOP condition.

Selective Read

The Read operation can also be started at an address different from the one stored in the internal address counter. The address counter can be initialized by performing a ‘dummy’ Write operation (Figure 11). Here the START is followed by the Slave address (with the R/$\overline{W}$ bit set to ‘0’) and the desired two byte address. Instead of following up with data, the Master then issues a 2nd START, followed by the ‘Immediate Address Read’ sequence, as described earlier.

Sequential Read

If the Master acknowledges the 1st data byte transmitted by the NV24M01, then the device will continue transmitting as long as each data byte is acknowledged by the Master (Figure 12). If the end of memory is reached during sequential Read, then the address counter will ‘wrap−around’ to the beginning of memory, etc. Sequential Read works with either ‘Immediate Address Read’ or ‘Selective Read’, the only difference being the starting byte address.

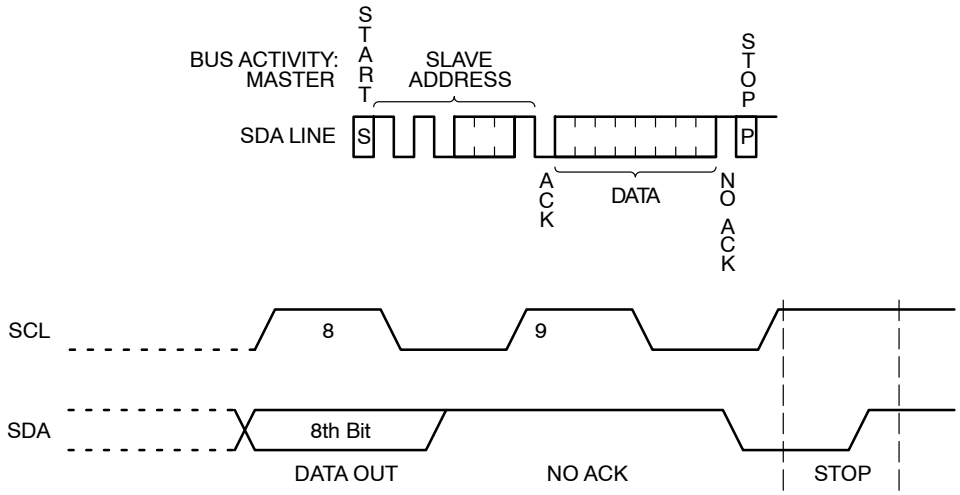


Figure 10. Immediate Address Read Timing

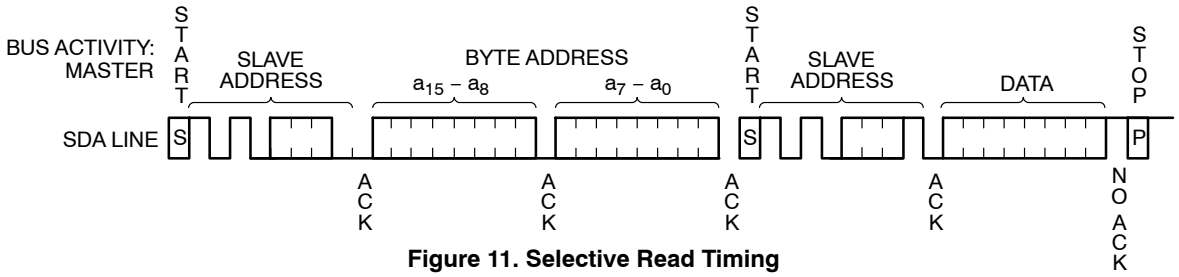


Figure 11. Selective Read Timing

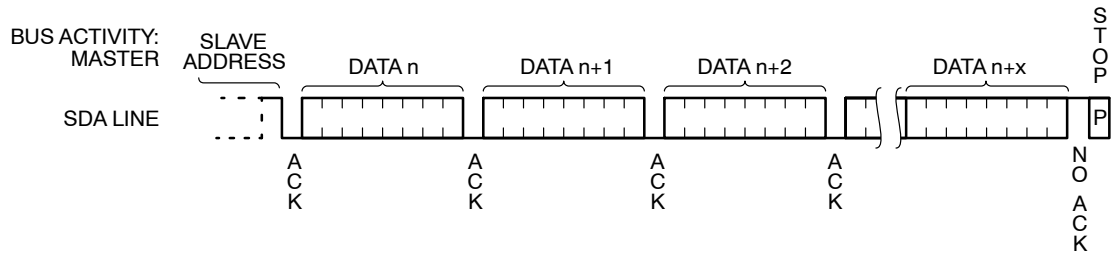


Figure 12. Sequential Read Timing

ORDERING INFORMATION

Device Order Number	Specific Device Marking	Temperature Range	Package Type	Shipping†
NV24M01MUW3VTBG	CAW	−40°C to +125°C	UDFN8 (Pb−Free, Wettable Flank)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

10. All packages are RoHS−compliant (Pb−Free, Halogen−free).

ON Semiconductor is licensed by the Philips Corporation to carry the I^2C bus protocol.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

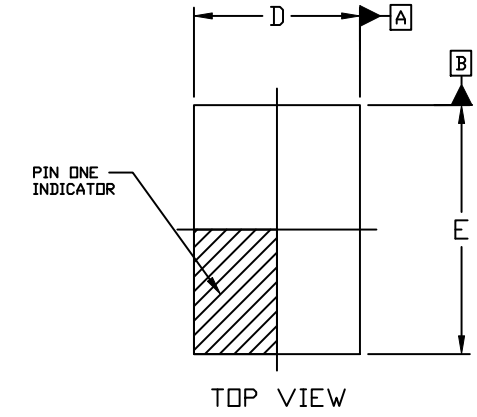
ON Semiconductor®

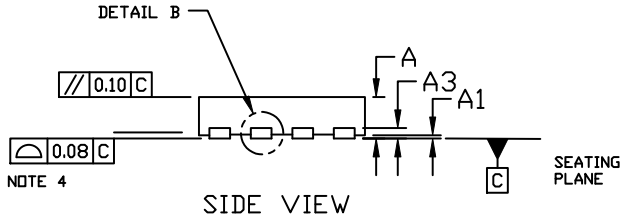


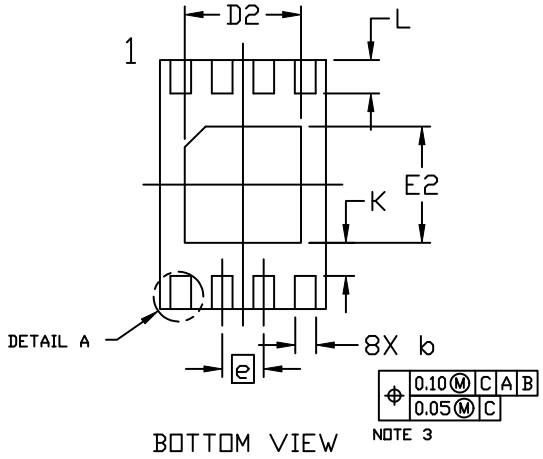
SCALE 2:1

UDFN8 2x3, 0.5P
CASE 517DH
ISSUE A

DATE 10 DEC 2020

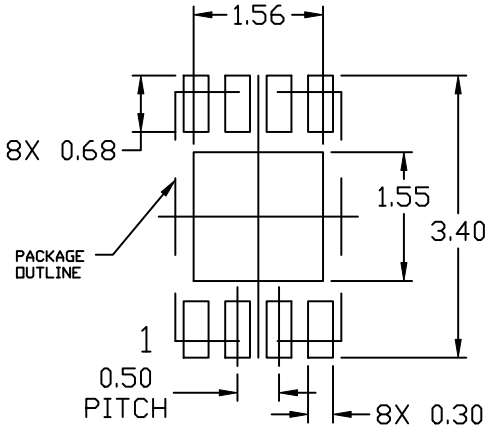






NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M,1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.25MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	0.45	0.50	0.55
A1	0.00	---	0.05
A3	0.13 REF		
b	0.20	0.25	0.30
D	1.90	2.00	2.10
D2	1.30	1.40	1.50
E	2.90	3.00	3.10
E2	1.30	1.40	1.50
e	0.50 BSC		
K	0.40 REF		
L	0.30	0.40	0.50



RECOMMENDED MOUNTING FOOTPRINT*

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX	= Specific Device Code
A	= Assembly Location
WL	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**UDFN8 2X3, 0.5P**	**PAGE 1 OF 1**

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