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NTE74HC259 **Integrated Circuit** **TTL – High Speed CMOS,** **8–Bit Addressable Latch**

Description:

The NTE74HC259 is an 8-bit addressable latch in a 16-Lead DIP type package that features the low-power consumption associated with CMOS circuitry and has speeds comparable to low-power Schottky.

This latches three active modes and one reset mode. When both the Latch Enable ($\overline{LE}$) and Master Reset ($\overline{MR}$) inputs are low (8-Line Demultiplexer Mode) the output of the addressed latch follows the Data input and all other outputs are forced low. When both $\overline{MR}$ and $\overline{LE}$ are high (Memory Mode), all outputs are isolated from the Data input, i.e., all latches hold the last data presented before the $\overline{LE}$ transition from low to high. A condition of $\overline{LE}$ low and $\overline{MR}$ high (Addressable Latch Mode) allows the addressed latch's output to follow the data input; all other latches are unaffected. The Reset mode (all outputs low) results when $\overline{LE}$ is high and $\overline{MR}$ is low.

Features:

- Wide Power Supply Range: 2V to 6V
- High Noise Immunity: $N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC} at $V_{CC} = 5V$
- Buffered Inputs and Outputs
- Four Operating Modes
- Typical Propagation Delay: 15ns at $V_{CC} = 5V$, $C_L = 15pF$, $T_A = +25^\circ C$
- Fanout (Over Temperature Range):
 - Standard Outputs . . . 10 LS-TTL Loads
 - Bus Driver Outputs . . 15 LS-TTL Loads
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LS-TTL Logic ICs

Absolute Maximum Ratings: (Note 1, Note 2)

Supply Voltage, V_{CC}	-0.5 to +7.0V
Clamp Diode Current, I_{IK} , I_{OK}	$\pm 20mA$
DC Drain Current (Per Output), I_{OUT}	$\pm 25mA$
DC Output Source or Sink Current (Per Output), I_{OUT}	$\pm 25mA$
DC V_{CC} or GND Current (Per Pin), I_{CC}	$\pm 50mA$
Maximum Junction, T_J	+150°C
Storage Temperature Range, T_{stg}	-65°C to +150°C
Typical Thermal Resistance, Junction-to-Ambient, R_{thJA}	67°C/W
Lead Temperature (During Soldering, 10sec), T_L	+300°C

Note 1. Absolute Maximum Ratings are those values beyond which damage to the device may occur.
Note 2. Unless otherwise specified, all voltages are referenced to GND.

Recommended Operating Conditions:

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	2.0	–	6.0	V
DC Input or Output Voltage	V_{IN}, V_{OUT}	0	–	V_{CC}	V
Operating Temperature Range	T_A	–40	–	+85	°C
Input Rise or Fall Times $V_{CC} = 2.0V$	t_r, t_f	–	–	1000	ns
$V_{CC} = 4.5V$		–	–	500	ns
$V_{CC} = 6.0V$		–	–	400	ns

DC Electrical Characteristics:

Parameter	Symbol	Test Conditions		V _{CC}	T _A = +25°C		T _A = -40° to +85°C	Unit
					Typ	Guaranteed Limits		
Minimum HIGH Level Input Voltage	V _{IH}			2.0	–	1.5	1.5	V
				4.5	–	3.15	3.15	V
				6.0	–	4.2	4.2	V
Maximum LOW Level Input Voltage	V _{IL}			2.0	–	0.5	0.5	V
				4.5	–	1.35	1.35	V
				6.0	–	1.8	1.8	V
Minimum HIGH Level Output Voltage	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OUT} = -20μA	–	V _{CC}	V _{CC} ^{-0.1}	V _{CC} ^{-0.1}	V
			I _{OUT} = -4mA	4.5	–	3.98	3.84	V
			I _{OUT} = -5.2mA	6.0	–	5.48	5.34	V
Minimum LOW Level Output Voltage	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OUT} = 20μA	–	–	0.1	0.1	V
			I _{OUT} = 4mA	4.5	–	0.26	0.33	V
			I _{OUT} = 5.2mA	6.0	0–	0.26	0.33	V
Maximum Input Current	I _{IN}	V _{IN} = V _{CC} or GND		6.0	–	±0.1	±1.0	μA
Maximum Quiescent Supply Current	I _{CC}	V _{IN} = V _{CC} or GND, I _{OUT} = 0μA		6.0	–	8.0	80	μA

Prerequisite for Switching Specifications:

Parameter	Symbol	Test Conditions	V _{CC}	T _A = +25°C		T _A = −40° to +85°C	Unit
				Typ	Guaranteed Limits		
Minimum Pulse Width ($\overline{LE}$)	t _{WL}		2.0	–	70	90	ns
			4.5	–	14	18	ns
			6.0	–	12	15	ns
Minimum Pulse Width ($\overline{MR}$)	t _{WL}		2.0	–	70	90	ns
			4.5	–	14	18	ns
			6.0	–	12	15	ns
Minimum Setup Time (D or A to $\overline{LE}$)	t _{SU}		2.0	–	80	100	ns
			4.5	–	16	20	ns
			6.0	–	14	17	ns
Minimum Hold Time (D or A to $\overline{LE}$)	t _H		2.0	–	0	0	ns
			4.5	–	0	0	ns
			6.0	–	0	0	ns

AC Electrical Characteristics: ($t_r = t_f = 6\text{ns}$, $C_L = 50\text{pF}$ unless otherwise specified)

Parameter	Symbol	Test Conditions	V _{CC}	T _A = +25°C		T _A = −40° to +85°C	Unit
				Typ	Guaranteed Limits		
Propagation Delay (A or D to Q)	t _{PHL}		2.0	–	185	230	ns
			4.5	–	37	46	ns
		C _L = 15pF	5.0	15	–	–	ns
			6.0	–	31	39	ns
Propagation Delay ($\overline{LE}$ to Q)	t _{PHL}		2.0	–	170	215	ns
			4.5	–	33	43	ns
		C _L = 15pF	5.0	14	–	–	ns
			6.0	–	29	37	ns
Propagation Delay ($\overline{MR}$ to Y)	t _{PHL} , t _{PLH}		2.0	–	155	195	ns
			4.5	–	31	39	ns
		C _L = 15pF	5.0	13	–	–	ns
			6.0	–	26	33	ns
Output Transition Time	t _{THL} , t _{TLH}		2.0	–	75	95	ns
			4.5	–	15	19	ns
			6.0	–	13	16	ns
Power Dissipation Capacitance	C _{PD}	C _L = 15pF, Note 3	5	21	–	–	pF
Maximum Input Capacitance	C _{IN}		–	–	10	10	pF

Note 3. C_{PD} is used to determine the dynamic power consumption, per channel.
 $P_D = V_{CC}^2 f_i + \sum C_L V_{CC}^2 f_O$ where f_i = Input Frequency, f_O = Output Frequency,
 C_L = Output Load Capacitance, V_{CC} = Supply Voltage.

Truth Table:

Inputs		Output of Address Latch	Each Other Output	Function
$\overline{MR}$	$\overline{LE}$			
H	L	D	Q_{io}	Addressable Latch
H	H	Q_{io}	Q_{io}	Memory
L	L	D	L	8-Line Demultiplexer
L	H	L	L	Reset

H = HIGH Level

L = LOW Level

D = The level at the data input

Q_{io} = The level of Q_i ($i = 0, 1 \dots 7$, as appropriate) before the indicated steady state input conditions were established.

Latch Selection Table:

Selected Inputs			Latch Addressed
A2	A1	A0	
L	L	L	0
L	L	H	1
L	H	L	2
L	H	H	3
H	L	L	4
H	L	H	5
H	H	L	6
H	H	H	7

Pin Connection Diagram

