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# NTE4522B
# Integrated Circuit
# CMOS, Programmable Divide–by–N 4–Bit BCD Counter

**Description:**

The NTE4522B is a BCD counter in a 16–Lead DIP type package constructed with MOS P–channel and N–channel enhancement mode devices is a single monolithic structure. This device is a programmable, cascadable down counter with a decoded “0” state output for divide–by–N applications. In single stage applications the “0” output is applied to the Preset Enable input. The Cascade Feedback input allows cascacade divide–by–N operation with no additional gates required. The Clock Inhibit input allows disabling of the pulse counting function.

The NTE4522B complementary MOS counter can be used in frequency synthesizers, phase–locked loops, an other frequency division applications requiring low power dissipation and/or high noise immunity.

**Features:**

- Quiescent Current = 5nA/Package (Typ) at 5Vdc
- Supply Voltage Range: 3Vdc to 18Vdc
- Internally Synchronized for High Internal and External Speeds
- Logic Edge–Clocked Design – Incremental on Positive Transition of Clock or Negative Transition of Clock Inhibit
- 5Mhz Counting Rate
- Asynchronous Preset Enable
- Capable of Driving Two Low–Power TTL Loads, One Low–Power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

**Absolute Maximum Ratings:** (Voltages referenced to $V_{SS}$, Note 1)

DC Supply Voltage, $V_{DD}$ . . . . . –0.5 to +18.0V
Input Voltage (All Inputs), $V_{in}$ . . . . . –0.5 to $V_{DD}$ to +0.5V
DC Current Drain (Per Pin), I . . . . . 10mA
Operating Temperature Range, $T_A$ . . . . . –55° to +125°C
Storage Temperature Range, $T_{stg}$ . . . . . –65° to +150°C

Note 1. Maximum Ratings are those values beyond which damage to the device may occur.
Note 2. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that $V_{in}$ and $V_{out}$ be constrained to the range $V_{SS} \le (V_{in} \text{ or } V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either $V_{SS}$ or $V_{DD}$).

**Electrical Characteristics:** (Voltages referenced to $V_{SS}$, Note 2)

| Parameter | Symbol | $V_{DD}$ Vdc | −55°C | | +25°C | | | +125°C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Typ | Max | Min | Max | |
| Output Voltage "0" Level | $V_{OL}$ | 5.0 | – | 0.05 | – | 0 | 0.05 | – | 0.05 | Vdc |
| $V_{in}$ = $V_{DD}$ or 0 | | 10 | – | 0.05 | – | 0 | 0.05 | – | 0.05 | Vdc |
| | | 15 | – | 0.05 | – | 0 | 0.05 | – | 0.05 | Vdc |
| "1" Level | $V_{OH}$ | 5.0 | 4.95 | – | 4.95 | 5.0 | – | 4.95 | – | Vdc |
| $V_{in}$ = 0 or $V_{DD}$ | | 10 | 9.95 | – | 9.95 | 10 | – | 9.95 | – | Vdc |
| | | 15 | 14.95 | – | 14.95 | 15 | – | 14.95 | – | Vdc |
| Input Voltage (Note 4) "0" Level | $V_{IL}$ | | | | | | | | | |
| ($V_O$ = 4.5 or 0.5Vdc) | | 5.0 | – | 1.5 | – | 2.25 | 1.5 | – | 1.5 | Vdc |
| ($V_O$ = 9.0 or 1.0Vdc) | | 10 | – | 3.0 | – | 4.50 | 3.0 | – | 3.0 | Vdc |
| ($V_O$ = 13.5 or 1.5Vdc) | | 15 | – | 4.0 | – | 6.75 | 4.0 | – | 4.0 | Vdc |
| "1" Level | $V_{IH}$ | | | | | | | | | |
| ($V_O$ = 0.5 or 4.5Vdc) | | 5.0 | 3.5 | – | 3.5 | 2.75 | – | 3.5 | – | Vdc |
| ($V_O$ = 1.0 or 9.0Vdc) | | 10 | 7.0 | – | 7.0 | 5.50 | – | 7.0 | – | Vdc |
| ($V_O$ = 1.5 or 13.5Vdc) | | 15 | 11.0 | – | 11.0 | 8.25 | – | 11.0 | – | Vdc |
| Output Drive Current Source | $I_{OH}$ | | | | | | | | | |
| ($V_{OH}$ = 2.5Vdc) | | 5.0 | –1.2 | – | –1.0 | –1.7 | – | –0.7 | – | mAdc |
| ($V_{OH}$ = 4.6Vdc) | | 5.0 | –0.25 | – | –0.2 | –0.36 | – | –0.14 | – | mAdc |
| ($V_{OH}$ = 9.5Vdc) | | 10 | –0.62 | – | –0.5 | –0.9 | – | –0.35 | – | mAdc |
| ($V_{OH}$ = 13.5Vdc) | | 15 | –1.8 | – | –1.5 | –3.5 | – | –1.1 | – | mAdc |
| Sink | $I_{OL}$ | | | | | | | | | |
| ($V_{OL}$ = 0.4Vdc) | | 5.0 | 0.64 | – | 0.51 | 0.88 | – | 0.36 | – | mAdc |
| ($V_{OL}$ = 0.5Vdc) | | 10 | 1.6 | – | 1.3 | 2.25 | – | 0.9 | – | mAdc |
| ($V_{OL}$ = 1.5Vdc) | | 15 | 4.2 | – | 3.4 | 8.8 | – | 2.4 | – | mAdc |
| Input Current | $I_{in}$ | 15 | – | ±0.1 | – | ±0.00001 | ±0.1 | – | ±0.1 | µAdc |
| Input Capacitance ($V_{IN}$ = 0) | $C_{in}$ | – | – | – | – | 5.0 | 7.5 | – | – | pF |
| Quiescent Current (Per Package) | $I_{DD}$ | 5.0 | – | 5.0 | – | 0.005 | 5.0 | – | 150 | µAdc |
| | | 10 | – | 10 | – | 0.010 | 10 | – | 300 | µAdc |
| | | 15 | – | 20 | – | 0.015 | 20 | – | 600 | µAdc |
| Total Supply Current (Dynamic plus Quiescent, Per Package, $C_L$ = 50pF on all outputs, all buffers switching, Note 3, Note 5) | $I_T$ | 5.0 | $I_T$ = (1.7µA/kHz) f + $I_{DD}$ | | | | | | | µAdc |
| | | 10 | $I_T$ = (3.4µA/kHz) f + $I_{DD}$ | | | | | | | µAdc |
| | | 15 | $I_T$ = (5.1µA/kHz) f + $I_{DD}$ | | | | | | | µAdc |

Note 2. Data labeled "Typ" is not to be used for design purposes but is intended as an indication of the device's potential performance.

Note 3. The formulas given are for the typical characteristics only at +25°C.

Note 4. Noise immunity specified for worst−case input combination.
Noise margin for both "1" and "0" = 1.0Vdc min @ $V_{DD}$ = 5Vdc
2.0Vdc min @ $V_{DD}$ = 10Vdc
2.5Vdc min @ $V_{DD}$ = 15Vdc

Note 5. To calculate total supply current at loads other than 50pF:

$$I_T(C_L) = I_T(50pF) + 1 \times 10^{-3} (C_L - 50) V_{DD} f$$

where: $I_T$ is in µA (per package), $C_L$ in pF, $V_{DD}$ in Vdc, f in kHz is input frequency.

**Switching Characteristics:** ($C_L$ = 50pF, $T_A$ = +25°C, Note 2)

| Parameter | Symbol | $V_{DD}$ Vdc | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Output Rise Time | $t_{TLH}$ | | | | | |
| $t_{TLH}$ = (3.0ns/pF) $C_L$ + 30ns | | 5.0 | – | 180 | 360 | ns |
| $t_{TLH}$ = (1.5ns/pF) $C_L$ + 15ns | | 10 | – | 90 | 180 | ns |
| $t_{TLH}$ = (1.1ns/pF) $C_L$ + 10ns | | 15 | – | 65 | 130 | ns |
| Output Fall Time | $t_{THL}$ | | | | | |
| $t_{THL}$ = (1.5ns/pF) $C_L$ + 25ns | | 5.0 | – | 100 | 200 | ns |
| $t_{THL}$ = (0.75ns/pF) $C_L$ + 12.5ns | | 10 | – | 50 | 100 | ns |
| $t_{THL}$ = (0.55ns/pF) $C_L$ + 9.5ns | | 15 | – | 40 | 80 | ns |
| Propagation Delay Time, Q Outputs | $t_{PLH}$, $t_{PHL}$ | | | | | |
| $t_{PLH}$, $t_{PHL}$ = (1.7ns/pF) $C_L$ + 465ns | | 5.0 | – | 550 | 1100 | ns |
| $t_{PLH}$, $t_{PHL}$ = (0.66ns/pF) $C_L$ + 197ns | | 10 | – | 225 | 450 | ns |
| $t_{PLH}$, $t_{PHL}$ = (0.5ns/pF) $C_L$ + 135ns | | 15 | – | 160 | 320 | ns |
| Propagation Delay Time, “0” Output | $t_{PLH}$, $t_{PHL}$ | | | | | |
| $t_{PLH}$, $t_{PHL}$ = (1.7ns/pF) $C_L$ + 155ns | | 5.0 | – | 240 | 480 | ns |
| $t_{PLH}$, $t_{PHL}$ = (0.66ns/pF) $C_L$ + 87ns | | 10 | – | 130 | 260 | ns |
| $t_{PLH}$, $t_{PHL}$ = (0.5ns/pF) $C_L$ + 65ns | | 15 | – | 100 | 200 | ns |
| Minimum Clock Pulse Width | $t_{WH(cl)}$ | 5.0 | 250 | 125 | – | ns |
| | | 10 | 100 | 50 | – | ns |
| | | 15 | 80 | 40 | – | ns |
| Minimum Clock Pulse Frequency | $f_{cl}$ | 5.0 | – | 2.0 | 1.5 | MHz |
| | | 10 | – | 5.0 | 3.0 | MHz |
| | | 15 | – | 6.6 | 4.0 | MHz |
| Maximum Clock or Inhibit Rise and Fall Time | $t_{TLH}$, $t_{THL}$ | 5.0 | – | – | 15 | ns |
| | | 10 | – | – | 15 | ns |
| | | 15 | – | – | 15 | ns |
| Hold Time | $t_h$ | 5.0 | 150 | 75 | – | ns |
| | | 10 | 50 | 25 | – | ns |
| | | 15 | 40 | 20 | – | ns |
| Minimum Preset Enable Pulse Width | $t_{WH(PE)}$ | 5.0 | 250 | 125 | – | ns |
| | | 10 | 100 | 50 | – | ns |
| | | 15 | 80 | 40 | – | ns |
| Minimum Master Reset Pulse Width | $t_{WH(R)}$ | 5.0 | 350 | 175 | – | ns |
| | | 10 | 250 | 125 | – | ns |
| | | 15 | 200 | 100 | – | ns |

Note 2. Data labeled “Typ” is not to be used for design purposes but is intended as an indication of the device’s potential performance.

Note 3. The formulas given are for the typical characteristics only at +25°C.

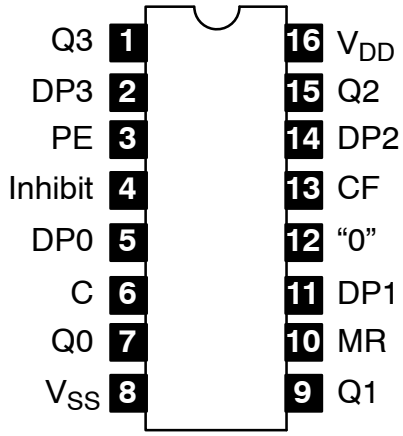
## Truth Tables

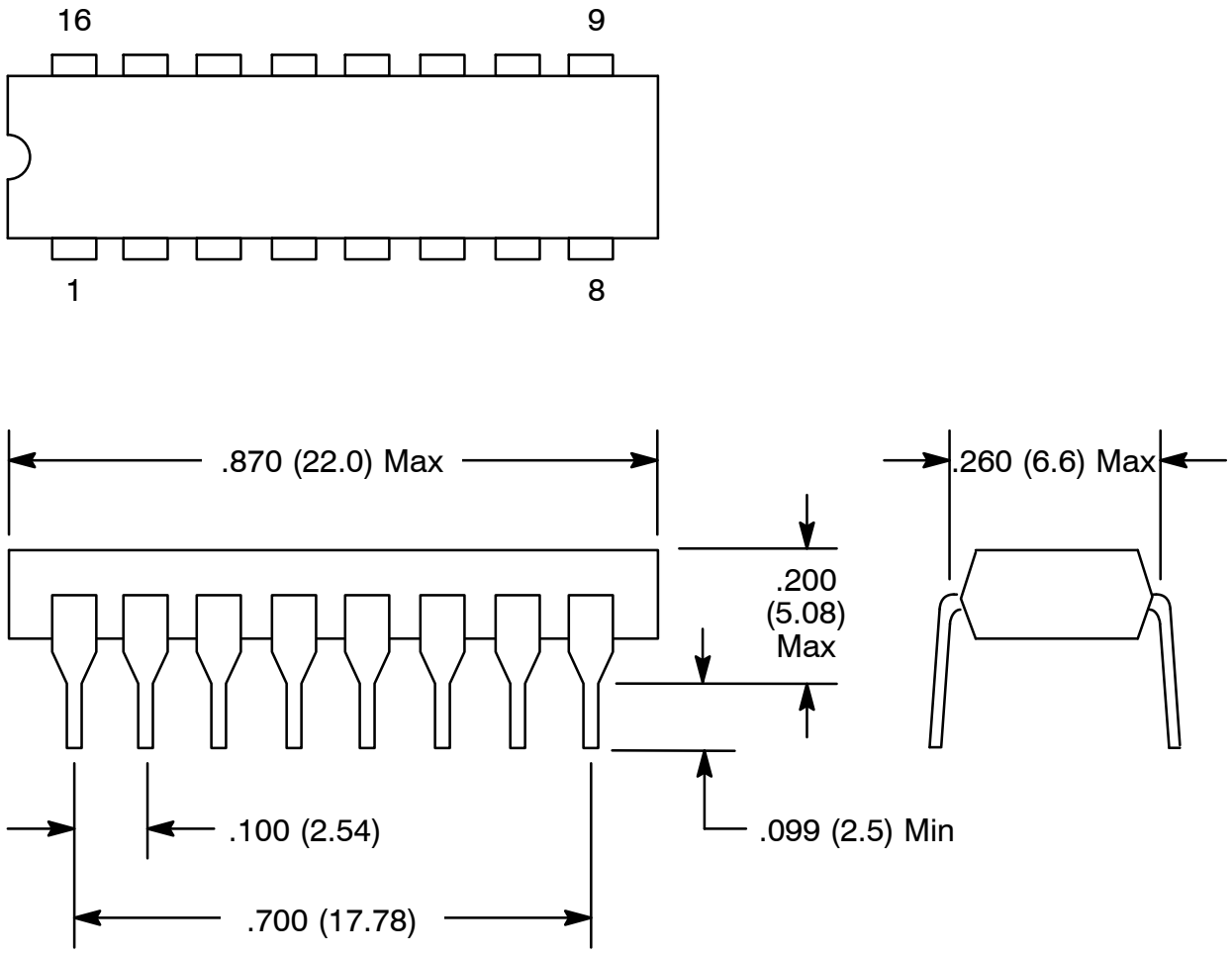
| Clock | Inhibit | Preset Enable | Master Reset | Action |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | No Count |
| ⎍ | 0 | 0 | 0 | Count 1 |
| X | 1 | 0 | 0 | No Count |
| 1 | ⎎ | 0 | 0 | Count 1 |
| X | X | 1 | 0 | Preset |
| X | X | X | 1 | Reset |

X = Don't Care

| Count | Output | | | |
|---|---|---|---|---|
| | Q3 | Q2 | Q1 | Q0 |
| 9 | 1 | 0 | 0 | 1 |
| 8 | 1 | 0 | 0 | 0 |
| 7 | 0 | 1 | 1 | 1 |
| 6 | 0 | 1 | 1 | 0 |
| 5 | 0 | 1 | 0 | 1 |
| 4 | 0 | 1 | 0 | 0 |
| 3 | 0 | 0 | 1 | 1 |
| 2 | 0 | 0 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 |

**Pin Connection Diagram**




16
9
1
8
.870 (22.0) Max
.260 (6.6) Max
.200
(5.08)
Max
.100 (2.54)
.099 (2.5) Min
.700 (17.78)