MP3438

2A, 16V, High-Efficiency, Fully Integrated, Synchronous Boost Converter

DESCRIPTION

The MP3438 is a highly integrated boost converter with a 1.2MHz fixed frequency and a wide input voltage (V_{IN}) range. The MP3438 starts up from a V_{IN} as low as 2.7V, and can support up to a 2A switching current limit with integrated, low $R_{DS(ON)}$ power MOSFETs.

The MP3438 adopts constant-off-time (COT) control to provide fast transient response. The cycle-by-cycle current limit on the low-side MOSFET (LS-FET) prevents current runaway, and the high-side MOSFET (HS-FET) eliminates the need for an external Schottky diode. The MP3438 supports an automatic pass-through function when V_{IN} exceeds the set output voltage ($V_{OUT-SET}$). This function supports high efficiency, even when the input exceeds the regulated output.

Full protection features include configurable V_{IN} under-voltage lockout (UVLO) and over-temperature protection (OTP).

The MP3438 is available in an SOT583 (1.6mmx2.1mm) package.

FEATURES

- 2.7V to 16V Start-Up Input Voltage (V_{ST})
- 0.8V to 16V Operating Input Voltage (V_{IN})
- Up to 16V Output Voltage (V_{OUT})
- 2A Switching Current Limit
- >91% Efficiency for 3.3V V_{IN} to 12V/0.3A
- 1.2MHz Fixed Switching Frequency (f_{SW})
- Adaptive Constant-Off-Time (COT) Control for Fast Transient Response
- Power-Save Mode (PSM) under Light Loads
- Automatic Pass-Through Mode when V_{IN} > Set Output Voltage ($V_{OUT-SET}$)
- Internal Soft Start and Compensation
- Configurable Under-Voltage Lockout (UVLO) and Hysteresis
- Over-Temperature Protection (OTP) and Over-Voltage Protection (OVP)
- Available in an SOT583 (1.6mmx2.1mm) Package

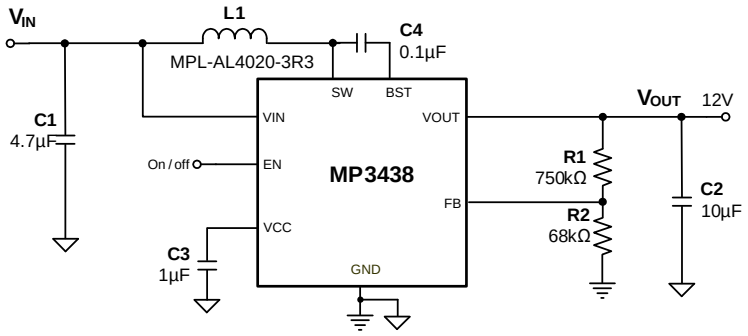
MPL Optimized Performance with MPS Inductor MPL-AL4020 Series

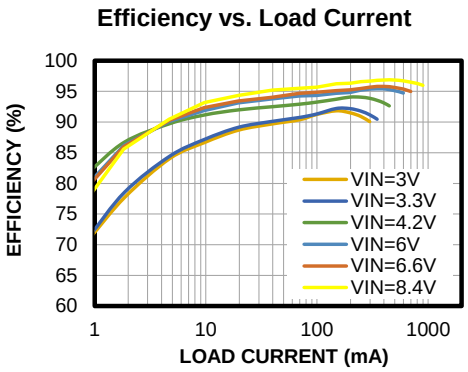
APPLICATIONS

- LCD Bias Supplies
- ADSLs/DSLs
- Electronic Cigarettes
- Instrumentation Equipment
- Portable Applications

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TYPICAL APPLICATION





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ORDERING INFORMATION

Part Number	Package	Top Marking	MSL Rating
MP3438GTL*	SOT583	*See Below*	1

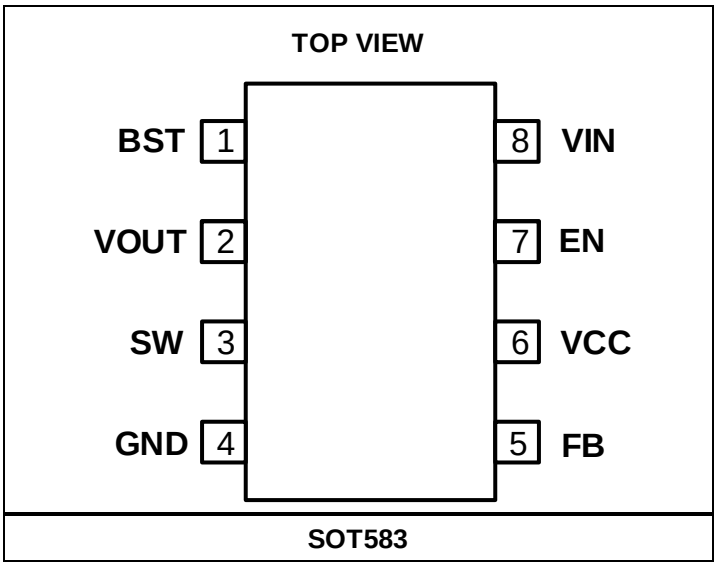
* For Tape & Reel, add suffix -Z (e.g. MP3438GTL-Z).

TOP MARKING

BRUY
LLL

BRU: Product code
Y: Year code
LLL: Lot number

PACKAGE REFERENCE



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PIN FUNCTIONS

Pin #	Name	Description
1	BST	**Bootstrap.** A capacitor between the BST and SW pins powers the synchronous high-side MOSFET (HS-FET).
2	VOUT	**Output.** The VOUT pin is connected to the drain of the HS-FET. VOUT powers VCC when V_{OUT} exceeds V_{IN}, and when V_{IN} is below 3.4V.
3	SW	**Converter switch.** The SW pin is connected to the drain of the internal low-side MOSFET (LS-FET) and the source of the internal HS-FET. Connect the power inductor to the SW pin.
4	GND	**Power ground.**
5	FB	**Feedback input.** Connect a resistor divider from VOUT to the FB pin.
6	VCC	**Internal bias supply.** Decouple the VCC pin with a 1µF ceramic capacitor, placed as close to this pin as possible. When V_{IN} exceeds 3.4V, VCC is powered by VIN. Otherwise, VCC is powered by the greater voltage between V_{IN} and V_{OUT}. If the biased voltage connected to VCC exceeds 3.4V, the regulators from VIN and VOUT are disabled. If EN is high, the VCC regulator starts to operate when V_{IN} exceeds 0.9V. To provide VCC with a sufficient power voltage during V_{IN} start-up, supply the VIN pin with a power source exceeding 2.7V.
7	EN	**Chip enable control.** Connect the EN pin to VIN for automatic start-up. EN can configure the VIN under-voltage lockout (UVLO) threshold. Do not float the EN pin. It must be externally pulled up or down.
8	VIN	**Input supply.** The VIN pin must be bypassed locally. To provide VCC with a sufficient power voltage during V_{IN} start-up, supply VIN with a power source exceeding 2.7V.

ABSOLUTE MAXIMUM RATINGS (1)

SW……..
..-0.3V (-2V for <10ns) to +20V (+24V for <10ns)
VIN, EN, VOUT ..... -0.3V to +20V
BST .....-0.3V to V_{SW} + 4.5V
All other pins ..... -0.3V to +4.5V
HS-FET body diode inrush current 6A (2)
Continuous power dissipation (T_A = 25°C) (3)
……1.9W (6)
Junction temperature ..... 150°C
Lead temperature..... 260°C
Storage temperature .....-65°C to +150°C

ESD Ratings

Human body model (HBM) 2000V
Charged device model (CDM) 1500V

Recommended Operating Conditions (4)

Start-up input voltage (V_{ST}).....2.7V to 16V (2)
Operating input voltage (V_{IN}) ..... 0.8V to 16V
Start-up input voltage with VCC bias (V_{ST2}) .....
..... 0.9V to 16V
Maximum external V_{CC} bias voltage 3.6V (5)
Boost output voltage (V_{OUT}) ..... V_{IN} to 16V
Operating junction temp (T_J).....-40°C to +125°C

Thermal Resistance θ_{JA} θ_{JC}

SOT583
EVL3438-TL-00A (6).....65.....25...°C/W
JESD51-7 (7)……130…..60...°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) During input start-up, the inrush current through the high-side MOSFET body diode should be limited below 6A. See the Input Start-Up Inrush Current Control section on page 16 for more details.
3) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) When the external VCC bias voltage is below the normal VCC pin's regulated voltage, the external power should prevent current from flowing out of the VCC pin.
6) Measured on the EVL3438-TL-00A, a 2-layer 51mmx51mm 1oz PCB.
7) The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

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ELECTRICAL CHARACTERISTICS

V_{IN} = V_{EN} = 3.3V, T_J = -40°C to 125°C [8], typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Supply						
Start-up input voltage [9]	V_{ST}	No V_{CC} bias	2.7		16	V
		V_{CC} = 3V	0.9		16	V
Operating input voltage	V_{IN}		0.8		16	V
Operating VCC voltage [10]	V_{CC}	V_{IN} = 2.7V, 0mA	2.3	2.55		V
		V_{IN} = 12V, 0mA to 10mA		3.4		V
VCC UVLO rising threshold [10]	VCC_{UVLO-R}	VCC rising	2.2	2.4	2.6	V
VCC UVLO falling threshold	VCC_{UVLO-F}	VCC falling	1.9	2.1	2.3	V
Shutdown current	I_{SD}	V_{EN} = 0V, measured on the VIN pin			1.5	µA
Quiescent current	I_Q	V_{FB} = 1.05V, V_{IN} = 3.3V, V_{OUT} = 12V, no switching, measured on the VIN pin			10	µA
		V_{FB} = 1.05V, V_{IN} = 3.3V, V_{OUT} = 12V, no switching, measured on the VOUT pin		150	200	µA
		V_{FB} = 1.05V, V_{IN} = 12V, V_{OUT} floating, pass-through mode, measure on VIN		300	360	µA
Enable (EN) Control						
EN turn-on threshold voltage	V_{EN-ON}	V_{EN} rising (switching)	1.1	1.2	1.3	V
EN high threshold voltage	V_{EN-H}	V_{EN} rising (micro-power)			1	V
EN low threshold voltage	V_{EN-L}	V_{EN} falling (micro-power)	0.4			V
EN turn-on hysteresis current	I_{EN-HYS}	1V < EN < V_{EN-ON}	3.5	5	7	µA
EN input current	I_{EN}	V_{EN} = 0V, 1.5V		0		µA
EN turn-on delay		EN on to switching		300		µs
Frequency						
Switching frequency	f_{SW}	V_{IN} = 3.3V, V_{OUT} = 12V	1	1.2	1.4	MHz
LS-FET minimum on time [11]	t_{MIN-ON}			80		ns
LS-FET maximum on time	t_{MAX-ON}			10		µs
LS-FET minimum off time [11]	$t_{MIN-OFF}$			220		ns
Loop Control						
FB reference voltage	V_{REF}	T_J = 25°C	0.99	1	1.01	V
		T_J = -40°C to +125°C	0.985	1	1.015	V
FB input current	I_{FB}	V_{FB} = 1.05V			50	nA
Soft-start time	t_{SS}		3.5	5	6	ms
Power Switch						
Low-side switch on-resistance	R_{ON-L}			55		mΩ
High-side synchronous switch on-resistance	R_{ON-H}			100		mΩ
Low-side switch leakage current		V_{SW} = 16V, T_J = 25°C			0.1	µA
High-side switch leakage current		V_{OUT} = 16V, V_{SW} = 0V, T_J = 25°C			0.1	µA

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = V_{EN} = 3.3V, T_J = -40°C to 125°C [8], typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
BST Power						
BST voltage		Boost mode		3.2		V
		Pass-through mode		3.5		V
Current Limit						
Switching current limit	$I_{PK-LIMT}$		1.8	2	2.3	A
HS-FET ZCD	I_{ZCD}		0	50	100	mA
Protection						
FB pin OVP threshold				110%		V_{REF}
FB pin OVP hysteresis				5%		V_{REF}
Thermal Protection						
Thermal shutdown [11]	T_{SD}			150		°C
Thermal shutdown hysteresis [11]	T_{SD-HYS}			25		°C

Notes:

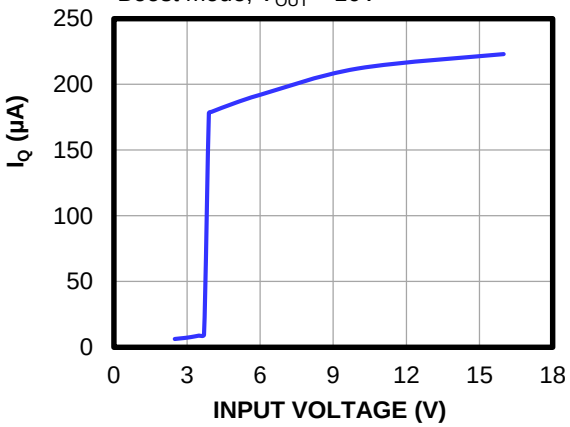
8) Not tested in production. Guaranteed by over-temperature correlation.
9) During input start-up, the inrush current through the HS-FET body diode should be limited below 6A. See the Input Start-Up Inrush Current Control section on page 16 for more details.
10) To guarantee IC start-up, ensure that V_{IN} exceeds 2.7V so that the VCC regulation voltage exceeds its UVLO rising threshold.
11) Guaranteed by sample characterization. Not tested in production.

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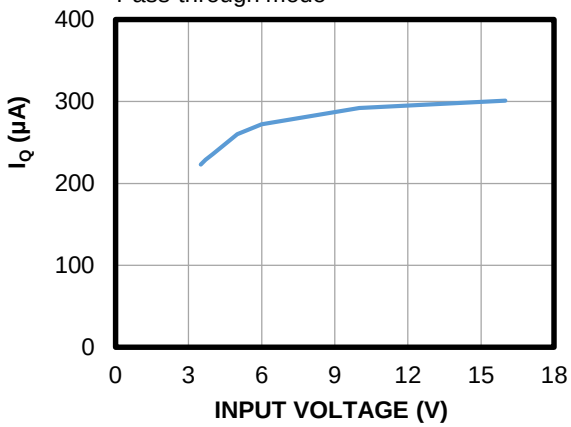
TYPICAL CHARACTERISTICS

V_{IN} = V_{EN} = 3.3V, V_{OUT} = 12V, L =3.3µH, T_A = 25°C, unless otherwise noted.

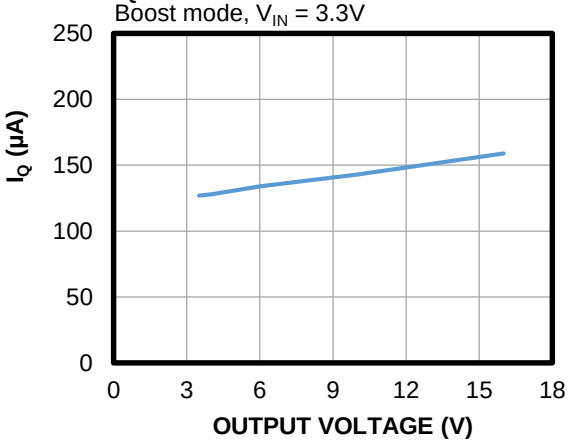
I_Q vs. Input Voltage (12)
Boost mode, V_{OUT} = 16V



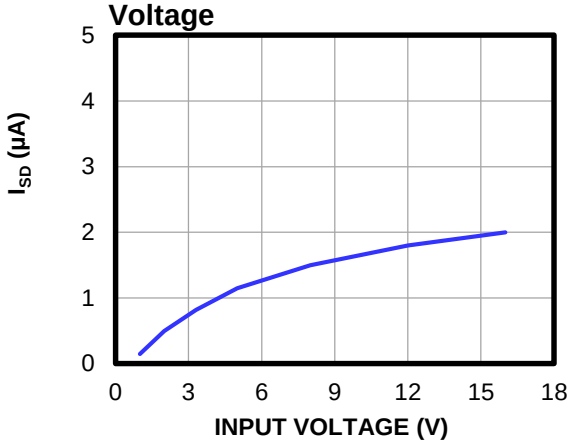
I_Q vs. Input Voltage
Pass-through mode



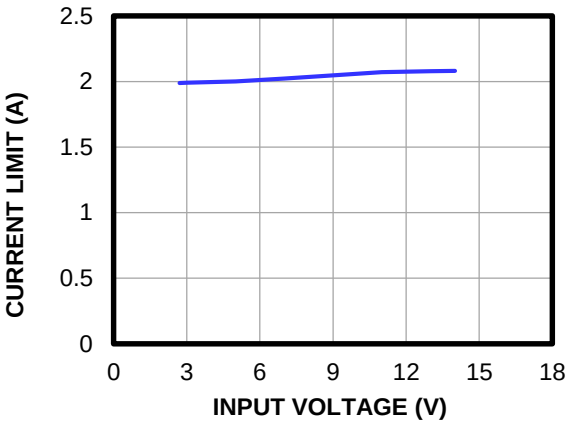
I_Q vs. Output Voltage
Boost mode, V_{IN} = 3.3V



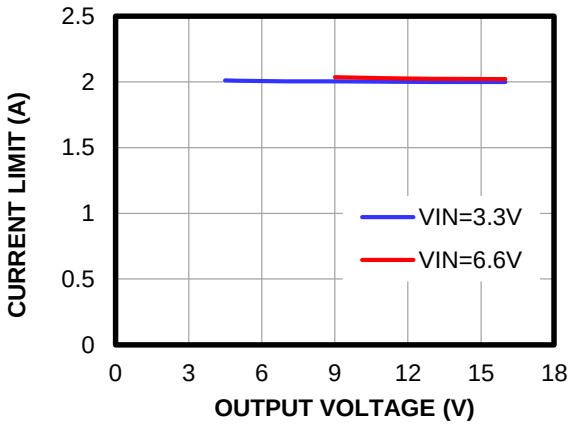
Shutdown Current vs. Input Voltage



Current Limit vs. Input Voltage
V_{OUT} = 16V



Current Limit vs. Output Voltage



Note:

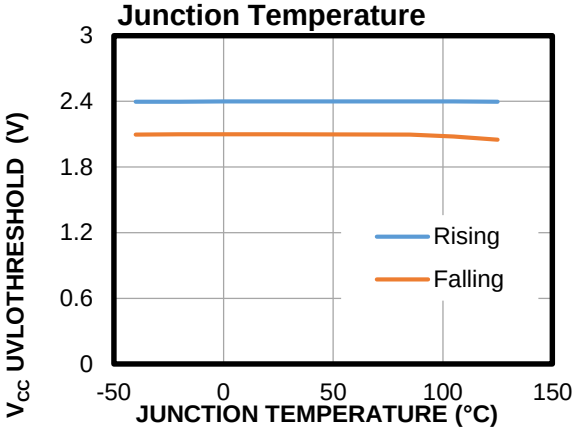
12) When V_{IN} exceeds 3.4V, VIN supplies power to VCC, so the I_Q on VIN rises when V_{IN} > 3.4V.

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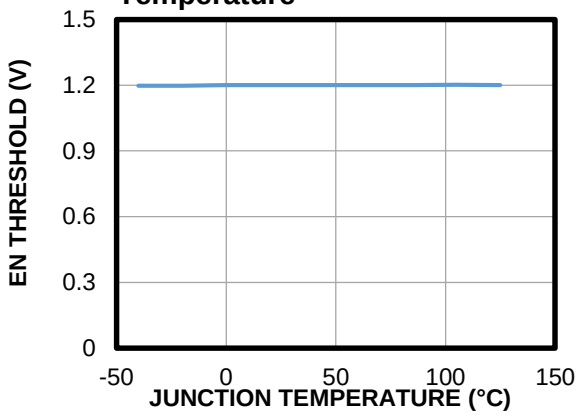
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = V_{EN} = 3.3V, V_{OUT} = 12V, L = 3.3µH, T_A = 25°C, unless otherwise noted.

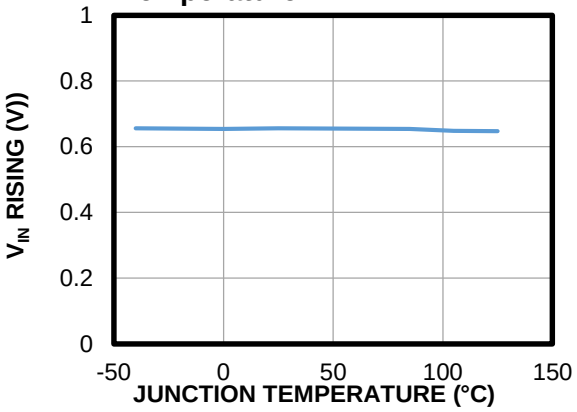
V_{CC} UVLO Threshold vs. Junction Temperature



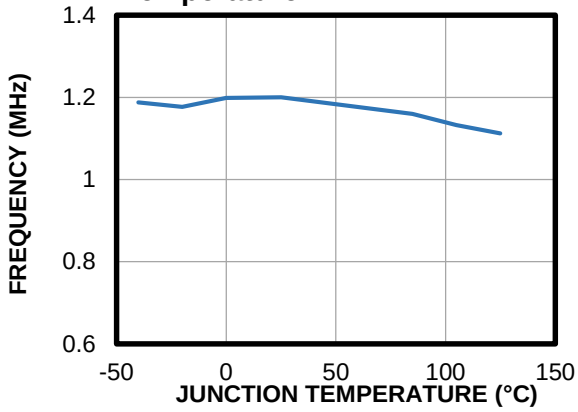
EN Threshold vs. Junction Temperature



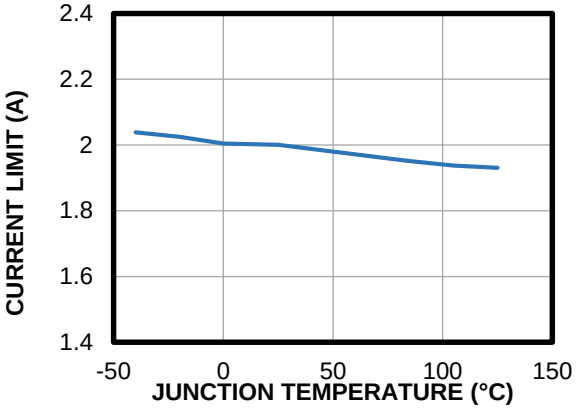
V_{IN} Rising vs. Junction Temperature



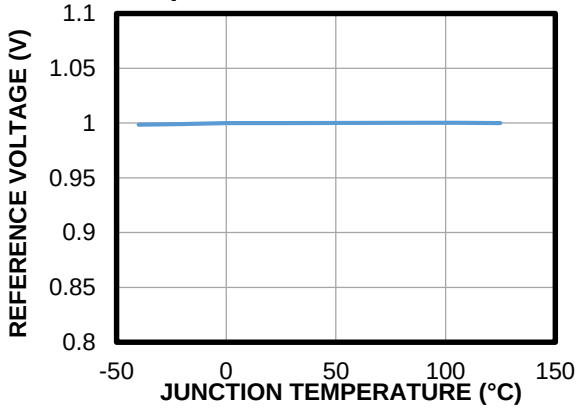
Frequency vs. Junction Temperature



Current Limit vs. Junction Temperature



Reference Voltage vs. Junction Temperature

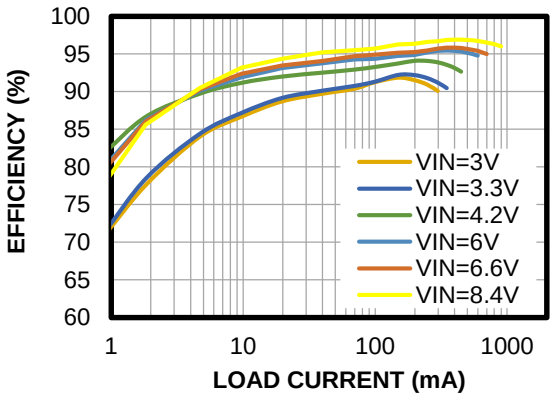


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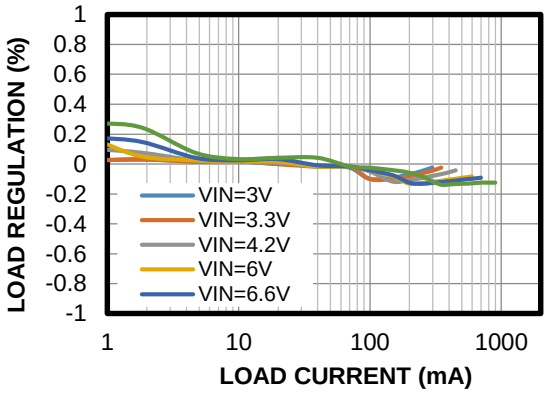
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 3.3V, V_{OUT} = 12V, L = 3.3µH, I_{OUT} = 0.3A, T_A = 25°C, unless otherwise noted.

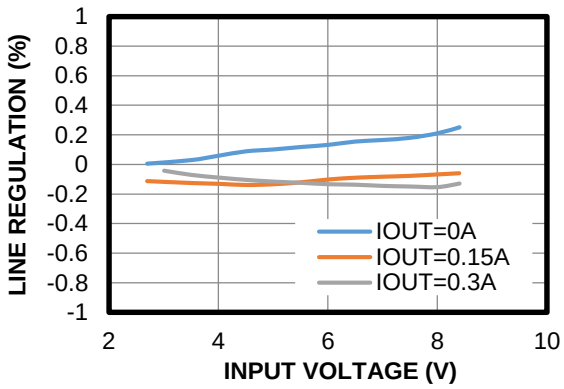
Efficiency vs. Load Current



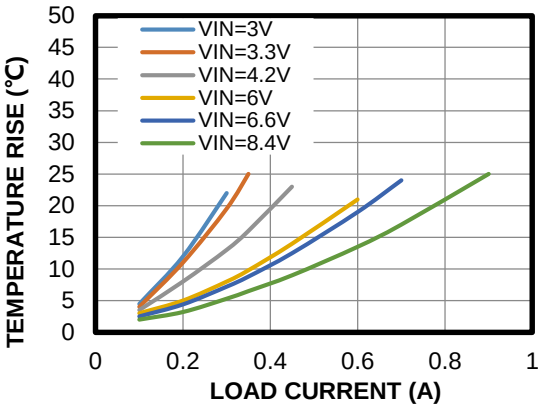
Load Regulation



Line Regulation

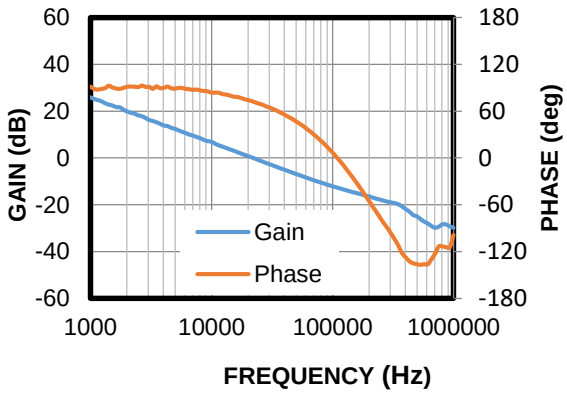


Case Temperature Rise



Bode Plot

I_{OUT} = 0.3A

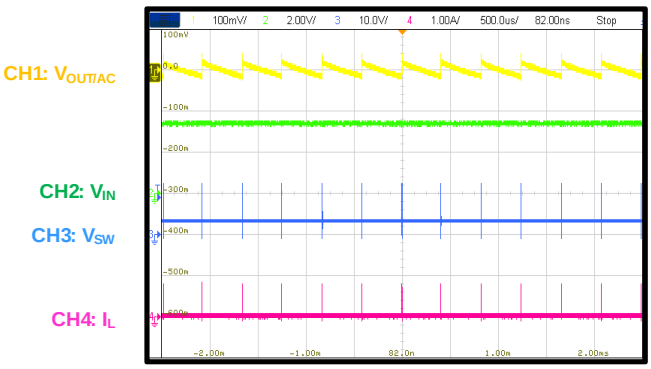


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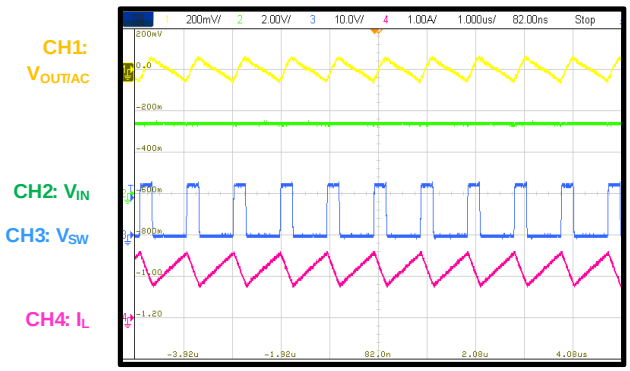
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

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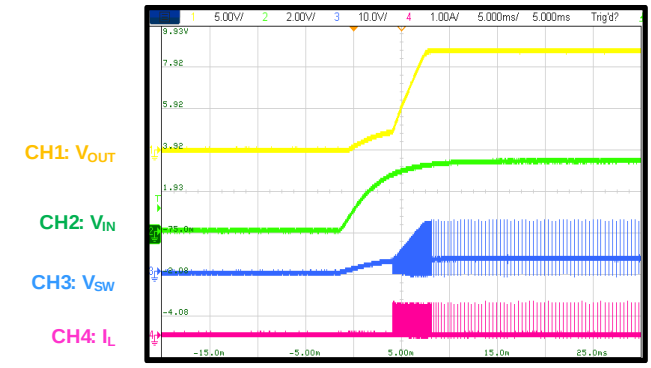
Steady State
I_{OUT} = 0A



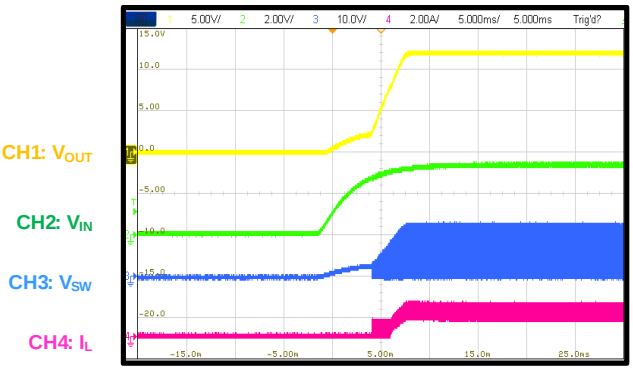
Steady State
I_{OUT} = 0.3A



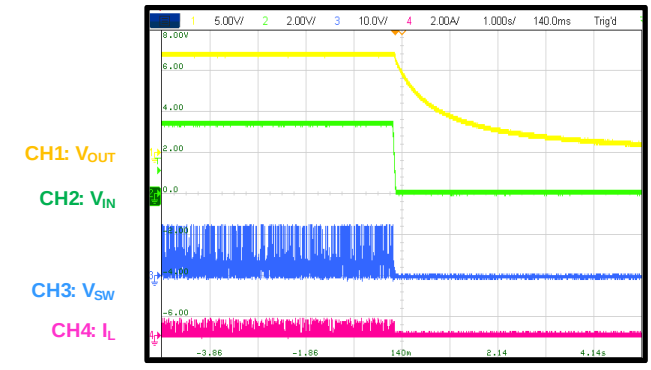
Start-Up through VIN
I_{OUT} = 0A



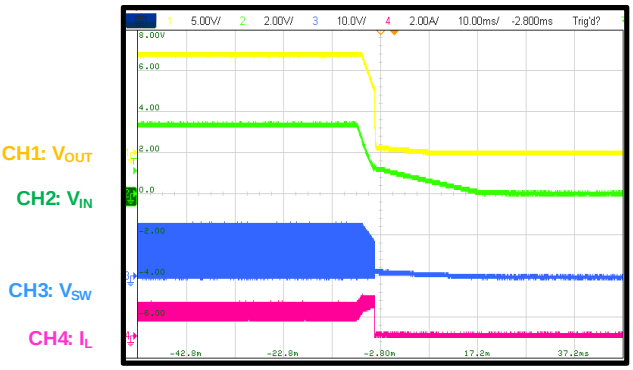
Start-Up through VIN
I_{OUT} = 0.3A



Shutdown through VIN
I_{OUT} = 0A



Shutdown through VIN
I_{OUT} = 0.3A



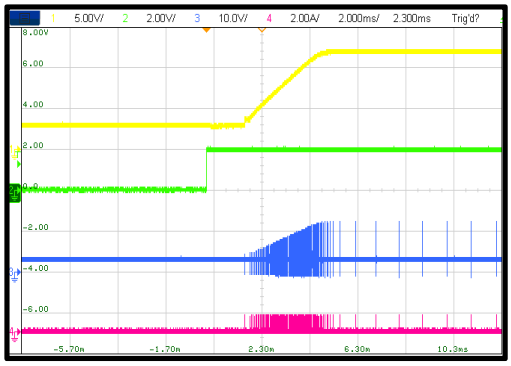
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

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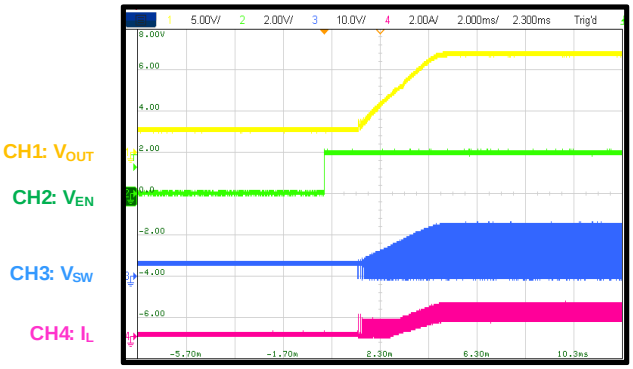
Start-Up through EN

I_{OUT} = 0A



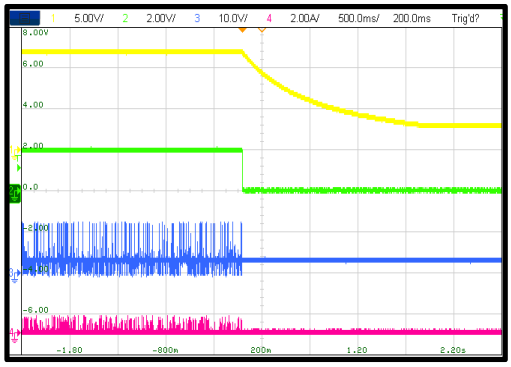
Start-Up through EN

I_{OUT} = 0.3A



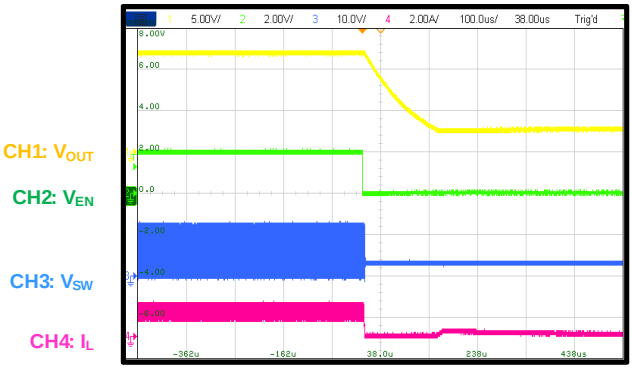
Shutdown through EN

I_{OUT} = 0A



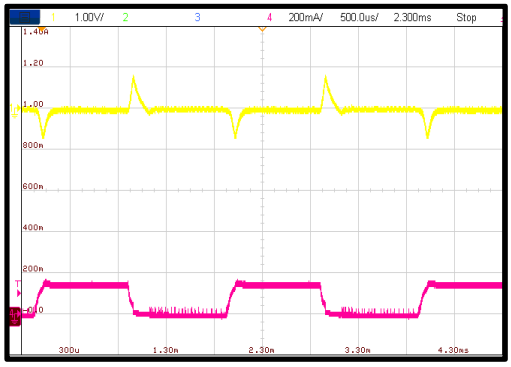
Shutdown through EN

I_{OUT} = 0.3A



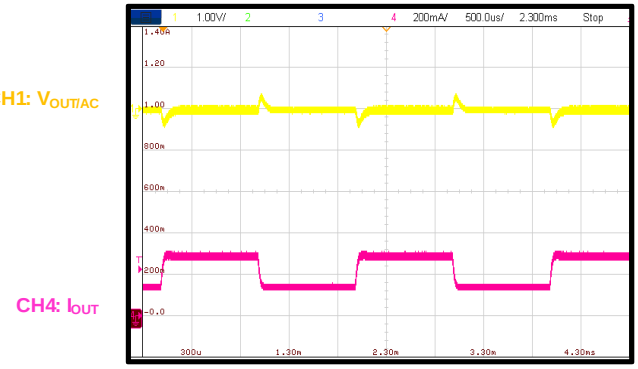
Load Transient Response

I_{OUT} = 0A to 0.15A, slew rate = 25mA/µs (e-load)



Load Transient Response

I_{OUT} = 0.15A to 0.3A, slew rate = 25mA/µs (e-load)



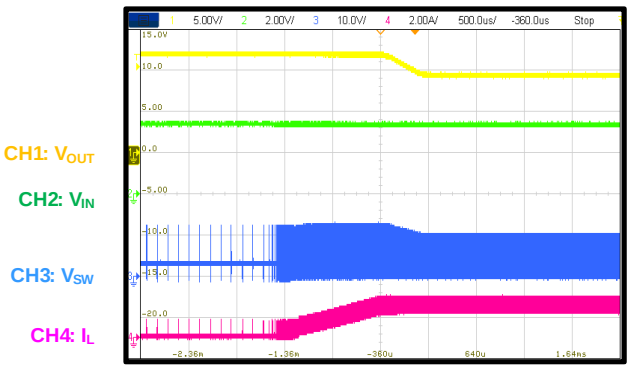
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 12V, L = 3.3µH, I_{OUT} = 0.3A, T_A = 25°C, unless otherwise noted.

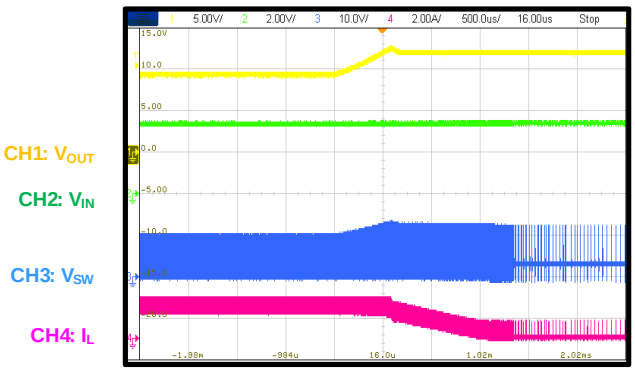
OCP Entry

Increase load current to overload



OCP Recovery

Decrease the load current to 0A



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FUNCTIONAL BLOCK DIAGRAM

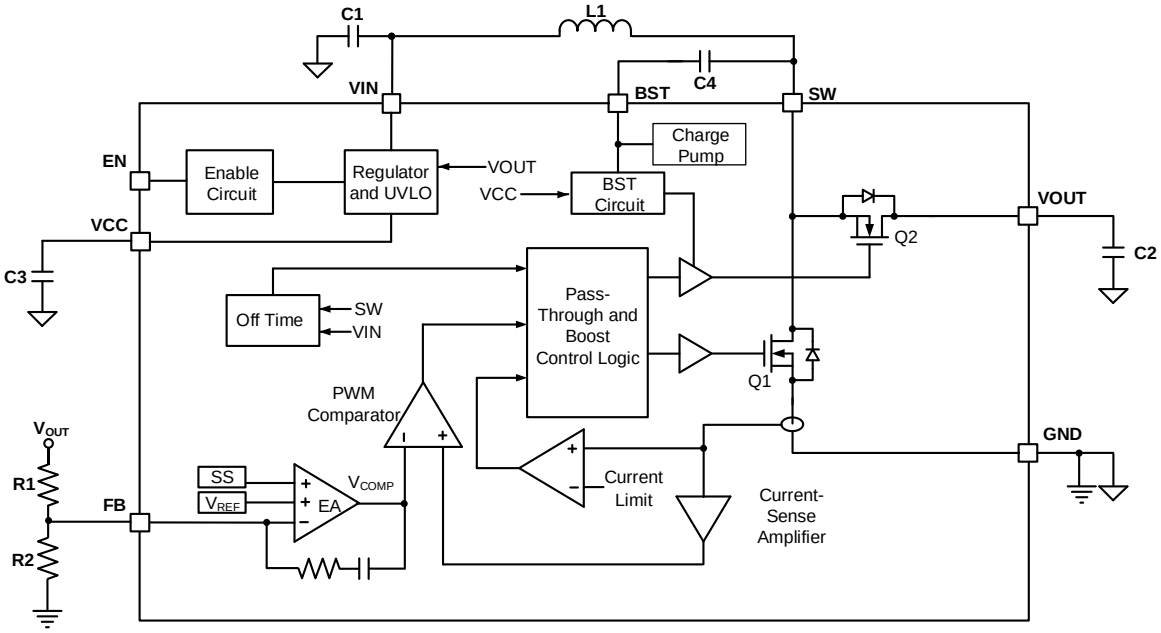


Figure 1: Functional Block Diagram

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OPERATION

The MP3438 is a high-efficiency boost converter with a 1.2MHz fixed frequency and a wide input voltage (V_{IN}) range. The device's fully integrated MOSFETs provide high efficiency in a reduced size for voltage step-up applications. Constant-off-time (COT) control provides fast transient response. Figure 1 on page 12 shows the internal block diagram.

Boost Operation

The MP3438 uses COT control to regulate the output voltage (V_{OUT}).

At the beginning of each cycle, the low-side N-channel MOSFET (LS-FET, also known as Q1) turns on, forcing the inductor current to rise. The current through the LS-FET is sensed. If the current signal rises above the value set by the COMP voltage (V_{COMP}), the pulse-width modulation (PWM) comparator flips and turns the LS-FET off. Then the inductor current flows to the output capacitor through the high-side MOSFET (HS-FET), causing the inductor current to decrease. COMP is an amplifier output that compares the FB feedback voltage against the internal reference voltage.

After a fixed off time, the LS-FET turns on again and the cycle repeats. During each cycle, the LS-FET off time is determined by the V_{IN} / V_{OUT} ratio, and the on time is controlled by V_{COMP}. This means that the inductor peak current is controlled by COMP, and COMP is controlled by V_{OUT}. By following this process, the device regulates V_{OUT} through the inductor current.

Power-Save Mode (PSM) (Light-Load Operation Mode)

The MP3438 works in power-save mode (PSM) under light load conditions. Once the inductor current drops to 0A, the HS-FET turns off to stop current flowing from VOUT to VIN, forcing the inductor current to work in discontinuous conduction mode (DCM). The internal off time becomes longer once the MP3438 enters DCM. The off time is inversely proportional to the HS-FET's on period in each cycle. In DCM, the off time is longer, and the MP3438 reduces the switching frequency (f_{SW}) to reduce power loss.

If V_{COMP} drops to the PSM threshold, the MP3438 stops switching to further decrease switching power loss. Switching resumes once V_{COMP} exceeds the PSM threshold. Under light-load conditions, the switching pulse skips based on V_{COMP}.

In DCM, the frequency stays low and the LS-FET does not turn on during the prolonged off time. If the load increases V_{COMP} rises, the off time shortens, and the MP3438 returns to normal operation with its 1.2MHz fixed frequency. This allows the loop to respond to higher load currents.

Automatic Pass-Through

If V_{IN} exceeds the set V_{OUT} ($V_{OUT-SET}$), the MP3438 keeps the LS-FET off and turns the HS-FET on continuously. This allows current to pass through the inductor and the HS-FET to the output terminal, which is called automatic pass-through mode. In this mode, the HS-FET turns on slowly to avoid creating an inrush current between VIN and VOUT. The MP3438 runs back to boost switching mode once V_{OUT} drops below 95% of its reference, and V_{COMP} exceeds the PSM threshold.

While the HS-FET is fully on, one internal charge pump is enabled to drive the HS-FET gate. This charge pump is only enabled after the IC runs automatic pass-through mode.

Minimum on Time and Minimum off Time

The MP3438 blanks the LS-FET with an 80ns minimum on time in each cycle to enhance noise immunity. The MP3438 also blanks the LS-FET off state with a minimum off time in each cycle. During the minimum off time, the LS-FET cannot turn on.

LS-FET Maximum on Time

If the inductor current cannot trigger V_{COMP} with a 10µs on time, the MP3438 shuts down the LS-FET. After the LS-FET shuts down, the inductor current can go through the HS-FET and charge V_{OUT} during the LS-FET's off time. Under heavy load transient conditions, this can help refresh V_{OUT} with a minimum 100kHz frequency.

VCC Power

The MP3438's internal circuit is powered by VCC. A minimum 1µF ceramic capacitor must

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be connected to VCC. When V_{IN} drops below 3.4V, VCC is powered from the higher value between either V_{IN} or V_{OUT}. This allows the MP3438 to maintain a low $R_{DS(ON)}$ and high efficiency even when V_{IN} is low. When V_{IN} exceeds 3.4V, VCC is always powered by VIN. This reduces regulator loss between the VOUT and VCC pins.

If VCC is powered by an external supply and V_{CC} exceeds 3.4V, the regulators from the VIN and VOUT pins are disabled. Under this condition, the MP3438 starts up once the external VCC power supply exceeds VCC_{UVLO}, even if V_{IN} is as low as 0.9V. When VCC is powered by an external power supply, the MP3438 continues working as long as V_{IN} and V_{OUT} both exceed 0.8V, even if V_{IN} and V_{OUT} are dropping. The external VCC power source should be limited to 3.6V.

There is a reverse-blocking circuit that limits the current flowing between VIN and VOUT. If the external VCC power source exceeds the VCC regulation voltage, the current is supplied from the external power, and there is no current path from VCC to VIN, or from VCC to VOUT.

VCC is charged when V_{IN} exceeds 0.9V and EN exceeds the micro-power threshold. If EN is low, VCC is disconnected from VIN and VOUT. Supply VIN with a power source exceeding 2.7V during V_{IN} start-up to provide VCC sufficient power voltage.

Start-Up

When the MP3438 input is powered up, and EN is high, the MP3438 starts charging VCC from VIN. Once V_{CC} exceeds its UVLO threshold, the MP3438 starts switching with closed-loop control. If VCC is powered by additional supply, the MP3438 starts switching once V_{CC} exceeds its UVLO rising threshold.

After the IC is enabled, the MP3438 starts with soft-start (SS) control. The SS signal is controlled by the internal signal from 0V and compared with the internal reference voltage (V_{REF}). The lower value is fed to the error amplifier to control V_{OUT}. After the SS signal exceeds V_{REF}, soft start completes and V_{REF} takes charge of the feedback loop regulation.

The internal SS signal quickly pulls low if the MP3438 turns off to due to UVLO or a protection.

If there is a biased voltage on VOUT, the MP3438 does not switch until the SS signal rises above V_{FB}, which is proportional to the V_{OUT} biased voltage.

Synchronous Rectifier and BST Function

The MP3438 integrates both an LS-FET (Q1) and HS-FET (Q2) to reduce the number of external components. During switching, Q2 is powered from the BST pin (typically 3.2V above the SW voltage). The 3.2V bootstrap voltage is charged from VCC when the LS-FET turns on.

During automatic pass-through mode, BST is regulated by an internal charge pump.

Switching Current Limit

The MP3438 provides a fixed, cycle-by-cycle switching peak current limit. In each cycle, the internal current-sense circuit monitors the LS-FET current signal. Once the sensed current reaches the 2A (typically) current limit, Q1 turns off. The LS-FET current signal is internally blanked for about 80ns to enhance noise immunity.

Enable (EN) and Configurable Under-Voltage Lockout (UVLO)

The EN pin enables and disables the MP3438. When a voltage is applied to EN and it exceeds the high threshold (1V maximum), the MP3438 starts up some of the internal circuits (micro-power mode). If the EN voltage exceeds the turn-on threshold (1.2V), the MP3438 enables all functions and starts boost operation.

Boost switching is disabled if the EN voltage falls below its turn-on threshold (1.2V). To completely shut down the MP3438, a <0.4V low-level voltage is required on the EN pin. After shutdown, the MP3438 sinks a very low current from the input power. The EN pin is compatible with voltages up to 16V. For automatic start-up, connect the EN pin directly to VIN.

The MP3438 features a configurable UVLO hysteresis. When powering up the device in micro-power mode, EN sinks a 5μA current

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from an upper resistor, R_{TOP} (see Figure 2). Then V_{IN} must rise to overcome the current sink.

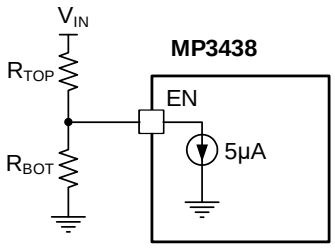


Figure 2: Configuring V_{IN} UVLO

The V_{IN} start-up threshold can be calculated with Equation (1):

$$V_{IN\text{-}ON} = V_{EN\text{-}ON} \times \left(1 + \frac{R_{TOP}}{R_{BOT}}\right) + 5\mu A \times R_{TOP} \quad (1)$$

Where $V_{EN\text{-}ON}$ is the EN pin's turn-on threshold (1.2V, typically).

Once the EN voltage reaches $V_{EN\text{-}ON}$, the 5μA sink current turns off to create a reverse hysteresis for the V_{IN} falling threshold. This hysteresis can be estimated with Equation (2):

$$V_{IN\text{-}UVLO\text{-}HYS} = 5\mu A \times R_{TOP} \quad (2)$$

Over-Voltage Protection (OVP)

The MP3438 supports FB pin over-voltage protection (OVP). If the FB voltage (V_{FB}) exceeds 110% of the reference voltage (V_{REF}), the MP3438 turns LS-FET the off. The device does not recover until V_{FB} drops below 105% of V_{REF}.

Thermal Protection

Thermal shutdown prevents the IC from operating at exceedingly high temperatures. If the die temperature exceeds 150°C, the MP3438 shuts down and resumes normal operation when the die temperature drops to 125°C.

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APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider sets the output voltage (V_{OUT}). The feedback resistor (R1) must be used for both stability and the dynamic response. Generally, set R1 between 100kΩ and 1MΩ. R2 can be calculated with Equation (3):

$$R2 = \frac{V_{REF}}{V_{OUT} - V_{REF}} \times R1 \quad (3)$$

Where V_{REF} is 1V.

Input Start-Up Inrush Current Control

During input start-up, the inrush current through the HS-FET body diode should be limited below 6A. If the start-up inrush current exceeds 6A during board evaluation, the system must be optimized. A few methods to reduce the inrush current are listed below.

1. Reduce the initial start-up V_{IN}, or reduce the V_{IN} start-up slew rate.
2. Reduce the large output capacitor's volume, or add a MOSFET between the MP3438's output and bulk capacitor to smoothly charge the bulk capacitor.

Selecting the Input Capacitor

The input capacitor (C1) is used to maintain the DC input voltage. Low-ESR ceramic capacitors are recommended. The input voltage ripple can be estimated with Equation (4):

$$\Delta V_{IN} = \frac{V_{IN}}{8f_{sw}^2 \times L \times C1} \times \left(1 - \frac{V_{IN}}{V_{OUT}}\right) \quad (4)$$

Where f_{SW} is the switching frequency, and L is the inductor value.

Selecting the Output Capacitor

The boost converter has a discontinuous output current, and requires an output capacitor (C2) to supply AC current to the load. For the best performance, low-ESR ceramic capacitors are recommended. The output voltage ripple can be calculated with Equation (5):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{sw} \times R_L \times C2} \times \left(1 - \frac{V_{IN}}{V_{OUT}}\right) \quad (5)$$

Where R_L is the value of the load resistor.

Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients.

Selecting the Inductor

MPL **Optimized Performance with MPS Inductor MPL-AL4020 Series**

An inductor is required to transfer the energy between the input source and the output capacitors. A larger-value inductor results in less ripple current and a lower peak inductor current, which reduces the stress on the power MOSFET. However, a larger-value inductor is physically larger, has a higher series resistance, and has a lower saturation current.

For most designs, the inductance can be estimated with Equation (6):

$$L = \frac{V_{IN}\left(V_{OUT} - V_{IN}\right)}{f_{sw} \times V_{OUT} \times \Delta I_L} \quad (6)$$

Where ΔI_L is the inductor ripple current.

Choose the inductor ripple current to be approximately 20% to 50% of the maximum inductor average current. Typically, a 3.3µH inductor is recommended. Ensure that the inductor does not saturate under the worst-case condition. The inductor should have a low series resistance (DCR) to reduce the resistive power loss.

MPS inductors are optimized and tested for use with our complete line of integrated circuits.

Table 1 lists our power inductor recommendations. Select a part number based on your design requirements.

Table 1: Power Inductor Selection

Part Number	Inductor Value	Manufacturer
MPL-AL	0.47µH to 4.7µH	MPS
MPL-AL4020-3R3	3.3µH	MPS

Visit MonolithicPower.com under Products > Inductors for more information.

Selecting the VCC Capacitor

The MP3438 integrates the VCC power at about 3.4V, which powers the internal MOSFET gate driver and internal control circuit.

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One 1µF or higher ceramic bypass capacitor is required for the internal regulator. Do not connect an external load to VCC.

Selecting the BST Capacitor

The MP3438 uses one bootstrap circuit to power the output N-channel MOSFET. One external bootstrap capacitor is required for the charge pump power. It is recommended to place a 0.1µF ceramic capacitor between the BST and SW pins.

Setting the Under-Voltage Lockout (UVLO) Threshold

The MP3438 features a configurable under-voltage lockout (UVLO) hysteresis set by the EN resistor dividers (see Figure 2 on page 15). When starting up, EN sinks a 5µA current from the upper resistor to configure the hysteresis.

The V_{IN} start-up threshold can be calculated with Equation (1) on page 15 and the hysteresis can be estimated with Equation (2) on page 15.

For automatic start-up, set a 150mV hysteresis by connecting EN to a 30kΩ R_{TOP}.

Design Example

Table 2 shows a design example following the application guidelines for the specifications below:

Table 2: Design Example

V_{IN}	3V to 16V
V_{OUT}	12V
I_{OUT}	0.3A

Figure 4 on page 19 shows the detailed application schematic. The typical performance and circuit waveforms are shown in the Typical Performance Characteristics section on page 8. For more device applications, refer to related evaluation board datasheet.

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PCB Layout Guidelines

Efficient PCB layout is critical for high-frequency switching power supplies. A poor layout can result in reduced performance, excessive EMI, resistive loss, and system instability.

For the best results, refer to Figure 3 and following the guidelines below:

1. Place the output capacitor (C2B) as close to VOUT and GND pins as possible.
2. Place a 0.1µF capacitor (C2A) close to the IC to reduce the PCB parasitic inductance (shown as the yellow components).
3. Keep the connection between VOUT and GND and the output capacitor short and wide, and use copper.
4. Place the copper, the IC, and C_{OUT} on the same layer.
5. Place the FB divider (R1 and R2) as close to the FB pin as possible.
6. Keep the FB trace far away from noise sources, such as the SW node.
7. Connect the VCC capacitor to GND with a short loop.
8. Keep the input loop (C1, L1, SW, and GND) as small as possible.
9. Places enough GND vias close to MP3438 for good thermal dissipation.

See Figure 3 for layout recommendation, which is based on the schematic in Figure 4.

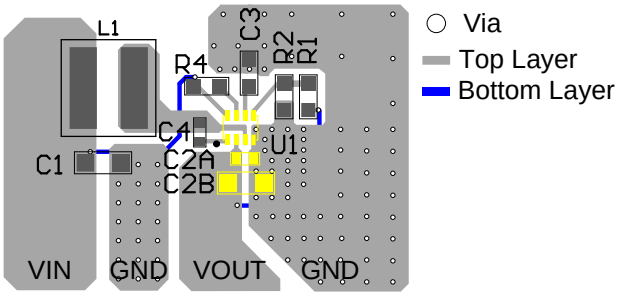


Figure 3: Recommended PCB Layout (13)

Note:

13) Figure 3 is based on Figure 4 on page 19.

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TYPICAL APPLICATION CIRCUIT

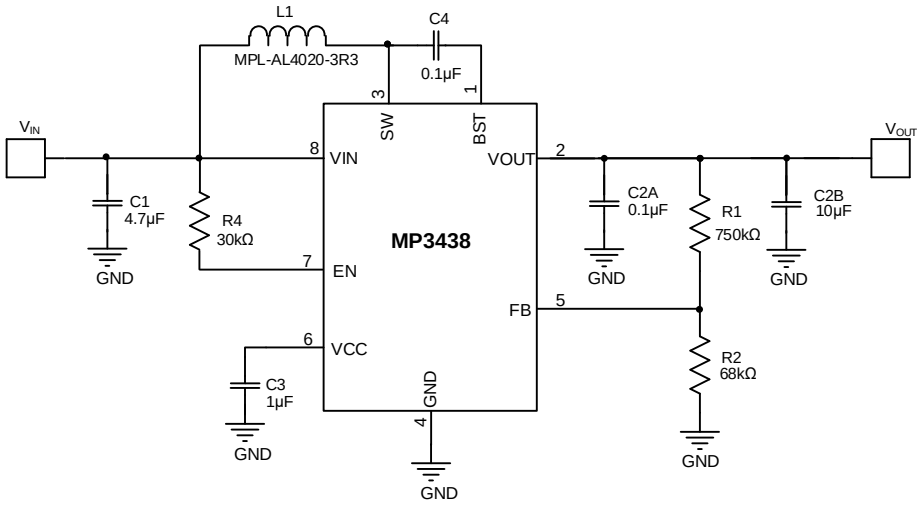
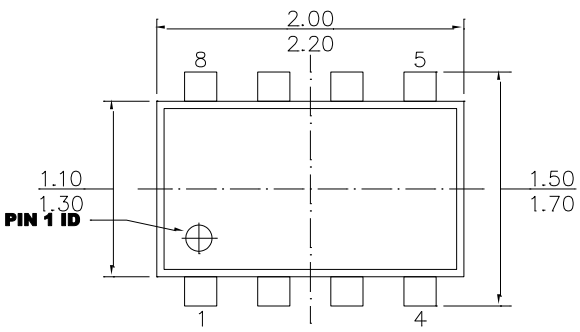


Figure 4: Typical Application Circuit for a 12V Output

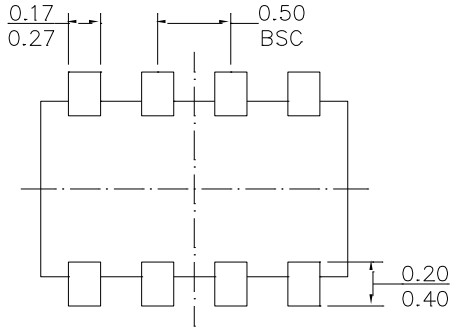
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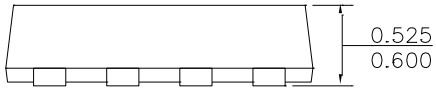
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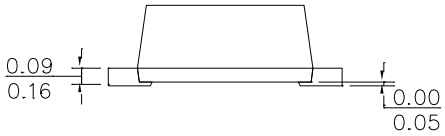
TOP VIEW



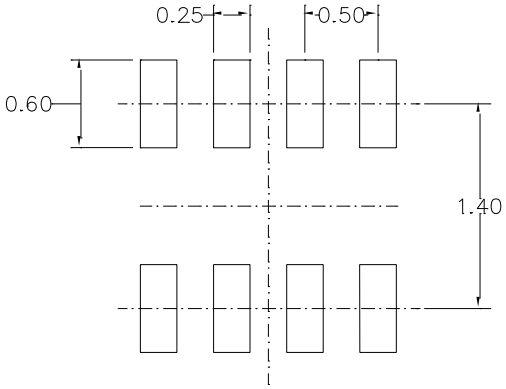
BOTTOM VIEW



FRONT VIEW



SIDE VIEW



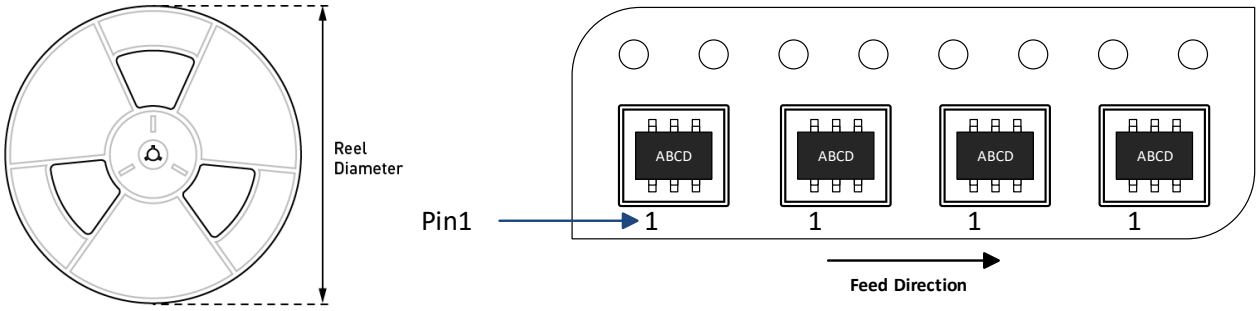
RECOMMENDED LAND PATTERN

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3) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
4) DRAWING IS NOT TO SCALE.

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CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP3438GTL-Z	SOT583	5000	N/A	N/A	7in	8mm	4mm

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	3/23/2022	Initial Release	-

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