4.7V to 17V Input, 5A Synchronous Buck Regulator with I²C Interface

Features

- Wide VIN Range: 4.7V to 17V
- Maximum Continuous Output Current: 5A
- I²C Control Interface
- Programmable Output Voltage from 0.8V to 5.5V
- Integrated High / Low-Side FETs (65mΩ / 35mΩ)
- Advanced Adaptive On-Time Control
- Fast Transient Response
- ±0.5% Feedback Voltage Reference
- Zero Shutdown Supply Current
- 50μA Non-Switching Operating Quiescent Current
- 80μA No Load Operating Quiescent Current
- High Efficiency in Light Load and Heavy Load.
- Programmable Switching Frequency with 500kHz, 1MHz, 1.5MHz, and 2MHz options
- Internal Soft-Start
- Programmable Forced CCM, Automatic CCM/PFM
- Built-in Cycle-by-Cycle Current Limit, Short Circuit Protection, Input UVLO, Output Under-Voltage Protection, Output Over-Voltage Protection, and Thermal Shutdown Protection
- Small 20-bump WLCSP (1.7mm x 2.0mm)

Applications

- CPU, GPU, AP, DSP, FPGA, VIO, VSYS
- HDD, LPDDR3, LPDDR4 Memory Power
- Tablets, Netbooks, Ultra-Books, Mobile Internet Devices, IoT, and Server.
- DSC, Drones, Gaming Consoles, TV Set Box

Description

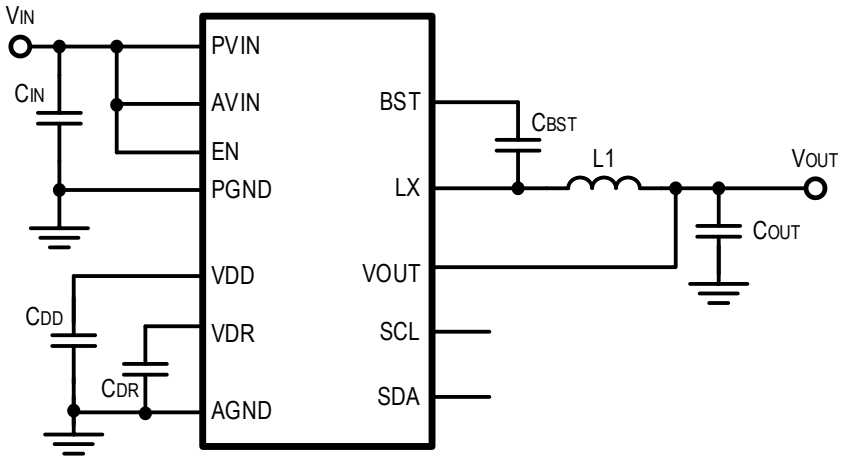
The KTB8371 is 5A, 17V synchronous buck regulators with integrated high-side and low-side power FETs. The device operates over a wide input voltage range to support a variety of applications with input voltage from regulated 5V and12V power rails and multicell batteries.

KTB8371 employs Kinetic's proprietary advanced adaptive on-time (AOT) control for fast transient response and high output voltage accuracy. This control technique eliminates external loop compensation network and allows the use of ceramic output capacitors without ripple-generating circuitry. These features enable very small total solution size and make the KTB8371 easy to use.

The device features an internal soft-start function to limit inrush current during start-up. The output voltage can be adjusted via I²C with 3μs/step ramp-up/down rate. The device has comprehensive built-in protection features including input voltage UVLO, high-side cycle-by-cycle peak current limit, low-side valley current limit, reverse current protection, short-circuit protection, output over-voltage protection, and thermal shutdown.

KTB8371 are available in RoHS and Green compliant 20-bump 1.7mm x 2.0mm x 0.6mm wafer-level chip-scale package (WLCSP20).

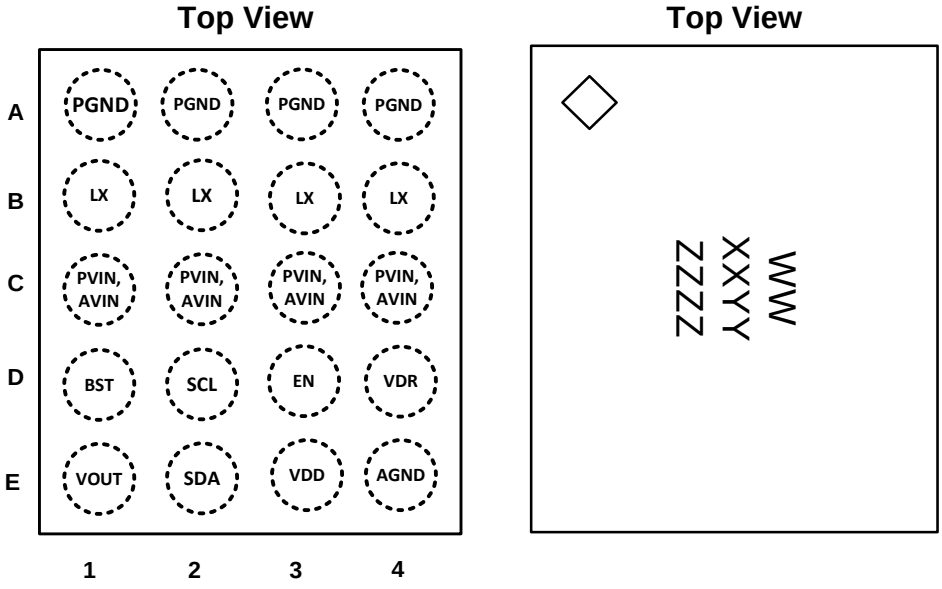
Typical Application Schematic



Pin Descriptions

Pin #	Pin Name	Function
A1, A2, A3, A4	PGND	Power ground for buck regulator
B1, B2, B3, B4	LX	Inductor connection for buck regulator
C1, C2, C3, C4	PVIN, AVIN	Input Voltage Power and Sense Pins for buck regulator. Connect to a power rail ranges from 4.7V to 17V.
D1	BST	Boost capacitor for charge pump gate driver
D2	SCL	I2C clock digital input
D3	EN	Chip enable logic input
D4	VDR	Power stage driver voltage
E1	VOUT	Output voltage sense input
E2	SDA	I2C data digital I/O
E3	VDD	Analog circuit bias voltage
E4	AGND	Analog ground for analog circuit

Pinout Diagram



20-Bump 1.710mm x 2.063mm x 0.62mm
WLCSP Package
Top Mark
WW = Device ID Code, XX = Date Code
YY = Assembly Code, ZZZZ = Serial Number

Absolute Maximum Ratings[1]

(T_A = 25°C unless otherwise noted)

Description		Value	Units
PVIN to PGND		-0.3 to 18	V
PGND to AGND		-0.3 to 0.3	V
LX to PGND		-0.3 to (PVIN +0.3)	V
BST to LX		-0.3 to 5.5	V
VOUT, VDD, and VDR to AGND		-0.3 to 5.5	V
EN, SCL, SDA to AGND		-0.3 to 5.5	V
LX	Continuous Current	7	ARMS
	Peak Current (2.5ms maximum)	10	APEAK
Operating Junction Temperature Range		-40 to 150	°C
Storage Temperature Range		-55 to 150	°C
Maximum Soldering Temperature (at leads, 10 sec)		260	°C

ESD Ratings[2]

Symbol	Description	Value	Units
V(ESD) Electrostatic Discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins	±2000	V
	Charged device model (CDM), per JEDEC specification JESD22C101, all pins	±500	

Thermal Capabilities[3]

Symbol	Description	Value	Units
Θ_{JA}	Thermal Resistance – Junction to Ambient	67.7	°C/W
P_D	Maximum Power Dissipation at T_A = 25°C	1.85	W
$\Delta P_D / \Delta T$	Derating Factor Above T_A = 25°C	-14.77	mW/°C

Ordering Information

Part Number	Marking[4]	Default Settings[5]			Package
		VOUT	Fsw	Mode	
KTB8371AEIB-5C-TR	OXXXYYZZZZ	5.0V	500kHz	Auto-Skip	WLCSP20
KTB8371BEIB-5C-TR	PBXXYYZZZZ	3.3V	500kHz	Auto-Skip	WLCSP20
KTB8371CEIB-5C-TR	PFXXYYZZZZ	1.8V	500kHz	Auto-Skip	WLCSP20

1. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum rating should be applied at any one time.
2. ESD Ratings conform to JEDEC industry standards. Some pins may actually have higher performance. Ratings apply with chip enabled, disabled, or unpowered, unless otherwise noted.
3. Junction to Ambient thermal resistance is highly dependent on PCB layout. Values are based on thermal properties of the device when soldered to an EV board.
4. XX = Date Code, YY = Assembly Code, ZZZZ = Serial Number.
5. The first released part is Vout = 3.3V. Please Contact a Kinetic Technologies representative regarding versions with other default settings.

Electrical Characteristics[6]

Unless otherwise noted, *Typ* values are specified at +25°C with V_{IN} = 12V. The *Min* and *Max* specs are applied over the full operation temperature range of -40°C to +85°C and V_{IN} = 4.7V to 17V.

Symbol	Description	Conditions	Min.	Typ.	Max.	Units
Supply Specifications						
PV_{IN}	Input Supply Operating Range		4.7		17	V
V_{UVLO}	Under-Voltage Lockout Threshold	V_{IN} rising	3.35	4.25	4.7	V
		Hysteresis		500		mV
I_{IN}	VIN Supply Current	EN = High, V_{IN} = 12V, Non-Switching		50		µA
		EN = High, V_{IN} = 12V, Auto-Skip		80		µA
		EN = High, V_{IN} = 12V, Forced-PWM		10		mA
I_{SHDN}	Shutdown Supply Current	EN = Low, T_A = 25°C		0.01	1	µA
Logic Pin Specifications (EN)						
V_{IH}	Input Logic High (EN)		3.8			V
V_{IL}	Input Logic Low (EN)				0.4	V
I_{I_LK}	Input Logic Leakage (EN)	T_A = 25°C, V_{EN} = 5V		0.01	1	µA
I2C-Compatible Interface Specifications (SCL, SDA), see Figure 1						
V_{IH}	Input Logic High Threshold		3.8			V
V_{IL}	Input Logic Low Threshold				0.4	V
V_{OL}	SDA Output Logic Low	I_{SDA} = 3mA			0.4	V
t_1	SCL clock period		2.5			µs
t_2	Data in setup time to SCL high		100			ns
t_3	Data out stable after SCL low		0			ns
t_4	SDA low setup time to SCL low (Start)		100			ns
t_5	SDA high hold time after SCL high (Stop)		100			ns
Thermal Shutdown Specifications						
T_{J_SHDN}	IC Junction Thermal Shutdown	T_J rising		150		°C
		Hysteresis		20		°C

Continue on page 5

6. Device is guaranteed to meet performance specifications over the -40°C to +85°C operating temperature range by design, characterization and correlation with statistical process controls.

Electrical Characteristics

Unless otherwise noted, *Typ* values are specified at +25°C with V_{IN} = 12V. The *Min* and *Max* specs are applied over the full operation temperature range of -40°C to +85°C and V_{IN} = 4.7V to 17V.

Buck Regulator Specifications						
V_{OUT}	KTB8371A Output Voltage Setting Range	I2C Programmable, see VSEL Configuration Register(0x00[5:0])	2.0		5.5	V
	KTB8371B Output Voltage Setting Range	I2C Programmable, see VSEL Configuration Register(0x00[5:0])	1.2		3.3	V
	KTB8371C Output Voltage Setting Range	I2C Programmable, see VSEL Configuration Register(0x00[5:0])	0.8		2.2	V
V_{OUT_STEP}	KTB8371A Output Voltage Setting Step size			100		mV
	KTB8371B Output Voltage Setting Step size			60		mV
	KTB8371C Output Voltage Setting Step size			40		mV
V_{OUT_acc}	Output Voltage DC Accuracy	T_A = 25°C, FPWM	-0.7		0.7	%
I_{OUT_max}	Maximum Continuous Output Current		5			A
I_{peak}	High-Side Switch Peak-Current Limiting Threshold		6.4	8	9.6	A
I_{valley}	Low-Side Switch Valley-Current Limiting Threshold		6	7.5	9	A
I_{rev}	Low-Side Reverse Current Limiting Threshold	Forced PWM Mode		-3		A
I_{zcd}	Zero-Crossing-Detection Threshold	Automatic Skip Mode		0		mA
R_{dson_h}	High-Side Switch On-Resistance			60	75	mΩ
R_{dson_l}	Low-Side Switch On-Resistance			30	40	mΩ
R_{LX_DIS}	LX Active Discharge Resistance	Auto discharge mode enable in Default Setting		200		Ω
K_{AOT}	Adaptive-On-Time Constant	t_{ON} = K_{AOT} x (V_{OUT}/V_{IN})		2100		ns
Fsw	Switching Frequency	Default Fsw = 500kHz		500		kHz
		Default Fsw = 1000kHz		1000		
		Default Fsw = 1500kHz		1500		
		Default Fsw = 2000kHz		2000		
t_{SS_DELAY}	V_{OUT} Soft-Start Delay	EN = Low to High		2		ms
V_{OUT_RR}	V_{OUT} Soft-Start Ramp Rate	VOUT = 5V		8		mV/µs
		VOUT = 3.3V		4		
		VOUT = 1.8V		3		

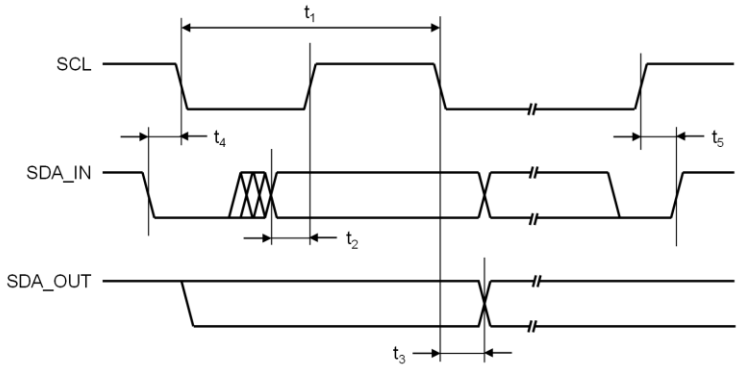
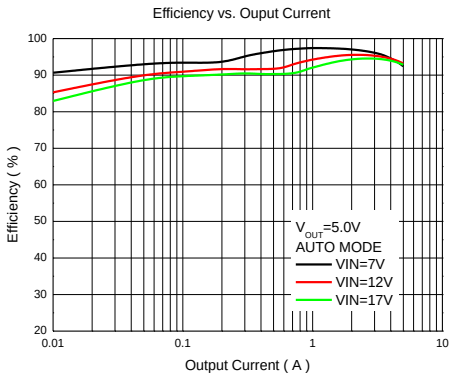


Figure 1. I²C Compatible Interface Timing

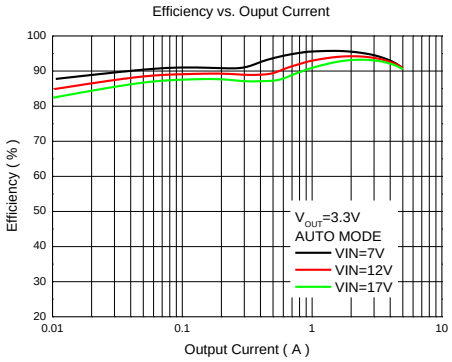
Typical Characteristics

Unless otherwise noted, V_{IN} = 12V, V_{OUT} = 3.3V, f_{SW} = 500kHz, and T_A = 25°C.

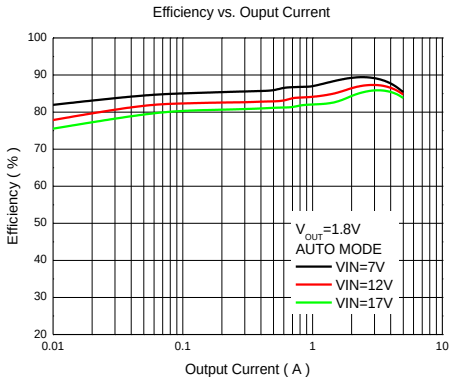
Efficiency (L1 = 2.2µH, fsw = 500kHz)



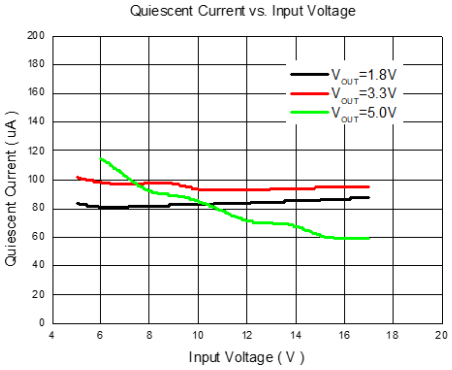
Efficiency (L1 = 2.2µH, fsw = 500kHz)



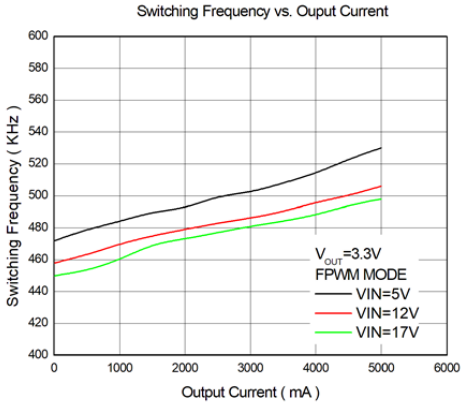
Efficiency (L1 = 2.2µH, fsw = 500kHz)



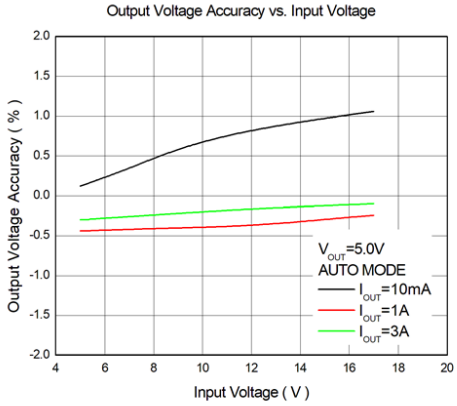
No Load Input Supply Current vs VIN



Switching Frequency vs. Output Current



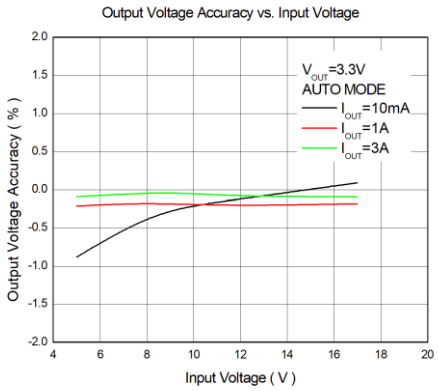
Line Regulation (V_{OUT} = 5V, Auto-Skip Mode)



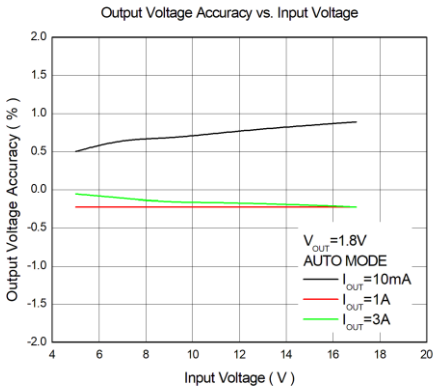
Typical Characteristics (continued)

Unless otherwise noted, V_{IN} = 12V, V_{OUT} = 3.3V, f_{SW} = 500KHz, and T_A = 25°C.

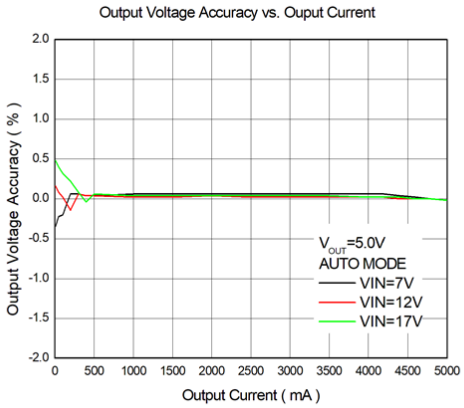
Line Regulation
(V_{OUT} = 3.3V, Auto-Skip Mode)



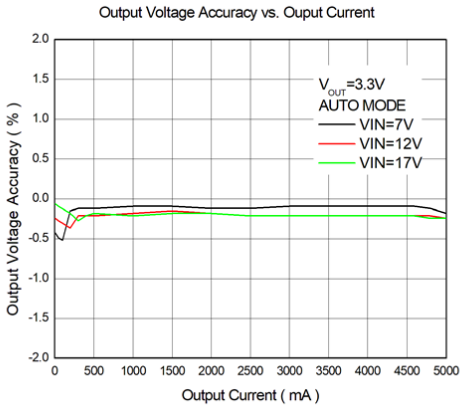
Line Regulation
(V_{OUT} = 1.8V, Auto-Skip Mode)



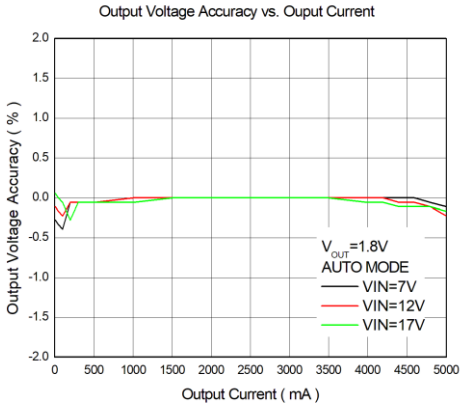
Load Regulation
(V_{OUT} = 5V, Auto-Skip Mode)



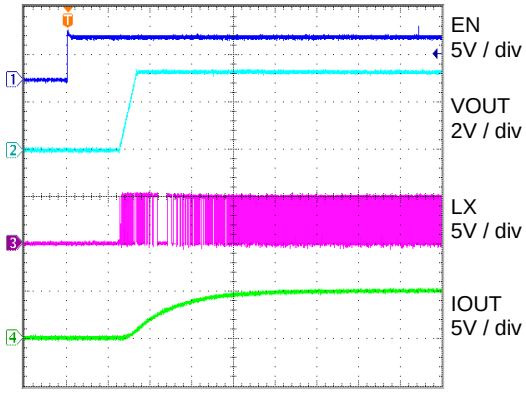
Load Regulation
(V_{OUT} = 3.3V, Auto-Skip Mode)



Load Regulation
(V_{OUT} = 1.8V, Auto-Skip Mode)



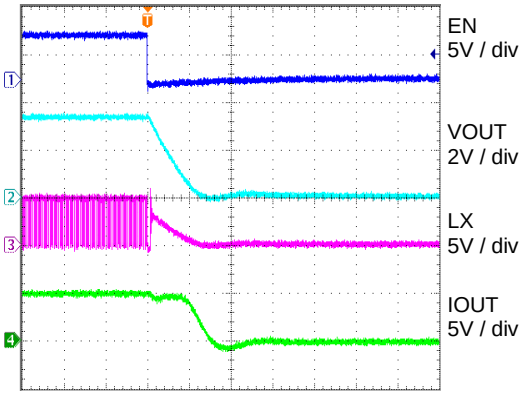
Soft Start with EN
(V_{IN} = 5V, I_{OUT} = 5.0A)



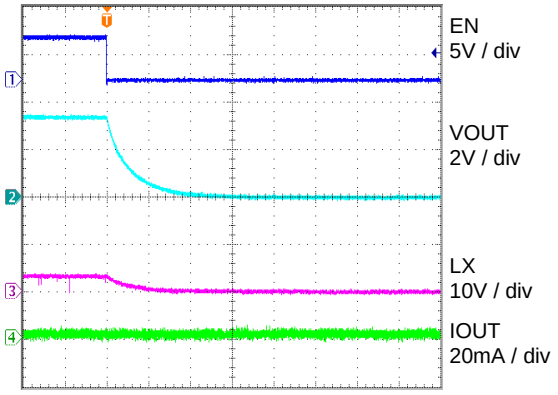
Typical Characteristics (continued)

Unless otherwise noted, V_{IN} = 12V, V_{OUT} = 3.3V, f_{SW} = 500kHz, and T_A = 25°C.

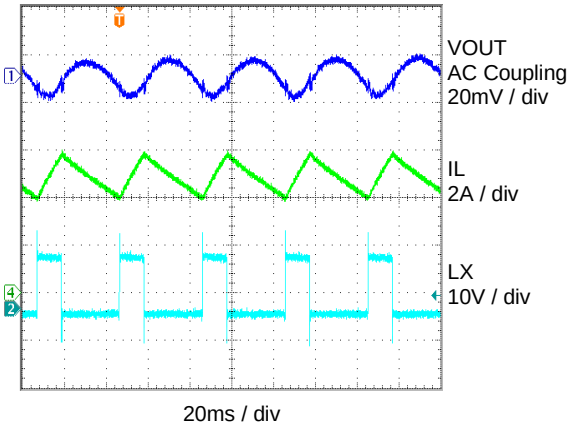
Shutdown with EN
(V_{IN} = 5V, I_{OUT} = 5.0A)



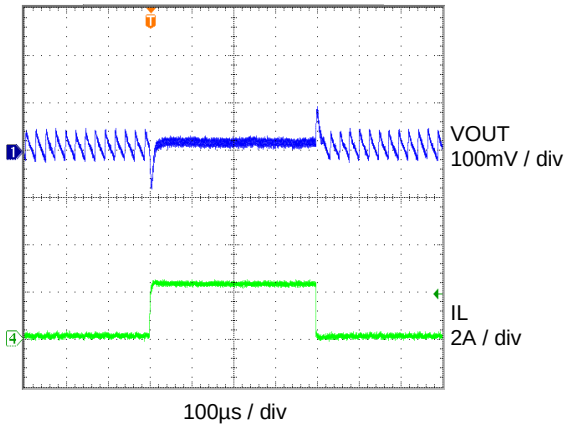
Output Active Discharge
(V_{IN} = 12V, I_{OUT} = 0mA)



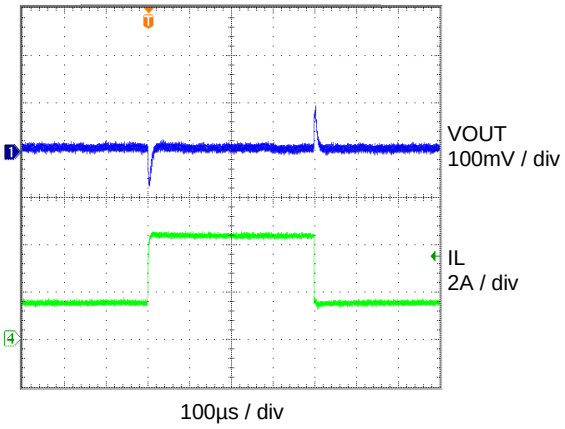
Output Voltage Ripple
(V_{IN} = 12V, IOUT = 5A)



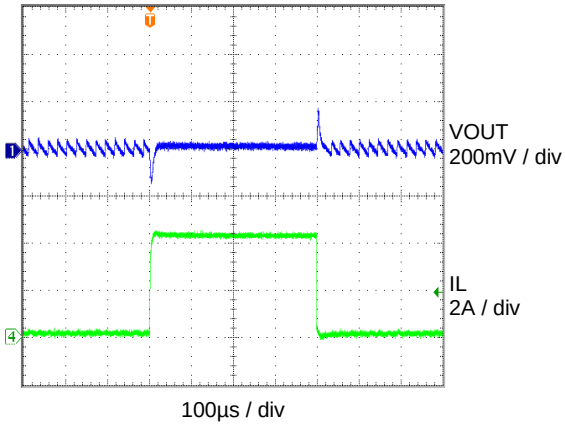
Load Transient
(0.1A-2.5A, Auto-Skip Mode)



Load Transient
(1.5A-4.5A, Auto-Skip Mode)



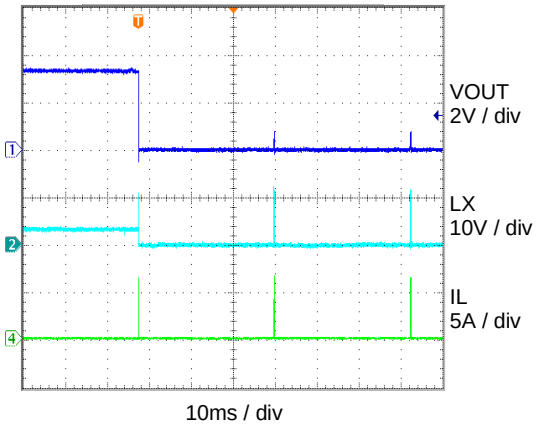
Load Transient
(0A-4.5A, Auto-Skip Mode)



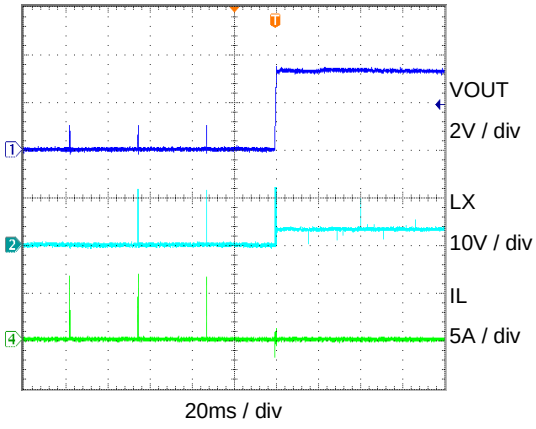
Typical Characteristics (continued)

Unless otherwise noted, V_{IN} = 12V, V_{OUT} = 3.3V, f_{SW} = 500kHz, and T_A = 25°C.

Short Circuit Protection
(Hiccup Mode)



Output Short Protection Recovery
(Hiccup Mode Recovery)



Functional Description

The KTB8371 is a highly efficient, high-performance, monolithic buck regulator that operates from an input voltage of 4.7V to 17.0V and can output up to 5A. It integrates the main switch, synchronous rectifier switch, PWM control circuitry, V_{OUT} setting DAC, various protection features, and an I^2C serial interface to configure the output voltage, dynamic voltage scaling (DVS), control modes change, and software enable/disable function.

Control Scheme

The KTB8371 uses a proprietary adaptive on-time (AOT) PWM control scheme to maintain a nearly constant switching frequency as input voltage and output voltage vary. Compared to typical current-mode PWM schemes, the AOT control scheme provides quick response to line and load transients with excellent stability and wide bandwidth, thereby minimizing output voltage droop and soar for dynamic loads, even with minimal output capacitance. The adaptive on-time approximates fixed-frequency switching without using a fixed clock oscillator, which eliminates the need to wait for the next clock before responding to a load transient.

The KTB8371 feedback loop also adds a proprietary, internal-compensated, integrating error amplifier to remove the output voltage offset normally associated with other AOT, constant on-time (COT), and hysteretic architectures.

Shutdown Mode

When the EN pin is low, the KTB8371 buck is in shutdown mode and draws 0 supply current.

Hardware Enable

The KTB8371 buck regulator is turned on and off via hardware enable using the EN pin. The default register settings allow simple hardware control. For hardware enable, drive the EN pin high. For hardware disable, drive the EN pin low.

Software Enable

KTB8371 also can be enabled using I^2C commands. For software enable/disable control, bring the chip's EN pin to high first. After that, write 1 into the bit (0) of CONTL1 configuration register(0x05) to enable the buck, and write 0 to disable the buck. Refer I2C register map for detailed information.

Soft-Start

The KTB8371 buck contains soft-start circuitry to ramp up V_{OUT} slowly in order to reduce inrush current at V_{IN} and prevent the inductor current from reaching the peak current limit during startup.

Setting the Output Voltage

KTB8371 has three parts (KTB8371A, KTB8371B and KTB8371C) which corresponding to three independent output voltage ranges. KTB8371A has output voltage range from 2.0V to 5.5V in 100mV steps. KTB8371B has output voltage range from 1.2V to 3.3V in 60mV steps. And KTB8371C has output voltage range from 0.8V to 2.2V in 40mV steps. The reference is controlled by VOUT[5:0] in the configuration register (0x00).

The target voltage can be set according to the following Table 1.

Table 1. Output Voltage Setting by VSEL Register(0x00[5:0])

VOUT(0x00[5:0])	VREF	KTB8371C	KTB8371B	KTB8371A
010100	0.40	0.8	1.2	2
010101	0.42	0.84	1.26	2.1
010110	0.44	0.88	1.32	2.2
010111	0.46	0.92	1.38	2.3
011000	0.48	0.96	1.44	2.4
011001	0.50	1	1.5	2.5
011010	0.52	1.04	1.56	2.6
011011	0.54	1.08	1.62	2.7
011100	0.56	1.12	1.68	2.8
011101	0.58	1.16	1.74	2.9
011110	0.60	1.2	1.8	3
011111	0.62	1.24	1.86	3.1
100000	0.64	1.28	1.92	3.2
100001	0.66	1.32	1.98	3.3
100010	0.68	1.36	2.04	3.4
100011	0.70	1.4	2.1	3.5
100100	0.72	1.44	2.16	3.6
100101	0.74	1.48	2.22	3.7
100110	0.76	1.52	2.28	3.8
100111	0.78	1.56	2.34	3.9
101000	0.80	1.6	2.4	4
101001	0.82	1.64	2.46	4.1
101010	0.84	1.68	2.52	4.2
101011	0.86	1.72	2.58	4.3
101100	0.88	1.76	2.64	4.4
101101	0.90	1.8(default)	2.7	4.5
101110	0.92	1.84	2.76	4.6
101111	0.94	1.88	2.82	4.7
110000	0.96	1.92	2.88	4.8
110001	0.98	1.96	2.94	4.9
110010	1.00	2	3	5(default)
110011	1.02	2.04	3.06	5.1
110100	1.04	2.08	3.12	5.2
110101	1.06	2.12	3.18	5.3
110110	1.08	2.16	3.24	5.4
110111	1.10	2.2	3.3(default)	5.5

Dynamic Voltage Scaling (DVS)

For KTB8371, each time VREF is set to different value, Dynamic Voltage Scaling (DVS) is used to slew the output voltage to the new voltage according above table. The DVS slew rate is 12µs/step ramp-up/down with each reference step 20mV. User should not change DIV register during the DVS. DIV register can only be changed when chip switching is disabled by setting “chipEnb” high. Chang DIV register value when chip is still switching can damage the chip.

Forced-PWM vs. Auto-Skip Modes

KTB8371 has two ways to control switching behavior – Forced-PWM mode and Auto-Skip mode.

In Forced-PWM, the switching frequency remains nearly constant. This mode is helpful for applications that are noise sensitive.

In Auto-Skip mode, the Buck converter transitions automatically between PWM switching at heavy loads and Skip/PFM switching at light loads. Auto-Skip mode is helpful for applications that need high efficiency at light loads. While skipping, single pulses are evenly spaced, resulting in the lowest output ripple and noise when compared to competing “pulse-grouping” or “burst mode” devices.

The switching mode is I^2C programmable using the FPWM bit (B2) in the CONTL0 configuration register (0x01). The default mode settings are factory trimmed, and several versions are available – see the *Ordering Information* section.

Active Discharge

When the KTB8371 buck is disabled, an active discharge feature can be achieved by connects an about 200ohm on-chip resistor (R_{LX_DIS}) between the LX and PGND pins. This resistor discharges the output capacitor through the inductor. This discharge function can be enabled or disabled using the DISCH bit (B0) in the CONTL0 register (0x01)

Register Reset

The KTB8371 does NOT contain non-volatile memory for the register settings. When V_{IN} rises above V_{UVLO}, either at initial power up or after a temporary V_{IN} droop below V_{UVLO}, a Power-On Reset (POR) circuit resets all registers to their factory default settings. Thereafter, as long as V_{IN} remains above V_{UVLO}, the I^2C registers can be written and read, and register contents are preserved, regardless if the buck is enabled or disabled.

Internal Status Monitor

The KTB8371 contains a MONITOR status register (0x04), which can be read to check the present status of the IC. The register has individual bits for the status of V_{IN} power-OK, V_{OUT} power-OK, over-temperature thermal shutdown, and boost low voltage. Refer to the MONITOR register (0x04) description for more details.

Input Under-Voltage Lockout (UVLO)

When the input voltage (V_{IN}) is below the under-voltage lockout threshold (V_{UVLO}), the buck is disabled. When V_{IN} rises above V_{UVLO}, either at initial power up or after a temporary V_{IN} droop below V_{UVLO}, a Power-On Reset (POR) circuit resets all registers to their factory default settings. After POR, and if the buck is enabled, the default soft-start ramp begins.

Inductor Over-Current Protection (OCP)

KTB8371 can protect the buck and the inductor during over-current faults. The current limits control the buck’s switching on a cycle-by-cycle basis and have a higher priority than the regulation threshold and adaptive on-time. During sustained over-current faults, the output voltage typically droops below the regulation threshold.

Both high side FET and low side FET have OCP protection circuit. When either high side or low side FET conduct a current high than OCP threshold, a 50ns timing pulse will be triggered. During this 50ns, high side FET will be OFF and lowside FET will be ON. After this 50ns timing pulse, if low side FET’s current is still larger than its OCP threshold, low side FET will continue be ON and high side FET will be kept OFF. High side FET can only be ON again when low side FET’s current goes below its OCP threshold.

Hiccup Mode and Output Short-Circuit Protection (SCP)

If above OCP event continuously (Eg. above 50ns timing pulses trigged within 2µs) happened 8 times, the buck enters hiccup mode and pause all switching. After 20ms, the buck attempts to soft-start. If the fault persists, the buck once again enters hiccup mode and periodically re-attempts soft-start until the fault is removed. The low duty-factor during hiccup mode prevents the IC from getting hot.

When BUCK output short happens, if OCP event continuously happened 8 times, the chip will enter hiccup mode. If not, but under voltage detected after chip reference ramp beyond 5 steps, chip will also enter hiccup mode.

Thermal Shutdown Over-Temperature (OT)

Over-temperature (OT) protection occurs if the die junction temperature exceeds the thermal shutdown threshold (T_{J_SHDN}). During thermal shutdown, the buck pauses all switching until the die temperature cools. Once cooled, the buck re-starts with the programmed soft-start ramp. The OT status is reflected in the MONITOR register.

Trim Options

The KTB8371 is factory trimmed using one-time programmable (OTP) registers. Standard versions are available for various default output voltage settings and modes – see the *Ordering Information* section. Contact a Kinetic Technologies representative regarding versions with other default settings or I²C slave addresses.

I²C Interface Description

I²C Serial Data Bus

The KTB8371 supports the I²C bus protocol. A device that sends data onto the bus is defined as a transmitter, and a device receiving data as a receiver. The device that controls the bus is called a master, whereas the devices controlled by the master are known as slaves. A master device must generate the serial clock (SCL), control bus access and generate START and STOP conditions to control the bus. The KTB8371 operates as a slave on the I²C bus. Within the bus specifications, a standard mode (100kHz maximum clock rate) and a fast mode (400kHz maximum clock rate) are defined. The KTB8371 works in both modes. Connections to the bus are made through the open-drain I/O lines SDA and SCL.

The following bus protocol has been defined in Figure 2:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is high are interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus Not Busy
Both data and clock lines remain HIGH.

Start Data Transfer
A change in the state of the data line, from HIGH to LOW, while the clock is HIGH, defines a START condition.

Stop Data Transfer
A change in the state of the data line, from LOW to HIGH, while the clock line is HIGH, defines the STOP condition.

Data Valid
The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions are not limited, and are determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth bit.

Acknowledge
Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse that is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse. Setup and hold times must also be taken into account.

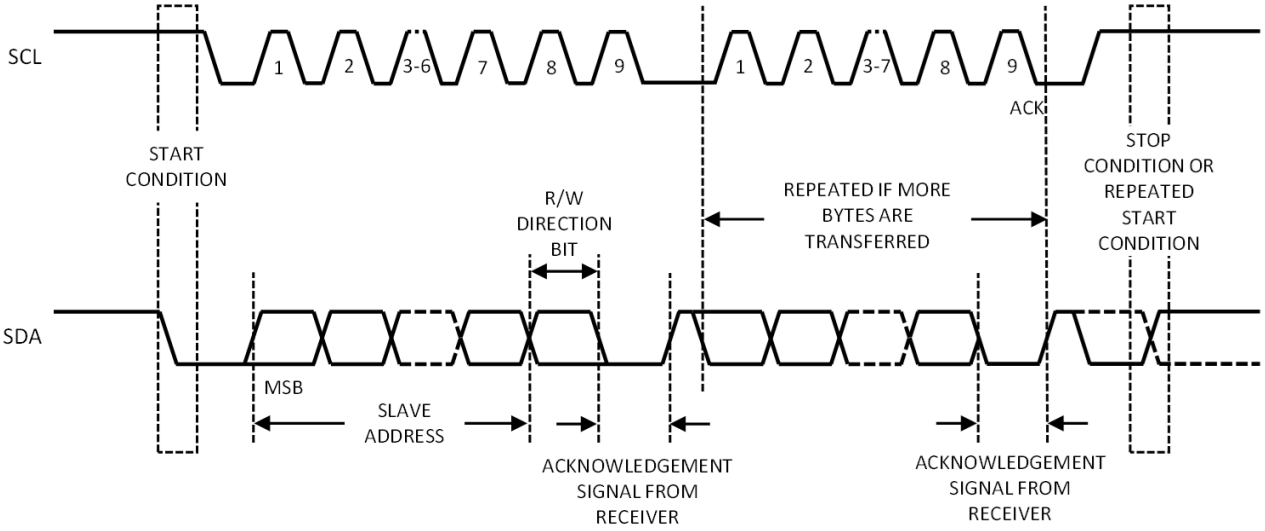


Figure 2. Data Transfer on I2C Serial Bus

The KTB8371 7-bit slave device address is 1100100 binary (0x64).

There are two kinds of I²C data transfer cycles: write cycle and read cycle.

I²C Write Cycle

For I²C write cycle, data is transferred from a master to a slave. The first byte transmitted is the 7-bit slave address plus one bit of '0' for write. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte. Data is transferred with the most significant bit (MSB) first. Figure 3 shows the sequence of the I²C write cycle.

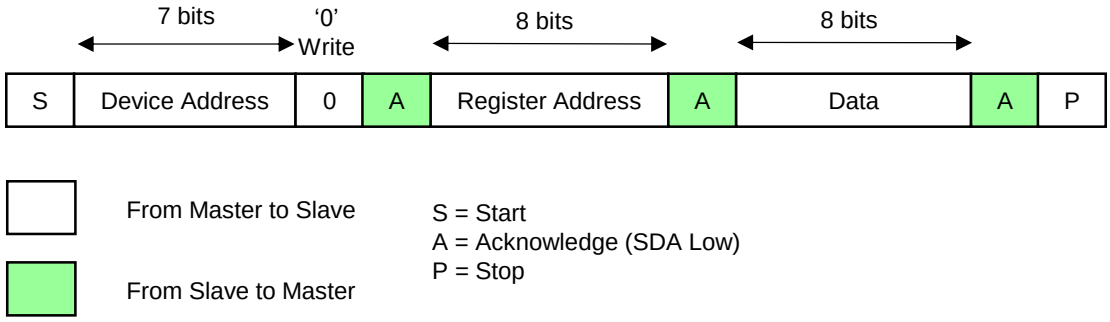


Figure 3. I²C Write Cycle

I²C Write Cycle Steps:

- Master generates start condition.
- Master sends 7-bit slave address (1100100) and 1-bit data direction ‘0’ for write.
- Slave sends acknowledge if the slave address is matched.
- Master sends 8-bit register address.
- Slave sends acknowledge.
- Master sends 8-bit data for that addressed register.
- Slave sends acknowledge.
- If master sends more data bytes, the register address will be incremented by one after each acknowledge.
- Master generate stop condition to finish the write cycle.

I²C Read Cycle

For I²C read cycle, data is transferred from a slave to a master. But to start the read cycle, master needs to write the register address first to define which register data to read. Figure 4 shows the steps of the I²C read cycle.

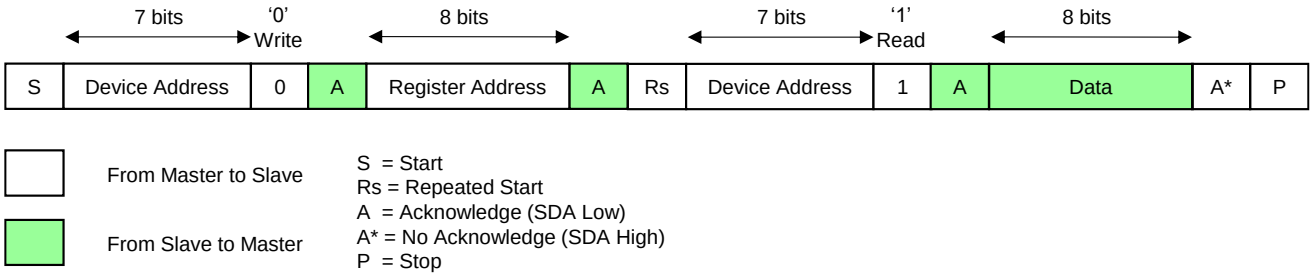


Figure 4. I²C Read Cycle

I²C Read Cycle Steps:

- Master generates start condition.
- Master sends 7-bit slave address (1100100) and 1-bit data direction ‘0’ for write.
- Slave sends acknowledge if the slave address is matched.
- Master sends 8-bit register address.
- Slave sends acknowledge.
- Master generates repeated start condition.
- Master sends 7-bit slave address (1100100) and 1-bit data direction ‘1’ for read.
- Slave sends acknowledge if the slave address is matched.
- Slave sends the data byte of that addressed register.
- If master sends acknowledge, the register address will be incremented by one after each acknowledge and the slave will continue to send the data for the updated addressed register.
- If master sends no acknowledge, the slave will stop sending the data.
- Master generate stop condition to finish the read cycle.

I²C Registers

I²C Slave Address

Options[7]	7-Bit Address	Write Address	Read Address	Bits 7 6 5 4 3 2 1 0
Default	0x64	0xC8	0xC9	1 1 0 0 1 0 0 *R/$\overline{W}$*
Alternate 1	0x65	0xCA	0xCB	1 1 0 0 1 0 1 *R/$\overline{W}$*
Alternate 2	0x66	0xCC	0xCD	1 1 0 0 1 1 0 *R/$\overline{W}$*
Alternate 3	0x67	0xCE	0xCF	1 1 0 0 1 1 1 *R/$\overline{W}$*

I²C Register Map

Hex Address	Name	Type	Access	Default Reset	B7	B6	B5	B4	B3	B2	B1	B0
0x00	VSEL	Config	R/W	0011 1010	ADDRESS[1:0]		V_{OUT}[5:0]					
0x01	CONTL0	Config	R/W	0000 0000	FSWSEL[1:0]		Reserved			FPWM	HIQ	DISCH
0x02	ID0	Status	R	1010 0010	VENDOR[2:0]			DIE_ID[4:0]				
0x03	ID1	Status	R	0000 xxxx	RSVD[3:0]				DIE_REV[3:0]			
0x04	ID2	Status	R	xxxx xxxx	FAULT	OT	Reserved			BSTLOW	PVINOK	PGOOD
0x05	CONTL1	Control	R/W	0000 0000	RSVD[5:0]						REGRST	BUCKENB

Register contents are reset in hardware to their defaults values by V_{IN} power-on reset. Additionally, most registers can be reset in software by writing 1 to the RESET bit (B7) in the CONTL1 register (0x05). Default Reset bits marked with lower-case "x" in the register map and register details tables depend upon the ordered part# suffix and die revision; please see the *Ordering Information* section. Upper-case "X" used elsewhere in the tables designates "don't care".

VSEL Configuration Register

Register Address 0x00

<table>
<tr><th>Bit</th><th>Name</th><th>Access</th><th>Default Reset</th><th>Description</th></tr>
<tr><td>7:6</td><td>ADDRESS [1:0]</td><td>R/W</td><td>00</td><td>Chip I2C Address Selection.
<table>
<tr><th>ADDRESS bits</th><th>7-Bit Address</th></tr>
<tr><td>00</td><td>0x64</td></tr>
<tr><td>01</td><td>0x65</td></tr>
<tr><td>10</td><td>0x66</td></tr>
<tr><td>11</td><td>0x67</td></tr>
</table></td></tr>
<tr><td>5:0</td><td>V_{OUT}[5:0]</td><td>R/W</td><td>101101 (KTB8371C)
110111 (KTB8371B)
110010 (KTB8371A)</td><td>Sets the nominal V_{OUT} regulation voltage.
<table>
<tr><th rowspan="2">V_{OUT} Setting</th><th rowspan="2">V_{OUT}[5:0] default</th><th colspan="2">V_{OUT} Range</th><th rowspan="2">$V_{OUT(step)}$</th></tr>
<tr><th>$V_{OUT(min)}$</th><th>$V_{OUT(max)}$</th></tr>
<tr><td>KTB8371C</td><td>101101</td><td>0.8V</td><td>2.2V</td><td>40mV</td></tr>
<tr><td>KTB8371B</td><td>110111</td><td>1.2V</td><td>3.3V</td><td>60mV</td></tr>
<tr><td>KTB8371A</td><td>110010</td><td>2.0V</td><td>5.5V</td><td>100mV</td></tr>
</table>
NOTE: to change VOUT to a particular value, refer to Table1</td></tr>
</table>

7. For Alternate 1/2/3 Slave Addresses, please contact a Kinetic Technologies representative.

CONTL0 Configuration Register

Register Address 0x01

Bit	Name	Access	Default Reset	Description
7:6	FSWSEL[1:0]	R/W	00	Switching Frequency control. 00 = 0.5MHz 01 = 1.0MHz 10 = 1.5MHz 11 = 2.0MHz
5:3	Reserved	R	00	
2	FPWM	R/W	0	Forced-PWM Mode control. 0 = Auto-Skip at light loads; PWM at heavy loads 1 = Forced-PWM at all loads
1	HIQ	R/W	0	High Quiescent Current Mode control. 0 = lowest quiescent current, but pulse-grouping in Skip Mode 1 = higher quiescent current for single-pulse PFM in Skip Mode
0	DISCH	R/W	0	Active Discharge of C_{OUT} when regulator is disabled. 0 = the buck output is high impedance(about200k) when regulator is disabled. 1 = the buck output is discharged via an internal pull-down resistor when regulator is disabled.

ID0 Data Register

Register Address 0x02

Bit	Name	Access	Default Reset	Description
7:5	VENDOR[2:0]	R	101	Vendor Identification 101 = Kinetic Technologies
4:0	DIE_ID[4:0]	R	0 0010	Die Type Identification 0 0010 = KTB8371

ID1 Status Register

Register Address 0x03

Bit	Name	Access	Default Reset	Description
7:4	RSVD[3:0]	R	0000	Reserved. Always reads back as 0000.
3:0	DIE_REV[3:0]	R	xxxx	Die Revision Identification 0000 = Rev. A

ID2 Data Register

Register Address 0x04

Bit	Name	Access	Default Reset	Description
7	FAULT	R	x	Indicate the IC at the fault status or not, 0 = normal status 1 = fault status (Any fault happens, like OT,OV,UV…listed in below. This bit will go to 1 to indicate a fault.)
6	OT	R	x	Indicate the IC at the OTP status or not, 0 = normal status 1 = OTP happens
5-3	Reserved	R	x	
2	BSTLOW	R	x	Indicate the IC at the Boost Low status or not, 0 = normal status 1 = Boost low voltage happens
1	PVINOK	R	x	Indicate the IC at the PVIN_OK status or not, 0 = normal status, VIN is OK 1 = Vin UV happens
0	POWERGOOD	R	x	Indicate the IC at the Power good status or not, 0 = normal states, out voltage is in good regulation 1 = out voltage is out of regulation

CONTL1 Configuration Register

Register Address 0x05

Bit	Name	Access	Default Reset	Description
7:2	RSVD[5:0]	R	0000 0	Reserved. Always reads back as 0000 0.
1	RESET	R/W	0	Software Reset to default register settings. 0 = No reset 1 = Resets all the user registers. The RESET bit always reads back as 0.
0	BUCKENB	R/W	0	Software Buck Enable control. 0 = buck is software enabled, external EN pin must be in high condition 1 = buck is software disabled, external EN pin must be in high condition

Applications Information

Recommended Inductors

The KTB8371 is trimmed for inductors with nominal inductance of 0.8µH~3.3µH. And inductance around 1µH provide best load transient response. Select an inductor with a saturation current rating that is higher than the KTB8371 peak current limit. Also, choose an inductor with sufficient temperature-rise current rating to satisfy the RMS load-current of the application. Consider the inductor's resistance (both DCR and ACR at 1MHz), since these will affect the efficiency. (Generally, the ACR vs. frequency characteristic is available upon request from the inductor supplier.) Larger physical case-sizes, good winding designs, and better magnetic materials can increase efficiency. Table 2 is a list of recommended inductors from leading suppliers.

Table 2. Recommended Inductors

Maker	Part #	L (typ)	DCR (typ)	I_{SAT} (min)	$I_{\Delta T+40C}$ (min)	Size (typ/typ/max)
We	744310095	0.95µH	6.2mΩ	13A	11A	7.0 x 6.9 x 3.0mm

Recommended Capacitors

Ceramic input and output capacitors with X5R or X6S or X7R are recommended due to their low ESR, low ESL, low temperature coefficients, and small physical sizes. Consider the voltage rating, size, and DC bias derating characteristic of the capacitor. Table 3 is a list of recommended capacitors from leading suppliers.

Table 3. Recommended Capacitors

Maker	Part #	C (typ)	C_{EFF}	V_{RATING}	T_{CHAR}	Size
Murata	GRM31CR61E226K	10µF	5.4µF (at 12V DC)	25V	X5R	(1206) 3.2 x 1.6mm
Murata	GRM31CR61A226K	22µF	12.8µF (at 5V DC)	10V	X5R	(1206) 3.2 x 1.6mm

Input Capacitor

Choose an input capacitor with voltage rating of 25V or more, 10µF nominal capacitance or more, and 0805 case-size or larger. Larger values and larger case-size provide more effective capacitance when considering the DC bias derating characteristic of the capacitor. If the application's input voltage is supplied through a connector or a cable, add additional bypass capacitance where V_{IN} first arrives to the PCB.

Output Capacitors

Choose output capacitors with voltage rating of 10.0V or more, 20µF total nominal capacitance or more, and 0805 case-size or larger. Consider the V_{OUT} setting of the regulator and how case size has a significant impact on DC bias derating. At high V_{OUT} settings, more total nominal capacitance is needed to achieve the same effective capacitance compared to lower V_{OUT} settings.

For the very best possible load transient response, use multiple capacitors in parallel to achieve sufficient total effective output capacitance:

$$C_{OUT_{EFFECTIVE}} \geq \frac{L \times I_{STEP}}{33m\Omega \times (V_{IN} - V_{OUT})}$$

Note: 33mΩ is a constant related to internal control circuit.

where I_{STEP} is the largest load transient step in the application. Please note that the above formula is already guard-banded by a margin of 2x to accommodate capacitor and inductor tolerances and the variability of a transient arrival time with respect to the switching cycle of the regulator.

If needed, the total effective output capacitance can be distributed by placing additional capacitors remotely at the point of load. In applications where transient performance is less critical, especially when V_{IN} minus V_{OUT} is small, it is acceptable to reduce the total effective output capacitance to save board space and cost at the expense of load transient droop and soar.

As a design example, consider a system with V_{IN} = 12V (min), V_{OUT} = 1.8V, and I_{STEP} = 5A (max):

$$C_{OUT_{EFFECTIVE}} \geq \frac{1uH \times 5A}{33m\Omega \times (12V - 1.8V)} \cong 18\mu F$$

In this example, choose output capacitors with total effective capacitance of 14µF or more at a DC bias of 1.8V. A single 15µF capacitor will not be enough when considering its DC bias characteristic, per Figure 5. At 1.8V bias, it retains only about 8µF; therefore, for best transient response, use two of these capacitors in parallel for a total effective capacitance of 16µF.

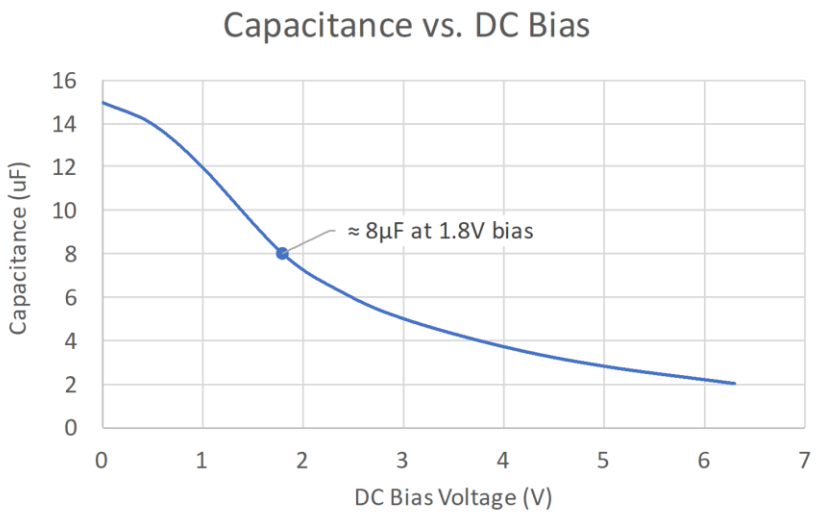


Figure 5. Typical DC Bias Derating Characteristic an Example 15µF Ceramic Capacitor.

Recommended PCB Layout

Refer to Figure 6 for example PCB layouts optimized for small footprint, low EMI, and good performance. The example follow the below PCB layout recommendations:

1. Connect the input capacitor C_{IN} as close as possible to the VIN and PGND pins using top-side thick metal traces.
2. Connect the ground terminals of output capacitors C_{OUT} as close as possible to the ground terminal of C_{IN} and the PGND pins using top-side metal.
3. Connect the Boost capacitor as close as possible to the Boost pin and Lx pin of the chip.
4. Connect the local top-side PGND island to the PCB ground plane using multiple parallel vias.
5. Do not connect the AGND pins directly to the top-side PGND. Instead, connect the AGND pins to the PCB ground plane using their own vias.
6. Connect the inductor to the LX pins with a wide trace.
7. Connect the V_{OUT} terminals of the inductor to the output capacitors with a wide and short trace.
8. Route the V_{OUT} sense trace from C_{OUT} to the VOUT pin with care to keep it away from noisy traces, especially the LX trace. Additionally, use ground fill to shield noise from coupling into the V_{OUT} sense.
9. Depending upon PCB design rules, it may be possible to place filled micro-vias directly under WLCSP bumps. If not, route short traces to nearby vias.

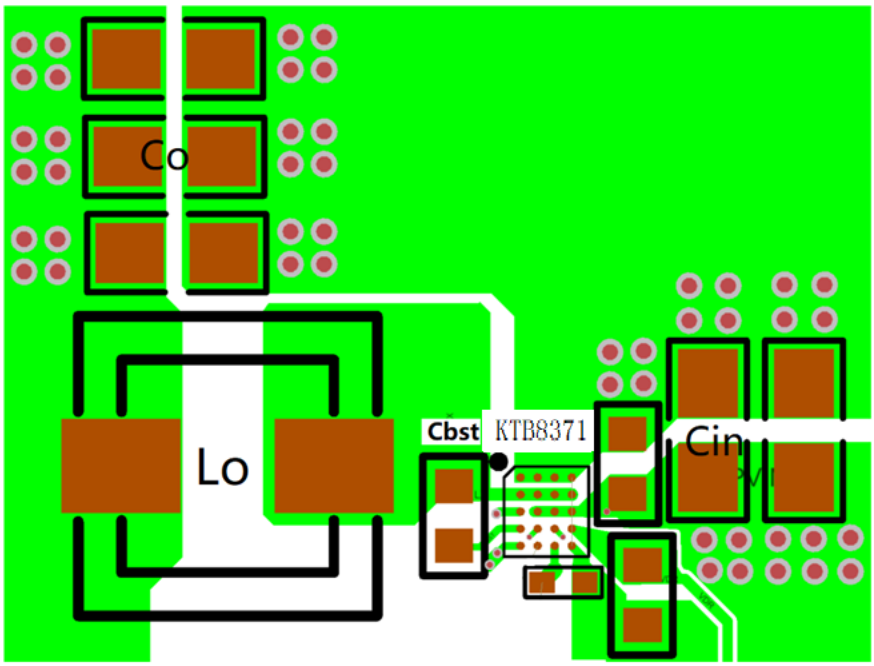
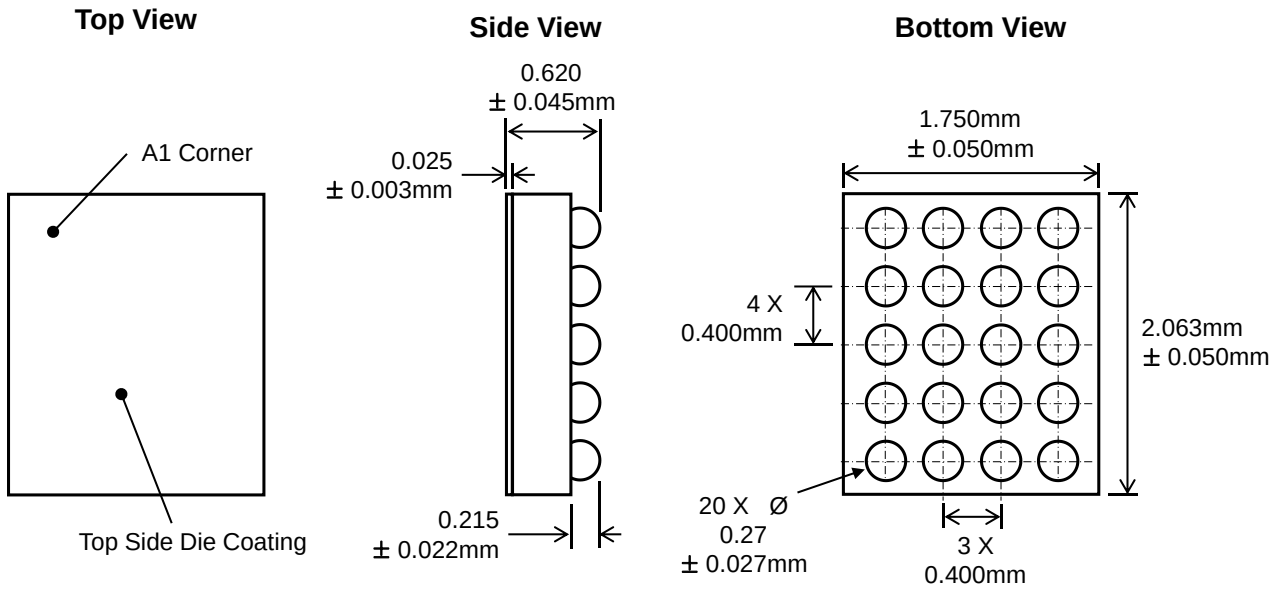


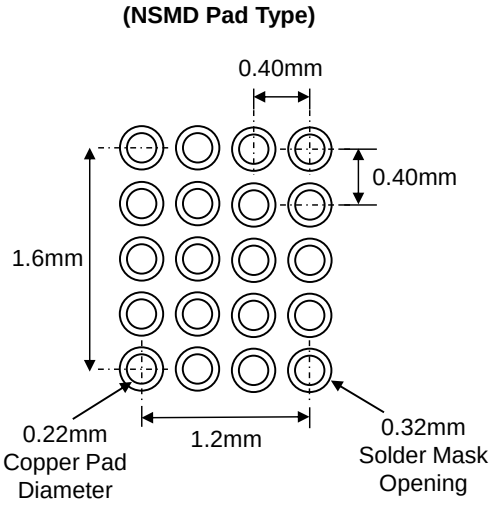
Figure 6. Recommended PCB Layouts

Packaging Information

WLCSP45-20 (1.750mm x 2.063mm x 0.62mm)



Recommended Footprint



* Dimensions are in millimeters.

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