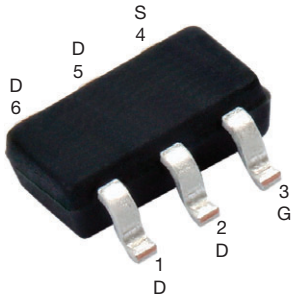
# P-Channel 20 V (D-S) MOSFET

**SC-70 (6 leads)**
**SOT-363 Single**




Top View

**Marking Code**: AN

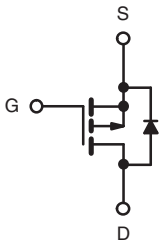
## FEATURES

- TrenchFET® power MOSFET
- 100 % $R_g$ tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Pb-free
RoHS COMPLIANT
HALOGEN FREE Available

## APPLICATIONS

- Load switch for portable devices




P-Channel MOSFET

| PRODUCT SUMMARY | |
|---|---|
| $V_{DS}$ (V) | -20 |
| $R_{DS(on)}$ max. (Ω) at $V_{GS}$ = -1.8 V | 0.150 |
| $R_{DS(on)}$ max. (Ω) at $V_{GS}$ = -2.5 V | 0.115 |
| $R_{DS(on)}$ max. (Ω) at $V_{GS}$ = -4.5 V | 0.090 |
| $Q_g$ typ. (nC) | 9.0 |
| $I_D$ (A) [a] | -2.7 |
| Configuration | Single |

| ORDERING INFORMATION | |
|---|---|
| Package | SOT-363 |
| Lead (Pb)-free | Si1467DH-T1-E3 |
| Lead (Pb)-free and halogen-free | Si1467DH-T1-GE3 |

**ABSOLUTE MAXIMUM RATINGS** ($T_A$ = 25 °C, unless otherwise noted)

| PARAMETER | | SYMBOL | LIMIT | UNIT |
|---|---|---|---|---|
| Drain-source voltage | | $V_{DS}$ | -20 | V |
| Gate-source voltage | | $V_{GS}$ | ± 8 | |
| Continuous drain current ($T_J$ = 150 °C) [a, b] | $T_C$ = 25 °C | $I_D$ | -2.7[c] | A |
| | $T_C$ = 70 °C | | -2.7[c] | |
| | $T_A$ = 25 °C | | -3.0[a, b] | |
| | $T_A$ = 70 °C | | -2.4[a, b] | |
| Pulsed drain current (10 µs pulse width) | | $I_{DM}$ | -8 | |
| Continuous source-drain diode current [a, b] | $T_C$ = 25 °C | $I_S$ | -2.3 | |
| | $T_A$ = 25 °C | | -1.25[a, b, c] | |
| Maximum power dissipation [a, b] | $T_C$ = 25 °C | $P_D$ | 2.78 | W |
| | $T_C$ = 70 °C | | 1.78 | |
| | $T_A$ = 25 °C | | 1.5[a, b] | |
| | $T_A$ = 70 °C | | 1[a, b] | |
| Operating junction and storage temperature range | | $T_J$, $T_{stg}$ | -55 to +150 | °C |
| Soldering recommendations (peak temperature) [c, d] | | | 260 | |

**THERMAL RESISTANCE RATINGS**

| PARAMETER | | SYMBOL | TYPICAL | MAXIMUM | UNIT |
|---|---|---|---|---|---|
| Maximum junction-to-ambient [a, d] | t ≤ 5 s | $R_{thJA}$ | 60 | 80 | °C/W |
| Maximum junction-to-foot (drain) | Steady state | $R_{thJF}$ | 34 | 45 | |

**Notes**
a. Surface mounted on 1" x 1" FR4 board
b. t = 5 s
c. Package limited
d. Maximum under steady state conditions is 125 °C/W


For technical questions, contact: pmostechsupport@vishay.com
THIS DOCUMENT IS SUBJECT TO CHANGE WITHOUT NOTICE. THE PRODUCTS DESCRIBED HEREIN AND THIS DOCUMENT ARE SUBJECT TO SPECIFIC DISCLAIMERS, SET FORTH AT www.vishay.com/doc?91000

| **SPECIFICATIONS** ($T_J$ = 25 °C, unless otherwise noted) | | | | | | |
|---|---|---|---|---|---|---|
| **PARAMETER** | **SYMBOL** | **TEST CONDITIONS** | **MIN.** | **TYP.** | **MAX.** | **UNIT** |
| **Static** | | | | | | |
| Drain-source breakdown voltage | $V_{DS}$ | $V_{GS}$ = 0 V, $I_D$ = -250 µA | -20 | - | - | V |
| $V_{DS}$ temperature coefficient | $\Delta V_{DS}/T_J$ | $I_D$ = -250 µA | - | -20 | - | mV/°C |
| $V_{GS(th)}$ temperature coefficient | $\Delta V_{GS(th)}/T_J$ | | - | -2.5 | - | |
| Gate-source threshold voltage | $V_{GS(th)}$ | $V_{DS}$ = $V_{GS}$, $I_D$ = -250 µA | -0.4 | - | -1.0 | V |
| Gate-source leakage | $I_{GSS}$ | $V_{DS}$ = 0 V, $V_{GS}$ = ± 8 V | - | - | -100 | nA |
| Zero gate voltage drain current | $I_{DSS}$ | $V_{DS}$ = -20 V, $V_{GS}$ = 0 V | - | - | -1 | µA |
| | | $V_{DS}$ = -20 V, $V_{GS}$ = 0 V, $T_J$ = 55 °C | - | - | -10 | |
| On-state drain current[a] | $I_{D(on)}$ | $V_{DS} \leq$ 5 V, $V_{GS}$ = -4.5 V | -3 | - | - | A |
| Drain-source on-state resistance [a] | $R_{DS(on)}$ | $V_{GS}$ = -4.5 V, $I_D$ = -2.0 A | - | 0.073 | 0.090 | Ω |
| | | $V_{GS}$ = -2.5 V, $I_D$ = -1.8 A | - | 0.090 | 0.115 | |
| | | $V_{GS}$ = -1.8 V, $I_D$ = -1.5 A | - | 0.115 | 0.150 | |
| Forward transconductance [a] | $g_{fs}$ | $V_{DS}$ = -10 V, $I_D$ = -2.0 A | - | 7 | - | S |
| **Dynamic [b]** | | | | | | |
| Input capacitance | $C_{iss}$ | $V_{DS}$ = -10 V, $V_{GS}$ = 0 V, f = 1 MHz | - | 561 | - | pF |
| Output capacitance | $C_{oss}$ | | - | 112 | - | |
| Reverse transfer capacitance | $C_{rss}$ | | - | 89 | - | |
| Total gate charge | $Q_g$ | $V_{DS}$ = -10 V, $V_{GS}$ = -4.5 V, $I_D$ = -2.5 A | - | 9 | 13.5 | nC |
| Gate-source charge | $Q_{gs}$ | | - | 1.0 | - | |
| Gate-drain charge | $Q_{gd}$ | | - | 2.5 | - | |
| Gate resistance | $R_g$ | f = 1 MHz | 2.0 | 10 | 20 | Ω |
| Turn-on delay time | $t_{d(on)}$ | $V_{DD}$ = -10 V, $R_L$ = 5 Ω<br>$I_D \cong$ -2 A, $V_{GEN}$ = -4.5 V, $R_g$ = 1 Ω | - | 16 | 30 | ns |
| Rise time | $t_r$ | | - | 43 | 75 | |
| Turn-off delay time | $t_{d(off)}$ | | - | 36 | 70 | |
| Fall time | $t_f$ | | - | 18 | 35 | |
| Turn-on delay time | $t_{d(on)}$ | $V_{DD}$ = -10 V, $R_L$ = 5 Ω<br>$I_D \cong$ -2 A, $V_{GEN}$ = -8 V, $R_g$ = 1 Ω | - | 7 | 14 | |
| Rise time | $t_r$ | | - | 10 | 20 | |
| Turn-off delay time | $t_{d(off)}$ | | - | 33 | 50 | |
| Fall time | $t_f$ | | - | 10 | 20 | |
| **Drain-source body diode characteristics** | | | | | | |
| Continuous source-drain diode current | $I_S$ | $T_C$ = 25 °C | - | - | -1.6 | A |
| Pulse diode forward current | $I_{SM}$ | | - | - | -6.5 | |
| Body diode voltage | $V_{SD}$ | $I_S$ = -2 A, $V_{GS}$ = 0 V | - | -0.78 | -1.2 | V |
| Body diode reverse recovery time | $t_{rr}$ | $I_F$ = -2.0 A, dI/dt = 100 A/µs, TJ = 25 °C | - | 21 | 35 | ns |
| Body diode reverse recovery charge | $Q_{rr}$ | | - | 15 | 25 | nC |
| Reverse recovery fall time | $t_a$ | | - | 9 | - | ns |
| Reverse recovery rise time | $t_b$ | | - | 12 | - | |

**Notes**

a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %

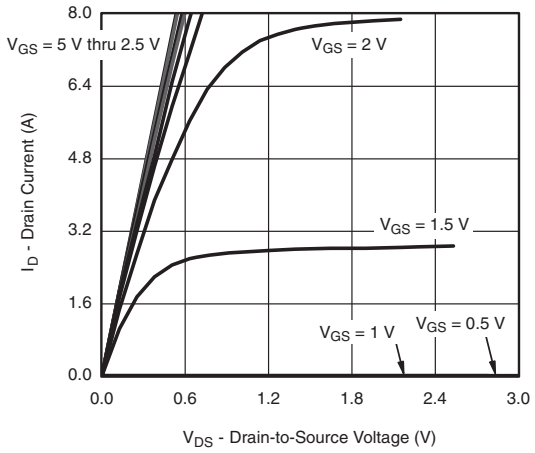
b. Guaranteed by design, not subject to production testing

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

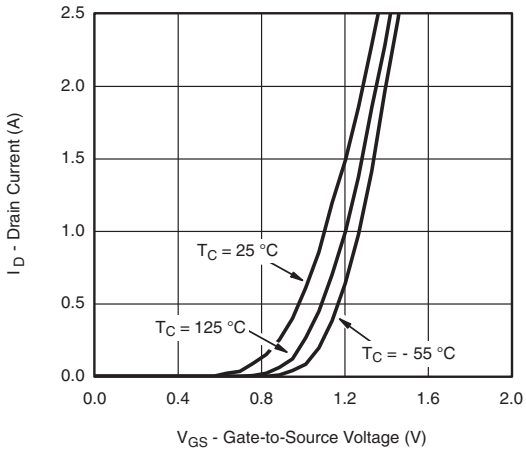


For technical questions, contact: pmostechsupport@vishay.com
THIS DOCUMENT IS SUBJECT TO CHANGE WITHOUT NOTICE. THE PRODUCTS DESCRIBED HEREIN AND THIS DOCUMENT ARE SUBJECT TO SPECIFIC DISCLAIMERS, SET FORTH AT www.vishay.com/doc?91000

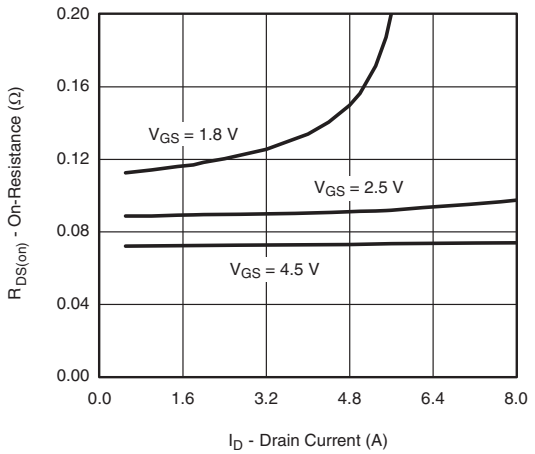
## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



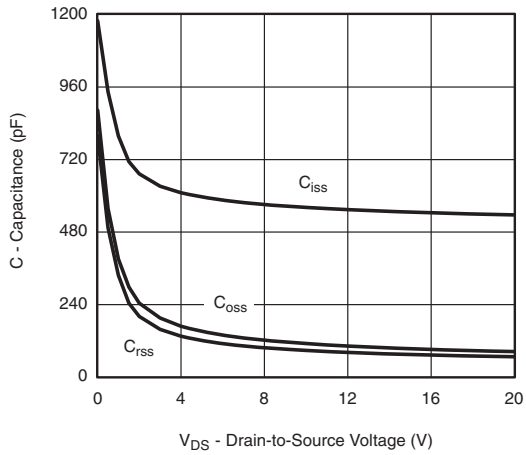

**Output Characteristics**



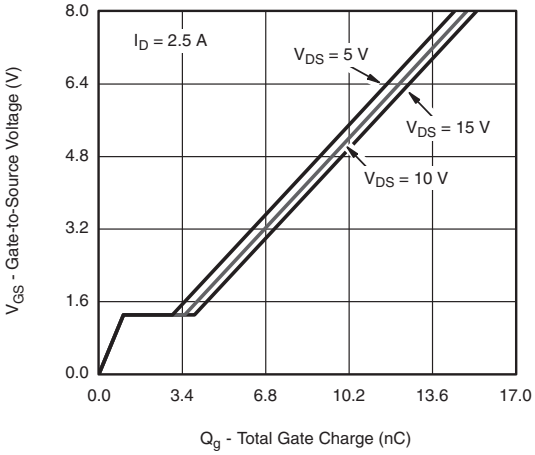

**Transfer Characteristics**



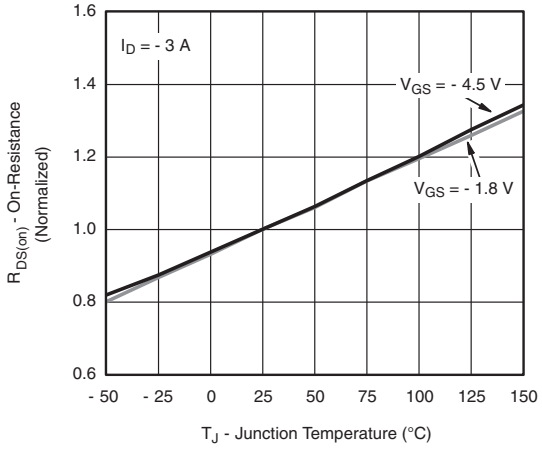

**On-Resistance vs. Drain Current and Gate Voltage**




**Capacitance**



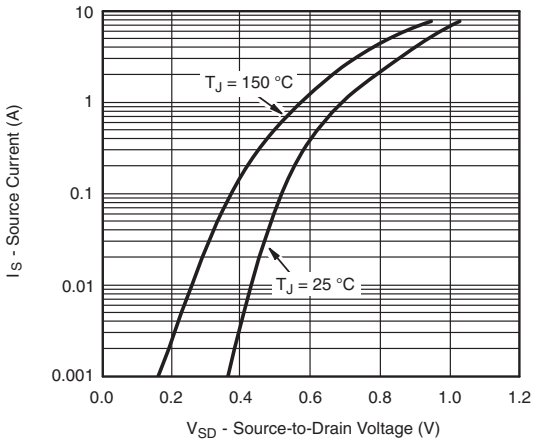

**Gate Charge**



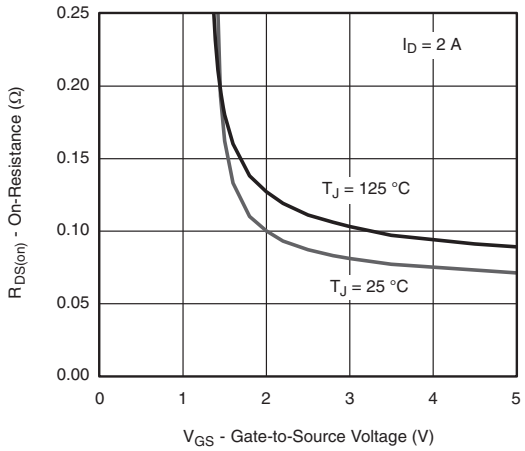

**On-Resistance vs. Junction Temperature**


For technical questions, contact: pmostechsupport@vishay.com
THIS DOCUMENT IS SUBJECT TO CHANGE WITHOUT NOTICE. THE PRODUCTS DESCRIBED HEREIN AND THIS DOCUMENT ARE SUBJECT TO SPECIFIC DISCLAIMERS, SET FORTH AT www.vishay.com/doc?91000

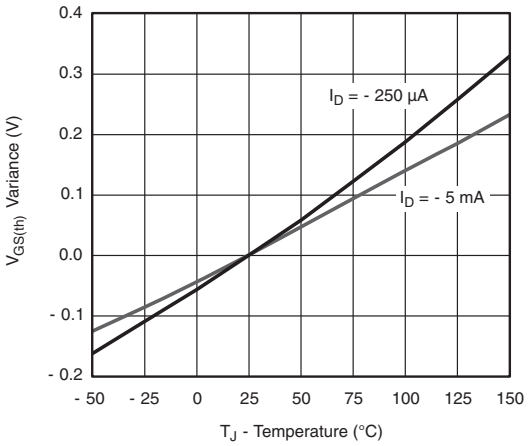
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



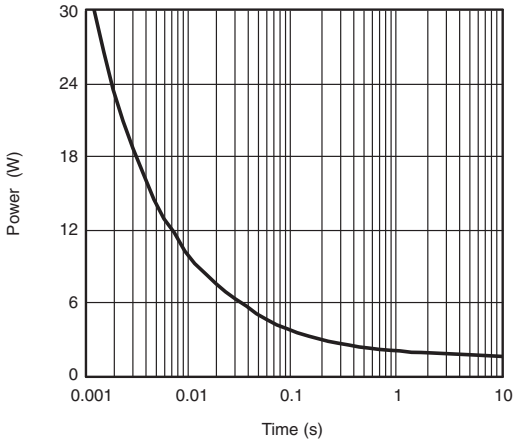

**Source-Drain Diode Forward Voltage**



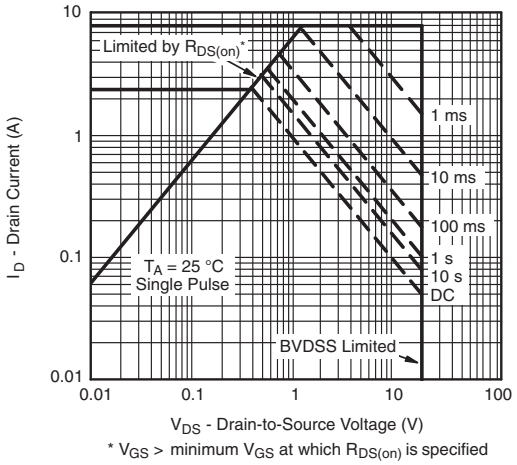

**On-Resistance vs. Gate-to-Source Voltage**




**Threshold Voltage**




**Single Pulse Power, Junction-to-Ambient**

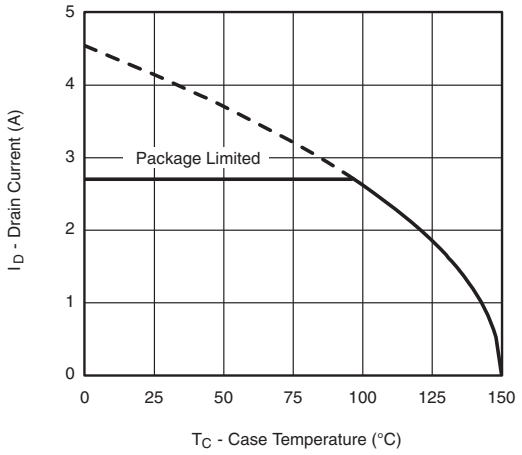



* $V_{GS}$ > minimum $V_{GS}$ at which $R_{DS(on)}$ is specified

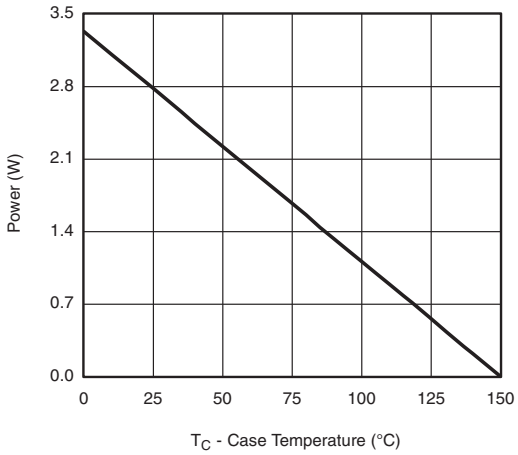
**Safe Operating Area, Junction-to-Ambient**


For technical questions, contact: pmostechsupport@vishay.com
THIS DOCUMENT IS SUBJECT TO CHANGE WITHOUT NOTICE. THE PRODUCTS DESCRIBED HEREIN AND THIS DOCUMENT ARE SUBJECT TO SPECIFIC DISCLAIMERS, SET FORTH AT www.vishay.com/doc?91000

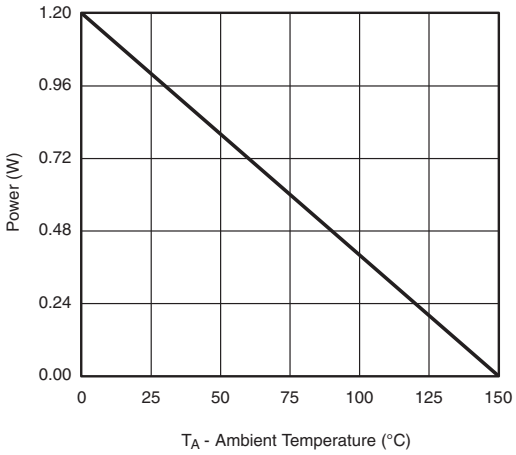
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)




**Current Derating** [a]




**Power Derating, Junction-to-Foot**



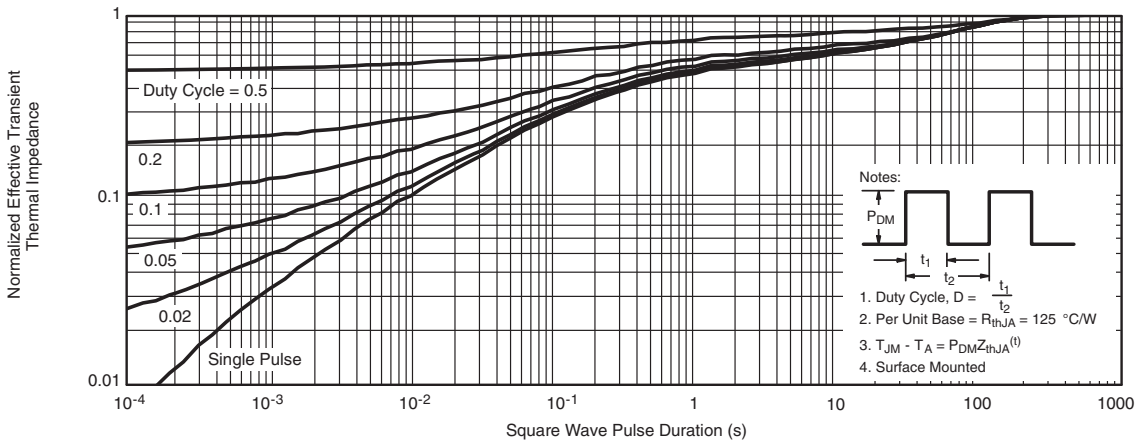

**Power Derating, Junction-to-Ambient**

**Note**

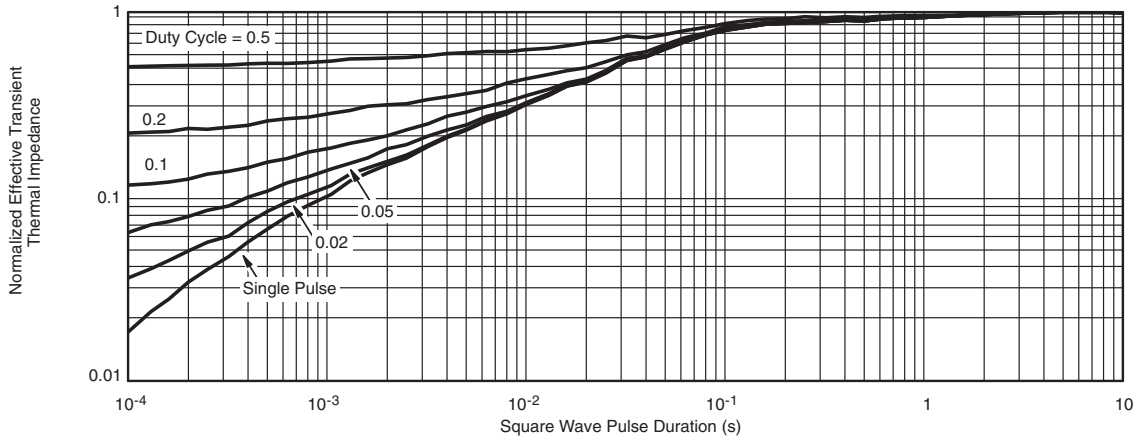
a. The power dissipation $P_D$ is based on $T_{J(max)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit


For technical questions, contact: pmostechsupport@vishay.com
THIS DOCUMENT IS SUBJECT TO CHANGE WITHOUT NOTICE. THE PRODUCTS DESCRIBED HEREIN AND THIS DOCUMENT ARE SUBJECT TO SPECIFIC DISCLAIMERS, SET FORTH AT www.vishay.com/doc?91000

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)




**Normalized Thermal Transient Impedance, Junction-to-Ambient**

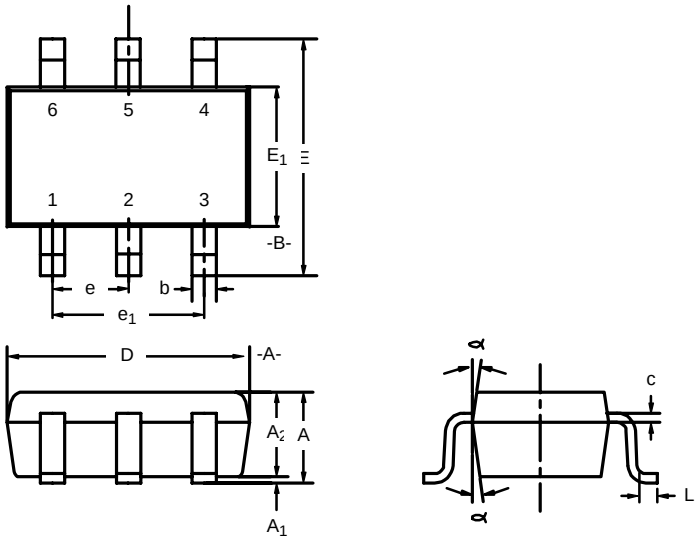



**Normalized Thermal Transient Impedance, Junction-to-Foot**

*Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?68663.*


For technical questions, contact: pmostechsupport@vishay.com
THIS DOCUMENT IS SUBJECT TO CHANGE WITHOUT NOTICE. THE PRODUCTS DESCRIBED HEREIN AND THIS DOCUMENT ARE SUBJECT TO SPECIFIC DISCLAIMERS, SET FORTH AT www.vishay.com/doc?91000

## SC-70: 6-LEADS




| Dim | MILLIMETERS | | | INCHES | | |
|---|---|---|---|---|---|---|
| | Min | Nom | Max | Min | Nom | Max |
| **A** | 0.90 | – | 1.10 | 0.035 | – | 0.043 |
| **$A_1$** | – | – | 0.10 | – | – | 0.004 |
| **$A_2$** | 0.80 | – | 1.00 | 0.031 | – | 0.039 |
| **b** | 0.15 | – | 0.30 | 0.006 | – | 0.012 |
| **c** | 0.10 | – | 0.25 | 0.004 | – | 0.010 |
| **D** | 1.80 | 2.00 | 2.20 | 0.071 | 0.079 | 0.087 |
| **E** | 1.80 | 2.10 | 2.40 | 0.071 | 0.083 | 0.094 |
| **$E_1$** | 1.15 | 1.25 | 1.35 | 0.045 | 0.049 | 0.053 |
| **e** | 0.65BSC | | | 0.026BSC | | |
| **$e_1$** | 1.20 | 1.30 | 1.40 | 0.047 | 0.051 | 0.055 |
| **L** | 0.10 | 0.20 | 0.30 | 0.004 | 0.008 | 0.012 |
| **α** | 7°Nom | | | 7°Nom | | |

ECN: S-03946—Rev. B, 09-Jul-01
DWG: 5550

# Single-Channel LITTLE FOOT® SC-70 6-Pin MOSFET Copper Leadframe Version Recommended Pad Pattern and Thermal Performance

## INTRODUCTION

The new single 6-pin SC-70 package with a copper leadframe enables improved on-resistance values and enhanced thermal performance as compared to the existing 3-pin and 6-pin packages with Alloy 42 leadframes. These devices are intended for small to medium load applications where a miniaturized package is required. Devices in this package come in a range of on-resistance values, in n-channel and p-channel versions. This technical note discusses pin-outs, package outlines, pad patterns, evaluation board layout, and thermal performance for the single-channel version.

## BASIC PAD PATTERNS

See Application Note 826, *Recommended Minimum Pad Patterns With Outline Drawing Access for Vishay Siliconix MOSFETs*, (http://www.vishay.com/doc?72286) for the basic pad layout and dimensions. These pad patterns are sufficient for the low to medium power applications for which this package is intended. Increasing the drain pad pattern yields a reduction in thermal resistance and is a preferred footprint. The availability of four drain leads rather than the traditional single drain lead allows a better thermal path from the package to the PCB and external environment.

## PIN-OUT

Figure 1 shows the pin-out description and Pin 1 identification.The pin-out of this device allows the use of four pins as drain leads, which helps to reduce on-resistance and junction-to-ambient thermal resistance.

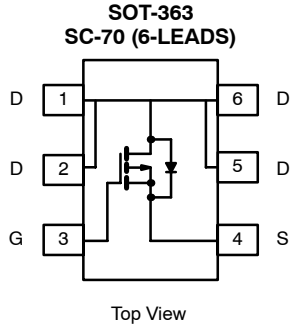



**FIGURE 1.**

For package dimensions see outline drawing SC-70 (6-Leads) (http://www.vishay.com/doc?71154)

## EVALUATION BOARDS — SINGLE SC70-6

The evaluation board (EVB) measures 0.6 inches by 0.5 inches. The copper pad traces are the same as in Figure 2. The board allows examination from the outer pins to 6-pin DIP connections, permitting test sockets to be used in evaluation testing. See Figure 3.

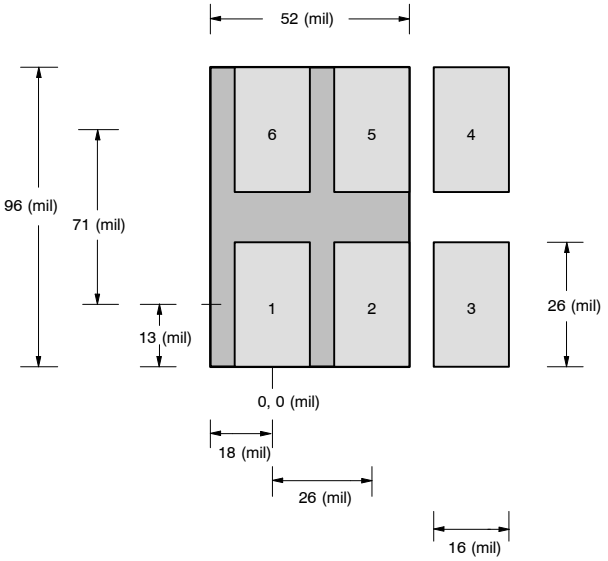



**FIGURE 2.** SC-70 (6 leads) Single

The thermal performance of the single 6-pin SC-70 has been measured on the EVB, comparing both the copper and Alloy 42 leadframes. This test was first conducted on the traditional Alloy 42 leadframe and was then repeated using the 1-inch$^2$ PCB with dual-side copper coating.

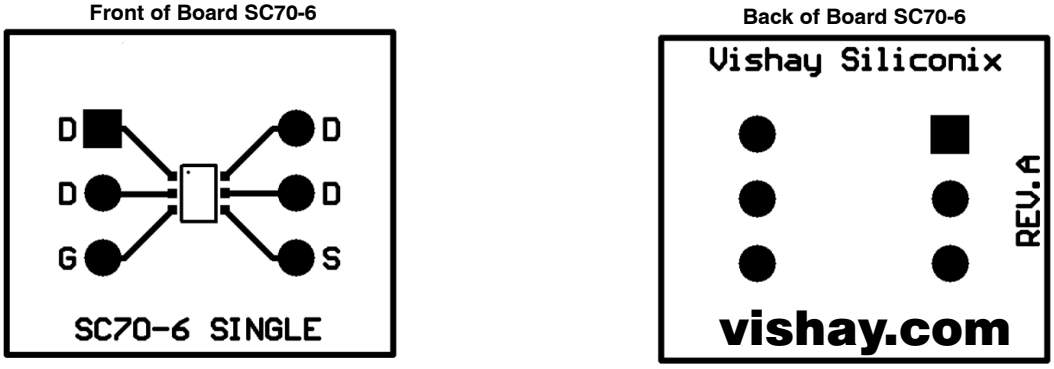



FIGURE 3.

## THERMAL PERFORMANCE

### Junction-to-Foot Thermal Resistance (Package Performance)

The junction to foot thermal resistance is a useful method of comparing different packages thermal performance.

A helpful way of presenting the thermal performance of the 6-Pin SC-70 copper leadframe device is to compare it to the traditional Alloy 42 version.

Thermal performance for the 6-pin SC-70 measured as junction-to-foot thermal resistance, where the “foot” is the drain lead of the device at the bottom where it meets the PCB. The junction-to-foot thermal resistance is typically 40°C/W in the copper leadframe and 163°C/W in the Alloy 42 leadframe — a four-fold improvement. This improved performance is obtained by the enhanced thermal conductivity of copper over Alloy 42.

### Power Dissipation

The typical $R\theta_{JA}$ for the single 6-pin SC-70 with copper leadframe is 103°C/W steady-state, compared with 212°C/W for the Alloy 42 version. The figures are based on the 1-inch$^2$ FR4 test board. The following example shows how the thermal resistance impacts power dissipation for the two different leadframes at varying ambient temperatures.

| ALLOY 42 LEADFRAME | |
|---|---|
| **Room Ambient 25 °C** | **Elevated Ambient 60 °C** |
| $P_D = \frac{T_{J(max)} - T_A}{R\theta_{JA}}$<br>$P_D = \frac{150°C - 25°C}{212°C/W}$<br>$P_D = 590$ mW | $P_D = \frac{T_{J(max)} - T_A}{R\theta_{JA}}$<br>$P_D = \frac{150°C - 25°C}{212°C/W}$<br>$P_D = 425$ mW |

| COOPER LEADFRAME | |
|---|---|
| **Room Ambient 25 °C** | **Elevated Ambient 60 °C** |
| $P_D = \frac{T_{J(max)} - T_A}{R\theta_{JA}}$<br>$P_D = \frac{150°C - 25°C}{124°C/W}$<br>$P_D = 1.01$ W | $P_D = \frac{T_{J(max)} - T_A}{R\theta_{JA}}$<br>$P_D = \frac{150°C - 60°C}{124°C/W}$<br>$P_D = 726$ mW |

As can be seen from the calculations above, the compact 6-pin SC-70 copper leadframe LITTLE FOOT power MOSFET can handle up to 1 W under the stated conditions.

### Testing

To further aid comparison of copper and Alloy 42 leadframes, Figure 5 illustrates single-channel 6-pin SC-70 thermal performance on two different board sizes and two different pad patterns. The measured steady-state values of $R\theta_{JA}$ for the two leadframes are as follows:

| LITTLE FOOT 6-PIN SC-70 | | |
|---|---|---|
| | **Alloy 42** | **Copper** |
| 1) Minimum recommended pad pattern on the EVB board V (see Figure 3. | 329.7°C/W | 208.5°C/W |
| 2) Industry standard 1-inch$^2$ PCB with maximum copper both sides. | 211.8°C/W | 103.5°C/W |

The results indicate that designers can reduce thermal resistance ($R\theta_{JA}$) by 36% simply by using the copper leadframe device rather than the Alloy 42 version. In this example, a 121°C/W reduction was achieved without an increase in board area. If increasing in board size is feasible, a further 105°C/W reduction could be obtained by utilizing a 1-inch$^2$ square PCB area.

The copper leadframe versions have the following suffix:

| | |
|---|---|
| Single: | Si14xxEDH |
| Dual: | Si19xxEDH |
| Complementary: | Si15xxEDH |

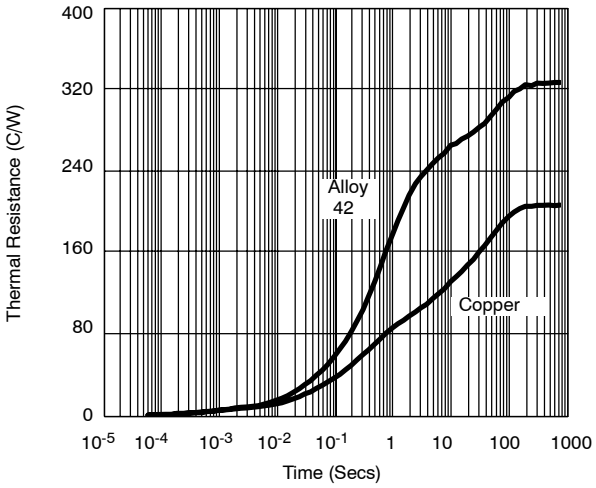



**FIGURE 4.** Leadframe Comparison on EVB

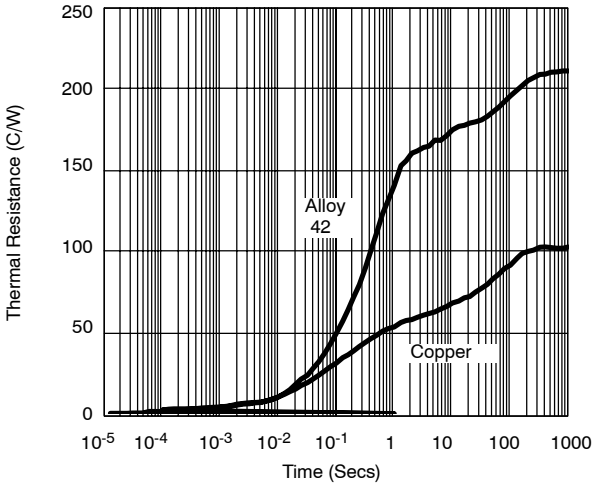
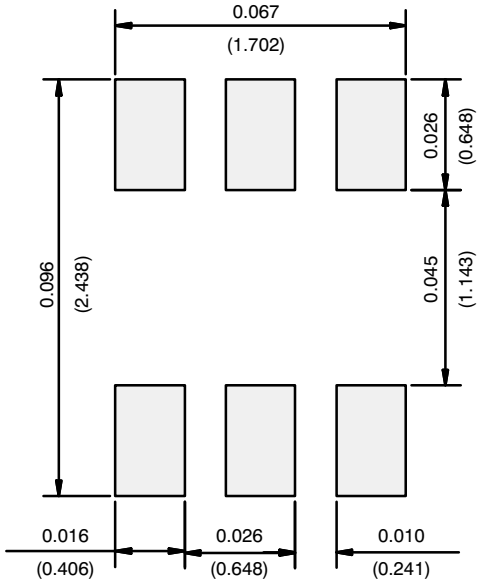



**FIGURE 5.** Leadframe Comparison on Alloy 42 1-inch$^2$ PCB

## RECOMMENDED MINIMUM PADS FOR SC-70: 6-Lead




Recommended Minimum Pads
Dimensions in Inches/(mm)

Return to Index

# Disclaimer

ALL PRODUCT, PRODUCT SPECIFICATIONS AND DATA ARE SUBJECT TO CHANGE WITHOUT NOTICE TO IMPROVE RELIABILITY, FUNCTION OR DESIGN OR OTHERWISE.

Vishay Intertechnology, Inc., its affiliates, agents, and employees, and all persons acting on its or their behalf (collectively, “Vishay”), disclaim any and all liability for any errors, inaccuracies or incompleteness contained in any datasheet or in any other disclosure relating to any product.

Vishay makes no warranty, representation or guarantee regarding the suitability of the products for any particular purpose or the continuing production of any product. To the maximum extent permitted by applicable law, Vishay disclaims (i) any and all liability arising out of the application or use of any product, (ii) any and all liability, including without limitation special, consequential or incidental damages, and (iii) any and all implied warranties, including warranties of fitness for particular purpose, non-infringement and merchantability.

Statements regarding the suitability of products for certain types of applications are based on Vishay's knowledge of typical requirements that are often placed on Vishay products in generic applications. Such statements are not binding statements about the suitability of products for a particular application. It is the customer's responsibility to validate that a particular product with the properties described in the product specification is suitable for use in a particular application. Parameters provided in datasheets and / or specifications may vary in different applications and performance may vary over time. All operating parameters, including typical parameters, must be validated for each customer application by the customer's technical experts. Product specifications do not expand or otherwise modify Vishay's terms and conditions of purchase, including but not limited to the warranty expressed therein.

Hyperlinks included in this datasheet may direct users to third-party websites. These links are provided as a convenience and for informational purposes only. Inclusion of these hyperlinks does not constitute an endorsement or an approval by Vishay of any of the products, services or opinions of the corporation, organization or individual associated with the third-party website. Vishay disclaims any and all liability and bears no responsibility for the accuracy, legality or content of the third-party website or for that of subsequent links.

Except as expressly indicated in writing, Vishay products are not designed for use in medical, life-saving, or life-sustaining applications or for any other application in which the failure of the Vishay product could result in personal injury or death. Customers using or selling Vishay products not expressly indicated for use in such applications do so at their own risk. Please contact authorized Vishay personnel to obtain written terms and conditions regarding products designed for such applications.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document or by any conduct of Vishay. Product names and markings noted herein may be trademarks of their respective owners.

*© 2024 VISHAY INTERTECHNOLOGY, INC. ALL RIGHTS RESERVED*