Automotive N-Channel 40 V (D-S) 175 °C MOSFET

PRODUCT SUMMARY	
V_{DS} (V)	40
$R_{DS(on)}$ (Ω) at V_{GS} = 10 V	0.0017
$R_{DS(on)}$ (Ω) at V_{GS} = 4.5 V	0.0020
I_D (A)	200
Configuration	Single
Package	TO-263-7L

FEATURES

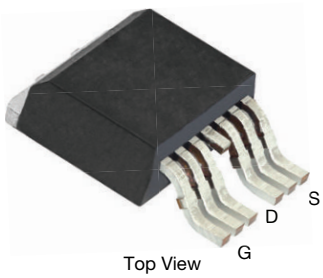
- TrenchFET® power MOSFET
- Package with low thermal resistance
- 100 % R_g and UIS tested
- AEC-Q101 qualified [d]
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

AUTOMOTIVE GRADE

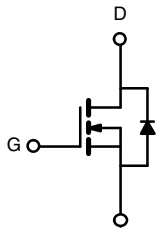
RoHS COMPLIANT

HALOGEN FREE

TO-263 7-Lead



Top View



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)				
PARAMETER		**SYMBOL**	**LIMIT**	**UNIT**
Drain-Source Voltage		V_{DS}	40	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current	T_C = 25 °C [a]	I_D	200	A
	T_C = 125 °C		193	
Continuous Source Current (Diode Conduction) [a]		I_S	200	
Pulsed Drain Current [b]		I_{DM}	600	
Single Pulse Avalanche Current	L = 0.1 mH	I_{AS}	95	
Single Pulse Avalanche Energy		E_{AS}	451	mJ
Maximum Power Dissipation [b]	T_C = 25 °C	P_D	375	W
	T_C = 125 °C		125	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to +175	°C

THERMAL RESISTANCE RATINGS				
PARAMETER		**SYMBOL**	**LIMIT**	**UNIT**
Junction-to-Ambient	PCB Mount [c]	R_{thJA}	40	°C/W
Junction-to-Case (Drain)		R_{thJC}	0.4	

Notes

a. Package limited.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
c. When mounted on 1" square PCB (FR4 material).
d. Parametric verification ongoing.

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SPECIFICATIONS (T_C = 25 °C, unless otherwise noted)							
PARAMETER	**SYMBOL**	**TEST CONDITIONS**		**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static							
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA		40	-	-	V
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		1.5	2.0	2.5	
Gate-Source Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V	V_{DS} = 40 V	-	-	1	µA
		V_{GS} = 0 V	V_{DS} = 40 V, T_J = 125 °C	-	-	50	
		V_{GS} = 0 V	V_{DS} = 40 V, T_J = 175 °C	-	-	250	
On-State Drain Current [a]	$I_{D(on)}$	V_{GS} = 10 V	V_{DS} ≥ 5 V	200	-	-	A
Drain-Source On-State Resistance [a]	$R_{DS(on)}$	V_{GS} = 10 V	I_D = 30 A	-	0.0012	0.0017	Ω
		V_{GS} = 10 V	I_D = 30 A, T_J = 125 °C	-	-	0.0028	
		V_{GS} = 10 V	I_D = 30 A, T_J = 175 °C	-	-	0.0034	
		V_{GS} = 4.5 V	I_D = 20 A	-	0.0014	0.0020	
Forward Transconductance [b]	g_{fs}	V_{DS} = 15 V, I_D = 30 A		-	181	-	S
Dynamic [b]							
Input Capacitance	C_{iss}	V_{GS} = 0 V	V_{DS} = 20 V, f = 1 MHz	-	8934	11 168	pF
Output Capacitance	C_{oss}			-	1592	1990	
Reverse Transfer Capacitance	C_{rss}			-	928	1160	
Total Gate Charge [c]	Q_g	V_{GS} = 10 V	V_{DS} = 20 V, I_D = 20 A	-	194	291	nC
Gate-Source Charge [c]	Q_{gs}			-	25	-	
Gate-Drain Charge [c]	Q_{gd}			-	40	-	
Gate Resistance	R_g	f = 1 MHz		0.25	0.8	1.8	Ω
Turn-On Delay Time [c]	$t_{d(on)}$	V_{DD} = 20 V, R_L = 1 Ω I_D ≅ 20 A, V_{GEN} = 10 V, R_g = 1 Ω		-	22	33	ns
Rise Time [c]	t_r			-	17	26	
Turn-Off Delay Time [c]	$t_{d(off)}$			-	70	105	
Fall Time [c]	t_f			-	16	24	
Source-Drain Diode Ratings and Characteristics [b]							
Pulsed Current [a]	I_{SM}			-	-	600	A
Forward Voltage	V_{SD}	I_F = 60 A, V_{GS} = 0 V		-	0.8	1.5	V

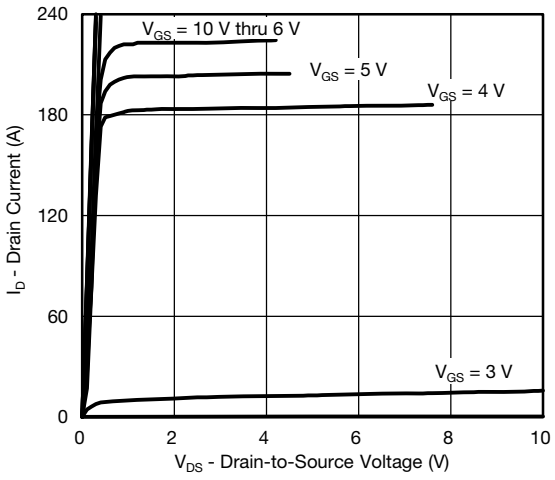
Notes

a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.
c. Independent of operating temperature.

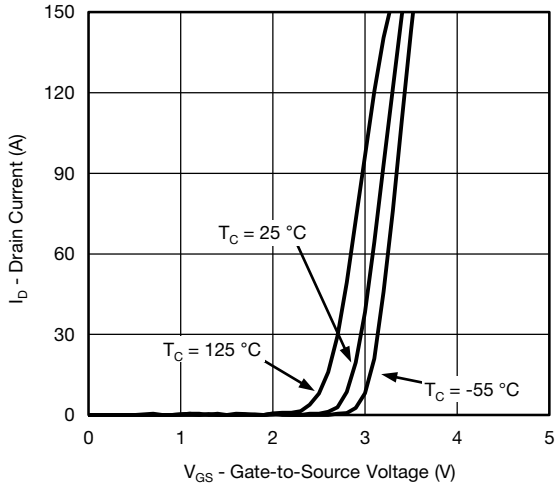
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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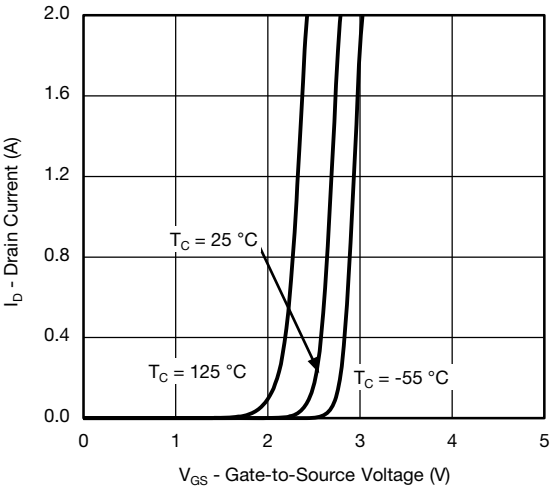
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



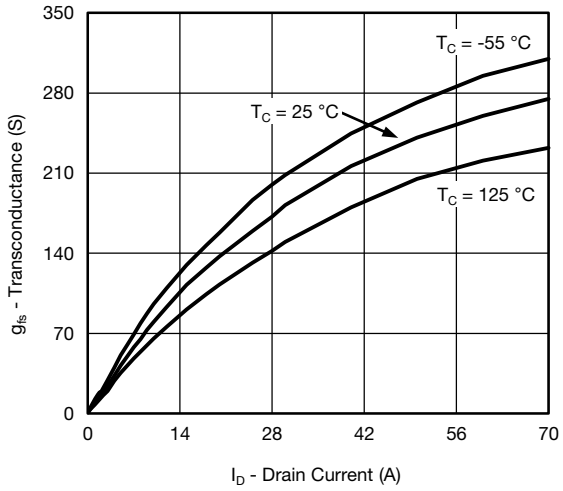
Output Characteristics



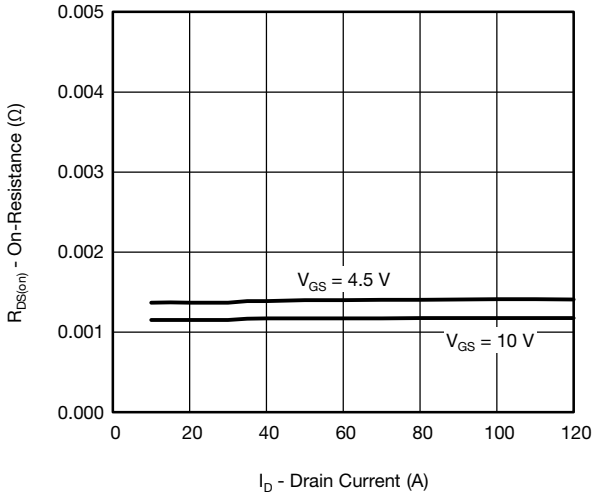
Transfer Characteristics



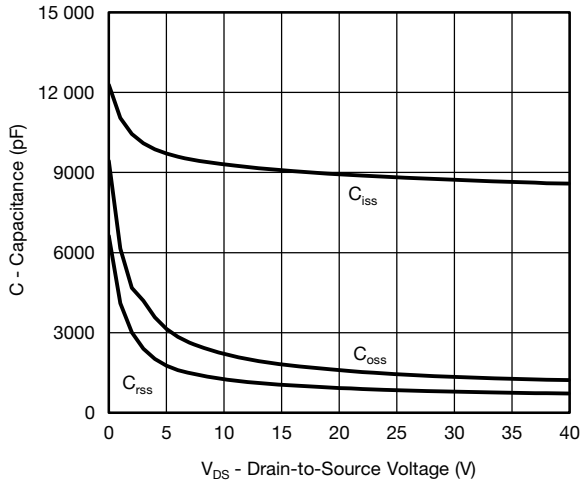
Transfer Characteristics



Transconductance



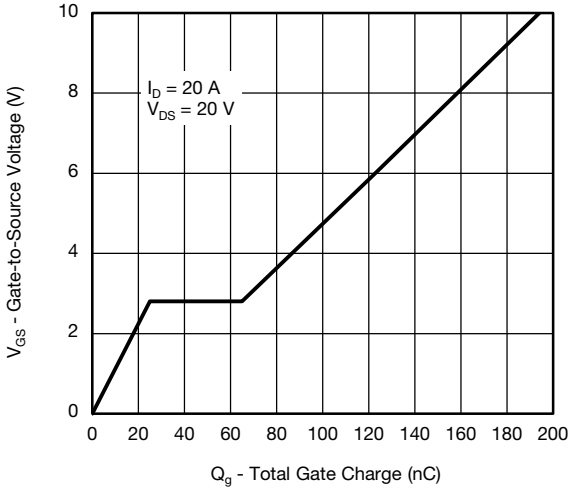
On-Resistance vs. Drain Current



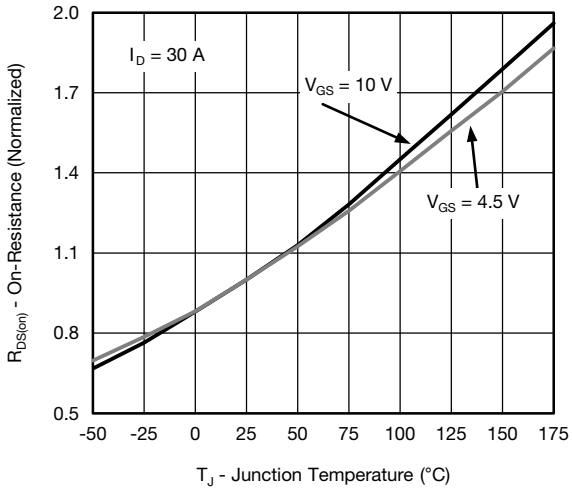
Capacitance

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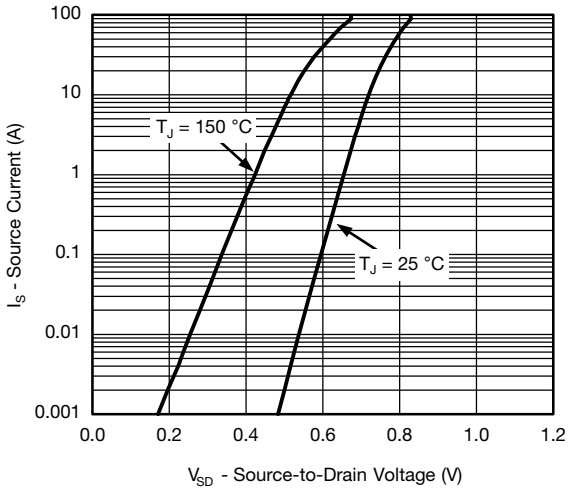
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



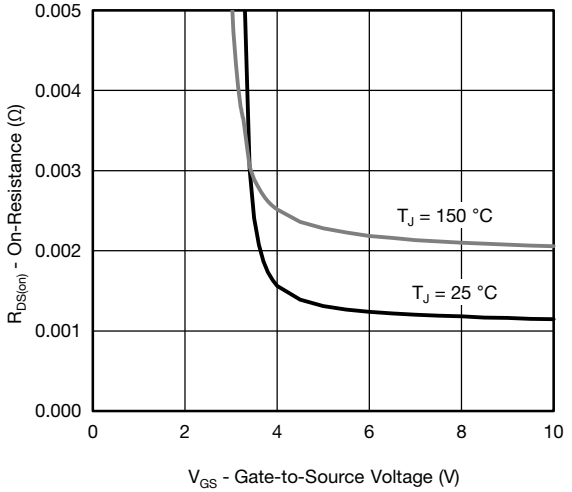
Gate Charge



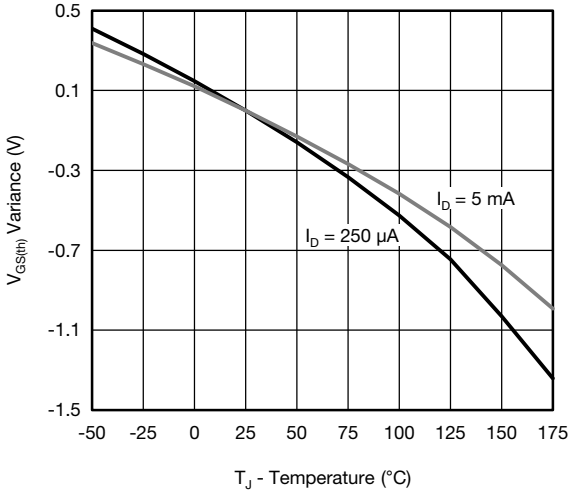
On-Resistance vs. Junction Temperature



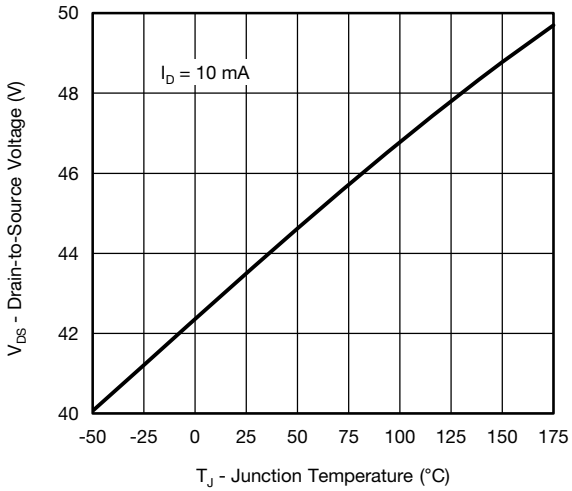
Source Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage



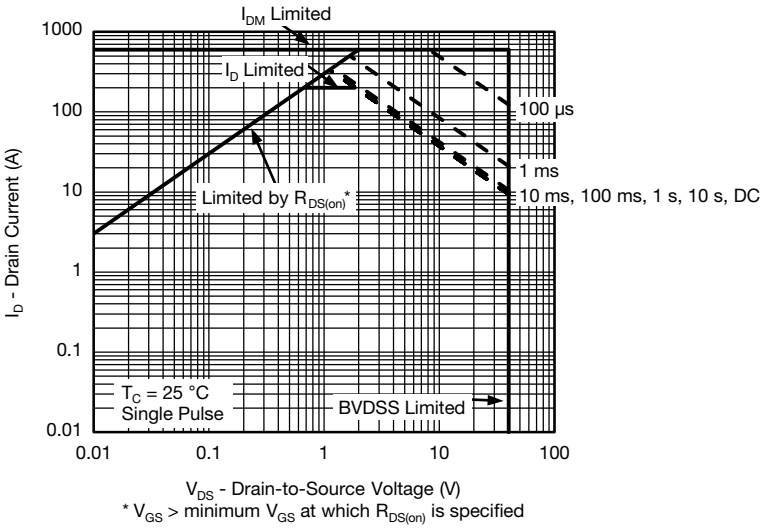
Threshold Voltage



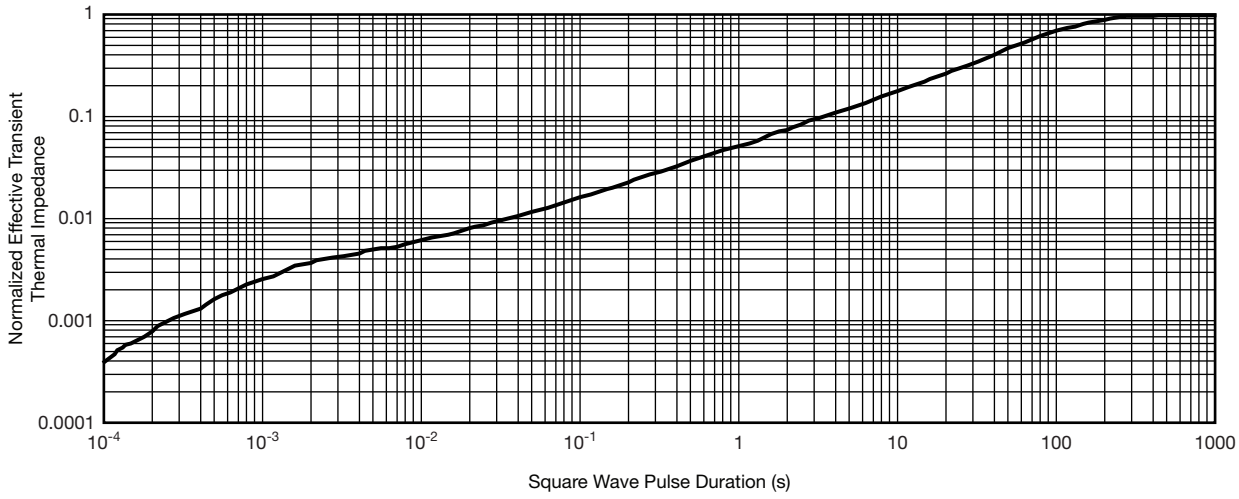
Drain Source Breakdown vs. Junction Temperature

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THERMAL RATINGS (T_A = 25 °C, unless otherwise noted)



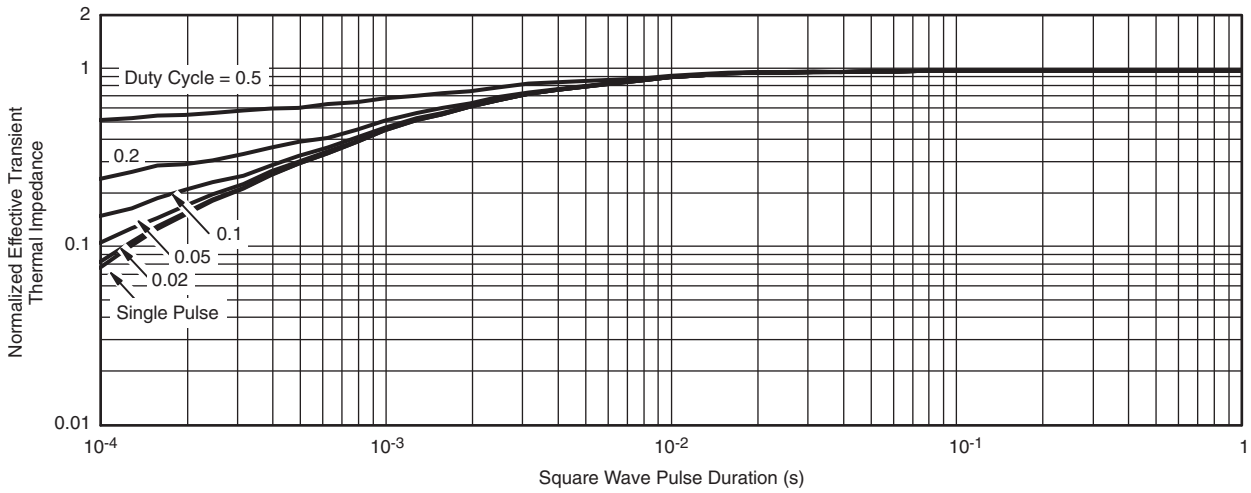
Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient

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THERMAL RATINGS (T_A = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Case

Note

- The characteristics shown in the two graphs
  - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
  - Normalized Transient Thermal Impedance Junction-to-Case (25 °C)

  are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

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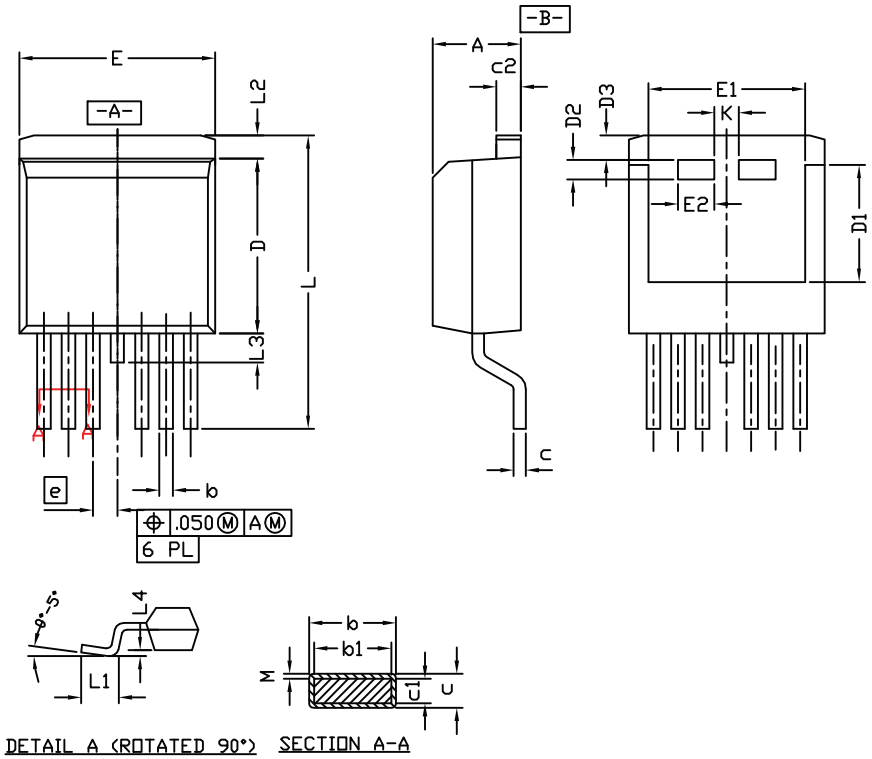
REVISION HISTORY [a]		
REVISION	DATE	DESCRIPTION OF CHANGE
B	04-Aug-15	• Revised R_g minimum limit

Note

a. As of April 2014

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D²PAK (TO-263-7L) Case Outline



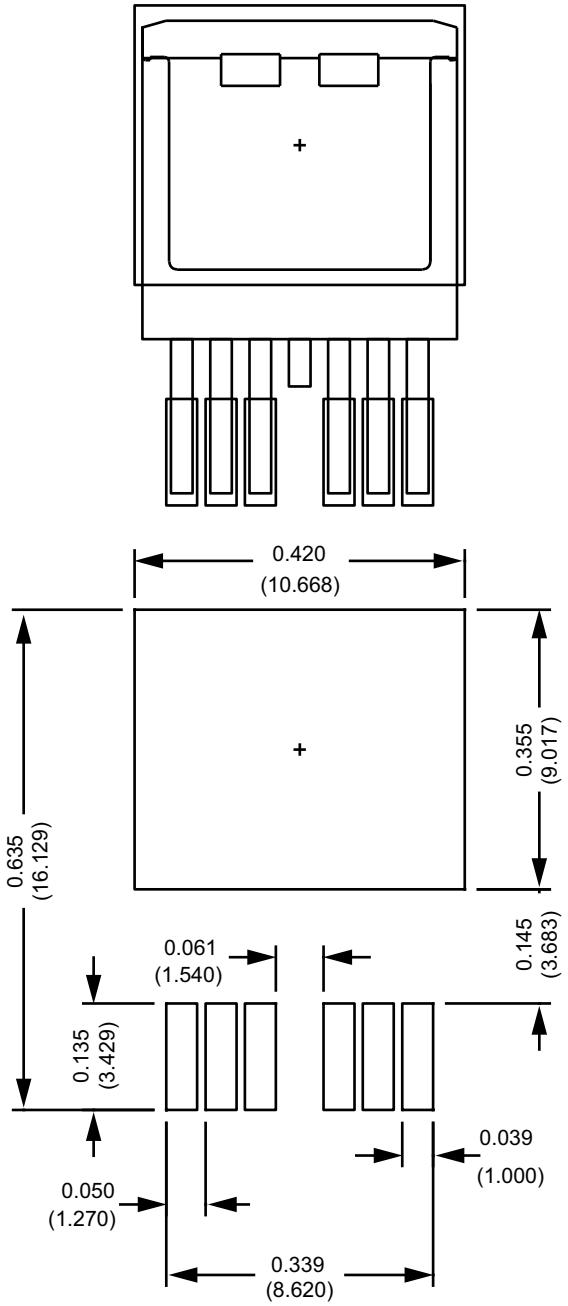
Notes

1. Plane B includes maximum features of heat sink tab and plastic.
2. No more than 25 % of L1 can fall above seating plane by max. 8 mils.
3. Pin to pin coplanarity max. 4 mils.
4. Lead thickness 25 mils.
5. For SUM part numbers lead thickness is 24 mils to 29 mils.
6. For reference only.
7. Use inches as the primary measurement.
8. This feature is only for SUM.

DIM.	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.160	0.190	4.064	4.826
b	0.020	0.039	0.508	0.990
b1	0.020	0.035	0.508	0.889
b2	0.045	0.055	1.143	1.397
c* SUB	0.012	0.018	0.305	0.457
c* SUM	0.022	0.028	0.559	0.711
c1	0.018	0.025	0.457	0.635
c2	0.045	0.055	1.143	1.397
D	0.340	0.380	8.636	9.652
D1	0.220	0.240	5.588	6.096
D2	0.038	0.042	0.965	1.067
D3	0.045	0.055	1.143	1.397
E	0.380	0.410	9.652	10.414
E1	0.245	-	6.223	-
E2	0.072	0.078	1.829	1.981
e	0.050 BSC		1.27 BSC	
K	0.045	0.055	1.143	1.397
L	0.575	0.625	14.605	15.875
L1	0.090	0.110	2.286	2.794
L2	0.040	0.055	1.016	1.397
L3	0.050	0.070	1.270	1.778
L4	0.010 BSC		0.254 BSC	
M	-	0.002	-	0.050
ECN: T13-0709-Rev. B, 30-Sep-13 DWG: 6006				

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Recommended Land Pattern D²PAK (TO-263-7L)



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