6-A Smart Load Switch Battery Charger

General Description

The RT9750 is a 6-A smart load switch battery charger, which integrates an internal load switch with charge pump control and 4-path constant current/constant voltage regulation, a 5-way hardware protection, and a 8-Channel 12-bit analog-to-digital converter. The RT9750 provides the accurate analog-to-digital converter for voltage/current measurement by I^2C serial interface to report the battery charging parameters and 3-way software protection and flags.

Ordering Information

RT9750□

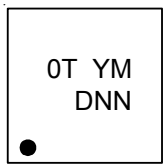
Package Type
WSC : WL-CSP-42B 2.75x3.05 (BSC)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Marking Information



0T : Product Code

YMDNN : Date Code

Features

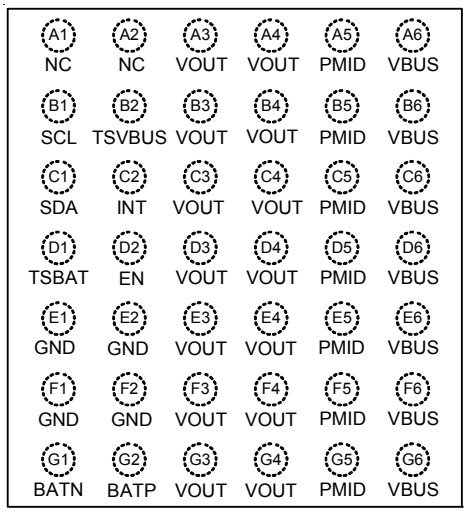
- **Internal Load Switch with Charge Pump Control**
  - **Dual NFETs in a Back to Back Configuration**
  - **Internal Charge Pump Control**
- **4-Path CC/CV Regulation**
  - **Input Current Regulation (ICR)**
  - **Output Voltage Regulation (OVR)**
  - **Battery Voltage Regulation (BVR)**
  - **Battery Current Regulation (BCR)**
- **5-Way Hardware Protection**
  - **VBUS Over-Voltage Protection (VBUS_OVP)**
  - **Drop-Out Over-Voltage Protection (VDR_OVP)**
  - **Reverse Over-Current Protection (RE_OCP)**
  - **Junction Over-Temperature Protection (TJ_OTP)**
  - **Input Over-Current Protection (IOC_OCP)**
- **8-Channel 12-bit ADC**
  - **High Accuracy of 12-bit Resolution**
  - **8-Channel for Voltage/Current Measurement**
  - **High Speed Data Rate for 8/16 Times Average per Channel**
- **3-Way Software Protection**
  - **Drop-Out Over-Voltage Protection Alarm (VDR_ALM)**
  - **TS of the VBUS Over-Temperature Protection (TBUS_OTP)**
  - **TS of the BAT Over-Temperature Protection (TBAT_OTP)**

Applications

- Handheld Products
- Portable Media Players

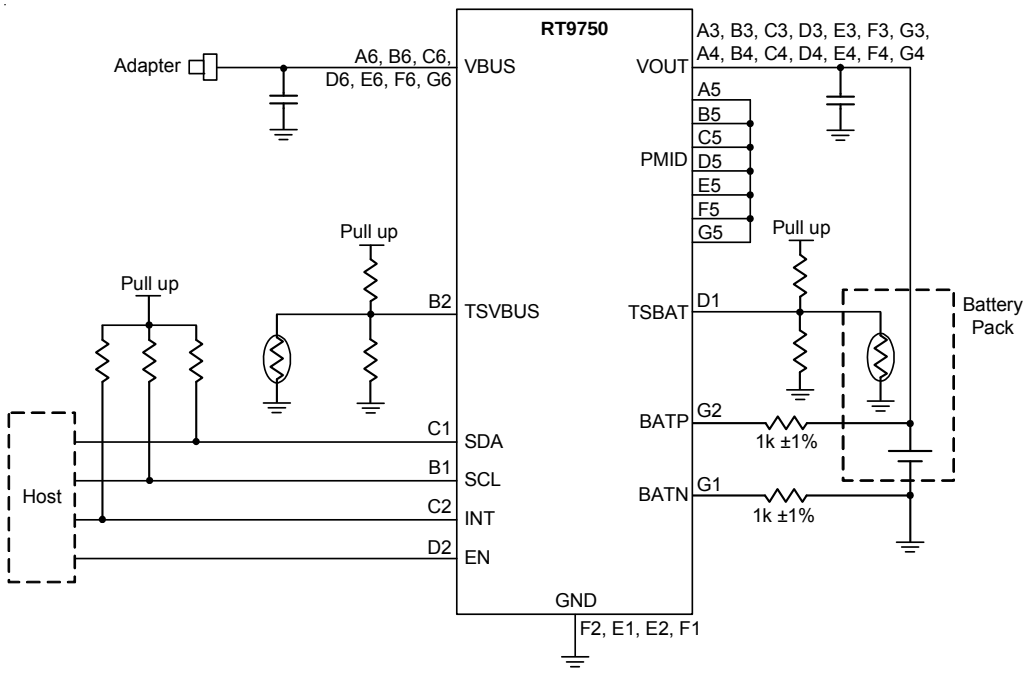
Pin Configuration

(TOP VIEW)



WL-CSP-42B 2.75x3.05 (BSC)

Typical Application Circuit



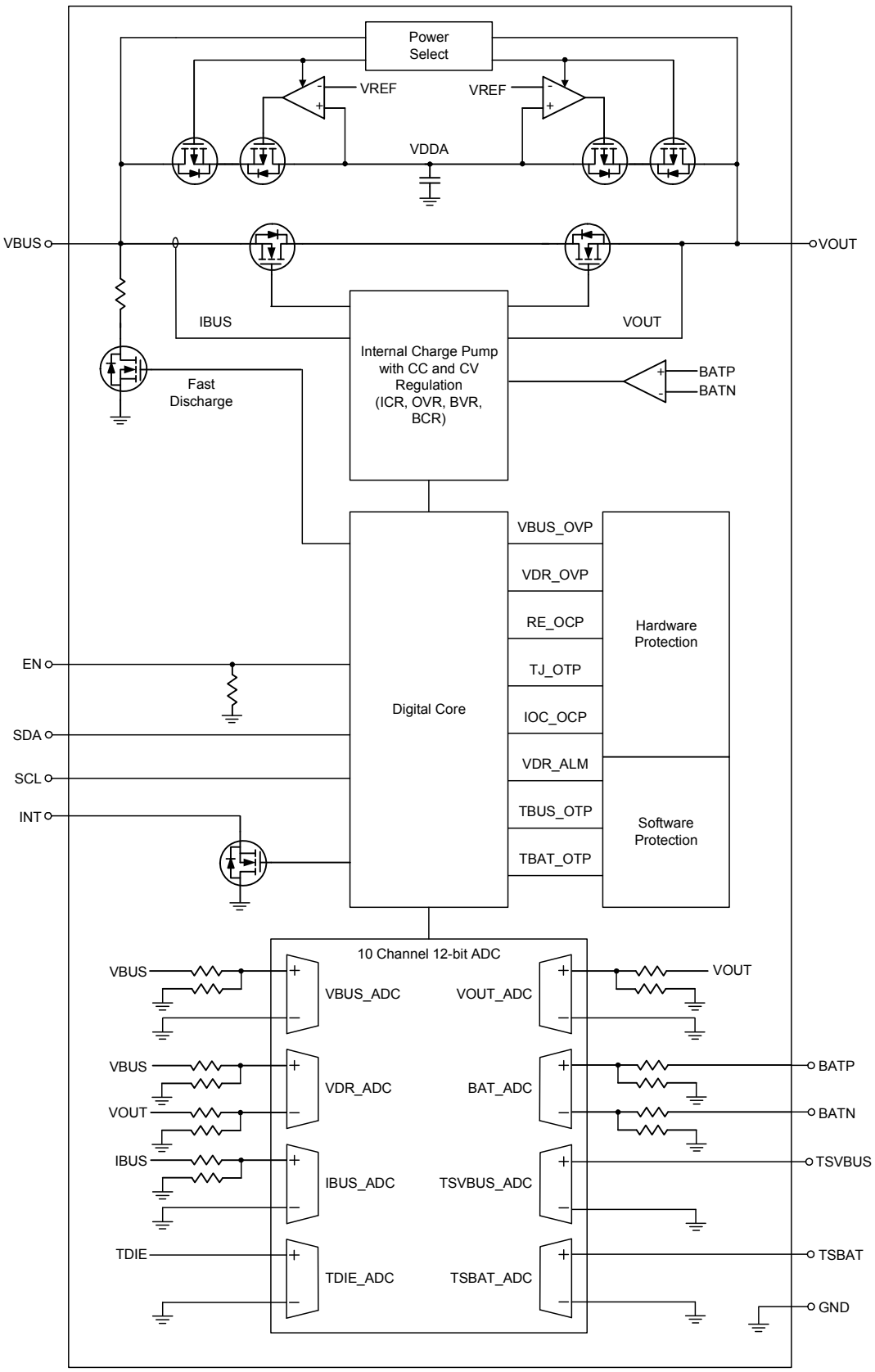
Below are recommended capacitor and inductor information

Pin	Description	Part Number	Package	Manufacturer
VBUS	1μF/25V	GRM185R61E105KA12	0603	muRata
VOUT	10μF/25V	GRM188R61E106MA73	0603	muRata
SRP / SRN	10mΩ ±1%	WMCS0805R010FSTA	0805	Wellcomp
BATP BATN	1kΩ ±1%	WR04X1001FTL	0402	WAISIN

Functional Pin Description

Pin No.	Pin Name	I/O	Pin Function
A1, A2	NC	NC	No internal connection.
A6, B6, C6, D6, E6, F6, G6	VBUS	P	DC input power supply.
A5, B5, C5, D5, E5, F5, G5	PMID	NC	Connect these pin together and do not connect to power input or ground.
A3, B3, C3, D3, E3, F3, G3, A4, B4, C4, D4, E4, F4, G4	VOUT	P	Battery connection point to positive terminal of the battery pack.
E1, E2, F1, F2	GND	P	Ground.
G1	BATN	AI	Negative input for battery current sensing by 1kΩ. Connect to negative terminal of battery pack.
G2	BATP	AI	Positive input for battery voltage sensing by 1kΩ. Connect to positive terminal of battery pack.
B2	TSVBUS	AI	VBUS temperature qualification voltage input. Require an external resistor divider and a voltage reference.
D1	TSBAT	AI	Battery temperature qualification voltage input. Require an external resistor divider and a voltage reference.
C1	SDA	DI	I^2C interface data. Connect to pull-up voltage via 10kΩ pull-up resistor.
B1	SCL	DIO	I^2C interface clock. Connect to pull-up voltage via 10kΩ pull-up resistor.
D2	EN	DI	Device enable control pin. Pull low to disable device. I^2C not available when disabled.
C2	INT	DO	Open drain interrupt output. connect to pull-up voltage via 10kΩ pull-up resistor. Normally high, the INT pin sends an active low.

Functional Block Diagram



Absolute Maximum Ratings (Note 1)

- Supply Pin Voltage, VBUS ---------- –0.3V to 22V
- Supply Pin Voltage, VOUT ---------- –0.3V to 22V
- Other Pin Voltage ---------- 0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  WL-CSP-42B 2.75x3.05 (BSC) ---------- 3.54W
- Package Thermal Resistance (Note 2)
  WL-CSP-42B 2.75x3.05 (BSC), θ_{JA} ---------- 28.2°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Input Voltage Range, VBUS ---------- 3.0V to 6V
- Supply Input Voltage Range, VOUT ---------- 3.0V to 6V
- Analog Sense Voltage Range, BATP, BATN ---------- 0V to 5V
- Temperature Sense Voltage Range, TSVBUS, TSBAT ---------- 0V to 3V
- Output Sink Current, INT ---------- 1mA
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Power Source						
VDDA UVLO Threshold	$V_{DDA\_VBUS\_UVLO}$	V_{DDA} rising, V_{BUS} > V_{OUT}, V_{DDA} = V_{BUS}	2.7	2.8	2.9	V
	$V_{DDA\_VOUT\_UVLO}$	V_{DDA} rising, V_{BUS} < V_{OUT}, V_{DDA} = V_{OUT}				
VDDA UVLO Hysteresis	$V_{DDA\_VBUS\_HYS}$	V_{DDA} falling, V_{BUS} > V_{OUT}, V_{DDA} = V_{BUS}	50	150	250	mV
	$V_{DDA\_VOUT\_HYS}$	V_{DDA} falling, V_{BUS} < V_{OUT}, V_{DDA} = V_{OUT}				
VBUS Quiescent Current	I_{Q_VBUS}	V_{BUS} = 4.2V > V_{OUT}, charge mode, LDSW enable	3	4	6	mA
VOUT Quiescent Current	I_{Q_VOUT}	V_{OUT} = 4.2V > V_{BUS}, battery mode, ADC enable	2	3	5	mA
VOUT Leakage Current	I_{LEAK_VOUT}	V_{OUT} = 4.2V > V_{BUS}, EN disable	0.5	1	1.5	µA
VBAT Insert	V_{BAT_INSERT}	V_{BAT} = BATP-BATN	1.9	2	2.1	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Load Switch On-Resistance and Regulation						
Load Switch **On-Resistance**	R_{ON_LDSW}		--	8	10	mΩ
IBUS REG Threshold Range	I_{BUS_REG}	I^2C programmable	0.4	--	6.35	A
IBUS REG Threshold Step		7-bit DAC	25	50	75	mA
VOUT REG Threshold Range	V_{OUT_REG}	I^2C programmable	4.2	--	5	V
VOUT REG Threshold Step		7-bit DAC	5	10	15	mV
VBAT REG Threshold Range	V_{BAT_REG}	I^2C programmable	4.2	--	5	V
VBAT REG Threshold Step		7-bit DAC	5	10	15	mV
Hardware Protection						
VBUS OVP Threshold Range	V_{BUS_OVP}	I^2C programmable	4.2	--	6.5	V
VBUS OVP Threshold Step		7-bit DAC	12.5	25	37.5	mV
Drop-Out OVP Threshold	V_{DROP_OVP}	I^2C programmable	0	--	1000	mV
Drop-Out OVP Step		7-bit DAC	5	10	15	mV
Reverse OCP Threshold	I_{RE_OCP}	Default, load switch R_{ON} = 10mΩ	0.5	1.5	2.5	A
Junction OTP Threshold	T_{JC_OTP}	1-value	115	125	140	°C
Input OCP Threshold	I_{OC_OCP}	I^2C programmable	0	--	6.5	A
Input OCP Step		4-bit DAC	250	500	750	mA
Software Protection						
Drop-Out ALM Threshold	V_{DROP_ALM}	I^2C programmable	0	--	1000	mV
Drop-Out ALM Step		7-bit DAC	5	10	15	mV
TSVBUS OTP Threshold	V_{TSVBUS_OTP}	I^2C programmable	0	--	2.4	V
TSVBUS OTP Step		7-bit DAC	10	20	30	mV
TSBAT OTP Threshold	V_{TSBAT_OTP}	I^2C programmable	0	--	2.4	V
TSBAT OTP Step		7-bit DAC	10	20	30	mV
ADC Specification						
ADC Sample Rate	f_{SAMPLE_ADC}	(Note 5)	--	2.25	--	MHz
ADC Data Rate	f_{DATA_ADC}	(Note 5), 16 averages	--	10	--	kHz

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VBUS ADC Range	$V_{BUS\_ADC\_RAN}$	VDDA > 3V, 16 averages	1.5	--	6.5	V
VBUS ADC Accuracy	$V_{BUS\_ADC\_ACC}$		–15	--	15	mV
IBUS ADC Range	$I_{BUS\_ADC\_RAN}$	VDDA > 3V, 16 averages	0	--	7	A
IBUS ADC Accuracy	$I_{BUS\_ADC\_ACC}$		–200	--	200	mA
VOUT ADC Range	$V_{OUT\_ADC\_RAN}$	VDDA > 3V, 16 averages	1.5	--	6.5	V
VOUT ADC Accuracy	$V_{OUT\_ADC\_ACC}$		–15	--	15	mV
VDROP ADC Range	$V_{DROP\_ADC\_RAN}$	VDDA > 3V, 16 averages	0	--	1000	mV
VDROP ADC Accuracy	$V_{DROP\_ADC\_ACC}$		–15	--	15	mV
VBAT ADC Range	$V_{BAT\_ADC\_RAN}$	VDDA > 3V, 16 averages	2.5	--	5	V
VBAT ADC Accuracy	$V_{BAT\_ADC\_ACC}$		–15	--	15	mV
TSVBUS ADC Range	$V_{TSVBUS\_ADC\_RAN}$	VDDA > 3V, 16 averages	0	--	2.4	V
TSVBUS ADC Accuracy	$V_{TSVBUS\_ADC\_ACC}$		–15	--	15	mV
TSBAT ADC Range	$V_{TSBAT\_ADC\_RAN}$	VDDA > 3V, 16 averages	0	--	2.4	V
TSBAT ADC Accuracy	$V_{TSBAT\_ADC\_ACC}$		–15	--	15	mV
Junction Thermal ADC Range	$T_{JC\_ADC\_RAN}$	VDDA > 3V, 16 averages	0	--	125	°C
Junction Thermal ADC Accuracy	$T_{JC\_ADC\_ACC}$		–3	--	3	°C
I^2C Interface						
Serial-Clock Frequency	f_{SCL_I2C}	(Note 5)	10	--	1000	kHz
I^2C Input Logic Threshold	V_{IH_I2C}	Logic high	1.5	--	--	V
	V_{IL_I2C}	Logic low	--	--	0.4	V
EN Input						
EN Input Logic Threshold	V_{IH_EN}	Logic high	1	--	--	V
	V_{IL_EN}	Logic low	--	--	0.4	V
EN Pull Down Resistor	R_{PD_EN}	On chip	--	500	--	kΩ
Device turn-on delay time after EN pull-high			--	--	500	μs

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

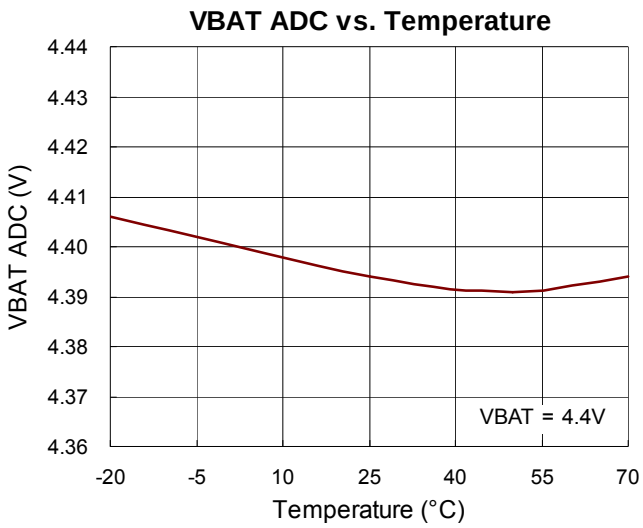
Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard.

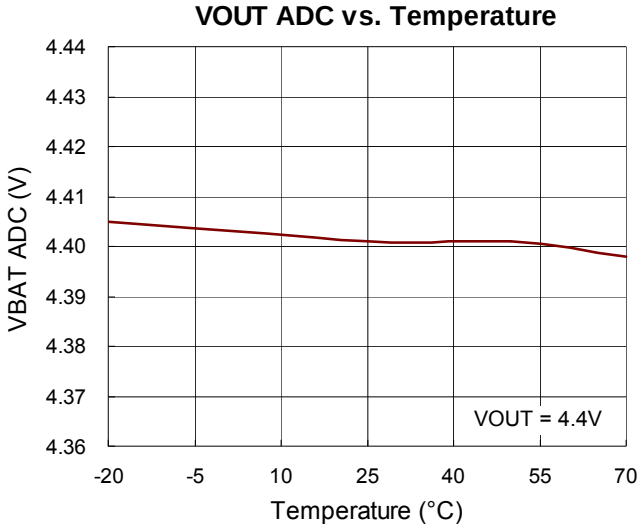
Note 3. Devices are ESD sensitive. Handling precaution is recommended.

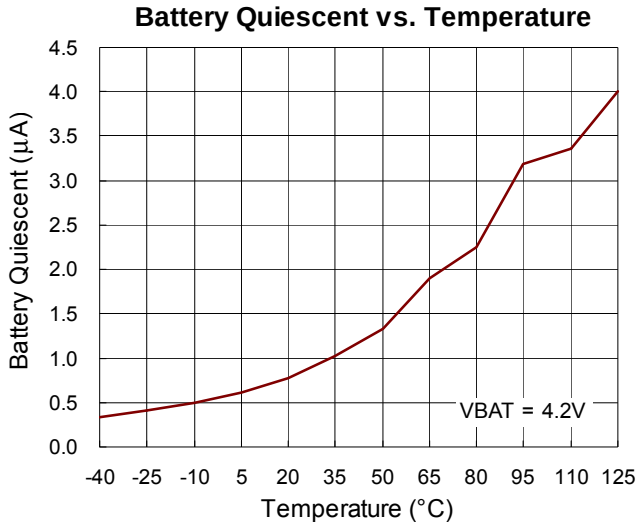
Note 4. The device is not guaranteed to function outside its operating conditions.

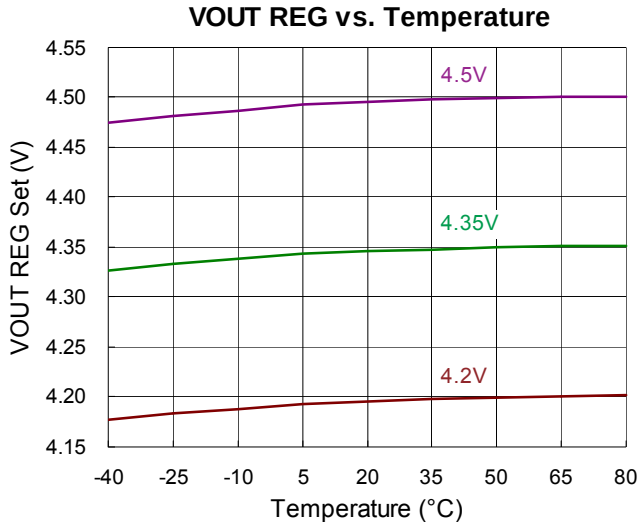
Note 5. Specification is guaranteed by design and/or correlation with statistical process control.

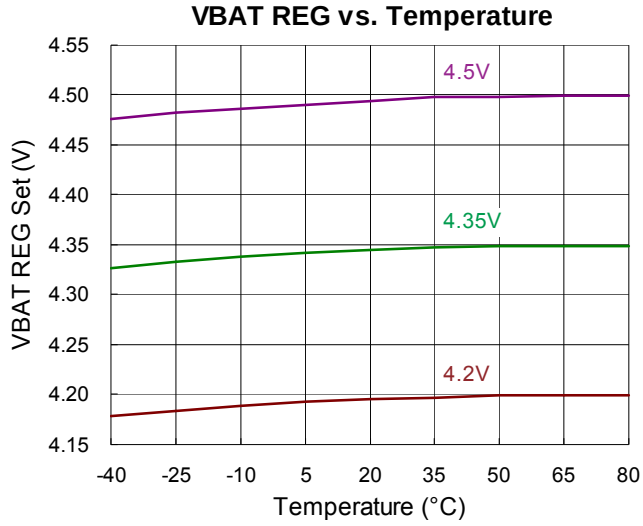
Typical Operating Characteristics

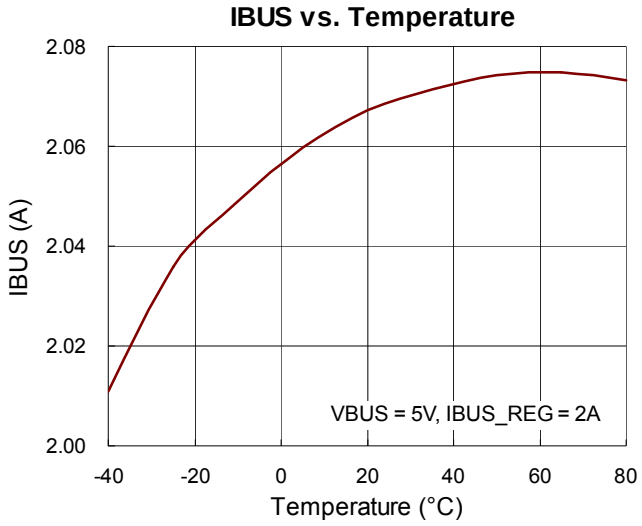


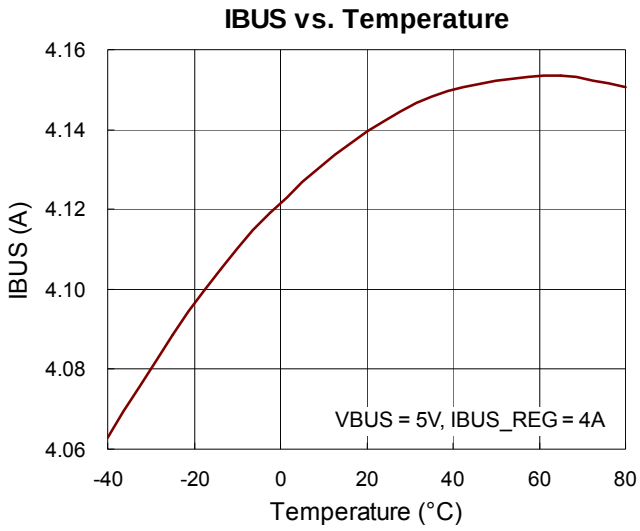












Application Information

Device Power On

The internal bias circuit (VDDA) are powered from higher of two voltages between VBUS and VOUT. The device will powered on when the VDDA is higher than VDDA UVLO threshold and EN pin is higher than V_{IH_EN}. In VBUS > VDDA UVLO & EN pin from low logic to high logic condition, the device need maximum 500μs turn on delay time after EN pin set to high logic.

Smart Load Switch

The RT9750 is a 8mΩ R_{ON} and loading can up to 6-A smart load switch battery charger. The load switch can be controlled by the host via I^2C. The load switch can be turn on by set CHG_EN bit to "1" (0x06 bit4) if no protection event happened (Please check 0X03 & 0X04). The load switch can be turn off by set CHG_EN bit to "0" or pull EN pin to low. If the protection event happen the load switch will be turn off automatically and set CHG_EN bit to "0" The smart load switch also implement soft-on & soft off to function minimize the inrush current and voltage spike.

8-Channel 12-bit Analog to Digital Converter

The device integrate 8-Cannel 12 bit ADC function, user can monitor voltage of VBUS, VOUT, VDROP (voltage different between VBUS and VOUT), and VBAT. The user also can monitor the internal junction temperature, battery temperature (by external resistor divider and NTC thermistor), and VBUS temperature (by external resistor divider and NTC thermistor). The ADC function also provide IBUS information for user to monitor.

User can set ADC_EN (0x07 bit3) bit to enable or disable ADC conversion. User also can enable or disable ADC channels respective by using register 0x07 and 0x08. The ADC has two conversion rate 1- shot mode and continuous mode. User can select the mode by ADC_RATE bit (0X07 bit2).

1. 1-shot mode

In this mode, user need to set ADC_EN bit to 1 to start ADC conversion. The ADC_EN bit will change to 0 automatically after ADC start conversion. After the ADC conversion complete, the ADC_DONE bit (0x04 bit6) will change to 1 and INT pin will pull low if the ADC_DONE_MASK bit is no mask. The typical conversion time of one channel is 100μs (16 averages).

2. Continuous mode

In continuous mode, ADC conversion continuously if user set ADC_EN bit to 1 and ADC stop conversion if user set ADC_EN bit to 0.

User can set the ADC_AVG_EN bit to enable or disable ADC measurement averaging function in both 1-shot mode and continuous mode. If ADC_AVG_EN = 0 the ADC is instantaneous measurement. If ADC_AVG_EN = 1 the ADC is averaging measurement and user can set the number of samples by ADC_SAMPLES bit.

Linear Regulation Mode (LDO)

The load switch implement LDO mode to regulate VOUT voltage, battery voltage and input current. If an event that VOUT_REG, VBAT_REG or IBUS_REG threshold is exceeded, the load switch act as LDO and will regulate VOUT, VBAT, IBUS (depending upon which threshold is exceeded). These regulations threshold can be selected by I^2C.

Protection Features

The load switch implement 5 way hardware protection and 2 temperature protection as below. All these protection functions have IRQ and active with INT pin to inform host to monitor which protection is active.

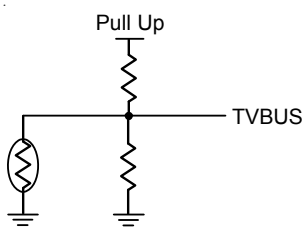
1. VBUS Over-Voltage Protection (VBUS_OVP)

When VBUS_OVP event is happened the device will turn off load switch and the CHG_EN bit will be set to 0. User can enable or disable this protection function by I^2C 0x06 bit 7. The protection threshold and deglitch time also can be selected by I^2C (Protection threshold is 0x0A, deglitch time is 0x09 bit0).

2. VBUS Over-Temperature Protection (TSVBUS_OTP)

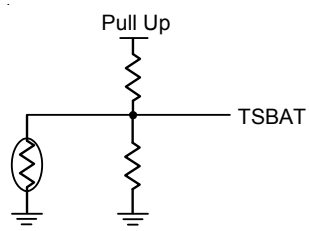
As below picture, user need to place an external NTC voltage dived circuit at TSBUS pin. When the voltage of TSBUS pin is over the threshold, the device will turn off load switch and set CHG_EN bit to 0. User can enable or

disable this protection function by I²C (0x05 bit2). Use also can set the threshold by I²C (0x11).



3. VBAT Over-Temperature Protection (TSBAT_OTP)

As below picture, user need to place an external NTC voltage dived circuit at TSBAT pin. When the voltage of TSBAT pin is over the threshold, the device will turn off load switch and set CHG_EN bit to 0. User can enable or disable this protection function by I²C (0x05 bit1). Use also can set the threshold by I²C (0x12).



4. IBUS Reverse Current Protection (IBUS_ IREV)

The device implement a reverse current protection function to turn off load switch when the reverse current is detected (current flow from VOUT to VBUS). The device set CHG_EN to "0" when this event is detected. The user can set the protection level and deglitch time by I²C (0x26 set level, 0x27 set deglitch).

5. Dropout Voltage Protection (VDROP_OVP)

VDROP is the voltage different between VBUS and VOUT. The device implement two VDROP threshold for user to set by I²C. One is VDROP_LAM and the other on is VDROP_OVP. User can use these thresholds to monitor the health of load switch. When the VDROP_ALM threshold be triggered the device assert INT pin low to alert the host. If VDROP_OVP threshold is be triggered the device will turn off the load switch and set CHG_EN bit to "0".

Due to the VDROP_ALM is an alarm signal, user should set VDROP_OVP threshold higher than VDROP_ALM.

6. Junction Thermal Shutdown (TSHUT_FLT)

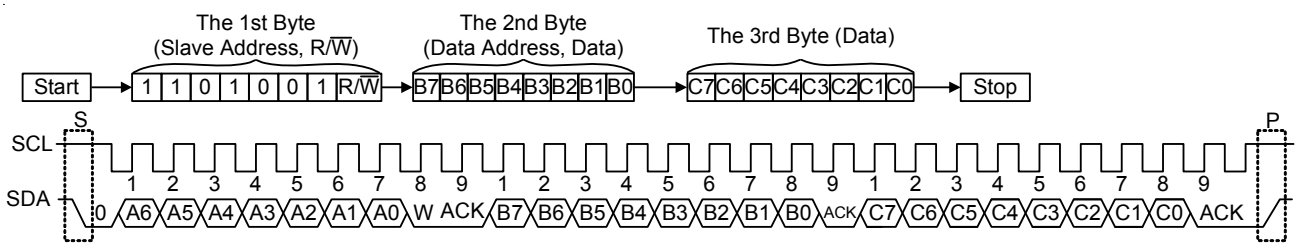
The device will turn off load switch and set CHG_EN bit to "0" if the threshold of junction temperature shutdown is triggered. If the junction thermal shutdown is triggered device asserted INT low to alert the host (no mask for TSHUT_FLT) and also set the TSHUT_FLT bit to "1".

7. IBUS Over-Current protection (IOC_FLT)

The device monitor the current flow from VBUS to VOUT. If the current over the threshold the device has two protection option for user to select by I²C. If user set OCP_RES bit "0" (blanking mode), the device will turn off load switch and set CHG_EN to "0" when IBUS current over IOC threshold. If user set OCP_RES bit "1" (hiccup mode), load switch is disabled instantaneously, and the device will attempt to turn on the load switch wait 250μs to check OCP and turn off every 100ms, up to 7 times before latching off.

I²C Interface Timing Diagram

The RT9750 acts as an I²C- bus slave. The I²C-bus master configures the settings for charge mode by sending command bytes to the RT9750 via the 2-wire7 I²C-bus. After the START condition the I²C master sends a chip address. This address is seven bits long followed by an eighth bit which is a data direction bit(R/W). The second byte selects the register to which the data will be written. The third byte contains data to the selected register.



Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WL-CSP-42B 2.75x3.05 (BSC) package, the thermal resistance, θ_{JA}, is 28.2°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C – 25°C) / (28.2°C/W) = 3.54W for a WL-CSP-42B 2.75x3.05 (BSC) package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 1 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

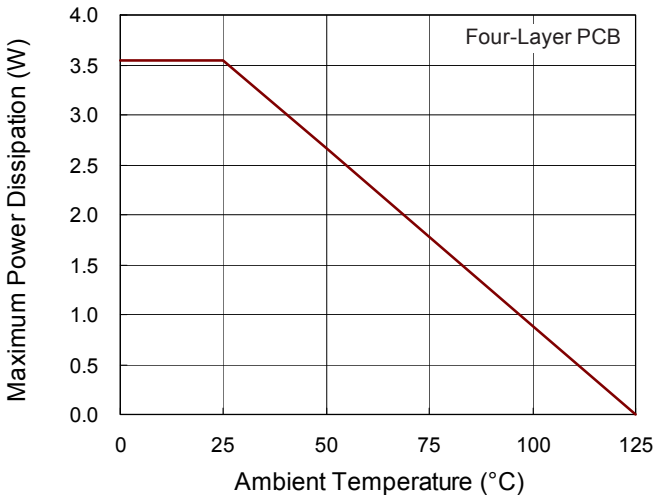


Figure 1. Derating Curve of Maximum Power Dissipation

Register Descriptions

I^2C Slave Address is 1100111 (67H)

Name		Function	Addr	Reset
DEVICE_INFO		DEVICE_INFO	0x00	0x00
Bit	**Mode**	**Name**	**Reset Value**	**Description**
[5:3]	R	DEVICE_RE	000	Device revision
[2:0]	R	DEVICE_ID	000	Device ID

Name		Function	Addr	Reset
EVENT_1_MASK		MASK	0x01	0x00
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R/W	VBUS_OVP_MASK	0	VBUS over-voltage fault mask. 0 – no mask. INT will toggle when VBUS_OVP_FLT bit is set. (default) 1 – VBUS_OVP_FLT is masked. INT will not toggle when VBUS_OVP_FLT bit is set.
6	R/W	IBUS_REG_MASK	0	IBUS over-current fault mask. 0 – no mask. INT will toggle when IBUS_REG_FLT bit is set. (default) 1 – IBUS_REG_FLT is masked. INT will not toggle when IBUS_REG_FLT bit is set.
5	R/W	VBAT_REG_MASK	0	VBAT over-voltage fault mask. 0 – no mask. INT will toggle when VBAT_REG_LDO bit is set. (default) 1 – VBAT_REG_LDO is masked. INT will not toggle when VBAT_REG_LDO bit is set.
4	R/W	Reserved	0	Reserved
3	R/W	VOUT_REG_MASK	0	VOUT over-voltage fault mask. 0 – no mask. INT will toggle when VOUT_REG_LDO bit is set. (default) 1 – VOUT_REG_LDO is masked. INT will not toggle when VOUT_REG_LDO bit is set.
2	R/W	TBUS_OTP_MASK	0	VBUS over-temperature fault mask. 0 – no mask. INT will toggle when TBUS_OTP_FLT bit is set. (default) 1 – TBUS_OTP_FLT is masked. INT will not toggle when TBUS_OTP_FLT bit is set.
1	R/W	TBAT_OTP_MASK	0	BAT over-temperature fault mask. 0 – no mask. INT will toggle when TBAT_OTP_FLT bit is set. (default) 1 – TBAT_OTP_FLT is masked. INT will not toggle when TBAT_OTP_FLT bit is set.
0	R/W	IBUS_IREV_MASK	0	IBUS reverse current fault mask. 0 – no mask. INT will toggle when IBUS_REV_FLT bit is set. (default) 1 – IBUS_REV_FLT is masked. INT will not toggle when IBUS_REV_FLT bit is set.

Name		Function	Addr	Reset
EVENT_2_MASK		MASK	0x02	0x00
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R/W	LOWCHG_ALM_MASK	0	LOWCHG_ALM event mask. 0 – no mask. INT will toggle when LOWCHG_ALM bit is set. (default) 1 – LOWCHG_ALM is masked. INT will not toggle when LOWCHG_ALM bit is set.
6	R/W	ADC_DONE_MASK	0	ADC_DONE event mask. After all required CHs complete, set ADC_DONE 0 – no mask. INT will toggle no mask when ADC_DONE bit is set. (default). 1 – ADC_DONE bit is masked. INT will not toggle when ADC_DONE bit is set.
5	R/W	VDROP_ALM_MASK	0	VDROP_ALM_FLT mask. 0 – no mask. INT will toggle when VDROP_ALM_FLT bit is set. (default) 1 – VDROP_ALM_FLT is masked. INT will not toggle when VDROP_ALM_FLT bit is set.
4	R/W	VDROP_OVP_MASK	0	VDROP_OVP_FLT mask. 0 – no mask. INT will toggle when VDROP_OVP_FLT bit is set. (default) 1 – VDROP_OVP_FLT is masked. INT will not toggle when VDROP_OVP_FLT bit is set.
3	R/W	VBUS_INSERT_MASK	0	VBUS_INSERT mask. 0 – no mask. INT will toggle when VBUS_INSERT bit is set. (default) 1 – VBUS_INSERT is masked. INT will not toggle when VBUS_INSERT bit is set.
2	R/W	BAT_INSERT_MASK	0	BAT_INSERT mask. 0 – no mask. INT will toggle when BAT_INSERT bit is set. (default) 1 – VBUS_INSERT is masked. INT will not toggle when BAT_INSERT bit is set.
1	R/W	TSHUT_FLT_MASK	0	TSHUT_FLT mask. 0 – no mask. INT will toggle when TSHUT_FLT bit is set. (default) 1 – TSHUT_FLT is masked. INT will not toggle when TSHUT_FLT bit is set.
0	R/W	IOC_FLT_MASK	0	IOC_FLT mask. 0 – no mask. INT will toggle when IOC_FLT bit is set. (default) 1 – IOC_FLT is masked. INT will not toggle when IOC_FLT bit is set.

Name		Function	Addr	Reset
EVENT_1		EVENT	0x03	0x00
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R/C	VBUS_OVP_FLT	0	VBUS over-voltage fault. This bit is set when the VBUS voltage exceeds the limit set in VBUS_OVP register. 0 – no fault (default) 1 – VBUS OVP fault
6	R/C	IBUS_REG_LDO	0	Indicates if in LDO mode due to IBUS regulation threshold. 0 – no fault (default) 1 – IBUS in regulation
5	R/C	VBAT_REG_LDO	0	Indicates if in LDO mode due to VBAT regulation threshold. 0 – no in regulation (default) 1 – VBAT in regulation
4	R/C	Reserved	0	Reserved
3	R/C	VOUT_REG_LDO	0	Indicates if in LDO mode due to VOUT regulation threshold. 0 – not in regulation (default) 1 – VOUT in regulation
2	R/C	TBUS_OTP_FLT	0	VBUS over-temperature fault. This bit is set when the TS_BUS voltage exceeds the limit set in TBUS_OTP register. 0 – no fault (default) 1 – VBUS over-temperature fault
1	R/C	TBAT_OTP_FLT	0	BAT over-temperature fault. This bit is set when the TS_BAT voltage exceeds the limit set in TBAT_OTP register. 0 – no fault (default) 1 – BAT over-temperature fault
0	R/C	IBUS_IREV_FLT	0	IBUS reverse current fault. This bit is set when current from BAT to VBUS is detected. The battery switch will be disabled when reverse current is detected. 0 – no fault (default) 1 – IBUS reverse current fault

Name		Function	Addr	Reset
EVENT_2		EVENT	0x04	0x00
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R/C	LOWCHG_ALM_FLT	0	Indicates if LOWCHG_ALM threshold is reached. 0 – no LOWCHG_ALM (default) 1 – LOWCHG_ALM when CHG_EN and IBUS < threshold
6	R/C	ADC_DONE	0	Indicates if the ADC conversion is complete for the requested parameters in 1-shot mode only (set from 0x07). 0 – Conversion not complete (default) 1 – Conversion complete
5	R/C	VDROP_ALM_FLT	0	Indicates if VDROP_ALM threshold is reached. 0 – no fault (default) 1 – VDROP_ALM fault
4	R/C	VDROP_OVP_FLT	0	Indicates if VDROP_OVP threshold is reached. 0 – no fault (default) 1 – VDROP_OVP fault
3	R/C	VBUS_INSERT	0	Indicates if VBUS is detected 0 – no VBUS (default) 1 – VBUS inserted (VBUS > 2.8V)
2	R/C	BAT_INSERT	0	Indicates if battery is detected (sensed between BATP and BATN). 0 – no BAT (default) 1 – BAT inserted (VBAT > 2.0V)
1	R/C	TSHUT_FLT	0	IC thermal shutdown fault indicator. (TDIE > 125°C) 0 – Normal operation (default) 1 – Thermal shutdown
0	R/C	IOC_FLT	0	Indicates if high current from VBUS to VOUT has hit the internal threshold. 0 – no fault (default) 1 – High current fault

Name		Function	Addr	Reset
EVENT_1_EN		EVENT_EN	0x05	0xFE
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R/W	VBUS_OVP_EN	1	Enables VBUS_OVP protection 0 – Disable VBUS OVP protection 1 – Enable VBUS OVP protection (default)
6	R/W	IBUS_REG_EN	1	Enables IBUS regulation for LDO mode 0 – Disable IBUS OCP protection 1 – Enable IBUS OCP protection (default)
5	R/W	VBAT_REG_EN	1	Enables VBAT regulation for LDO mode 0 – Disable VBAT regulation 1 – Enable VBAT regulation (default)
4	R/W	Reserved	1	Reserved
3	R/W	VOUT_REG_EN	1	Enables VOUT regulation in LDO mode 0 – Disable VOUT regulation 1 – Enable VOUT regulation (default)
2	R/W	TBUS_OTP_EN	1	Enables TS_VBUS pin protection 0 – Disable TBUS_OTP 1 – Enable TBUS_OTP (default)
1	R/W	TBAT_OTP_EN	1	Enables TS_BAT pin protection 0 – Disable TBAT_OTP 1 – Enable TBAT_OTP (default)
0	R/W	VBUS_PD_EN	0	Enables the VBUS pull-down resistor 0 – Disable RVBUS_PD (default) 1 – Enable RVBUS_PD

Name		Function	Addr	Reset
CONTROL		CONTROL	0x06	0x2A
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R/W	VDROP_OVP_EN	0	Enables VDROP_OVP protection 0 – Disable VDROP_OVP (default) 1 – Enable VDROP_OVP
6	R/W	VDROP_ALM_EN	0	Enables VDROP_ALM alarm 0 – Disable VDROP_ALM (default) 1 – Enable VDROP_ALM
5	R/W	Reserved	1	Reserved
4	R/W	CHG_EN	0	Software bit for charge enable. This enables the Load Switch. This bit will be set to '0' if reset or any action of FET turned off (STATUS register). 0 – Charge disabled (default) 1 – Charge enabled
[3:2]	R/W	WATCHDOG<1:0>	10	Watchdog timer setting. R/W any register will clear the watchdog timer. FET must turn off after watchdog timer out. 00 – Disable watchdog timer 01 – 0.5sec 10 – 1.0sec (default) 11 – 2.0sec
1	R/W	IREV_EN	1	Reverse current protection (RCP) comparator control. 0 – RCP disable 1 – RCP enable (default)
0	R/W	REG_RST	0	Register reset 0 – no reset (default) 1 – Reset all registers to their default values

Name		Function	Addr	Reset
ADC_CTRL		ADC_CTRL	0x07	0x8F
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R/W	TDIE_ADC_EN	1	Enable/disable TDIE_ADC sampling 0 – Disable sampling 1 – Enable sampling (default)
3	R/W	ADC_EN	1	Enable/disable ADC 0 – Disable ADC 1 – Enable ADC (default)
2	R/W	ADC_RATE	1	Sets ADC conversion rate 0 – 1-shot conversion 1 – Continuous conversion (default)
1	R/W	ADC_AVG_EN	1	Enable/disable ADC measurement averaging 0 – Disable averaging (instantaneous measurement) 1 – Enable averaging (default)
0	R/W	ADC_SAMPLES	1	Sets the number of samples to be taken for an ADC conversion 0 – 8 samples taken for averaging 1 – 16 samples taken for averaging (default)

Name		Function	Addr	Reset
SAMPLE_EN		SAMPLE_EN	0x08	0xFF
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R/W	VBUS_ADC_EN	1	Enable/disable VBUS_ADC sampling 0 – Disable sampling 1 – Enable sampling (default)
6	R/W	IBUS_ADC_EN	1	Enable/disable IBUS_ADC sampling 0 – Disable sampling 1 – Enable sampling (default)
5	R/W	VOUT_ADC_EN	1	Enable/disable VOUT_ADC sampling 0 – Disable sampling 1 – Enable sampling (default)
4	R/W	VDROP_ADC_EN	1	Enable/disable VDROP_ADC sampling 0 – Disable sampling 1 – Enable sampling (default)
3	R/W	VBAT_ADC_EN	1	Enable/disable VBAT_ADC sampling 0 – Disable sampling 1 – Enable sampling (default)
2	R/W	Reserved	1	Reserved
1	R/W	TBUS_ADC_EN	1	Enable/disable TBUS_ADC sampling 0 – Disable sampling 1 – Enable sampling (default)
0	R/W	TBAT_ADC_EN	1	Enable/disable TBAT_ADC sampling 0 – Disable sampling 1 – Enable sampling (default)

Name		Function	Addr	Reset
PROT_DLY&OCP		PROT_DLY&OCP	0x09	0xA0
Bit	**Mode**	**Name**	**Reset Value**	**Description**
[7:4]	R/W	IOC_OCP<3:0>	1010	IOC_OCP (Input Over-Current Protection) Offset : 0A LSB<3:0> : 4A, 2A, 1A, 0.5A Range Min : 0A (0b0000) Range Max : 6.5A (0b1101) Default : 5A (0b1010)
3	R/W	LOWCHG_ALM_EN	0	Enables LOWCHG_ALM in CHG mode 0 – Disable LOWCHG_ALM (default) 1 – Enable LOWCHG_ALM
2	R/W	LOWCHG_ALM	0	LOWCHG_ALM 0 – 50mA (default) (0x15<4:0> = 00000, 0x16<7:0> = 00110010) 1 – 100mA (0x15<4:0> = 00000, 0x16<7:0> = 01100100)
1	R/W	OCP_RES	0	Controls the response of the OCP event for IBUS. 0 – Blanking mode; the device will wait 50μs before the battery switch is disabled and latched off (default) 1 – Hiccup mode; battery switch is disabled instantaneously, and the device will attempt to turn on the battery switch wait 250μs to check OCP and turn off every 100ms, up to 7 times before latching off.
0	R/W	VBUS_OVP_DLY	0	Sets VBUS fault deglitch time 0 – 4μs deglitch time (default) 1 – 20μs deglitch time

Name		Function	Addr	Reset
VBUS_OVP		VBUS_OVP	0x0A	0x34
Bit	**Mode**	**Name**	**Reset Value**	**Description**
[6:0]	R/W	VBUS_OVP<6:0>	0110100	VBUS_OVP Offset : 4.2V LSB<6:0> : 1600mV, 800mV, 400mV, 200mV, 100mV, 50mV, 25mV Range Min : 4.2V (0b0000000) Range Max : 6.5V (0b1011100) Default : 5.5V (0b0110100)

Name		Function	Addr	Reset
VOUT_REG		VOUT_REG	0x0B	0x14
Bit	**Mode**	**Name**	**Reset Value**	**Description**
[6:0]	R/W	VOUT_REG <6:0>	0010100	VOUT_Regulation (BAT – GND) Offset : 4.2V LSB<6:0> : 640mV, 320mV, 160mV, 80mV, 40mV, 20mV, 10mV Range Min : 4.2V (0b0000000) Range Max : 5.0V (0b1010000) Default : 4.4V (0b0010100)

Name		Function	Addr	Reset
VDROP_OVP		VDROP_OVP	0x0C	0x1E
Bit	**Mode**	**Name**	**Reset Value**	**Description**
[6:0]	R/W	VDROP_OVP<6:0>	0011110	VDROP_OVP Offset : 0V LSB<6:0> : 640mV, 320mV, 160mV, 80mV, 40mV, 20mV, 10mV Range Min : 0mV (0b0000000) Range Max : 1000mV (0b1100100) Default : 300mV (0b0011110)

Name		Function	Addr	Reset
VDROP_ALM		VDROP_ALM	0x0D	0x0A
Bit	**Mode**	**Name**	**Reset Value**	**Description**
[6:0]	R/W	VDROP_ALM<6:0>	0001010	VDROP_ALM Offset : 0V LSB<6:0> : 640mV, 320mV, 160mV, 80mV, 40mV, 20mV, 10mV Range Min : 0mV (0b0000000) Range Max : 1000mV (0b1100100) Default : 100mV (0b0001010)

Name		Function	Addr	Reset
VBAT_REG		VBAT_REG	0x0E	0x0A
Bit	**Mode**	**Name**	**Reset Value**	**Description**
[6:0]	R/W	VBAT_REG<6:0>	0001010	VBAT_Regulation (BATP – BATN) Offset : 4.2V LSB<6:0> : 640mV, 320mV, 160mV, 80mV, 40mV, 20mV, 10mV Range Min : 4.2V (0b0000000) Range Max : 5.0V (0b1010000) Default : 4.3V (0b0001010)

Name		Function	Addr	Reset
IBUS_OCP		IBUS_OCP	0x10	0x64
Bit	**Mode**	**Name**	**Reset Value**	**Description**
[6:0]	R/W	IBUS_OCP<6:0>	1100100	IBUS_OCP (Input Current Regulation) Offset : 0A LSB<6:0> : 3200mA, 1600mA, 800mA, 400mA, 200mA, 100mA, 50mA Range Min : 0.40A (0b0001000) Range Max : 6.35A (0b1111111) Default : 5A (0b1100100)

Name		Function	Addr	Reset
TBUS_OTP		TBUS_OTP	0x11	0x1E
Bit	**Mode**	**Name**	**Reset Value**	**Description**
[6:0]	R/W	TBUS_OTP<6:0>	0011110	TBUS_OTP Offset : 0V LSB<6:0> : 1280mV, 640mV, 320mV, 160mV, 80mV, 40mV, 20mV Range Min : 0V (0b0000000) Range Max : 2.4V (0b1111000) Default:0.6V (0b0011110) External VREF = 1.8V, 10K/10K Divide

Name		Function	Addr	Reset
TBAT_OTP		TBAT_OTP	0x12	0x23
Bit	**Mode**	**Name**	**Reset Value**	**Description**
[6:0]	R/W	TBAT_OTP<6:0>	0100011	TBAT_OTP Offset : 0V LSB<6:0> : 1280mV, 640mV, 320mV, 160mV, 80mV, 40mV, 20mV Range Min : 0V (0b0000000) Range Max : 2.4V (0b1111000) Default : 0.7V (0b0100011) External VREF = 1.8V, 10K/10K Divide

Name		Function	Addr	Reset
VBUS_ADC2		VBUS_ADC2	0x13	0x00
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R	VBUS_POL	0	Indicates polarity of VBUS 0 - Positive voltage 1 - Negative voltage
[4:0]	R	VBUS_ADC2<4:0>	00000	VBUS_ADC2 LSB : 1mV LSB<4:0> : 4096, 2048, 1024, 512, 256

Name		Function	Addr	Reset
VBUS_ADC1		VBUS_ADC1	0x14	0x00
Bit	**Mode**	**Name**	**Reset Value**	**Description**
[7:0]	R	VBUS_ADC1<7:0>	00000000	VBUS_ADC1 LSB : 1mV LSB<7:0> : 128, 64, 32, 16, 8, 4, 2, 1

Name		Function	Addr	Reset
IBUS_ADC2		IBUS_ADC2	0x15	0x00
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R	IBUS_POL	0	Indicates polarity of IBUS 0 - Positive current 1 - Negative current
[4:0]	R	IBUS_ADC2<4:0>	00000	IBUS_ADC2 LSB : 1mA LSB<4:0> : 4096, 2048, 1024, 512, 256

Name		Function	Addr	Reset
IBUS_ADC1		IBUS_ADC1	0x16	0x00
Bit	**Mode**	**Name**	**Reset Value**	**Description**
[7:0]	R	IBUS_ADC1<7:0>	00000000	IBUS_ADC1 LSB : 1mA LSB<7:0> : 128, 64, 32, 16, 8, 4, 2, 1

Name		Function	Addr	Reset
VOUT_ADC2		VOUT_ADC2	0x17	0x00
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R	VOUT_POL	0	Indicates polarity of VOUT 0 - Positive voltage 1 - Negative voltage
[4:0]	R	VOUT_ADC2<4:0>	00000	VOUT_ADC2 LSB : 1mV LSB<4:0> : 4096, 2048, 1024, 512, 256

Name		Function	Addr	Reset
VOUT_ADC1		VOUT_ADC1	0x18	0x00
Bit	**Mode**	**Name**	**Reset Value**	**Description**
[7:0]	R	VOUT_ADC1	00000000	VOUT_ADC1 LSB : 1mV LSB<7:0> : 128, 64, 32, 16, 8, 4, 2, 1

Name		Function	Addr	Reset
VDROP_ADC2		VDROP_ADC2	0x19	0x00
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R	VDROP_POL	0	Indicates polarity of VDROP 0 - Positive voltage 1 - Negative voltage
[1:0]	R	VDROP_ADC2<1:0>	00	VDROP_ADC2 LSB : 1mV LSB<1:0> : 512, 256

Name		Function	Addr	Reset
VDROP_ADC1		VDROP_ADC1	0x1A	0x00
Bit	**Mode**	**Name**	**Reset Value**	**Description**
[7:0]	R	VDROP_ADC1<7:0>	00000000	VDROP_ADC1 LSB : 1mV LSB<7:0> : 128, 64, 32, 16, 8, 4, 2, 1

Name		Function	Addr	Reset
VBAT_ADC2		VBAT_ADC2	0x1B	0x00
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R	VBAT_POL	0	Indicates polarity of VBAT 0 - Positive voltage 1 - Negative voltage
[4:0]	R	VBAT_ADC2<4:0>	00000	VBAT_ADC2 LSB : 1mV LSB<4:0> : 4096, 2048, 1024, 512, 256

Name		Function	Addr	Reset
VBAT_ADC1		VBAT_ADC1	0x1C	0x00
Bit	**Mode**	**Name**	**Reset Value**	**Description**
[7:0]	R	VBAT_ADC1<7:0>	00000000	VBAT_ADC1 LSB : 1mV LSB<7:0> : 128, 64, 32, 16, 8, 4, 2, 1

Name		Function	Addr	Reset
TBUS_ADC2		TBUS_ADC2	0x1F	0x03
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R	TBUS_POL	0	Indicates polarity of TBUS 0 - Positive voltage 1 - Negative voltage
[3:0]	R	TBUS_ADC2<3:0>	0011	TBUS_ADC2 LSB : 1mV LSB<3:0> : 2048, 1024, 512, 256

Name		Function	Addr	Reset
TBUS_ADC1		TBUS_ADC1	0x20	0x84
Bit	**Mode**	**Name**	**Reset Value**	**Description**
[7:0]	R	TBUS_ADC1<7:0>	10000100	TBUS_ADC1 LSB : 1mV LSB<7:0> : 128, 64, 32, 16, 8, 4, 2, 1

Name		Function	Addr	Reset
TBAT_ADC2		TBAT_ADC2	0x21	0x03
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R	TBAT_POL	0	Indicates polarity of TBAT 0 - Positive voltage 1 - Negative voltage
[3:0]	R	TBAT_ADC2<3:0>	0011	TBAT_ADC2 LSB : 1mV LSB<3:0> : 2048, 1024, 512, 256

Name		Function	Addr	Reset
TBAT_ADC1		TBAT_ADC1	0x22	0x84
Bit	**Mode**	**Name**	**Reset Value**	**Description**
[7:0]	R	TBAT_ADC1<7:0>	10000100	TBAT_ADC1 LSB : 1mV LSB<7:0> : 128, 64, 32, 16, 8, 4, 2, 1

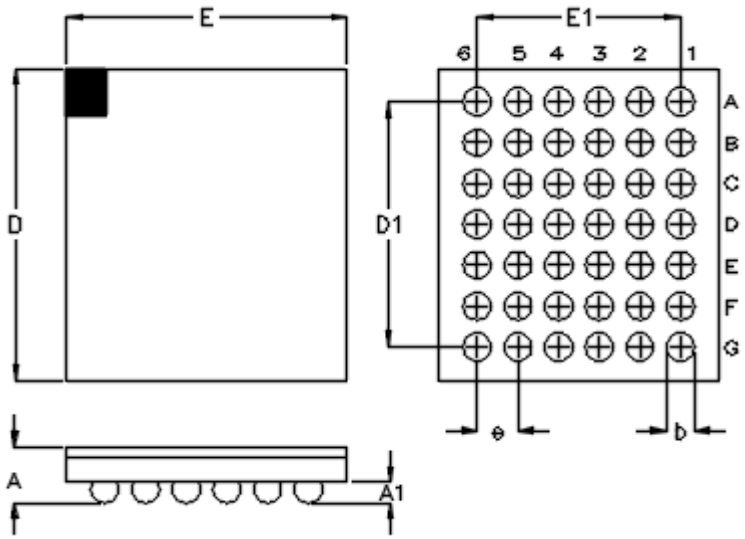
Name		Function	Addr	Reset
TDIE_ADC1		TDIE_ADC1	0x23	0x00
Bit	**Mode**	**Name**	**Reset Value**	**Description**
[7:0]	R	TDIE_ADC1<7:0>	00000000	TDIE_ADC1 LSB : 1°C LSB<7:0> : 128, 64, 32, 16, 8, 4, 2, 1

Name		Function	Addr	Reset
EVENT_STATUS_1		STATUS_1	0x24	0x00
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R	VBUS_OVP_STATUS	0	VBUS over-voltage fault. This bit is set when the VBUS voltage exceeds the limit set in VBUS_OVP register. 0 – no fault (default) 1 – VBUS OVP fault
6	R	IBUS_REG_STATUS	0	Indicates if in LDO mode due to IBUS regulation threshold. 0 – no fault (default) 1 – IBUS in regulation
5	R	VBAT_REG_STATUS	0	Indicates if in LDO mode due to VBAT regulation threshold. 0 – no in regulation (default) 1 – VBAT in regulation
4	R	Reserved	0	Reserved
3	R	VOUT_REG_STATUS	0	Indicates if in LDO mode due to VOUT regulation threshold. 0 – not in regulation (default) 1 – VOUT in regulation
2	R	TBUS_OTP_STATUS	0	"VBUS over-temperature fault. This bit is set when the TS_BUS voltage exceeds the limit set in TBUS_OTP register. 0 – no fault (default) 1 – VBUS over-temperature fault"
1	R	TBAT_OTP_STATUS	0	"BAT over-temperature fault. This bit is set when the TS_BAT voltage exceeds the limit set in TBAT_OTP register. 0 – no fault (default) 1 – BAT over-temperature fault"
0	R	IBUS_IREV_STATUS	0	"IBUS reverse current fault. This bit is set when current from BAT to VBUS is detected. The battery switch will be disabled when reverse current is detected. 0 – no fault (default) 1 – IBUS reverse current fault"

Name		Function	Addr	Reset
EVENT_STATUS_2		STATUS_2	0x25	0x00
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R	LOWCHG_ALM_STATUS	0	Indicates if LOWCHG_ALM threshold is reached. 0 – no LOWCHG_ALM (default) 1 – LOWCHG_ALM when CHG_EN and IBUS < threshold
6	R	ADC_DONE_STATUS	0	Indicates if the ADC conversion is complete for the requested parameters in 1-shot mode only (set from 0x07). 0 – Conversion not complete (default) 1 – Conversion complete
5	R	VDROP_ALM_STATUS	0	Indicates if VDROP_ALM threshold is reached. 0 – no fault (default) 1 – VDROP_ALM fault
4	R	VDROP_OVP_STATUS	0	Indicates if VDROP_OVP threshold is reached. 0 – no fault (default) 1 – VDROP_OVP fault
3	R	VBUS_INSERT_STATUS	0	Indicates if VBUS is detected 0 – no VBUS (default) 1 – VBUS inserted (VBUS > 2.8V)
2	R	BAT_INSERT_STATUS	0	Indicates if battery is detected (sensed between BATP and BATN). 0 – no BAT (default) 1 – BAT inserted (VBAT > 2.0V)
1	R	TSHUT_STATUS	0	IC thermal shutdown fault indicator. (TDIE > 125°C) 0 – Normal operation (default) 1 – Thermal shutdown
0	R	IOC_STATUS	0	Indicates if high current from VBUS to VOUT has hit the internal threshold. 0 – no fault (default) 1 – High current fault

Name		Function	Addr	Reset
Control		Control	0x26	0x01
Bit	**Mode**	**Name**	**Reset Value**	**Description**
[3:0]	R/W	IREV_OCP	0001	IREV_OCP (Ron = 10mΩ) Offset : 0A LSB<3:0> : 4A (40mV), 2A (20mV), 1A (10mV), 0.5A (5mV) Range Min : 0A (0b0000) Range Max : 4A (0b1000) Default : 500Ma (0b0001)

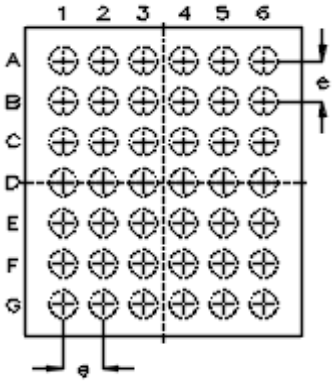
Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.500	0.600	0.020	0.024
A1	0.170	0.230	0.007	0.009
b	0.240	0.300	0.009	0.012
D	3.010	3.090	0.119	0.122
D1	2.400		0.094	
E	2.710	2.790	0.107	0.110
E1	2.000		0.079	
e	0.400		0.016	

42B WL-CSP 2.75x3.05 Package (BSC)

Footprint Information



Package	Number of Pin	Type	Footprint Dimension (mm)			Tolerance
			e	A	B	
WL-CSP2.75*3.05-42(BSC)	42	NSMD	0.400	0.240	0.340	±0.025
		SMD		0.270	0.240	

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