18W AccuSwitch™ Quasi-Resonant PWM Controller with Integrated 800V Power BJT

1 Description

The iW1819 integrates a high performance AC/DC power supply controller using digital control technology and a power BJT switch in one package to enable compact peak current mode PWM flyback power supplies. The device operates in quasi-resonant mode and features multiple key protection features, allowing designs with improved efficiency and lower EMI, while lowering the bill of material cost.

The iW1819 features a distinctive soft-start scheme, which allows for fast and yet smooth start-up with both small and large capacitive loads. It removes the need for a secondary feedback circuit while achieving excellent line and load regulation. It also eliminates the need for loop compensation components while maintaining stability across all operating conditions. The pulse-by-pulse waveform analysis allows for fast dynamic load response. The built-in power limit function enables optimized transformer design for a wide input voltage range.

Dialog's innovative, proprietary technology ensures that power supplies built with the iW1819 can achieve both the highest average efficiency and less than 30mW no-load power consumption. And, the iW1819 can start-up into a wide range of capacitive loads at 5V to 12V or higher output voltages, making it ideal for networking, set-top box and home appliance power supply applications.

2 Features

- Optimized for 12V/1.5A AC/DC adapters with < 30mW no-load power consumption at $230V_{AC}$ and fast dynamic response
- ***AccuSwitch™*** technology − integrated 800V bipolar junction transistor (BJT)
- Adaptively controlled soft-start enables fast and smooth start-up for a wide range of capacitive loads (from 330µF to 6,000µF)
- Very tight constant voltage and constant current regulation over entire operating range
- ***PrimAccurate™*** primary-side feedback eliminates optocoupler and simplifies design
- ***EZ-EMI™*** design enhances manufacturability
- Intrinsically low common mode noise
- Optimized 72kHz maximum PWM switching frequency achieves best size and efficiency
- Adaptive multi-mode PWM/PFM control improves efficiency
- Quasi-resonant operation for highest overall efficiency
- Dynamic base current control
- No external loop compensation components required
- Built-in single-point protections against output short-circuit, output low impedance, and output overvoltage
- Built-in over-temperature protection (OTP)
- No audible noise over entire operating range

3 Applications

- Network power adapters for ADSL, wireless access
- AC/DC adaptor for set top box
- AC/DC power supplies for home appliances and industrial applications

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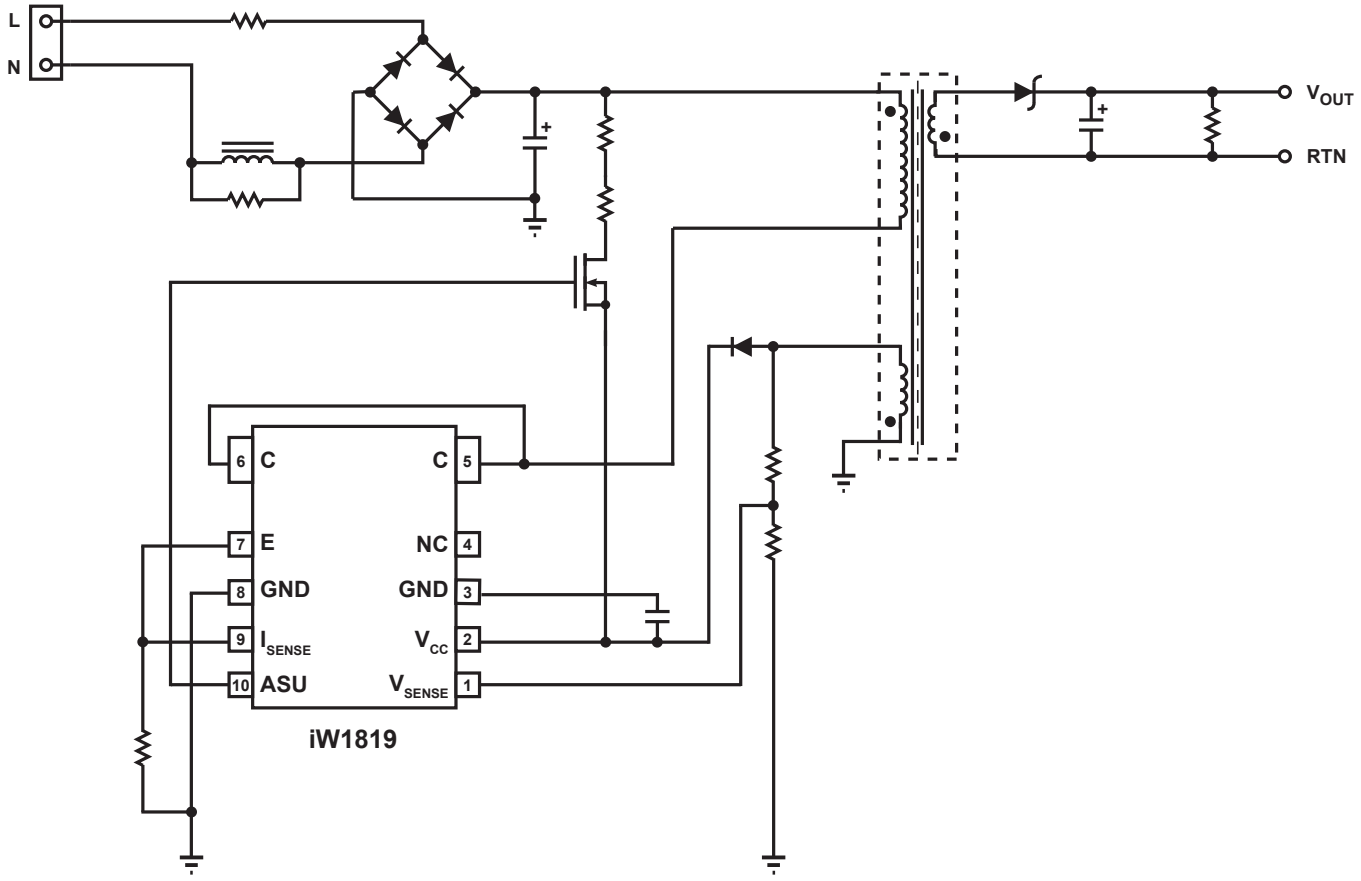


Figure 3.1 : iW1819 Typical Application Circuit

WARNING:

The iW1819 is intended for high voltage AC/DC offline applications. Contact with live high voltage offline circuits or improper use of components may cause lethal or life threatening injuries or property damage. Only qualified professionals with safety training and proper precaution should operate with high voltage offline circuits.

iW1819 Output Power Table at Universal Input ($85V_{AC}$–$264V_{AC}$)

Condition	Open Frame[1]
Output Power (W)[2]	18

Notes:

Note 1. Maximum practical continuous output power measured at open frame ambient temperature of 50°C while minimum bulk capacitor voltage is kept above 90V (test unit is placed in a non-ventilated environment).

Note 2. The output power can vary depending on the power supply system designs and operating conditions.

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4 Pinout Description

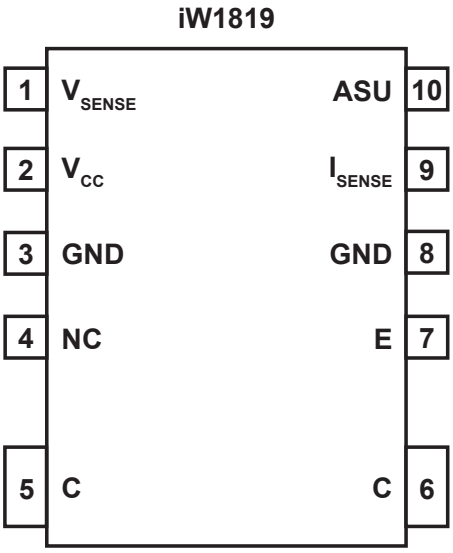


Figure 4.1 : 10-Lead SOIC Batwing Package

Pin Number	Pin Name	Type	Pin Description
1	V_{SENSE}	Analog Input	Auxiliary voltage sense (used for primary-side regulation).
2	V_{CC}	Power Input	Power supply for control logic.
3	GND	Ground	Ground.
4	NC		This pin must be left floating.
5	C	BJT Collector	Collector of internal BJT.
6	C	BJT Collector	Collector of internal BJT.
7	E	BJT Emitter	Emitter of internal BJT.
8	GND	Ground	Ground.
9	I_{SENSE}	Analog Input	Primary current sense. Used for cycle-by-cycle peak current control and current limit.
10	ASU	Output	Control signal. Used for active start-up device.

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5 Absolute Maximum Ratings

Absolute maximum ratings are the parameter values or ranges which can cause permanent damage if exceeded.

Parameter	Symbol	Value	Units
DC supply voltage range (pin 2, I_{CC} = 20mA max)	V_{CC}	-0.3 to 25.0	V
Continuous DC supply current at V_{CC} pin (V_{CC} = 15V)	I_{CC}	25	mA
ASU output (pin 10)		-0.3 to 19.0	V
V_{SENSE} input (pin 1, I_{VSENSE} ≤ 10mA)		-0.7 to 4.0	V
I_{SENSE} input (pin 9)		-0.3 to 4.0	V
Collector-Base breakdown voltage	V_{CBO}	800	V
Collector-Emitter breakdown voltage	V_{CES}	800	V
Collector current (Note 1)	I_C	4	A
Collector peak current (Note 1) (t_p < 1ms)	I_{CM}	8	A
Maximum junction temperature	T_{JMAX}	150	°C
Operating junction temperature	T_{JOPT}	-40 to 150	°C
Storage temperature	T_{STG}	-55 to 150	°C
Electrostatic Discharge Capability (Human Body Model), JEDEC JS-001-2017	$ESD_{(HBM)}$	±2000	V
Electrostatic Discharge Capability (Charged Device Model), JS-002-2014	$ESD_{(CDM)}$	±1000	V
Latch-up test per JESD78E		±100	mA

Notes:

Note 1. Limited by maximum junction temperature.

6 Thermal Characteristics

Parameter	Symbol	Value	Units
Thermal Resistance Junction-to-Ambient[1]	θ_{JA}	55.2	°C/W
Characterization Parameter Junction-to-Collector pin (pin 5 and pin 6)[2]	$\Psi_{J\text{-}COLLECTOR}$	5.8	°C/W
Thermal Shutdown Threshold[3]	T_{SD}	150	°C
Thermal Shutdown Recovery[3]	$T_{SD\text{-}R}$	100	°C
Thermal Shutdown Recovery[3] (iW1819-11)	$T_{SD\text{-}R}$	120	°C

Notes:

Note 1. Device is mounted on a 4-layer JEDEC board with 100mm² of 70µm thick copper, in a one-cubic-foot natural convection chamber.

Note 2. $\Psi_{J\text{-}COLLECTOR}$ [Psi Junction to Collector pin] provides an estimation of the die junction temperature relative to the Collector pin [internal BJT Collector] surface temperature.

Note 3. These parameters are typical and they are guaranteed by design.

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7 Electrical Characteristics

V_{CC} = 12V, -40°C ≤ T_A ≤ 85°C, unless otherwise specified (Note 1)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
V_{SENSE} SECTION (Pin 1)						
Input leakage current	I_{BVS}	V_{SENSE} = 2V			1	µA
Nominal voltage threshold	$V_{SENSE(NOM)}$	T_A = 25°C, negative edge	1.521	1.536	1.551	V
V_{SENSE}-based output OVP threshold	$V_{SENSE(MAX)}$	T_A = 25°C, negative edge		1.838		V
I_{SENSE} SECTION (Pin 9)						
Switching-cycle over-current threshold	V_{OCP}		1.11	1.15	1.19	V
I_{SENSE} regulation upper limit (Note 1)	$V_{IPK(HIGH)}$			1.00		V
I_{SENSE} regulation lower limit (Note 1)	$V_{IPK(LOW)}$			0.23		V
Input leakage current	I_{LK}	I_{SENSE} = 1.0V			1	µA
V_{CC} SECTION (Pin 2)						
Operating voltage (Note 1)	V_{CC}				20	V
Start-up threshold	$V_{CC(ST)}$	V_{CC} rising	13.5	14.5	15.5	V
Under-voltage lockout threshold	$V_{CC(UVL)}$	V_{CC} falling	4.1	4.4	4.7	V
Start-up current	$I_{IN(ST)}$	V_{CC} = 13V		1.6		µA
Quiescent current	I_{CCQ}	V_{CC} = 14V, without driver switching		2.7	4.0	mA
No-load operating current (Note 1)	I_{CC_NL}	No-load operation in DDPWM mode		0.25		mA
BJT SECTION (Pin 5, 6 and 7)						
Collector-base cutoff current	I_{CBO}	V_{CB} = 800V, I_E = 0A			0.1	mA
Collector-emitter cutoff current	I_{CEO}	V_{CE} = 450V, R_{EB} = 0Ω			0.1	mA
Emitter-base cutoff current	I_{EBO}	V_{EB} = 9V, I_C = 0A			0.1	mA
Collector-base breakdown voltage	V_{CBO}	I_C = 0.1mA	800			V
Collector-emitter breakdown voltage (Emitter and base shorted together)	V_{CES}	I_C = 1mA, R_{EB} = 0Ω	800			V
Collector-emitter breakdown voltage	V_{CEO}	I_C = 1mA	450			V
DC current gain (Note 2)	h_{EF}	V_{CE} = 5V, I_C = 1.0A	25		35	
Collector-emitter saturation voltage (Note 2)	$V_{CE(SAT)}$	I_C = 2A, I_B = 0.5A		0.35	1.0	V
Maximum switching frequency at PWM mode (Note 1) (Note 3)	f_{SW}	> 50% load		72		kHz

Notes:

Note 1: These parameters are not 100% tested. They are guaranteed by design and characterization.

Note 2: Operating frequency varies based on the load conditions, see Section 10.6 for more details.

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8 Typical Performance Characteristics

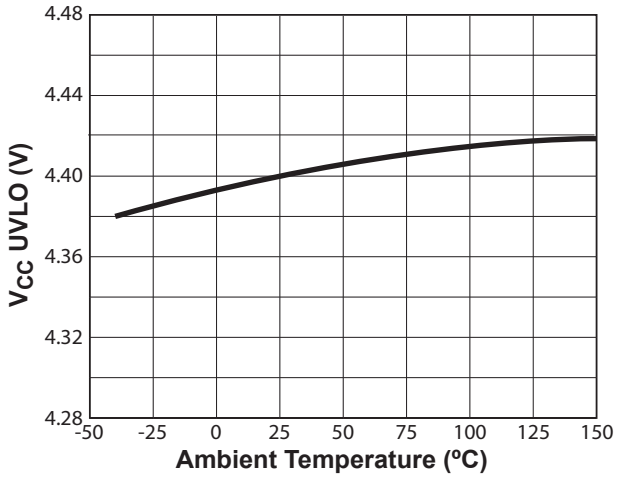


Figure 8.1 : V_{CC} UVLO vs. Temperature

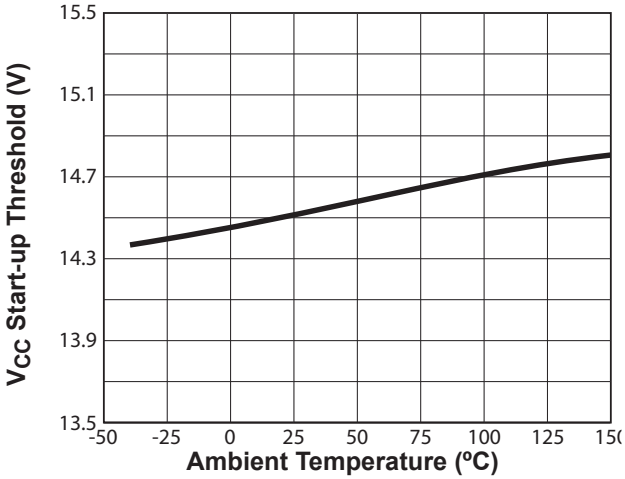


Figure 8.2 : V_{CC} Start-up Threshold vs. Temperature

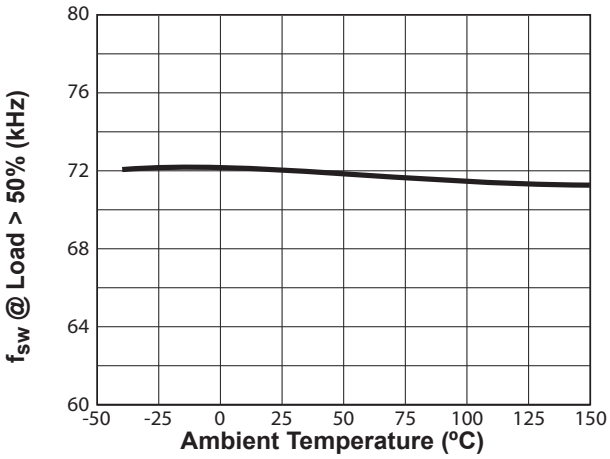


Figure 8.3 : Switching Frequency vs. Temperature[1]

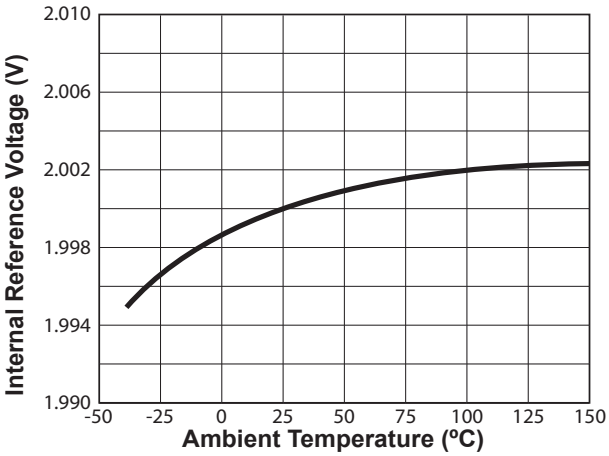


Figure 8.5 : Internal Reference Voltage vs. Temperature

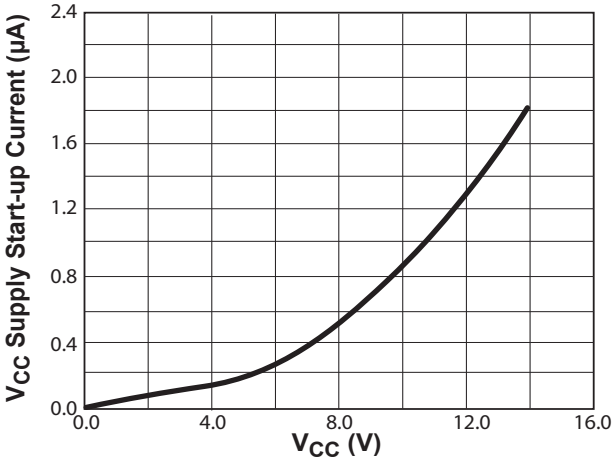


Figure 8.4 : V_{CC} Supply Start-up Current vs. V_{CC}

Notes:

Note 1. Operating frequency varies based on the load conditions, see Section 10.6 for more details.

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9 Functional Block Diagram

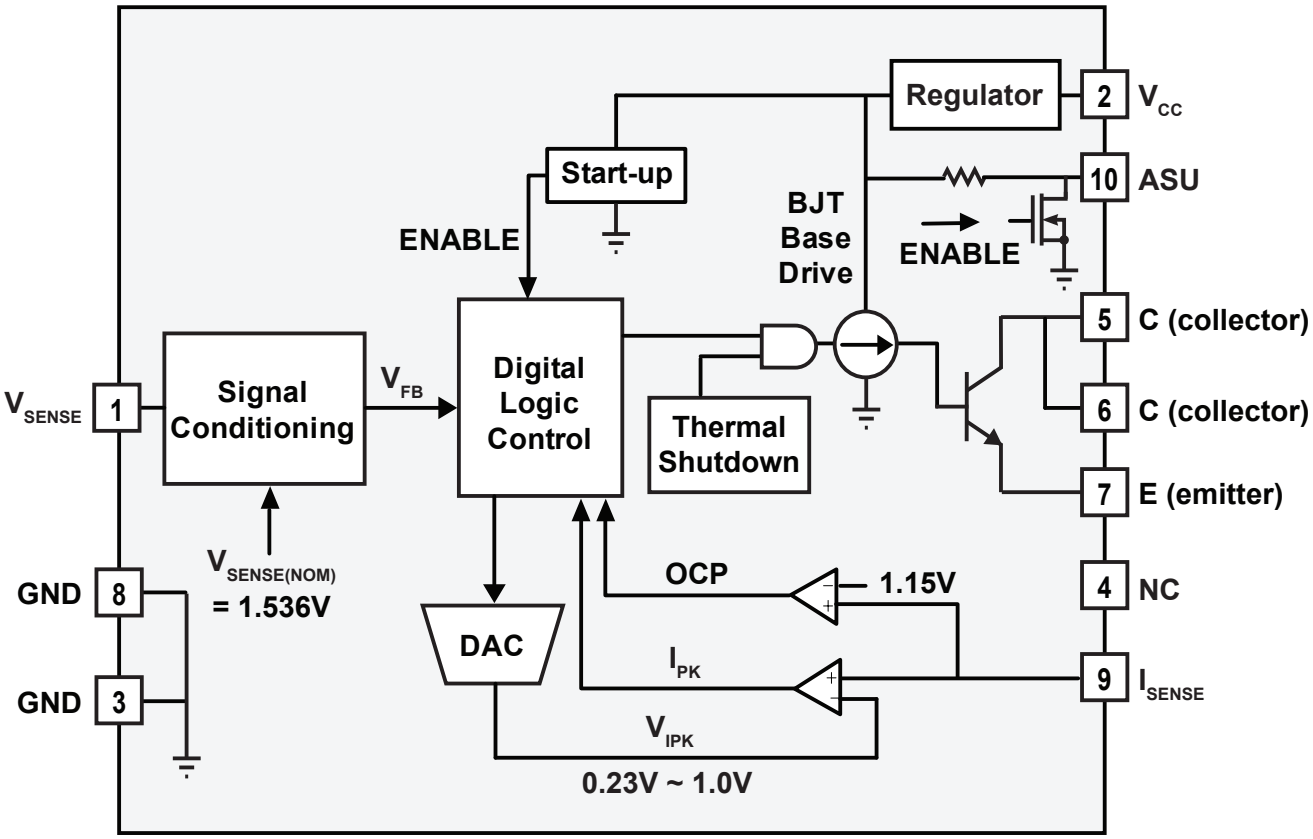


Figure 9.1 : iW1819 Functional Block Diagram

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10 Theory of Operation

The iW1819 is a digital controller integrated with a power BJT. It uses a proprietary primary-side control technology to eliminate the opto-isolated feedback and secondary regulation circuits required in traditional designs. This results in a low-cost solution for low-power AC/DC adapters. The core PWM processor uses fixed-frequency discontinuous conduction mode (DCM) operation at higher power levels and switches to variable frequency operation at light loads to maximize efficiency. Furthermore, Dialog's digital control technology enables fast dynamic response, tight output regulation, and full-featured circuit protection with primary-side control.

Figure 9.1 shows that the iW1819 operates in peak current mode control. The digital logic control block generates the switching on-time and off-time information based on the output voltage and current feedback signal and provides commands to dynamically control the internal BJT base current. The I_{SENSE} is an analog input configured to sense the primary current in a voltage form. To achieve the peak current mode control and cycle-by-cycle current limit, the V_{IPK} sets the threshold for the I_{SENSE} to compare with, and it varies in the range of 0.23V (typical) and 1.00V (typical) under different line and load conditions. The system loop is automatically compensated internally by a digital error amplifier. Adequate system phase margin and gain margin are guaranteed by design and no external analog components are required for loop compensation. The iW1819 uses an advanced digital control algorithm to reduce system design time and increase reliability.

Accurate secondary constant-current operation is achieved without the need for any secondary-side sense and control circuits.

The iW1819 uses adaptive multi-mode PWM/PFM control to dynamically change the BJT switching frequency for efficiency, EMI, and power consumption optimization. In addition, it achieves unique BJT quasi-resonant switching to further improve efficiency and reduce EMI. Built-in single-point fault protection features include overvoltage protection (OVP), output short-circuit protection (SCP), over-current protection (OCP), I_{SENSE} fault detection, and OTP. In particular, it ensures that power supplies built with the iW1819 are best suited for power adaptor applications such as networking devices and set-top boxes that have large input capacitance.

Dialog's digital control scheme is specifically designed to address the challenges and trade-offs of power conversion design. This innovative technology is ideal for balancing new regulatory requirements for green-mode operation with more practical design considerations such as lowest possible cost, smallest size, and high performance output control.

10.1 Pin Detail

Pin 1 – V_{SENSE}

Auxiliary voltage sense. Used for primary side regulation.

Pin 2 – V_{CC}

IC power supply.

Pin 3 and Pin 8 – GND

Ground.

Pin 4 – NC

NC

Pin 5 and Pin 6 – C

Collector pins of the internal BJT.

Pin 7 – E

Emitter pin of the internal power BJT. This pin must be shorted to pin 9 (the I_{SENSE} pin).

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Pin 9 – I_{SENSE}
Primary current sense. Used for cycle-by-cycle peak current control and limit (pin 7 and pin 9 must be shorted externally on the PCB).

Pin 10 – ASU
Control signal. Used for active start-up device (BJT or depletion mode NFET).

10.2 Start-up and Adaptively Controlled Soft-start

The iW1819 features an innovative proprietary soft-start scheme to achieve fast yet smooth build-up of output voltage with a wide range of output loads, including capacitive loads typically from 330µF to 6,000µF. Prior to start-up, the ENABLE signal is low, when the V_{CC} capacitor is charged to a voltag higher than the start-up threshold $V_{CC(ST)}$, the ENABLE signal becomes active and the iW1819 begins to perform initial OTP check (See Section 10.14). The iW1819 then commences a soft-start function. During the start-up process, the peak current is limited cycle by cycle by the I_{PEAK} comparator. The whole soft-start process can be broken down into several stages based on the output voltage levels, which is indirectly sensed by the V_{SENSE} signal at the primary side. At different stages, the iW1819 adaptively controls the switching frequency and primary-side peak current so that the output voltage can always build up very fast at the early stages and smoothly transition into the desired regulation voltage at the final stage, regardless of any capacitive and resistive loads that the applications may incur. With a minimum system cost, this adaptively controlled soft-start feature makes the iW1819 ideal in network power adapter applications such as wireless routers in which the adapter needs to drive large capacitive loads with output voltage of 12V and above.

If at any time the V_{CC} voltage drops below the under-voltage lockout (UVLO) threshold $V_{CC(UVL)}$, then the iW1819 shuts down. At this time the ENABLE signal becomes low.

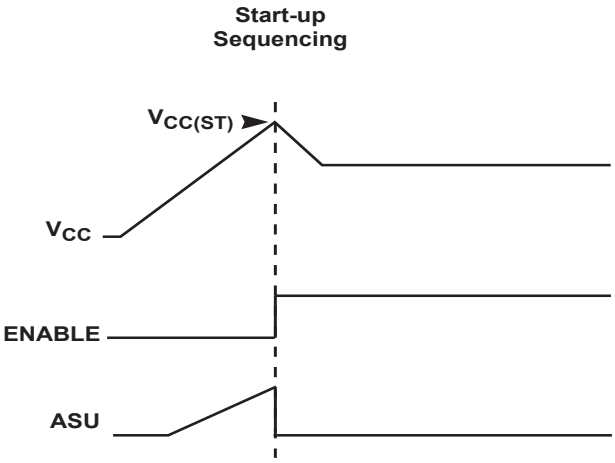


Figure 10.1 : Start-up Sequencing Diagram

10.3 Understanding Primary Feedback

Figure 10.2 illustrates a simplified flyback converter. When the switch Q1 conducts during $t_{ON}(t)$, the current $i_g(t)$ is directly drawn from rectified $v_g(t)$. The energy $E_g(t)$ is stored in the magnetizing inductance L_M. The rectifying diode D1 is reversely-biased and the load current I_O is supplied by the secondary capacitor C_O. When Q1 turns off, D1 conducts and the stored energy $E_g(t)$ is delivered to the output.

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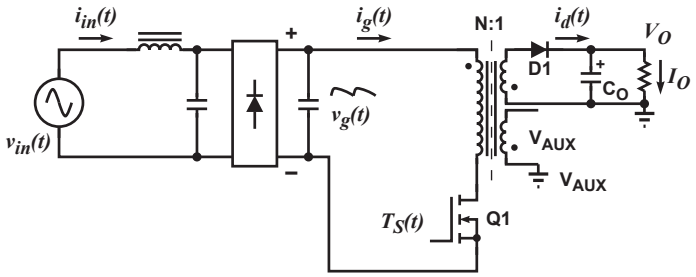


Figure 10.2 : Simplified Flyback Converter

In order to tightly regulate the output voltage, the information about the output voltage and load current must be accurately sensed. In the DCM flyback converter, this information can be read via the auxiliary winding or the primary magnetizing inductance (L_M). During the Q1 on-time, the load current is supplied from the output filter capacitor C_O. The voltage across L_M is $v_g(t)$, assuming the voltage dropped across Q1 is zero. The current in Q1 ramps up linearly at a rate of:

$$\frac{di_g(t)}{dt} = \frac{v_g(t)}{L_M} \qquad (10.1)$$

At the end of on-time, the current has ramped up to:

$$i_{g_peak}(t) = \frac{v_g(t) \times t_{ON}}{L_M} \qquad (10.2)$$

This current represents a stored energy of

$$E_g = \frac{L_M}{2} \times i_{g_peak}(t)^2 \qquad (10.3)$$

When Q1 turns off at t_O, $i_g(t)$ in L_M forces a reversal of polarities on all windings. Ignoring the commutation time caused by the leakage inductance L_K at the instant of turn-off t_O, the primary current transfers to the secondary at a peak amplitude of:

$$i_d(t) = \frac{N_P}{N_S} \times i_{g_peak}(t) \qquad (10.4)$$

Assuming the secondary winding is master, and the auxiliary winding is slave,

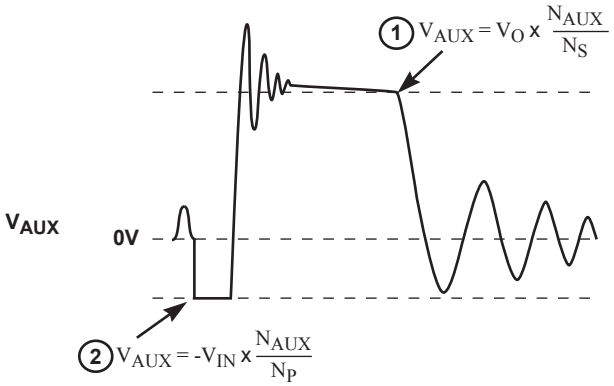


Figure 10.3 : Auxiliary Voltage Waveforms

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The auxiliary voltage is given by:

$$V_{AUX} = \frac{N_{AUX}}{N_S}(V_O + \Delta V) \qquad (10.5)$$

and reflects the output voltage as shown in Figure 10.3.

The voltage at the load differs from the secondary voltage by a diode drop and IR losses. Thus, if the secondary voltage is always read at a constant secondary current, the difference between the output voltage and the secondary voltage is a fixed ΔV. Furthermore, if the voltage can be read when the secondary current is small, ΔV is also small. With the iW1819, ΔV can be ignored.

The real-time waveform analyzer in the iW1819 reads this information cycle by cycle. The device then generates a feedback voltage V_{FB}. The V_{FB} signal precisely represents the output voltage under most conditions and is used to regulate the output voltage.

10.4 Constant Voltage Operation

After soft-start has been completed, the digital control block measures the output conditions. It determines output power levels and adjusts the control system according to a light load or heavy load. If this is in the normal range, the device operates in the Constant Voltage (CV) mode, and changes the pulse width (t_{ON}) and off time (t_{OFF}) in order to meet the output voltage regulation requirements.

If no voltage is detected on V_{SENSE} it is assumed that the auxiliary winding of the transformer is either open or shorted and the iW1819 shuts down.

10.5 Current Limit

At overload condition, the iW1819 enters constant current (CC) mode to limit the output current on a cycle-by-cycle basis. During this mode of operation the iW1819 regulates the output current at a constant level regardless of the output voltage, while avoiding the continuous conduction mode. In case of very heavy loading, when the output voltage is low enough, the iW1819 shuts down.

To achieve this regulation the iW1819 senses the load current indirectly through the primary current, which is detected by the I_{SENSE} pin through a resistor from the BJT emitter to ground.

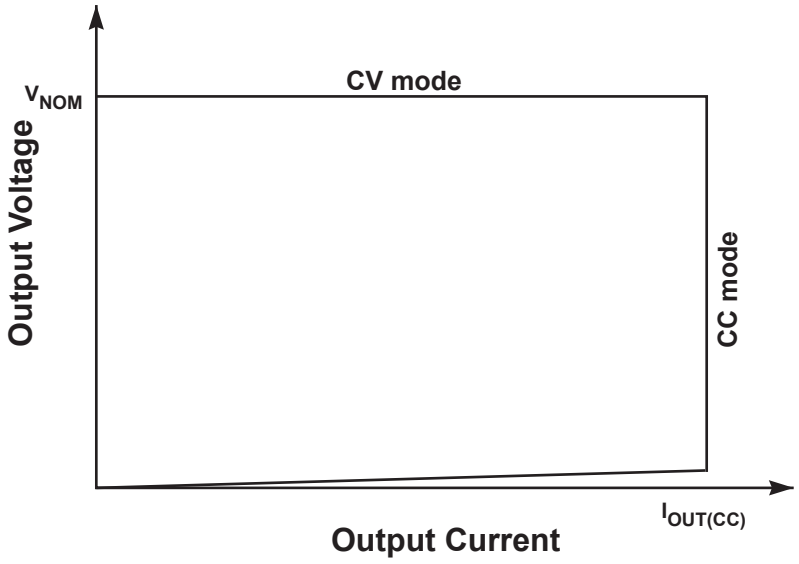


Figure 10.4 : Power Envelope

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10.6 Multi-Mode PWM/PFM Control and Quasi-Resonant Switching

The iW1819 uses a proprietary adaptive multi-mode PWM/PFM control to dramatically improve the light-load efficiency and the overall average efficiency.

During the constant voltage (CV) operation, the iW1819 normally operates in a pulse-width-modulation (PWM) mode in heavy load conditions. In the PWM mode, the switching frequency keeps around constant. As the output load I_{OUT} is reduced, the on-time t_{ON} is decreased, and the controller adaptively transitions to a pulse-frequency-modulation (PFM) mode. In the PFM mode, the BJT is turned on for a set duration under a given instantly-rectified AC input voltage, but its off-time is modulated by the load current. With a decreasing load current, the off-time increases and thus the switching frequency decreases.

When the switching frequency approaches the human ear audio band, the iW1819 transitions to a second level of PWM mode, namely deep PWM mode (DPWM). During the DPWM mode, the switching frequency keeps around 25kHz to avoid audible noise. As the load current is further reduced, the iW1819 transitions to a second level of PFM mode, namely deep PFM mode (DPFM), which can reduce the switching frequency to a low level. Although the switching frequency drops across the audible frequency range during the DPFM mode, the output current in the power converter has reduced to an insignificant level in the DPWM mode before transitioning to the DPFM mode. The power converter produces no audible noise, while achieving high efficiency across varying load conditions.

As the load current reduces to low or no-load condition, the iW1819 transitions from the DPFM to the third level of PWM mode, namely deep-deep PWM mode (DDPWM), where the switching frequency is fixed at around 2.1kHz.

The iW1819 also incorporates a unique proprietary quasi-resonant switching scheme that achieves valley-mode turn on for every PWM/PFM switching cycle, during all PFM and PWM modes and in both CV and CC operations. This unique feature greatly reduces the switching loss and dv/dt across the entire operating range of the power supply. Due to the nature of quasi-resonant switching, the switching frequency can vary slightly cycle by cycle, providing the additional benefit of reducing EMI. Together these innovative digital control architecture and algorithms enable the iW1819 to achieve highest overall efficiency and lowest EMI, without causing audible noise over entire operating range.

10.7 Less Than 30mW No-Load Power with Fast Load Transient Response

The iW1819 features the distinctive DDPWM control at no-load conditions to help achieve super-low no-load power consumption (< 30mW for typical applications) and meanwhile to ensure fast dynamic load response. The power supply system designs including the pre-load resistor selection should ensure the power supply can stably operate in the DDPWM mode at the steady-state no-load condition. If the pre-load resistor is too small, the no-load power consumption increases; on the other hand, if it is too large, the output voltage may increase and even cause overvoltage since the switching frequency is fixed at around 2.1kHz. For typical designs, the pre-load resistor is in the range of 5kΩ to 10kΩ.

Aside from the appropriate use of pre-load resistor, the iW1819 enjoys a few other features to bring down no-load power consumption as well. First, the iW1819 implements an intelligent low-power management technique that achieves ultra-low chip operating current at no-load (typically around 250µA). Second, the use of a BJT power switch instead of a MOSFET requires a lower driving voltage, enabling a low UVLO threshold (typically 4.4V). The power supply system design can fully use this low UVLO feature to have a low V_{CC} voltage at the no-load operation in order to minimize the no-load power. All together these features ensure the lowest system cost power supplies built with the iW1819 can achieve less than 30mW no-load power consumption at 230V_{AC} input and very tight constant voltage and constant current regulation over the entire operating range including the no-load operation.

While achieving super-low no-load power consumption, the iW1819 implements innovative proprietary digital control technology to intelligently detect any load transient events, and achieve fast dynamic load response for both one-time and repetitive load transients. In particular, for load transients that are demanded in some applications as from absolutely no load to full load, the iW1819 can still guarantee a fast enough response to meet the most stringent requirements, with the no-load operating frequency designed at around 2.1kHz.

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10.8 Variable Frequency Operation Mode

In each of the switching cycles, the falling edge of V_{SENSE} is checked. If the falling edge of V_{SENSE} is not detected, the off-time is extended until the falling edge of V_{SENSE} is detected. The maximum allowed transformer reset time is 110µs. When the transformer reset time reaches 110µs, the iW1819 shuts off.

10.9 Internal Loop Compensation

The iW1819 incorporates an internal Digital Error Amplifier with no requirement for external loop compensation. For a typical power supply design, the loop stability is guaranteed to provide at least 45 degrees of phase margin and -20dB of gain margin.

10.10 Voltage Protection Features

The secondary maximum output DC voltage is limited by the iW1819. When the V_{SENSE} signal exceeds the output OVP threshold at point 1 indicated in Figure 10.3, the iW1819 shuts down.

Although there is no pin available to directly sense the input voltage, the iW1819 uses an innovative proprietary digital control method to detect and analyze the switch ON time, which provides real-time indirect sensing and monitoring of the magnitude and shape of the DC bulk capacitor voltage. This enables the iW1819 to determine and distinguish various conditions of the AC input voltage such as brown-out, brown-in and unplug, and to take appropriate actions. When the AC input voltage drops to below normal operation range and the power supply input is still connected to the AC source, the iW1819 initiates brown-out protection and shuts down the power supply adaptively according to the power supply load condition. Meanwhile, a brown-in input voltage threshold is set with hysteresis. In the case of the power supply input being unplugged or disconnected from the AC source, the iW1819 continues to control the switching actions to discharge the DC bulk capacitor voltage to a safe level before shutting down the power supply. Also, the iW1819 monitors the voltage on the V_{CC} pin and when the voltage on this pin is below UVLO threshold the IC shuts down immediately.

When any of these faults are met the IC remains biased to discharge the V_{CC} supply. Once V_{CC} drops below UVLO threshold, the controller resets itself and then initiates a new soft-start cycle. The controller continues attempting start up until the fault condition is removed.

10.11 PCL, OCP and SRS Protection

Peak-current limit (PCL), (OCP), and sense-resistor short protection (SRSP) are features built-in to the iW1819. With the I_{SENSE} pin the iW1819 is able to monitor the peak primary current. This allows for cycle-by-cycle peak current control and limit. When the primary peak current multiplied by the I_{SENSE} resistor is greater than 1.15V, over current (OCP) is detected and the IC immediately turns off the base driver until the next cycle. The output driver sends out a switching pulse in the next cycle, and the switching pulse continues if the OCP threshold is not reached; or, the switching pulse turns off again if the OCP threshold is reached. If the OCP occurs for several consecutive switching cycles, the iW1819 shuts down.

If the I_{SENSE} resistor is shorted, a potential danger of the over current condition not being detected exists. Thus, the IC is designed to detect this sense-resistor-short fault during startup and shut down immediately. The V_{CC} is discharged since the IC remains biased. Once V_{CC} drops below the UVLO threshold, the controller resets itself and then initiates a new soft-start cycle. The controller continues attempting to start up, but does not fully start up until the fault condition is removed.

10.12 Dynamic Base Current Control

One important feature of the iW1819 is that it directly drives a BJT switching device with dynamic base current control to optimize performance. The iW1819 is optimized for 18W. AC/DC adapters/chargers. The BJT base current ranges from 16mA to 50mA, and is dynamically controlled according to the power supply load change. The higher the output power, the higher the base current. Specifically, the base current is related to V_{IPK}.

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10.13 Cable Drop Compensation

The iW1819 incorporates an innovative method to compensate for any IR drop in the secondary circuit including cable and cable connector. A 18W adapter with 12V DC output has 2.5% deviation at 1.5A load current due to the drop across a 24 AWG, 1.8 meter DC cable without cable compensation. The iW1819 compensates for this voltage drop by providing a voltage offset to the feedback signal based on the amount of load current detected.

The “cable comp” specified in the table in Section 12 refers to the voltage increment at PCB end from no-load to fullload conditions in the CV mode, with the assumption that the secondary diode voltage drop can be ignored at the point when the secondary voltage is sensed. Also, the “cable comp” is specified based on the nominal output voltage of 5V. For different output voltage, the actual voltage increment must be scaled accordingly. For example, for 12V output, the corresponding cable comp will be: 0mV for the iW1819-00 and 360mV for the iW1819-01 and iW1819-11.

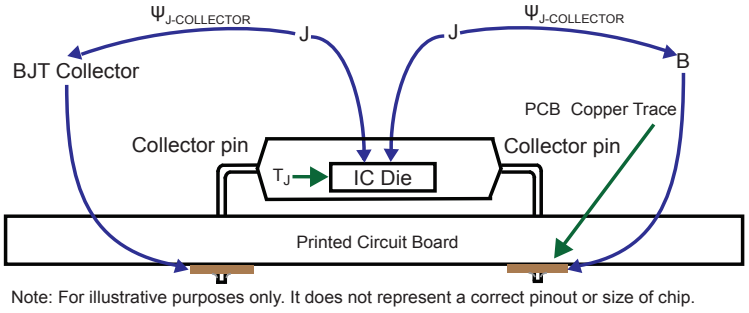
To calculate the amount of cable compensation needed, take the resistance of the cable and connector and multiply by the maximum output current.

10.14 Internal OTP

The iW1819 features an internal OTP that shuts down the device if the internal die junction temperature reaches above T_{SD}. The device is kept off until the junction temperature drops below T_{SD-R}, when the device initiates a new soft-start process to build up the output voltage.

10.15 Thermal Design

The iW1819 may be installed inside a small enclosure, where space and air volumes are constrained. Under these circumstances θ_{JA} (thermal resistance, junction-to-ambient) measurements do not provide useful information for this type of application. Hence we have also provided $\Psi_{J\text{-}COLLECTOR}$ which estimates the increase in die junction temperature relative to the PCB surface temperature. Figure 10.5 shows the PCB surface temperature is measured at the IC’s GND pin pad.



Note: For illustrative purposes only. It does not represent a correct pinout or size of chip.

Figure 10.5 : Thermal Resistance

The actual IC power dissipation is related to the power supply application circuit, component selection and operation conditions. The maximum IC power dissipation should be used to estimate the maximum junction temperature. For a typical 18W power supply, the power dissipation can be around 0.9W.

The output power table in Section 3.0 recommends maximum practical continuous output power level be achieved under the following conditions:

- Typical 12V-output power supply designs with a Schottky rectifier diode
- Ambient temperature of 50°C for open frame in a non-ventilated environment
- AC Input voltage is $85V_{AC}$ at 47Hz
- Minimum bulk capacitor voltage is 90V for open frame

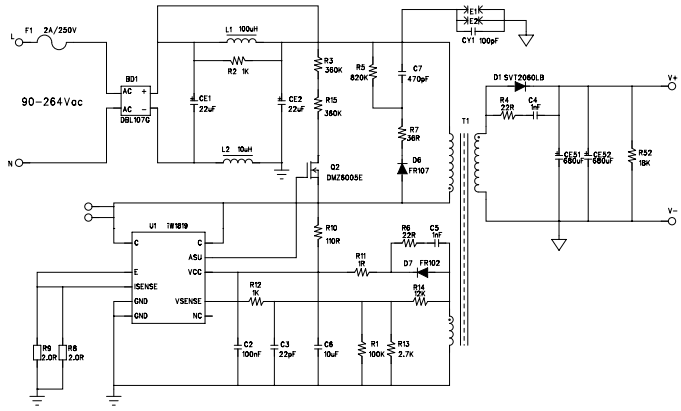
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- The iW1819 device is mounted on PCB with no special enhancement for heatsinking and the package/pin temperature is kept below 90°C

Under a given power dissipation, reducing the GND, emitter, and collector pin temperature reduces the junction temperature. Generally, increasing the PCB area and associated amount of copper trace reduces the junction temperature. In particular, the power BJT is a power source and therefore the PCB plating area attached to the two collector pins and the emitter pin can be reasonably large to gain the thermal benefits without violating the high voltage creepage requirements if higher output power is desired. Higher output power is also achievable if bulk capacitor voltage is higher, design is for high line only, design components temperature restriction limit is higher, ambient temperature is lower, or extra metal piece/heat spreader is attached to related pins or package.

10.16 PCB Layout

Careful considerations need to be taken when designing a PCB for use with the iW1819. This section describes a few key characteristics of the PCB design for best circuit performance. Figure 10.6 shows a PCB layout for a typical design using the iW1819. For each section of the layout considerations, a simplified view of the layout is used for clarity.



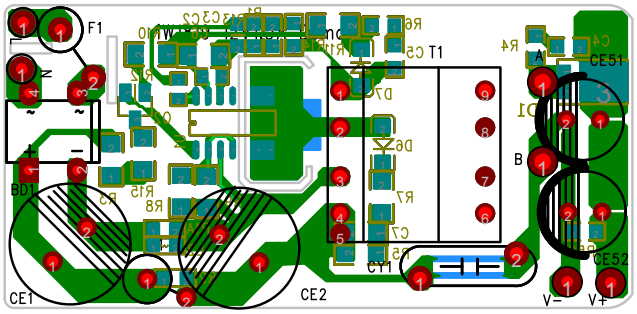


Figure 10.6a : Application Schematic of Typical iW1819 Circuit **Figure 10.6b : Typical Layout of iW1819 Application Circuit**

10.16.1 Creepage

The iW1819 integrates a high-voltage BJT in the same package as the control circuit. The SO-10 package is made especially with a minimum spacing of 1.47mm between the high voltage pins and low voltage pins. For applications that require a creepage rating higher than 1.47mm can use a slot in the PCB between the pins. Figure 10.7 shows the slots on a recommended layout used in a reference design for the iW1819.

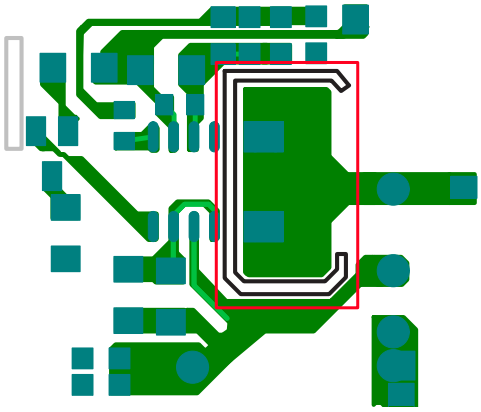


Figure 10.6 : Creepage Layout Example

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10.16.2 Primary-Side Power Loop

The main power loop, consisting of the input capacitor, primary-side winding, power path through the IC and subsequently through the sense resistor to ground, needs careful consideration during PCB layout. The loop should be as short as possible and the traces, which carry very high dv/dt and di/dt need to be short and wide to keep parasitic resistance and inductance to a minimum. Figure 10.8 shows the paths of concern in a typical layout.

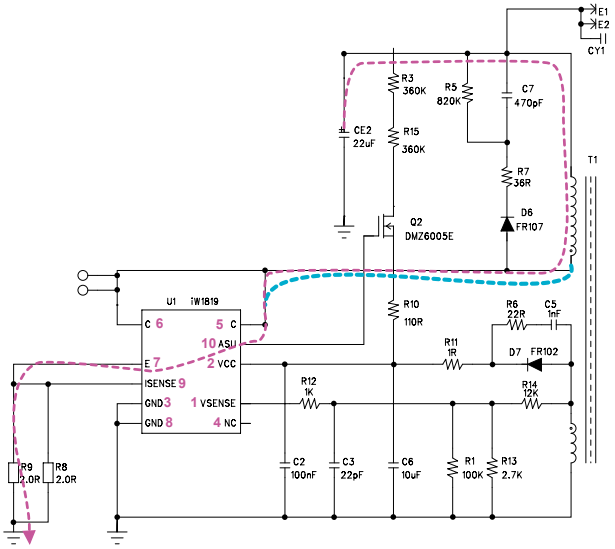


Figure 10.8a : Primary-Side Power Path

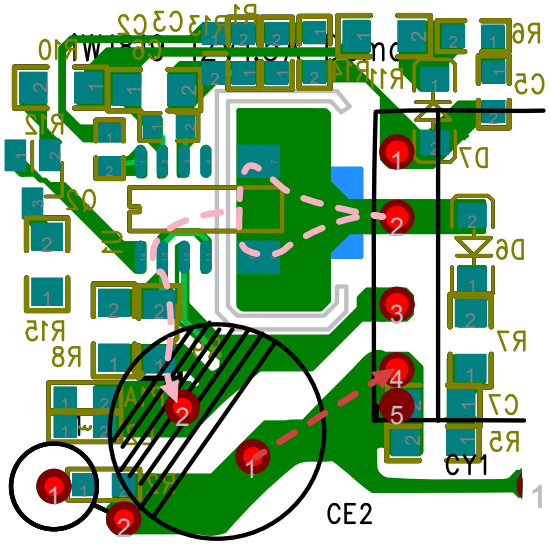


Figure 10.8b : Layout of Primary-Side Power Path

10.16.2 Secondary-Side Power Loop

The secondary-side of the circuit also needs care to optimize performance. The copper trace between the positive connection of the secondary winding of the transformer (NS) and the Schottky rectifier diode should be as short as possible, as it is a hot-point. The copper trace between Schottky diode and the positive terminal of the output capacitor(s) should be as short as possible. The copper trace between the return trace of the secondary winding and the negative terminal of the output capacitor(s) should be as short as possible as well. Finally, the traces connecting the output capacitor should be short and wide so that the current can be fully filtered. Otherwise, the current will bypass the filter capacitor(s) if the copper traces at these points are too large.

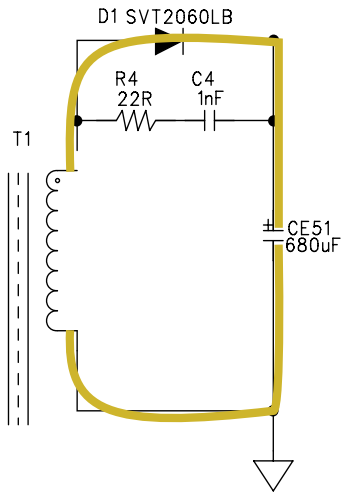


Figure 10.9a : Secondary-Side Power Path

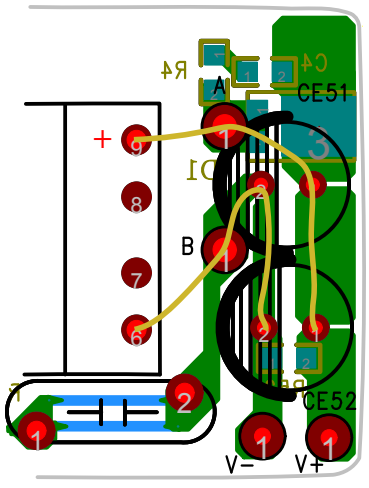


Figure 10.9b : Secondary-Side Layout Path Recommendation

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10.16.3 V_{SENSE} Voltage Feedback Loop

The voltage sense loop provides the voltage feedback to the controller and it is important to have a clean layout for best performance. The most important points of the layout of the V_{SENSE} traces is to keep them away from hot points or traces with high di/dts or high dv/dts. This prevents noise from coupling into the sensitive voltage feedback loop. The loop should be as small as possible and the trace lengths as short as possible.

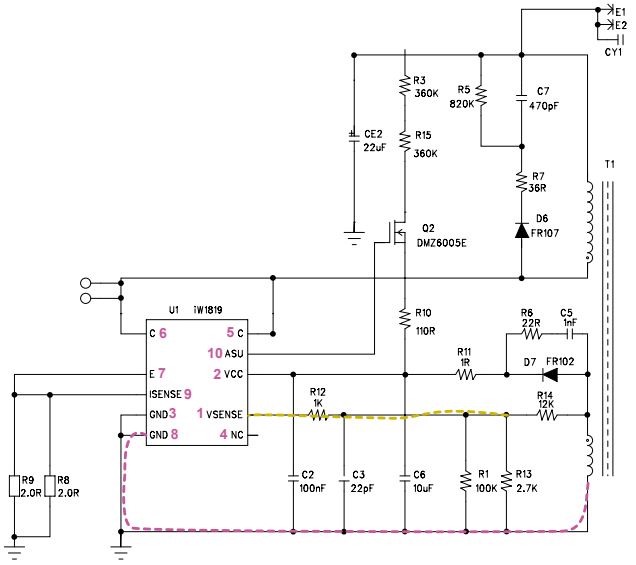


Figure 10.10a : V_{SENSE} Feedback Path

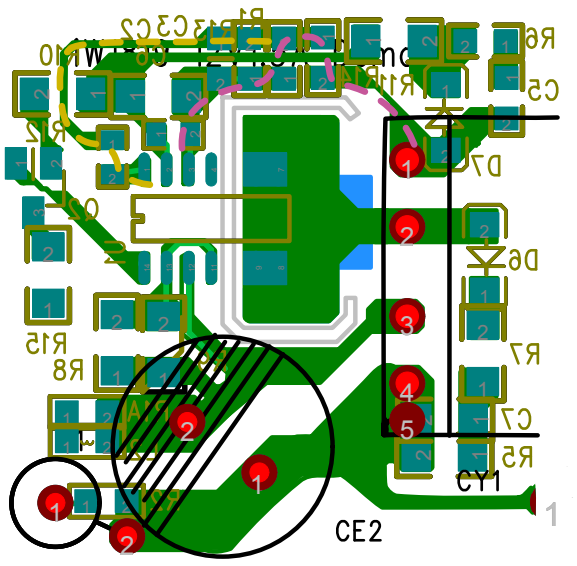


Figure 10.10b : V_{SENSE} Feedback Layout Path

10.16.4 IC and Transformer Ground

The ground traces should not overlap the power loop if at all possible. If it is not possible to avoid overlap, it should be minimized. The copper traces of both the IC ground and the transformer ground should be as short as possible to minimize EMI.

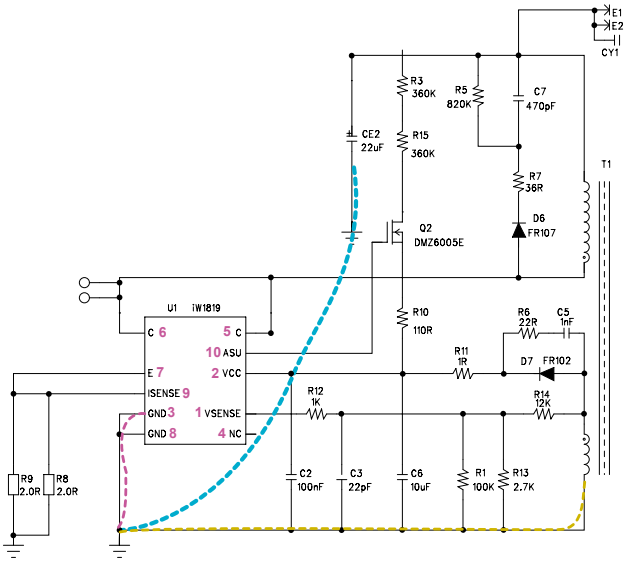


Figure 10.11a : IC and Transformer Ground Path

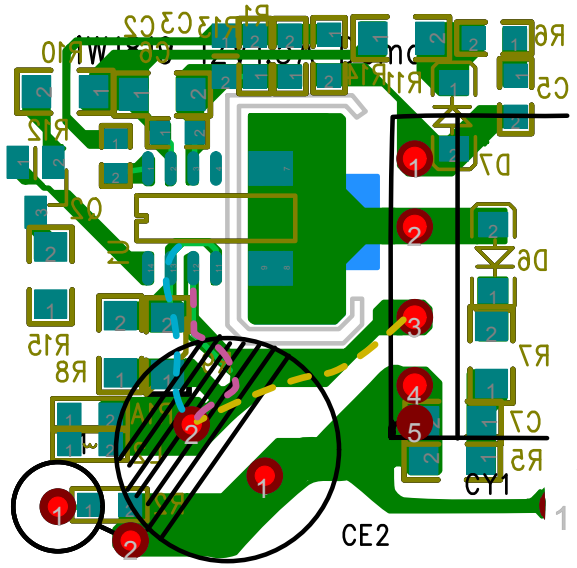


Figure 10.11b : IC and Transformer Ground Layout Path

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10.16.5 Snubber Circuit

The snubber circuit should be located near the primary-side winding and the copper traces should be as short as possible. The current path from the bulk input capacitor to the snubber circuit and primary-side winding should be as short as possible.

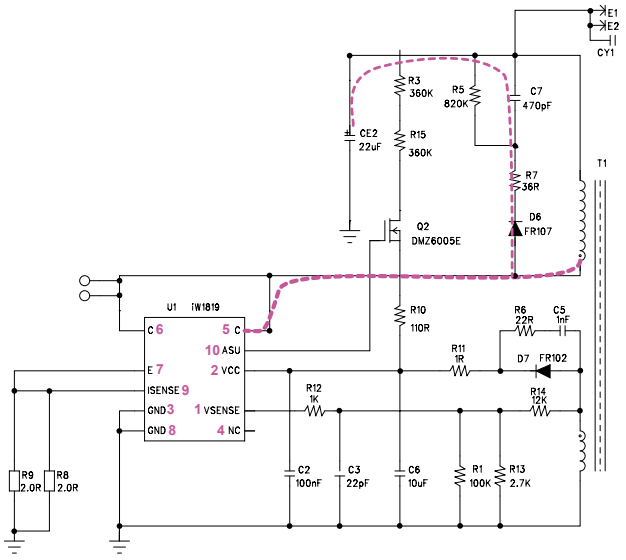


Figure 10.12a : Snubber Circuit Path

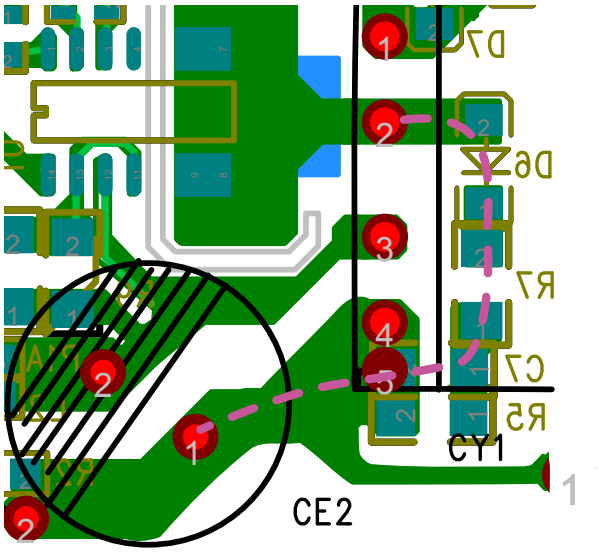


Figure 10.12b : Snubber Circuit Layout Path

10.16.6 IC Power Supply

The power supply for the IC, V_{CC}, needs careful consideration to keep noise out of the control circuit. The bypass capacitors should be as close to the V_{CC} pin as possible, in particular the high frequency bypassing capacitor. This fully filters the aux winding voltage prior to being applied to the V_{CC} pin.

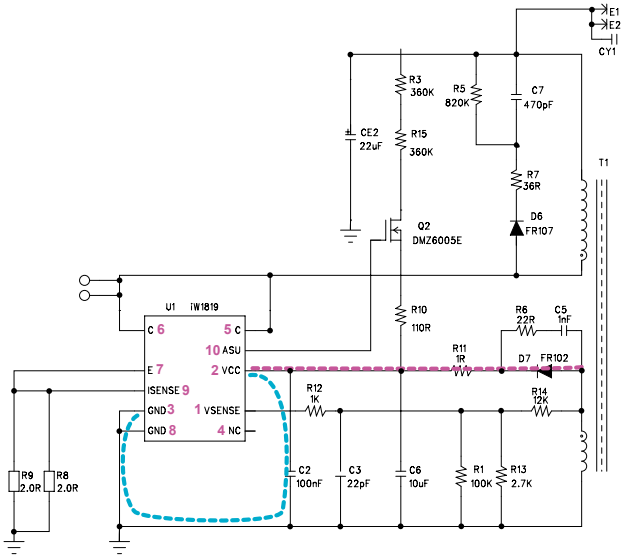


Figure 10.13a : IC Power Supply Path

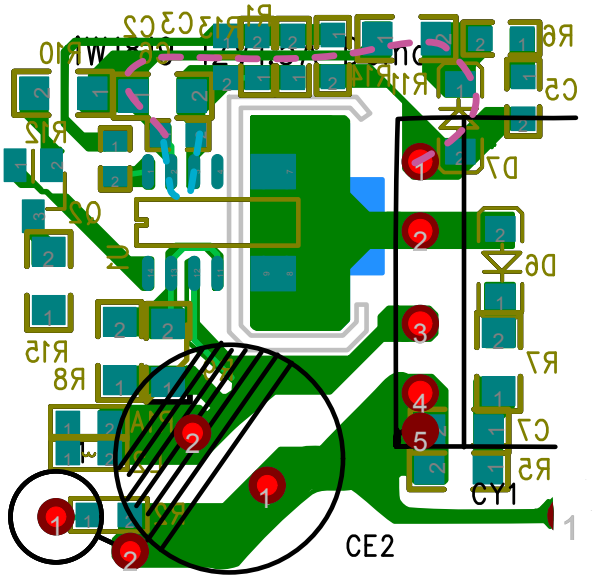


Figure 10.13b : IC Power Supply Layout Path

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10.16.7 Y-Cap

Similar to the grounding considerations, the copper traces should be as short as possible to help improve EMI performance. Depending on your practical case, the connection to the primary can be the “+” or “-” of the primary bulk E-Cap (but the E-Cap should be the one that is closest to the transformer, CE2 in this example).

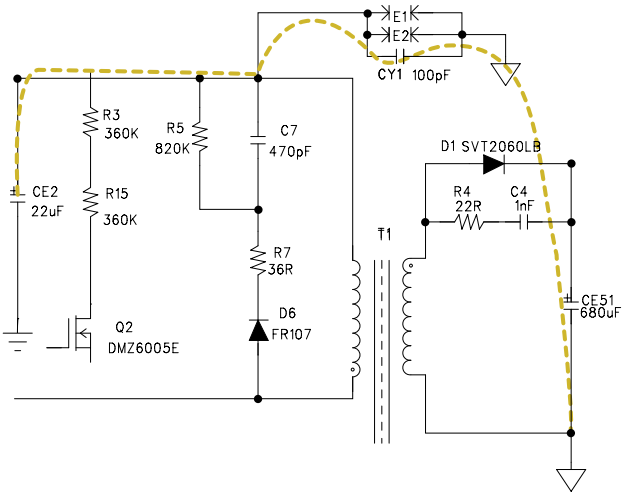


Figure 10.13a : Y-Cap Path

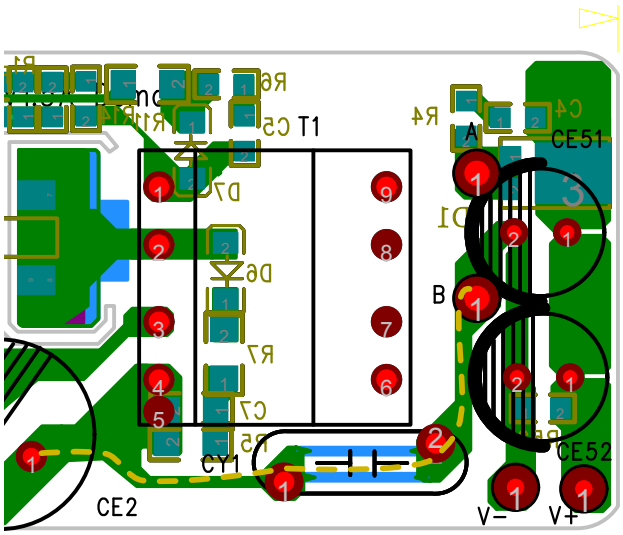
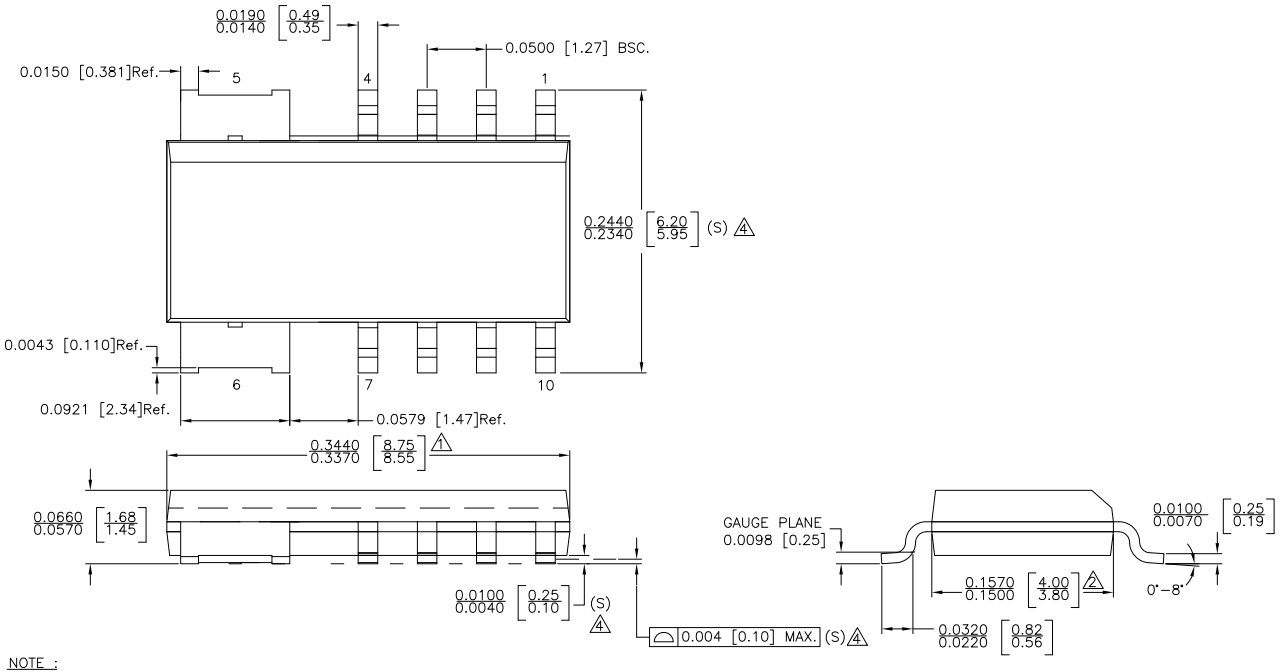


Figure 10.13b : Y-Cap Layout Path

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11 Physical Dimensions



NOTE :

1. DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .006 INCH PER SIDE.
2. DOES NOT INCLUDE INTER–LEAD FLASH OR PROTRUSIONS. INTER–LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .010 INCH PER SIDE.
3. THIS PART IS COMPLIANT WITH JEDEC SPECIFICATION MS–012 AB.
4. LEAD SPAN/STAND OFF HEIGHT/COPLANARITY ARE CONSIDERED AS SPECIAL CHARACTERISTIC.(S)
5. CONTROL DIMENSIONS IN INECHES.[mm]

STATUS: RELEASED	SCALE: DO NOT SCALE
TERMINAL FINISH: NiPdAu (PPF)	
TITLE: 10 SOIC BATWING PACKAGE OUTLINE	
REV: A	REVISION NOTE: NEW DRAWING
	DATE: 29–SEP–2015

12 Ordering Information

Part no.	Options	Package	Description
iW1819-00	Cable Comp = 0mV, OTP recovery threshold = 100°C	SO-10 Batwing	Tape & Reel[1]
iW1819-01	Cable Comp = 150mV, OTP recovery threshold = 100°C	SO-10 Batwing	Tape & Reel[1]
iW1819-11	Cable Comp = 150mV, OTP recovery threshold = 120°C	SO-10 Batwing	Tape & Reel[1]

Note 1: Tape & Reel packing quantity is 2,500/reel. Minimum packing quantity is 2,500.

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18W AccuSwitch™ Quasi-Resonant PWM Controller with Integrated 800V Power BJT

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