CMX979
Dual PLL + VCO

CMX979 RF Frac-N Synth, IF Integer-N Synth and VCOs

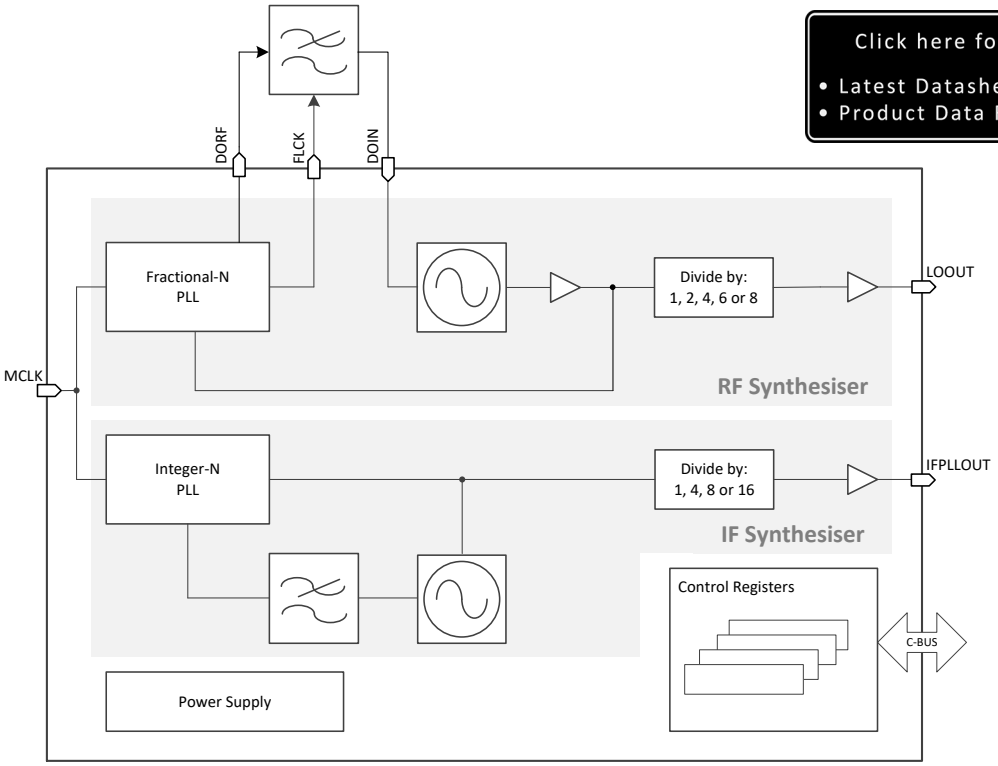
D/979/5 December 2019 **DATASHEET** Provisional

Features

- RF synthesiser/PLL
  - Fractional-N 24-bit divider
  - Output range 338MHz – 3.6GHz
  - Programmable output divider
  - Fast lock function
  - Programmable charge pump current
- IF synthesiser/PLL
  - Integer-N 14-bit divider
  - Output range 31MHz – 1GHz
  - Programmable output divider
- -209dBc/Hz normalised phase noise
- Integrated low noise LDO regulator
- Single 2.7V to 3.6V supply
- 1.8V digital interface supported
- -40˚ to +85˚ operating temp. range
- Small outline 6mm x 6mm VQFN package

Applications

- Satellite modems
- Custom ISM band modems
- Wireless data links
- CATV equipment
- General purpose RF use



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1 Brief Description

The CMX979 is a low-power, wideband, dual synthesiser and VCO, supporting signal generation over a wide range of frequencies. The 'RF' high frequency synthesiser employs a Fractional-N design and will operate at up to 3.6GHz using a fully-integrated internal VCO. The 'IF' synthesiser employs an integer-N design and will operate at up to 1GHz. It has an integrated VCO requiring only an external inductor to set the fundamental frequency. Internal dividers and buffers are provided for each synthesiser/PLL allowing a wide range of frequency generation options.

Designed primarily for radio transmitters and receivers using superhetrodyne architectures, the CMX979 provides a compact solution for frequency generation requiring a minimum of external components. The CMX979 operates from a single supply voltage and is available in a small 6x6mm VQFN package.

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1.1 History

Version	Changes	Date
5	Section 9: Updated Q4 package diagram	December 2019
4	Section 3.1.3.1: Typical current from DV_{DD} changed from 380µA to 630µA. Maximum current from DV_{DD} changed from 600µA to 900µA Datasheet status changed to Provisional	October 2017
3	Section 3.1.3.3: RF LO frequency range data added to AC parameters table	September 2017
2	Section 3.1.3.1: Typical operating current for RF synth + VCO corrected from 20 to 30mA Section 3.1.3.1: Typical operating current for IF LO divider (0.9mA) added	July 2017
1	First public release	June 2017

This is Provisional Information; changes and additions may be made to this specification. Parameters marked TBD or left blank will be included in later issues. Items that are highlighted or greyed out should be ignored. These will be clarified in later issues of this document. Information in this datasheet should not be relied upon for final product design.

2 Block Diagram

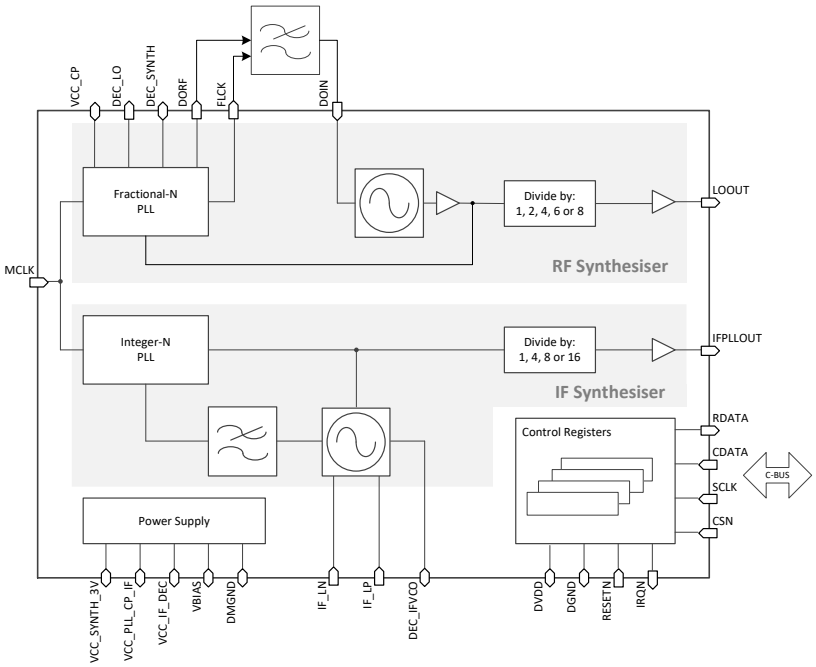


Figure 1 CMX979 Block Diagram

3 Performance Specification

3.1 Electrical Performance

3.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

	Min.	Max.	Units
Supply (AV_{DD} - AV_{SS}) or (DV_{DD} - DV_{SS}) or (CPV_{DD} - AV_{SS})	-0.3	+4.0	V
Voltage on any pin to AV_{SS} or DV_{SS}	-0.3	V_{max} + 0.3	V
Voltage between AV_{SS} pins and DV_{SS}	-50	+50	mV
Voltage between AV_{DD} and CPV_{DD}	-0.3	+0.3	V
Current into or out of pins: connected to AV_{DD}, AV_{DDTX}, AV_{SS}, DV_{DD}, DV_{SS} or CPV_{DD}	-75	+75	mA
any other pin	-30	+30	mA

Q4 Package	Min.	Max.	Units
Total Allowable Power Dissipation at T_{AMB} = 25°C	–	1820	mW
Derating (see Note below)	–	18.2	mW/°C
Storage Temperature	-55	+125	°C
Operating Temperature	-40	+85	°C

Note: Junction-to-ambient thermal resistance is dependent on board layout and mounting arrangements. The derating factor stated will be better than this with good connection between the device and a ground plane or heat sink.

3.1.2 Operating Limits

	Notes	Min.	Max.	Units
Analogue Supply (AV_{DD} – AV_{SS})		2.7	3.6	V
Charge Pump Supply (CPV_{DD} – AV_{SS})		2.7	3.6	V
Digital Supply (DV_{DD} – DV_{SS})		1.7	3.6	V
Operating Temperature (see Note above)		-40	+85	°C

3.1.3 Operating Characteristics

3.1.3.1 DC Parameters

For the following conditions unless otherwise specified:
AV_{DD} = CPV_{DD} = 2.7V to 3.6V; DV_{DD} = 1.7V to 3.6V; AV_{SS} = DV_{SS} = 0V; and T_{AMB} = +25ºC.
External components and values as shown in section 5

DC Parameters	Notes	Min.	Typ.	Max.	Units
Total Current Consumption					
Power save mode	1	–	64	–	µA
V_{BIAS} only	3	–	1	–	mA
Operating Currents					
RFSynth + VCO		–	30	–	mA
IFSynth + VCO		–	8	13	mA
RF LO Output (Divide by 1, minimum bias)	5	–	4.5	–	mA
RF LO Output (Divide by 8, maximum bias)	5	–	14	–	mA
IF LO Divider	5a		0.9		mA
Current from DV_{DD}	2	–	630	900	µA
Logic “1” Input Level		70%	–	–	DV_{DD}
Logic ‘0’ Input Level		–	–	30%	DV_{DD}
Output Logic ‘1’ Level (I_{OH} = 0.6 mA)		80%	–	–	DV_{DD}
Output Logic ‘0’ Level (I_{OL} = -1.0 mA)		–	–	+0.4	V
External Bias Voltage (V_{BIAS})	6	–	1.2	–	V
Power up time					
Voltage Reference	4	–	–	0.5	ms
All blocks except Voltage Reference	4	–	–	10	µs

Notes:
1. Powersave mode includes after a general reset with all analogue and digital supplies applied and also in the case with DV_{DD} applied but with all analogue supplies disconnected (i.e. in this later scenario power from DV_{DD} will not exceed the specified value whatever the state of the registers).
2. Assumes 30pF on each C-BUS interface line and an operating serial clock frequency of 5MHz.
3. The stated current drawn here is with the bandgap reference and accompanying bias current generators enabled only, all other circuitry is disabled.
4. As measured from the rising edge of CSN.
5. Additional current when LO Output (to LOOUT pin) is enabled.
5a. Additional current when IF LO output divider is enabled, independent of division ratio.
6. R1 = 47.5kΩ, as shown in Figure 4.

3.1.3.2 AC Parameters – PLLs

For the following conditions unless otherwise specified:
AV_{DD} = CPV_{DD} = 3.0V; DV_{DD} = 1.8V; AV_{SS} = DV_{SS} = 0V; and T_{AMB} = +25ºC.
External components and values as shown in section 5

AC Parameters	Notes	Min.	Typ.	Max.	Unit
Clocks					
MCLK frequency (f_{MCLK})		5	–	40	MHz
MCLK sensitivity (AC-coupled)		0.2	–	1.2	Vp-p
MCLK slew rate (AC-coupled)		10	–	–	V/µs
MCLK amplifier phase noise		–	-142	–	dBc/Hz
RF Synthesiser					
Charge pump sink/source (programmable)		25	–	400	µA
Charge pump absolute accuracy		-20	–	20	%
Charge pump matching		-4	–	4	%
Charge pump compliance range		0.5	–	CPV_{DD1} - 0.5	V
PD comparison frequency (f_{COMP})	10	1.2	–	40	MHz
N-Divider range (Integer mode)		32	–	2047	
N-Divider range (Fractional mode)		32	–	2047	
1Hz normalised phase noise floor	12, 14	–	-209	–	dBc/Hz
IF Synthesiser					
RF frequency		500	–	1000	MHz
PD comparison frequency		100	1000	2500	kHz
Nominal charge pump current		25	–	400	µA
N-Divider range		25	–	10000	
R-Divider range		2	–	400	
1Hz normalised phase noise floor	11, 12, 13	–	-211	–	dBc/Hz

Notes:
10. During internal RF VCO calibration, the comparison frequency should be ≥4.8 MHz.
11. MCLK = 19.2MHz sinewave, 400mVp-p, measured at 1kHz offset.
12. 1Hz Normalised Phase Noise Floor (PN1Hz) can be used to calculate the phase noise within the PLL loop bandwidth by:
Measured Phase Noise (in 1Hz) = -PN1Hz - 20log10(N) - $10\log_{10}(f_{comparison})$.
where: $f_{comparison}$ = Frequency at the output of the reference divider; N = main divider ratio.
13. IF PLL locked at 900 MHz; IFFPLL_RDIV = 8 (2.4 MHz), IFPLL_NDIV = 375, Icp = 200 µA; improves with higher Icp setting.
14. RF PLL / VCO locked at 3.6GHz;_RFPLL_RDIV = 1 (19.2 MHz), RFPLL_IDIV = 187, Icp = 400 µA; Fractional-N mode.

3.1.3.3 VCO and LO

For the following conditions unless otherwise specified:
AV_{DD} = CPV_{DD} = 3.0V; DV_{DD} = 1.8V; AV_{SS} = DV_{SS} = 0V; and T_{AMB} = +25ºC.External components and values as shown in Figure 4 and Table 2.

AC Parameters	Notes	Min.	Typ.	Max.	Unit
RF VCO					
Frequency range		2700	–	3600	MHz
K_{VCO}		–	60	–	MHz/V
Phase Noise at 100 kHz offset	20	–	-105	–	dBc/Hz
Phase Noise at 1 MHz offset	20	–	-130	–	dBc/Hz
Phase Noise at 10 MHz offset	20	–	-148	–	dBc/Hz
RF LO Output					
Frequency Range	21	337.5	–	3600	MHz
LO Output divide by 2	22	1350		1800	MHz
..LO Output divide by 4	22	675		900	MHz
LO Output divide by 6	22	450		600	MHz
LO Output divide by 8	22	337.5		450	MHz
Output Level		–	-7	–	dBm
IF VCO					
Frequency range	23	500	–	1000	MHz
K_{VCO}		–	11	–	MHz/V
Phase Noise at 10kHz offset	24	–	-90	–	dBc/Hz
Phase Noise at 100kHz offset	24	–	-111	–	dBc/Hz
Phase Noise at 1MHz offset	24	-	-135	-	dBc/Hz
IF LO Output					
Frequency Range	21	500	–	1000	MHz
LO Output divide by 4	22	125		250	MHz
LO Output divide by 8	22	62.5		125	MHz
LO Output divide by 16	22	31.25		62.5	MHz
Output Level	25	-20	-15	–	dBm

Notes:
20. RF frequency of 1.6GHz (VCO / PLL at 3.2GHz, output divide by 2); loop comparison frequency = 19.2MHz.
21 LO output divide function disabled.
22 LO output divide function enabled.
23 Tuned with external inductor or PCB track. While operation is possible with other inductor values above and below this frequency range, performance is not validated.
24 Operating frequency 500MHz.
25 Unmatched, high current mode

3.1.3.4 C-BUS Timing Parameters

For the following conditions unless otherwise specified:
AV_{DD} = CPV_{DD} = 2.7V to 3.6V; DV_{DD} = 1.7V to 3.6V; AV_{SS} = DV_{SS} = 0V; T_{AMB} = +25°C.
External components and values as shown in Figure 4 and Table 2.

C-BUS Timings (See Figure 2**)**		**Notes**	**Min.**	**Typ.**	**Max.**	**Units**
t_{CSE}	CSN-enable to clock-high time		100	–	–	ns
t_{CSH}	Last clock-high to CSN-high time		100	–	–	ns
t_{LOZ}	Clock-low to reply output enable time		0.0	–	–	ns
t_{HIZ}	CSN-high to reply output 3-state time		–	–	1.0	µs
t_{CSOFF}	CSN-high time between transactions		1.0	–	–	µs
t_{NXT}	Inter-byte time		200	–	–	ns
t_{CK}	Clock-cycle time		200	–	100	ns
t_{CH}	Serial clock-high time		100	–	–	ns
t_{CL}	Serial clock-low time		100	–	–	ns
t_{CDS}	Command data set-up time		75.0	–	–	ns
t_{CDH}	Command data hold time		25.0	–	–	ns
t_{RDS}	Reply data set-up time		50.0	–	–	ns
t_{RDH}	Reply data hold time		0.0	–	–	ns

Maximum 30pF load on each C-BUS interface line.

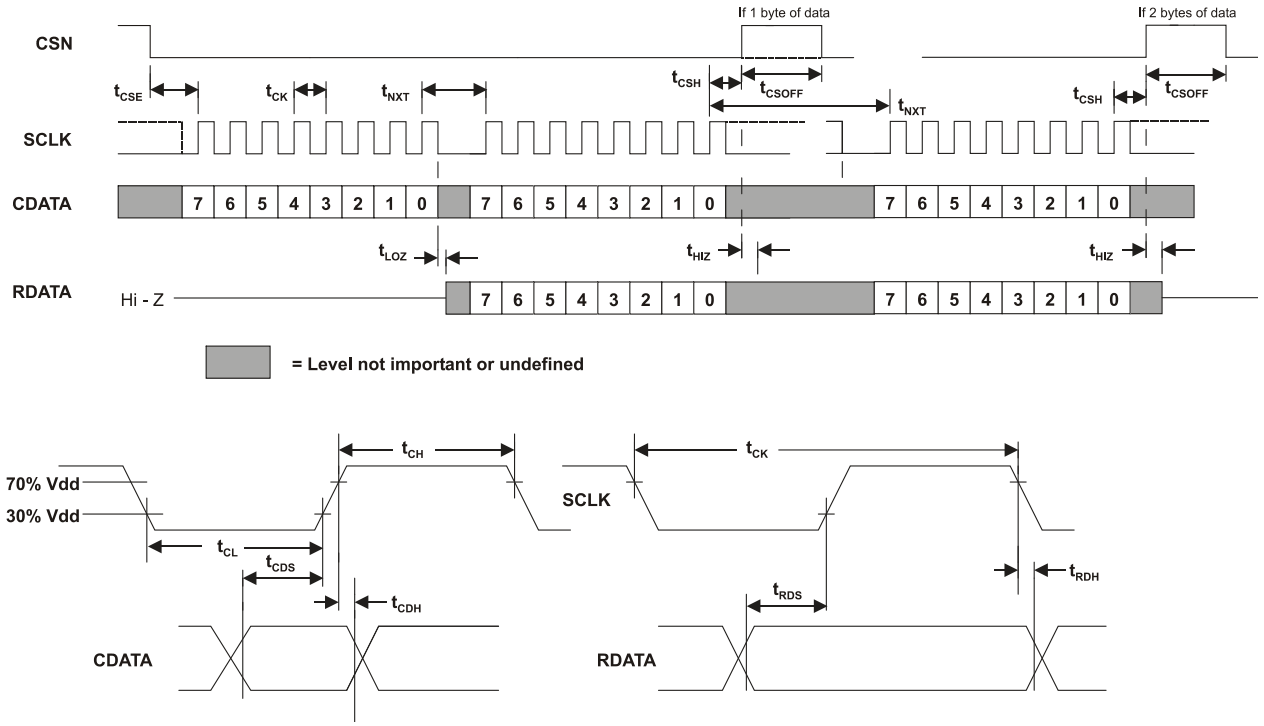


Figure 2 C-BUS Timing

4 Pin and Signal Definitions

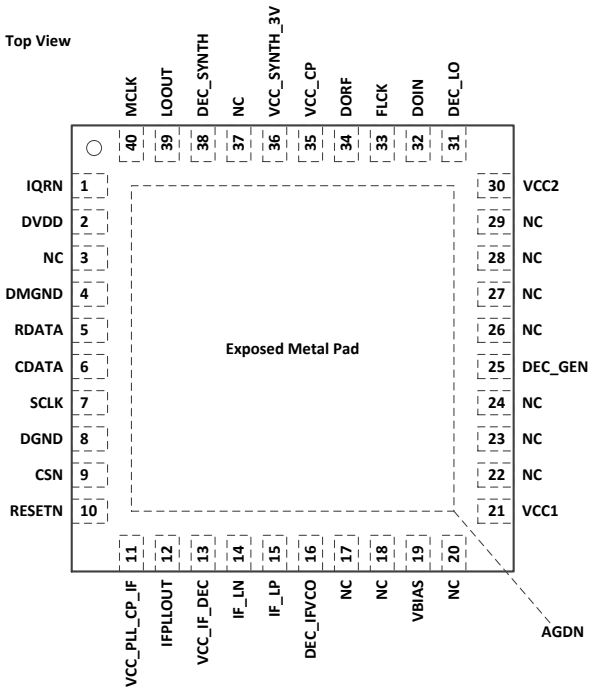


Figure 3 Pin Configuration

4.1 Pin List

Pin No	Pin Name	Type	Pin Function
1	IRQN	OP	C-BUS interrupt request. The output is driven low to DGND when active and is high-impedance when inactive. An external 100kΩ pull-up resistor to DV_{DD} should be connected to this pin.
2	DVDD	PWR	Global digital power supply and decoupling
3	NC	NC	Do not connect to this pin
4	DMGND	PWR	Digital Ground (moat connection)
5	RDATA	TS	A tri-state C-BUS data output. This output is high impedance when not sending data to the host µC. Care should be taken to ensure any inputs to which this pin is connected are not left floating when RDATA is in a high impedance state.
6	CDATA	IP	C-BUS data input
7	SCLK	IP	C-BUS clock
8	DGND	PWR	Digital Ground
9	CSN	IP	C-BUS chip select
10	RESETN	IP	Active low reset pin with internal 75kΩ pull-up resistor
11	VCC_PLL_CP_IF	PWR	IF PLL Charge Pump power supply and decoupling; connect to CPV_{DD2} and decouple when PLL not used.
12	IFPLLOUT	OP	Single ended IF PLL output
13	VCC_IF_DEC	PWR	Decoupling for IF PLL (retain decoupling when IF PLL not used)
14	IF_LN	IP	IF VCO tank negative
15	IF_LP	IP	IF VCO tank positive
16	DEC_IFVCO	PWR	IF VCO Decoupling decouple when PLL not used.
17	NC	NC	Do not connect to this pin.
18	NC	NC	Do not connect to this pin.
19	VBIAS	BIAS	47.5kΩ External bias resistor and decoupling to AV_{SS}. This pin should not be used as a voltage reference.

Pin No	Pin Name	Type	Pin Function
20	NC	NC	Do not connect to this pin.
21	VCC1	PWR	AV_{DD} power supply and decoupling
22	NC	NC	Do not connect to this pin.
23	NC	NC	Do not connect to this pin.
24	NC	NC	Do not connect to this pin.
25	DEC_GEN	PWR	1.2V regulator decoupling (GEN)
26	NC	NC	Do not connect to this pin.
27	NC	NC	Do not connect to this pin.
28	NC	NC	Do not connect to this pin.
29	NC	NC	Do not connect to this pin.
30	VCC2	PWR	AV_{DD} power supply and decoupling
31	DEC_LO	PWR	Decoupling for VCO supply and RF PLL loop filter reference point (1.2V)
32	DOIN	IP	VCO tuning node (0V to CPV_{DD})
33	FLCK	OP	RF PLL fast lock output
34	DORF	OP	Charge pump output
35	VCC_CP	PWR	Power supply and decoupling for RF PLL charge pump; connect to CPV_{DD1} and decouple even if not used.
36	VCC_SYNTH_3V	PWR	Analogue power supply and decoupling (RF PLL, bias and MCLK buffer); connect to AV_{DD} and decouple when PLL not used.
37	NC	NC	Do not connect to this pin.
38	DEC_SYNTH	OP	1.2V regulator decoupling (RF PLL)
39	LOOUT	OP	RF VCO/PLL output
40	MCLK	IP	Master Clock input used for RF and IF PLLs.
EXPOSED METAL PAD	AGND	PWR	The exposed metal pad must be electrically connected to analogue ground.

Notes:

Total = 41 Pins (40 pins and central, exposed metal ground pad)
Unused pins may be left not connected unless otherwise specified.

PWR = Power connection
IP = Input
OP = Output
TS = 3-state output
NC = Do not connect to this pin

4.2 Signal Definitions

Signal Name	Pins	Usage
V_{max}		The maximum value of the supplies DV_{DD} , $AV_{DD,}$ CPV_{DD1}, and CPV_{DD2}
AV_{DD}	VCC_SYNTH_3V,VCC1, VCC2	Power supply for analogue circuit
CPV_{DD1}	VCC_CP	Power supply for RF PLL charge pump
CPV_{DD2}	VCC_PLL_CP_IF	Power supply for IF PLL charge pump
CPV_{DD}	VCC_CP , VCC_PLL_CP_IF	CPV_{DD1} and CPV_{DD2}
DV_{DD}	DVDD	Power supply for digital circuits and C-BUS interface
DV_{SS}	DGND, DMGND	Ground for digital circuits
AV_{SS}	AGND	Ground for analogue circuits

Table 1 Definition of Power Supplies

5 Power Supply and Decoupling

This device has separate supply pins for the analogue and digital circuitry; a 3.0V nominal supply is recommended for AV_{DD}, DV_{DD}, CPV_{DD1} and CPV_{DD2}. The digital interface can run at a lower voltage than the rest of the device by setting the DV_{DD} supply to the required interface voltage (see section 3.1.2).

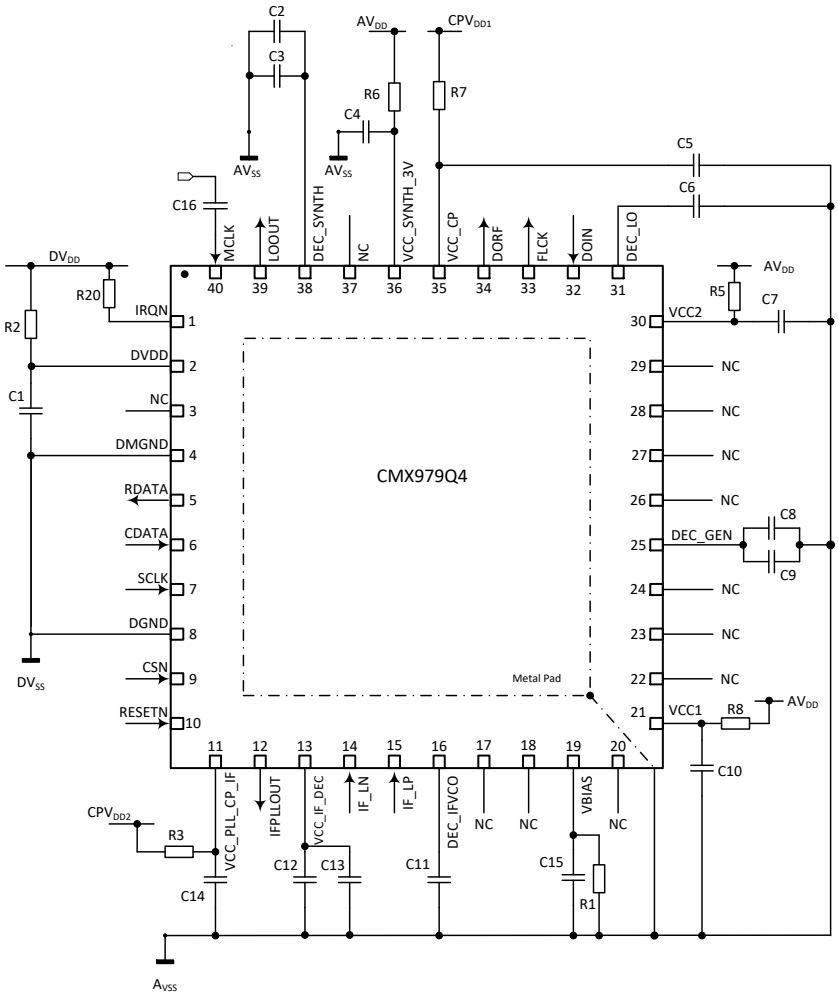


Figure 4 Power Supply and AC coupling

C1	10nF		C9	NF
C2	100nF		C10	10nF
C3	100pF		C11	56nF
C4	10nF		C12	100nF
C5	10nF		C13	NF
C6	150nF		C14	10nF
C7	NF		C15	10nF
C8	100nF		C16	10nF
R1	47.5kΩ		R6	3.3Ω
R2	10Ω		R7	3.3Ω
R3	3.3Ω		R8	3.3Ω
R5	3.3Ω		R20	100kΩ

Table 2 Power Supply and Decoupling Component Values

Notes:

1. Maximum Tolerances: Capacitors ±5% Resistors ±1%
2. It is expected that any low-frequency interference on the power supplies will be removed by active regulation; a large capacitor is an alternative but may require more board space and so may not be preferred. It is particularly important to ensure that there is no

interference from the DV_{DD} to sensitive analogue supplies (AV_{DD}). It is therefore advisable to use separate power supplies for digital and analogue circuits.

3. The supply decoupling shown is intended for RF noise suppression. It is necessary to have a small series impedance prior to the decoupling capacitor for the decoupling to work well. This may be achieved cost effectively by using the resistor and capacitor values shown. The use of resistors results in small dc voltage drops (up to approx 0.1V). Choosing resistor values approximately inversely proportional to the dc current requirements of each supply ensures the dc voltage drop on each supply is reasonably matched. In any case, the resultant dc voltage change is well within the design tolerance of the device. If higher impedance resistors are used (not recommended) then greater care will be needed to ensure the supply voltages are maintained within tolerance, even when parts of the device are enabled or disabled.
4. It is advisable to have separate ground planes for analogue and digital circuits.

5.1 Layout Recommendations

The RF performance of the CMX979 is dependant on the PCB design and layout. Grounding arrangements are particularly important to achieving the specified performance. Recommendations are contained in the following guidance:

A recommended layout may be taken from the evaluation kit (EV9790), Gerber data for which can be downloaded from the CML website (www.cmlmicro.com).

The evaluation kit has, in general, RF components, connectors and configuration links placed on the top layer, with voltage regulators, supplies and decoupling for the device on the bottom layer. The layout has been optimised for low ground impedance, the shortest possible RF tracking to the pins, and minimal stray capacitance for operation at high frequencies.

To provide all the connections to a small QFN package in a compact layout, along with its associated components and isolation between certain signals, a multi-layer PCB layout is necessary.

A good quality dielectric should be used for low loss and consistent high frequency performance. The EV9790 uses Rogers RO4003C ceramic substrate for the upper layer, with the other layers using FR4 / VT481 2116 dielectric.

The central ground pad should provide a good low impedance to ground plane layers, whilst also allowing for reliable solder reflow. A grid of 5 x 5 plated through vias (0.3mm diameter) is recommended.

6 Detailed Description

6.1 Power Management

There are four on-chip regulators each with the basic architecture of an error amplifier with an output pass transistor. Three of the regulators have external local decoupling capacitors. These regulators will supply 1.2V to the RF Synthesiser, IF Synthesiser and RF domains respectively. The fourth regulator provides 1.2V for the digital sections of the chip; C-BUS registers, power control and delta-sigma logic. This regulator is internally stablised and does not require an external capacitor. There are two on-chip bandgap reference circuits, one of which provides the 1.2V reference for the three analogue 1.2V supply regulators, while the other provides the 1.2V reference for the digital 1.2V supply regulator.

The on-chip Power On Reset (POR) is used to monitor the 3V digital and analogue supply rails and generate a power down signal in the case of loss of any supply rail. Whenever power is applied to the DVDD pin, the POR circuit ensures that the device powers up into the same state as follows a General Reset command. The RESETN pin on the device will also reset the device to the same state. The POWER STATUS register indicates when each of these regulators is stable.

6.2 Clock Generator

The MCLK amplifier must be enabled when a digital reference clock is required and is enabled automatically when either the RF or IF PLLs are enabled.
The MCLK amplifier receives the output of an external oscillator, which may be a low amplitude sine wave, and turns it into a 1.2V full range digital signal for use by the RF and IF PLL reference clock dividers and as a reference clock for the digital block. As the input to the amplifier is ac coupled and the amplifier may be enabled or disabled dependent on system configuration, the digital output clock may be unstable for a period of time.
A clock generator circuit will “hold off” the clock to the digital block until it is stable and then start the clock with a full and complete cycle. The status of the MCLK is reported in the status register ($C4, b7), see section 7.7.

6.3 RF VCO and Fractional-N PLL

The RF Synthesiser is a programmable 3.6GHz fractional-N PLL and VCO; a block diagram of the synthesiser is shown in Figure 5. A 1.2V voltage regulator provides the supply required for the synthesiser.

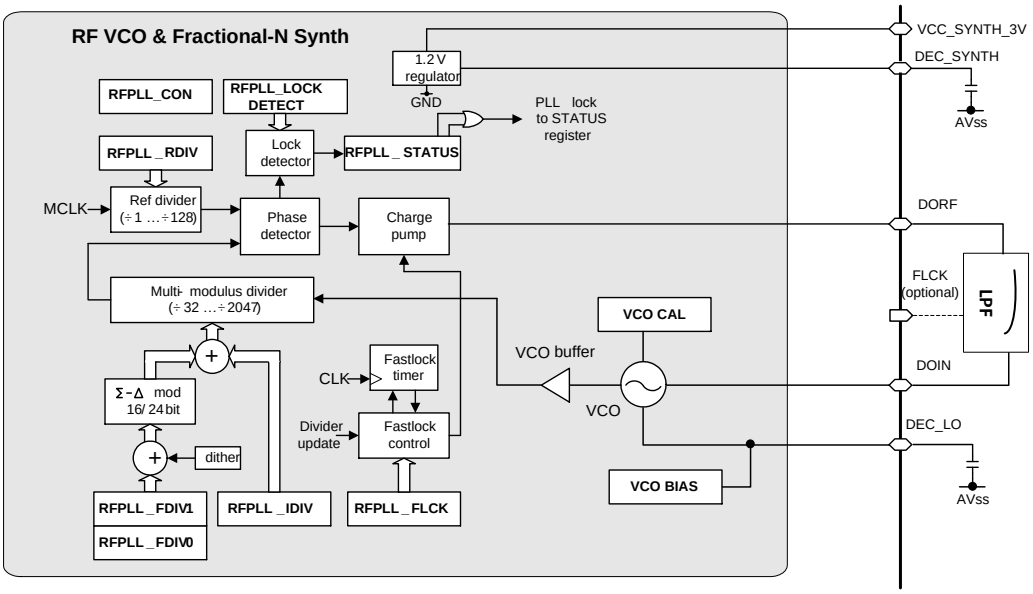


Figure 5 Fractional-N Frequency Synthesiser

6.3.1 RF Fractional-N Synthesiser

The RF Synthesiser uses a sigma-delta modulation technique that allows use of a high reference frequency, thus providing rapid frequency switching and low phase noise performance. The 24-bit fractional divider resolution provides an ultra-fine step size that may be useful in narrowband applications, or can be used to compensate for crystal oscillator frequency drift, Doppler shift, etc.

A fast locking mechanism is provided that increases the transition rate when changing to a new operating frequency. This is done by temporarily modifying the loop filter characteristics and charge pump gain whenever the main divider settings are updated, allowing the responsiveness of the closed loop system to be increased without compromising the loop stability. The fast lock mode automatically turns off after a predetermined delay, returning the PLL to its standard, low noise mode of operation.

The RF synthesiser has a programmable lock detector circuit that indicates when the loop is in lock. The lock detectors can be configured for analogue or digital operation and no external components are required, a programming example is given in section 8. The registers associated with initialisation of the RF synthesiser are:

- GCR - $31
- GCR_RD - $C1

The registers used to configure the RF Synthesiser are:

- RFPLL_CON - $34
- RFPLL_BLEED - $35
- RFPLL_LOCKDET - $36
- RFPLL_FLCK - $37
- RFPLL_RDIV - $38
- RFPLL_RDIV_RD - $C8
- RFPLL_IDIV - $39
- RFPLL_IDIV_RD - $C9
- RFPLL_FDIV0 - $3A
- RFPLL_FDIV0_RD - $CA
- RFPLL_FDIV1 - $3B
- RFPLL_FDIV1_RD - $CB
- LO_CONTROL - $3F
- LO_CONTROL_RD - $CF

Control of the RF Synthesiser is via the following registers:

- POWER_STATUS - $C6
- DEVICE_STATUS - $C4
- IRQ_ENABLE - $C5

6.3.2 Register Loading Order

To use the RF Synthesiser, the registers must be loaded in the order specified below.

The RF PLL enable bit (General Control Register ($31) bit 2) should be set to power up the synthesiser and MCLK amplifier (note: the charge pump output will remain in a high impedance state until the main divider registers are loaded).

Registers RFPLL_CON, RFPLL_LOCKDET, RFPLL_FLCK and RFPLL_RDIV should be initialised before the main divider registers are loaded for the first time.

After the main divider registers are loaded, the RF Synthesiser begins operating. The main divider registers can be changed at any subsequent time, but must always be updated in the following order:

Integer-N mode:
Load RFPLL_IDIV with the desired value, at which point the new divide ratio will take effect.

Fractional-N mode, 16-bit fractional resolution:
Load RFPLL_IDIV (if necessary), then load RFPLL_FDIV0. The new divide ratio only takes effect when RFPLL_FDIV0 is loaded.

Fractional-N mode, 24-bit fractional resolution:
Load RFPLL_IDIV and RFPLL_FDIV1 (if necessary), then load RFPLL_FDIV0. The new divide ratio only takes effect when RFPLL_FDIV0 is loaded.

If fastlock is enabled ($36, b12='1') each time the main divider registers are updated at the point when the new divide ratio takes effect a fastlock sequence is triggered.

6.3.3 Fractional-N Programming Example

The PLL functions are shown in Figure 5. The output frequency of the PLL is set by the following calculation:

$f_{out} = f_{ref} \times (N / R)$

where:

f_{out} = The desired output frequency in MHz
f_{ref} = The reference frequency supplied to the PLL on pin MCLK in MHz
N = Divider value programmed in the N divider registers (This then comprises of Integer and Fractional components, see sections 7.3.6 to 7.3.8)
R = Divider value programmed in the R divider register (see section 7.3.5)

Also note that the comparison frequency $f_{comp} = f_{ref} / R$

To operate the RFPLL in 24-bit fractional mode with an internal VCO frequency f_{VCO} = 3525.05MHz, a master clock frequency f_{MCLK} = 19.2MHz, and a PLL comparison frequency f_{COMP} = 19.2MHz.

Rdiv = $f_{MCLK} \div f_{COMP}$ = 19.2MHz ÷ 19.2MHz = 1

Ndiv = $f_{VCO} \div f_{COMP}$ = 3525.05MHz ÷ 19.2MHz = 183.5963542

Split the N divider value into integer and fractional parts:

Idiv = Round (183.5963542) = 184 (decimal) = 0x00B8 (hex)

Fdiv (24-bit mode) = Round (2^{24} × (Ndiv – Idiv)) = -6772053 (decimal) = 0x98AAAB (hex)

Load C-BUS registers:

GCR, bit 2 = 1(enable RF PLL)
RFPLL_CON
bit 14-11 = 1101 (fractional N-divider with 3rd order max length MASH 1-1-1 post-filtered modulator)
bit 9 = 0 (24-bit resolution)
Set RFPLL_LOCKDET and RFPLL_FLCK as desired
RFPLL_RDIV = 0x01
RFPLL_IDIV = 0x00B8
RFPLL_FDIV1 = 0x98
RFPLL_FDIV0 = 0xAAAB

At this point, the charge pump is enabled and RFPLL begins to acquire lock. The frequency step size in this example is 19.2MHz ÷ 2^{24} ≈ 1.14Hz.

6.3.4 RF VCO

The internal RF VCO consists of a negative resistance core cell, inductor, fine and coarse capacitor tuning banks, biasing and calibration circuits. An external loop filter is connected as shown in Figure 6 and Table 3.

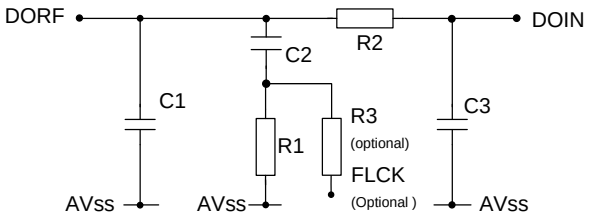


Figure 6 Example External Components – VCO External Loop Filter

VCO Frequency	C1	C2	C3	R1	R2	R3 (optional FLCK)
2.925GHz	750pF	6.2nF	27pF	1.6kΩ	5.1kΩ	See section 7.3.4
3.0GHz	680pF	5.6nF	27pF	2.2kΩ	5.6kΩ	See section 7.3.4
3.5GHz	470pF	3.6nF	22pF	2.4kΩ	6.8kΩ	See section 7.3.4

Table 3 3rd Order Loop Filter Example Values

Note: C1, C2, C3,R1 and R2 assume a Kvco=70MHz/V, Icp=400µA. The 3.0GHz example is as per the worked example in section 8.1.1 and these are the default values used on evaluation kits.

6.3.4.1 RF VCO Calibration

After configuring the RF PLL divider settings and enabling the RF PLL, the on-chip VCO bias and RF VCO should be calibrated. The device is instructed to calibrate the VCO bias current by setting b0 in the VCO_CAL_CTRL ($50) register with b15-b8 set to the MCLK frequency in MHz. The loop comparison frequency during calibration should be 4.8 MHz or greater. The reference divider can be increased after calibration. The calibration status may be monitored by reading the VCO_CAL_STAT ($5E) register. When calibration has completed, the 5-bit VCO bias calibration value may be read from the VCO_BIAS_CAL_READ ($5B) register.

Following VCO bias current calibration, the device should be instructed to calibrate the RF VCO resonant frequency by setting b1 in the VCO_CAL_CTRL ($50) register. The calibration status may be read from the VCO_CAL_STAT ($5E) register and, when calibration has completed, the 9-bit RF VCO calibration value may be read from the RFVCO_CAL_READ ($5C) register.The calibration of the VCO bias and RF VCO may be simultaneously requested by setting b0 and b1 in the VCO_CAL_CTRL ($50) register. In this case, the device will first perform calibration of the VCO bias followed by calibration of the RF VCO.

The registers used during RF VCO calibration are:

- VCO_BIAS_CAL_WRITE - $51
- VCO_BIAS_CAL_READ - $5B
- VCO_BIAS_CAL_TIME - $52
- RFVCO_CAL_WRITE - $53
- RFVCO_CAL_READ - $5C
- RFVCO_CAL_COUNT - $54
- RFVCO_CAL_TIME - $55
- RFVCO_STARTUP_TIME - $56
- LO_CONTROL - $3F
- LO_CONTROL_RD - $CF

Control of the RFVCO is via the following registers:

- VCO_CAL_CTRL - $50
- VCO_CAL_STAT - $5E
- DEVICE_STATUS - $C4
- IRQ_ENABLE - $C5

6.3.4.2 RF VCO Calibration Duration

The total calibration duration of the RF VCO in µs, $t_{rf\text{-}cal}$, is approximately given by the following equation:

$t_{rf\text{-}cal} \approx 6.t_{bias} + t_{rf\text{-}start\text{-}up} + 6.t_{rf\text{-}open\text{-}loop}.R_{rf\text{-}rdiv}/f_{MCLK} + t_{rf\text{-}settle} + 4.t_{rf\text{-}close\text{-}loop}$

where:

t_{bias} = VCO_BIAS_CAL_TIME ($52) register b5-b0 (µs).
$t_{rf\text{-}start\text{-}up}$ = RFVCO_STARTUP_TIME ($56) register b11-b0 (µs).
$t_{rf\text{-}open\text{-}loop}$ = RFVCO_CAL_COUNT ($54) register b9-b0.
$R_{rf\text{-}rdiv}$ = RFPLL_RDIV ($38) register b6-b0.
f_{MCLK} = MCLK frequency (MHz).
$t_{rf\text{-}settle}$ = RFVCO_CAL_TIME ($55) register b15-b8 (x8µs).
$t_{rf\text{-}close\text{-}loop}$ = RFVCO_CAL_TIME ($55) register b7-b0 (x8µs).

For example, assuming a 3500MHz RF VCO with 19.2MHz comparison frequency:

t_{bias} = 6µs
$t_{rf\text{-}start\text{-}up}$ = 300µs
$t_{rf\text{-}open\text{-}loop}$ = 350
$R_{rf\text{-}rdiv}$ = 1
f_{MCLK} = 19.2MHz
$t_{rf\text{-}settle}$ = 104µs
$t_{rf\text{-}close\text{-}loop}$ = 48µs

Therefore,

$t_{rf\text{-}cal} \approx 6x6 + 300 + 6x350x1/19.2 + 104 + 4x48 \approx 742µs$

6.3.4.3 RF VCO Calibration Indicators

The RF VCO calibration indicators signal to the host that the RF VCO should be recalibrated for optimum phase noise performance due to temperature or supply voltage change since the last calibration.
The RF VCO recalibration indicators may be read from the DEVICE_STATUS ($C4) register - bits 6/5 indicate if the RF VCO is running too slow/fast.
How often the DEVICE_STATUS ($C4) register should be read depends on the change in temperature and voltage since the last calibration, which will be application dependent.
If any of the RF VCO calibration indicators are high, the host should perform one of the following two actions:

1. Initiate a full recalibration of the VCO bias current and RF VCO resonant frequency by setting b1 and b0 of VCO_CAL_CTRL ($50).
2. Initiate a recalibration of the VCO bias current by setting b0 of VCO_CAL_CTRL ($50). The RF VCO resonant frequency may be subsequently increased/decreased if required by manually increasing/decreasing the RF VCO calibration code. The present RF VCO calibration code may be read from the RFVCO_CAL_READ ($5C) register. The new RF VCO calibration code may be written to the RF VCO_CAL_WRITE ($53) register. When the RF VCO is too slow/fast the calibration code should be increased/decreased until the RF VCO calibration indicators are all low. This method is much faster than initiating a full recalibration of the RF VCO.

6.4 IF PLL and VCO

6.4.1 IF PLL

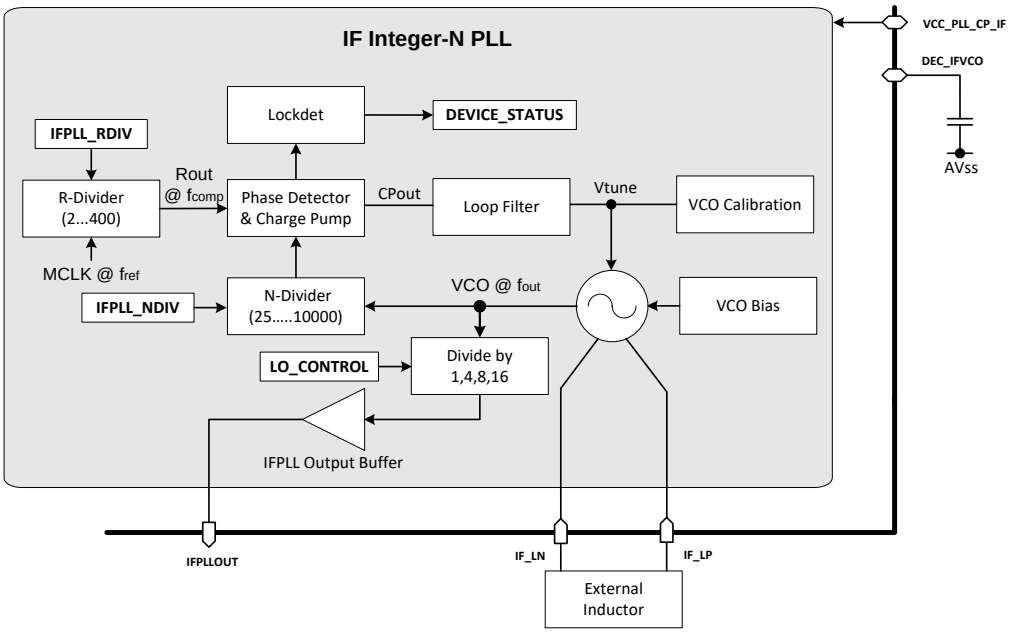


Figure 7 IF PLL Architecture

The IF PLL is an integer-N type and the functions are shown in Figure 7. The output frequency of the PLL is set by the following calculation:

$f_{out} = f_{ref} \times (N / R)$

where:
f_{out} = The desired output frequency in MHz
f_{ref} = The reference frequency supplied to the PLL on pin MCLK in MHz
N = Divider value programmed in the N divider register (see section 7.4.1)
R = Divider value programmed in the R divider register (see section 7.4.2)
also note that the comparison frequency $f_{comp} = f_{ref} / R$

The IF PLL provides a lock detect function which can be read via the DEVICE_STATUS ($C4) register, see section 7.7.1.

Initialisation of the IF Synthesiser is via the following registers:

- GCR - $31
- GCR_RD - $C1

Configuration of the IF Synthesiser is via the following registers:

- IFPLL_NDIV - $3C
- IFPLL_NDIV_RD - $CC
- IFPLL_RDIV - $3D
- IFPLL_RDIV_RD - $CD
- IFPLL_CURRENT - $3E
- IFPLL_CURRENT_RD - $CE

Control of the IF Synthesiser is via the following registers:

- POWER_STATUS - $C6
- DEVICE_STATUS - $C4
- IRQ_ENABLE - $C5

6.4.1.1 Integer-N Programming Example

To operate the IFPLL with a VCO frequency f_{VCO} = 900 MHz, a master clock frequency f_{MCLK} = 19.2MHz, and a PLL comparison frequency f_{COMP} = 1.2MHz.

IF PLL Rdiv = $f_{MCLK} \div f_{COMP}$ = 19.2MHz ÷ 1.2MHz = 16 (dec) = 0x 0010

IF PLL Ndiv = $f_{VCO} \div f_{COMP}$ = 900MHz ÷ 1.2MHz = 750 (dec) = 0x 02EE

The VCO frequency can then be further divided if required via the LO_CONTROL IFPLLDIV bits (see section 7.6.1).

6.4.1.2 IF PLL Loop Filter

The IF PLL loop filter is integrated on chip with the component values shown in Figure 8 and Table 4.

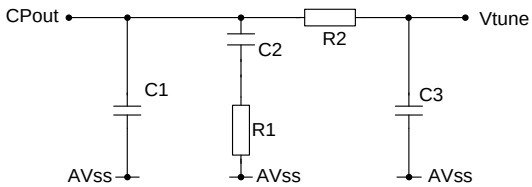


Figure 8 On-chip IF PLL Low Pass Filter Components

C1	C2	C3	R1	R2
53pF	790pF	16pF	28.88kΩ	86.6kΩ

Table 4 On-chip IF PLL Low Pass Filter Components

C1, C2, C3 ,R1 and R2 have been calculated to achieve a PLL phase margin of 50 degrees assuming 900MHz operation, F_{Comp} =2MHz and Kvco=10MHz/V, Icp=200uA. These values result in a nominal PLL bandwidth of ~40kHz and a phase noise profile closest to meeting the specification shown in Figure 17.

6.4.2 IF VCO

The IF VCO is a reflection oscillator that requires an external resonator circuit to set its operating frequency. Table 5 gives the IF VCO external inductor value for a given centre frequency.

Typical Centre Frequency & Approximate Tuning Range (MHz)	Inductor value (nH)
520 (~ 410- 640)	30
780 (~ 600-960)	12
900 (~ 680-1100)	8.2
1015 (~ 800-1250)	5.6
1170 (~ 900-1450)	3.6

Table 5 External Inductor Values for IF Centre Frequencies

Notes:

- The above inductor values assume that there is about 2.5mm of PCB track length from each chip output to the corresponding inductor pad.
- The on-chip capacitance can typically be changed from 5pF to 1.6pF with 1.2V on the VCO control voltage (Vtune) by changing the VCO Calibration Code.
- The approximate external inductor value can be selected by use of the following equation:

  $f_{centre}=(1/(2\pi\sqrt{((5.8nH+L_{ext})2.6pF)}))$
  where:
  - 5.8nH is the value of the package and typical PCB inductance
  - 2.6pF is the on-chip capacitance at the given centre frequency with 1.2V on the VCO control voltage.

It is recommended that the frequency of oscillation be measured at the highest and lowest code and an inductor chosen to give a median frequency between these two measured values.

The frequency and capacitance variation due to the analogue control voltage is much less than due to the VCO Calibration Code and the varactor is chosen to give a VCO gain of typically 11MHz/V at 900MHz. The VCO gain scales approximately linearly with frequency and the measured gain is typically 13MHz/V and 4.0MHz/V at 1GHz and 680MHz, respectively, using a 8.2 nH external inductor.

The IFPLL output impedance is independent of divider setting and is high, typically 8 kΩ in parallel with 0.5pF. The following diagrams (Figure 9, Figure 10 and Figure 11) show the VCO output buffer matching components required when evaluated with 50Ω measurement equipment and when driving the CMX973 at 500MHz, 900MHz and 1GHz respectively. Note that a DC blocking capacitor at the IFPLLOUT pin is required.

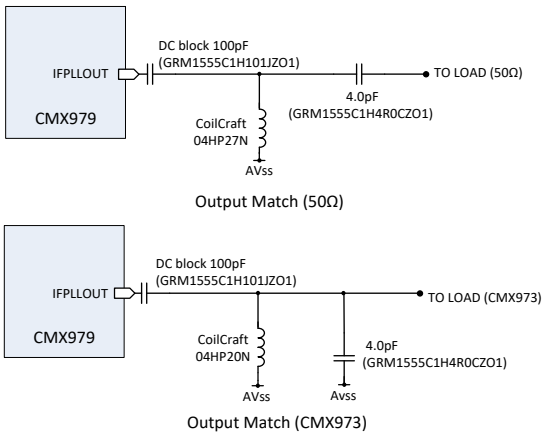


Figure 9 Output Matching Components at 500MHz

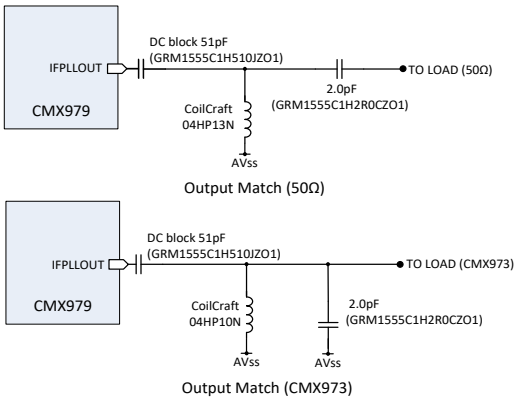


Figure 10 Output Matching Components at 900MHz

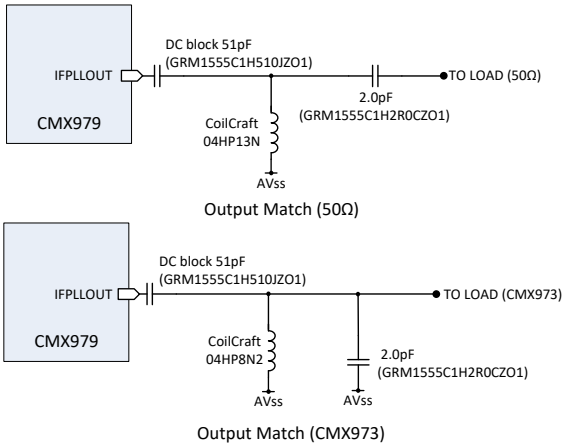


Figure 11 Output Matching Components at 1000MHz

Note: the components for the 50Ω match are the same at 1GHz and 900MHz.

When driving the CMX973, the signal may be high enough without matching components except for the dc blocking capacitor, which is required.

Note: for matching values for the divide by 4/8/16 frequency ranges consult CML Technical Support.

6.4.2.1 IF VCO Divider

The IF VCO divider is provided for applications that require a common IF frequency that is less than the minimum VCO frequency of 500MHz, the divider options are shown in Table 6.

The divider value is set via the LO CONTROL ($3F) register b5-b4 (section 7.6.1).

LO_CONTROL b5-b4	Divider Value
00	1
01	4
10	8
11	16

Table 6 IF VCO Divider Settings

6.4.2.2 IF VCO Calibration

IF VCO calibration is configured with the following registers:

- VCO_BIAS_CAL_WRITE - $51
- VCO_BIAS_CAL_READ - $5B
- VCO_BIAS_CAL_TIME - $52
- IFVCO_CAL_WRITE - $57
- IFVCO_CAL_READ - $5D
- IFVCO_CAL_COUNT - $58
- IFVCO_CAL_TIME - $59
- VCO_CAL_CTRL - $50
- VCO_CAL_STAT - $5E
- DEVICE_STATUS - $C4
- IRQ_ENABLE - $C5

After configuring the IF PLL divider settings and enabling the IF PLL, the on-chip VCO bias and IF VCO should be calibrated. The device is instructed to calibrate the VCO bias current by setting b0 in the VCO_CAL_CTRL ($50) register with b15-b8 set to the MCLK frequency in MHz. The calibration status may be monitored by reading the VCO_CAL_STAT ($5E) register. When calibration has completed, the 5-bit VCO bias calibration value may be read from the VCO_BIAS_CAL_READ ($5B) register.

Following VCO bias current calibration, the device should be instructed to calibrate the IF VCO resonant frequency by setting b2 in the VCO_CAL_CTRL ($50) register. The calibration status may be read from the VCO_CAL_STAT ($5E) register and, when calibration has completed, the 9-bit IF VCO calibration value may be read from the IFVCO_CAL_READ ($5D) register.

The calibration of the VCO bias and IF VCO may be simultaneously requested by setting b0 and b2 in the VCO_CAL_CTRL ($50) register. In this case, the device will first perform calibration of the VCO bias followed by calibration of the IF VCO.

6.4.2.3 IF VCO Calibration Duration

The total calibration duration of the IF VCO in µs, $t_{if\text{-}cal}$, is approximately given by the following equation:

$t_{if\text{-}cal} \approx 6.t_{bias} + t_{if\text{-}start\text{-}up} + 7.t_{if\text{-}open\text{-}loop}.R_{if\text{-}rdiv}/f_{MCLK} + t_{if\text{-}settle} + 3.t_{if\text{-}close\text{-}loop}$
where:
t_{bias} = VCO_BIAS_CAL_TIME ($52) register b5-b0 (µs).
$t_{if\text{-}start\text{-}up}$ = IFVCO_STARTUP_TIME ($5A) register b11-b0 (µs).
$t_{if\text{-}open\text{-}loop}$ = IFVCO_CAL_COUNT ($58) register b9-b0.
$R_{if\text{-}rdiv}$ = IFPLL_RDIV ($3D) register b8-b0.
f_{MCLK} = MCLK frequency (MHz).
$t_{if\text{-}settle}$ = IFVCO_CAL_TIME ($59) register b15-b8 (x8µs).
$t_{if\text{-}close\text{-}loop}$ = IFVCO_CAL_TIME ($59) register b7-b0 (x8µs).

For example, assuming a 900MHz IF VCO with 1.92MHz comparison frequency:
t_{bias} = 6µs
$t_{if\text{-}start\text{-}up}$ = 325µs
$t_{if\text{-}open\text{-}loop}$ = 450
$R_{if\text{-}rdiv}$ = 10
f_{MCLK} = 19.2MHz
$t_{if\text{-}settle}$ = 104µs
$t_{if\text{-}close\text{-}loop}$ = 104µs

Therefore,
$t_{if\text{-}cal} \approx 6x6 + 325 + 7x450x10/19.2 + 104 + 3x104 \approx 2418µs$

6.4.2.4 IF VCO Calibration Indicators

The IF VCO calibration indicators signal to the host that the VCO should be recalibrated for optimum phase noise performance due to temperature or supply voltage change since the last calibration.

The IF VCO recalibration indicators may be read from the DEVICE_STATUS ($C4) register - bits 4/3 indicate if the IF VCO is running too slow/fast.

How often the DEVICE_STATUS ($C4) register should be read depends on the change in temperature and voltage since the last calibration, which will be application dependent.

If any of the IF VCO calibration indicators are high, the host should perform one of the following two actions:

1. Initiate a full recalibration of the VCO bias current and IF VCO resonant frequency by setting b2 and b0 of VCO_CAL_CTRL ($50).
2. Initiate a recalibration of the VCO bias current by setting b0 of VCO_CAL_CTRL ($50). The IF VCO resonant frequency may be subsequently increased/decreased if required by manually increasing/decreasing the IF VCO calibration code. The present IF VCO calibration code may be read from the IFVCO_CAL_READ ($5D) register. The new IF VCO calibration code may be written to the RF VCO_CAL_WRITE ($57) register. When the IF VCO is too slow/fast the calibration code should be increased/decreased until the IF VCO calibration indicators are all low. This method is much faster than initiating a full recalibration of the IF VCO.

6.5 Local Oscillator (LO)

The CMX979 uses the internal VCO and a divider chain to produce a LO output. Four bits in the General Control Register are used to define the allowed states (X = don't care). The valid combinations are shown in Table 7.

The LO is controlled by the following registers:

- GCR - $31
- GCR_RD - $C1
- LO_CONTROL - $3F
- LO_CONTROL_RD - $CF

LOOUT ($31, b6)	RFPLLEN ($31,b2)	S ($34, b8)	PLL & Output
0	1	X	VCO output connected to PLL
1	1	X	VCO output connected to PLL & LOUT Pin enabled

Notes:
1. Combinations not shown are invalid.

Table 7 LO Connections

6.5.1 LO Output (LOOUT)

The CMX979 has a single-ended LOOUT with a frequency range from 337.5MHz to 3.6GHz. The output can be configured to internally divide the signal by 1/2/4/6/8 before it reaches LOOUT. Using the LO Output dividers the following frequency ranges are available using the RF VCO:

Divider value	1	2	4	6	8
F Low MHz	2700	1350	675	450	337.5
F High MHz	3600	1800	900	600	450

Table 8 RF VCO Frequency Limits with LO Output Divider Value

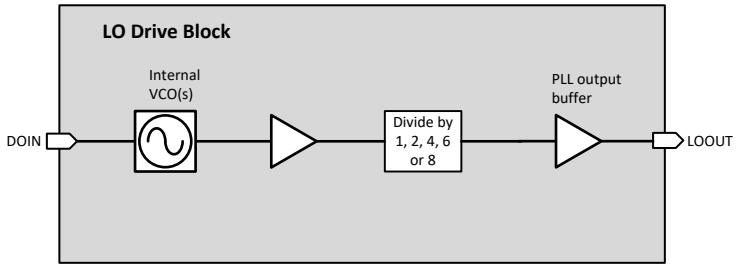


Figure 12 LO Drive Block Schematic

The LO output is designed to operate with a 50Ω load but presents an impedance of typically 130 Ω in parallel with 1 pF. A typical output match from LOOUT is shown in Figure 13 and Table 9. The L-match produced by L1 and C2 loads the LOOUT port with approximately 120Ω, while C1 provides AC coupling. The matching (L1/C2) can be omitted resulting in a reduced output level. In practice, the narrow tracking required to the LOOUT pin is sufficient to provide a good match to 50Ω in the divide by 1 setting. The use of matching for the divided outputs can improve the levels of LO harmonics.

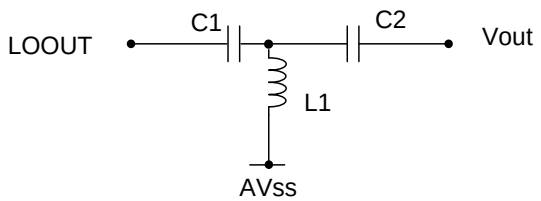


Figure 13 LOOUT Matching Components

Frequency	3200 MHz (divide 1)	1600 MHz (divide 2)	800 MHz (divide 4)	535 MHz (divide 6)	400 MHz (divide 8)
C1	3.9 pF	22 pF	100 pF	180 pF	470 pF
C2	0Ω	2.2 pF	5.6 pF	5.6 pF	8.2 pF
L1	Not Fitted	5.6 nH	12nH	18 nH	30 nH
Note: C1 is selected to be at its series resonant frequency at the LOOUT frequency. Inductor values are from the 0402CS series.					

Table 9 LOOUT Matching Typical Values

6.6 Status and Interrupts

There is a status register ($C4) that indicates the status of the RFPLL lock, the IFPLL lock, the clock-ready status and the RF/IF VCO comparator status signals. There is also an interrupt enable register that allows each of the status bits (or combination thereof) to generate an interrupt on the IRQN pin.

The lock signals from the PLLs are real-time indications of lock status and will be set immediately the PLL attains/regains lock and clear immediately the PLL loses lock. Consequently, if the lock status is enabled for interrupt, the IRQN pin may de-activate before the status register is read.

There will be a third lock status bit which is an AND of the 2 individual PLL lock bits, thus creating a “both in lock” status bit. If only this status bit is enabled for interrupt, the IRQN will behave similarly to a dedicated “in lock” pin (active low). The clock ready status bit can be interrogated by the user to ensure the digital clock is running prior to issuing C-BUS commands that rely on an active clock.

7 Register Description and C-BUS Interface

The C-BUS serial interface supports the transfer of data and control or status information between the CMX979's internal registers and an external host. Each C-BUS transaction consists of the host sending a single Register Address byte, which may then be followed by zero or more data bytes that are written into the corresponding CMX979 register.

Data sent from the host on the Command Data (CDATA) line is clocked into the CMX979 on the rising edge of the Serial Clock (SCLK) input. The C-BUS interface is compatible with common µC/DSP serial interfaces and may also be easily implemented with general purpose I/O pins controlled by a simple software routine. Section 3.1.3.4 gives the detailed C-BUS timing requirements.

Whether a C-BUS register is of read or write type, it is fixed for a given C-BUS register address, thus one cannot both read and write the same C-BUS register address.

In order to provide ease of addressing when using this device with other CML RF devices, the C-BUS addresses below are arranged so as not to overlap those used on the existing CML RF Devices. Thus, a common chip select (CSN) signal can be used, as well as common CDATA, RDATA and SCLK signals.

The following C-BUS register addresses are used:

Table 10 C-BUS Register Map

R/W	Size (bits)	Description	Address
W	0	GEN_RST (Address only, no data)	$30
W	8	GCR	$31
W	16	RFPLL_CON	$34
W	8	RFPLL_BLEED	$35
W	16	RFPLL_LOCKDET	$36
W	16	RFPLL_FLCK	$37
W	8	RFPLL_RDIV	$38
W	16	RFPLL_IDIV	$39
W	16	RFPLL_FDIV0	$3A
W	8	RFPLL_FDIV1	$3B
W	16	IFPLL_NDIV	$3C
W	16	IFPLL RDIV	$3D
W	8	IFPLL_CURRENT	$3E
W	8	LO_CONTROL	$3F
W	8	VCO_CAL_CTRL	$50
W	8	VCO_BIAS_CAL_WRITE	$51
W	8	VCO_BIAS_CAL_TIME	$52
W	16	RFVCO_CAL_WRITE	$53
W	16	RFVCO_CAL_COUNT	$54
W	16	RFVCO CAL_TIME	$55
W	16	RFVCO_STARTUP_TIME	$56
W	16	IFVCO_CAL_WRITE	$57
W	16	IFVCO_CAL_COUNT	$58
W	16	IFVCO_CAL_TIME	$59
W	16	IFVCO_STARTUP_TIME	$5A
R	8	VCO_BIAS_CAL_READ	$5B
R	16	RFVCO_CAL_READ	$5C
R	16	IFVCO_CAL_READ	$5D
R	8	VCO_CAL_STAT	$5E
R	8	GCR_RD	$C1
R	8	DEVICE_STATUS	$C4
W	8	IRQ_ENABLE	$C5
R	8	POWER_STATUS	$C6
R	8	RFPLL_RDIV_RD	$C8
R	16	RFPLL_IDIV_RD	$C9
R	16	RFPLL_FDIV0_RD	$CA
R	8	RFPLL_FDIV1_RD	$CB
R	16	IFPLL_NDIV	$CC
R	16	IFPLL_RDIV_RD	$CD
R	8	IFPLL_CURRENT_RD	$CE

R/W	Size (bits)	Description	Address
R	8	LO_CONTROL_RD	$CF

Notes:

- All registers will retain data if DVDD pin is held high, even if all other power supply pins are disconnected.
- The digital interface can run at a lower voltage than the rest of the device by setting the DV_{DD} supply to the required interface voltage see section 3.1.2.
- If clock and data lines are shared with other devices DV_{DD} must be maintained in its normal operating range, otherwise ESD protection diodes may cause a problem with loading signals connected to SCLK, RDATA and CDATA pins, preventing correct programming of other devices. Other supplies may be turned off and all circuits on the device may be powered down without causing this problem.

7.1 General Reset Command

7.1.1 GEN_RST - $30

(no data)

This command resets the device and clears all bits of all registers. The General Reset command places the device into Powersave mode.

See also section 6.1.

7.2 General Control Register

7.2.1 GCR - $31

8-bit Write
Reset value: $00

This register controls general features such as Powersave.
All bits of this register are cleared to ‘0’ during a General Reset command.

7	6	5	4	3	2	1	0
0	LOOUT	IFPLLEN	ENBIAS	0	RFPLLEN	0	0

GCR b6: LO Output Enable
0: LO output disabled, 1: LO output enabled.
To enable the LO output, the LO Control Register ($3F) b2-0 must be set to a legal value other than ‘000’ divider off.

GCR b5: IF PLL Enable
0: IF PLL disabled, 1: IF PLL enabled.

GCR b4: Bias Pre-enable
0: Bias pre-enable off, 1: Bias pre-enable on.
Setting this bit to “1” enables the bias block, which may be be done ahead of enabling any of the functional blocks. This will reduce the overall turn-on time for any functional block. The bias block is also enabled when any of the functional blocks are enabled, although the turn-on time will be longer, as both the bias block and the functional block need to turn on. Under this condition, bit 4 will remain cleared to ‘0’.

GCR b2: RF PLL Enable
0: RF PLL disabled, 1: RF PLL enabled.

All other bits should be cleared to zero for correct operation.

7.2.2 GCR_RD - $C1

8-bit Read
This register reads the value in register $31, see section 7.2.1 for details of bit functions.

7.3 RF PLL

7.3.1 RFPLL_CON - $34

16-bit Write
Reset value: $0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	Mode select				Enable dither	Res	0	*Reserved*		1	Invert CP	Charge pump current			

RFPLL_CON b15:
Clear to ‘0’

RFPLL_CON b14-b11: Mode select
Set these bits as follows:
0000 - Integer mode operation
0010 - Fractional-N divider with 3rd order MASH 2-1 modulator.
0001 - Fractional-N divider with 3rd order feed-forward modulator.
0011 - Reserved do not use
0100 - Reserved do not use
0101 - Reserved do not use
0110 - Reserved do not use
0111 - Reserved do not use
1000 - Reserved do not use
1001 - Reserved do not use
1010 - Reserved do not use
1011 - Reserved do not use
1100 - Fractional-N divider with 3rd order maximum length MASH 1-1-1 modulator.
1101 - Fractional-N divider with 3rd order maximum length MASH 1-1-1 post-filtered modulator.
1110 - Reserved do not use
1111 - Reserved do not use

RFPLL_CON b10: Enable dither
Set this bit to ‘1’ to add a “dither” to the LSB of the fractional divide value. This helps to suppress idle tones from the sigma-delta modulator output. Set this bit to ‘0’ to disable the dither.

RFPLL_CON b9: Resolution
Set this bit to ‘0’ to select a 24-bit fractional value for the main divider (using registers RFPLL_FDIV1 and RFPLL_FDIV0). Set this bit to ‘1’ to select a 16-bit fractional value for the main divider (using register RFPLL_FDIV0 only).

RFPLL_CON b8:
Clear to ‘0’

RFPLL_CON b7-b6
Reserved, Clear to ‘0’

RFPLL_CON b5:
Set to ‘1’

RFPLL_CON b4: Invert Charge Pump
When this bit is cleared to ‘0’, the charge pump will sink current when the multi modulus divider output frequency is higher than the reference divider output frequency. Set this bit to ‘1’ to invert the charge pump output, so it sources current when the reference divider output frequency is greater than the multi modulus divider output frequency.

RFPLL_CON b3-b0: Charge pump current
Sets the value of the charge pump output current pulses. The value can be set in increments of 25µA, from 25µA (0000) to 400µA (1111).

7.3.2 RFPLL_BLEED - $35

8-bit Write
Reset value: $00

7	6	5	4	3	2	1	0
Reserved		Enable bleed	Bleed_setting				

RFPLL_BLEED b7-b6
Reserved, clear to '0'.

RFPLL_BLEED b5: Enable bleed
Set to '1' to enable a constant bleed current to be sourced into the associated charge pump output pin.

RFPLL_BLEED b4-b0: Bleed current setting
These bits control the nominal bleed current sourced into the charge pump output pin, according to the following formula:

$$I_{bleed} = 3.125\,\mu A \times (1 + Bleed_setting)$$

The bleed current can therefore be set to a value within the range 3.125µA … 100µA. For example, if RFPLL_BLEED bits 4-0 = 1100_2, the resulting nominal bleed current will be 3.125µA×(1+12) = 40.625µA.

7.3.3 RFPLL_LOCKDET - $36

16-bit Write
Reset value: $0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Lock detect enab	*reserved*	Reset lock	*reserved*		Lock window			Loss-of-lock threshold			Lock threshold				

RFPLL_LOCKDET b15: Lock detect enable
Set this bit to '1' to enable the lock detector circuit. Set this bit to '0' to disable and powersave the lock detector circuit.

RFPLL_LOCKDET b14
Reserved, clear to '0'.

RFPLL_LOCKDET b13: Reset lock
Writing a '1' to this bit generates a short pulse that resets the lock detector (either analogue or digital) to an out-of-lock condition and clears DEVICE_STATUS Register bit 0. Immediately after writing a '1' to the reset lock bit, it is cleared back to '0' and the lock detector and lock status bits resume normal operation.

RFPLL_LOCKDET b12-b11
Reserved, clear to '0'.

RFPLL_LOCKDET b10-b8: Lock window
While the lock counter is active (i.e. lock = '1'), these bits determine the phase detector error window: if the difference in arrival time of the phase detector inputs is within this window, they are deemed to be "in phase". When sufficient consecutive "in phase" pulses occur (determined by RFPLL_LOCKDET bits 4-0) then the lock signal gets set to '1'. The nominal value of the error window is shown in the following table:

bits 10-8	*Lock window*	*bits 10-8*	*Lock window*
$0	±7 ns	$4	±30 ns
$1	±10 ns	$5	±50 ns
$2	±15 ns	$6	±70 ns
$3	±20 ns	$7	±100 ns

RFPLL_LOCKDET b7-b5: Loss-of-lock threshold
While the lock indicator is active (lock = '1'), these bits determine how many consecutive "out of phase" signals must occur at the phase detector before loss-of-lock is detected, causing the lock indicator to go inactive (lock = '0'). The loss-of-lock threshold can be set from 1 to 8 ('000' = 8).

RFPLL_LOCKDET b4-b0: Lock threshold
While the lock indicator is inactive (lock = '0'), these bits determine how many consecutive "in phase" signals must occur at the phase detector before lock is detected, causing the lock indicator to go active (lock = '1'). The lock threshold can be set to between 1 and 32 ('00000' = 32).

7.3.4 RFPLL_FLCK - $37

16-bit Write
Reset value: $0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved			Enab fastlck	Fastlock timer coarse divide			Fastlock timer fine divide							Fastlock current	

RFPLL_FLCK b15-b13
Reserved, clear to '0'.

RFPLL_FLCK b12: Enable fastlock
Set to '1' to enable fastlock. Then each time the main divider registers are updated (see section 7.3.8) the associated fastlock pin (FLCK) is pulled to ground, the charge pump current changes to the value set by RFPLL_FLCK bits 1-0, and the fastlock timer is started. The fastlock state continues until the timer expires, at which point the fastlock pin returns to a high impedance state and the charge pump current reverts to the value determined by RFPLL_CON bits 3-0.

RFPLL_FLCK b11-b9: Fastlock timer coarse divide
RFPLL_FLCK b8-b2: Fastlock timer fine divide
These bits control the duration of the fastlock mode. The coarse divide can be set to a value between 0 and 7, and the fine divide can be set to between 1 and 128 ('0000000' = 128). The fastlock timer is clocked by the internal system clock CLK, and its period is given by the following expression:

$$T_{FASTLOCK} = \frac{4^{CoarseDivide} \times FineDivide}{f_{CLK}}$$

RFPLL_FLCK b1-b0: Fastlock current
Set the value of the charge pump output current pulses in fastlock mode. The value is set as a multiple M of the nominal charge pump current:

RFPLL_FLCK_b1-0	Charge pump multiplier
00	4x
01	8x
10	12x
11	16x

To maintain loop stability with fastlock active the resistor R3 shown in Figure 6 will typically need to be set to the following value:

$$R3 \approx \frac{R1}{\sqrt{M} - 1}$$

With fastlock active the PLL lock time is decreased by a factor of approximately $\sqrt{M}$. In practice, an even greater reduction is often achieved because fastlock can reduce or eliminate "cycle slipping" in the phase detector.

7.3.5 RFPLL_RDIV - $38

8-bit Write
Reset value: $00

7	6	5	4	3	2	1	0
Reserved	Reference divider						

RFPLL_RDIV b7
Reserved, clear to '0'.

RFPLL_RDIV b6-b0
Sets the division ratio between the master clock MCLK and the PLL reference clock. This value can be set to between 1 and 128 ('0000000' = 128).

7.3.6 RFPLL_IDIV - $39

16-bit Write
Reset value: $0080

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					Main divider integer value										

RFPLL_IDIV b15-b11
Reserved, clear to '0'.

RFPLL_IDIV b10-b0: Main divider integer value
These bits represent the integer portion closest to the desired fractional-N divider value. The integer value is combined with the fractional value from registers RFPLL_FDIV1 and RFPLL_FDIV0 (which represent a fractional offset of between approximately +0.5 and -0.5) to allow selection of the desired VCO frequency. The valid range for the main divider integer value is from 32 to 2047 (in integer-N mode). When operating in fractional-N mode, the fractional-N range should be adjusted so that when added to the maximum sigma-delta modulus value, the resulting range should not exceed 32-2047 range. This register may be reconfigured during RFPLL operation.

7.3.7 RFPLL_FDIV0 - $3A

16-bit Write
Reset value: $0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Main divider fractional value (LSB)															

See section 7.3.8 for details of bit functions.

7.3.8 RFPLL_FDIV1 - $3B

8-bit Write
Reset value: $00

7	6	5	4	3	2	1	0
Main divider fractional value (MSB)							

RFPLL_FDIV0 b15-b0: Main divider fractional value (LSB)
RFPLL_FDIV1 b7-b0: Main divider fractional value (MSB)
In fractional-N mode, the fractional divide value ranges between approximately -0.5 and +0.5 as determined by the RFPLL_FDIV1 and RFPLL_FDIV0 registers:

With fractional resolution set to 24 bits, the registers are concatenated to form a 24-bit 2's complement number *fdiv*. The resulting fractional divide value is equal to (fdiv ÷ 2^{24}), which is in the range -0.5 to +0.49999994…

With fractional resolution set to 16 bits, the RFPLL_FDIV1 register is ignored and the value in the RFPLL_FDIV0 register is treated as a 16-bit 2's complement number *fdiv*. The fractional divide value is equal to (fdiv ÷ 2^{16}), which is in the range –0.5 to +0.49998474…

In integer-N mode, both the RFPLL_FDIV1 and RFPLL_FDIV0 registers are ignored.
The RFPLL_FDIV1 and RFPLL_FDIV0 registers may be reconfigured during RFPLL operation.

7.3.9 RFPLL_RDIV_RD - $C8

8-bit Read

7	6	5	4	3	2	1	0
Reserved	Reference divider						

This register reads the value in register $38, see section 7.3.5 for details of bit functions.

7.3.10 RFPLL_IDIV_RD - $C9

16-bit Read

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					Main divider integer value										

This register reads the value in register $39, see section 7.3.6 for details of bit functions.

7.3.11 RFPLL_FDIV0_RD - $CA

16-bit Read

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Main divider fractional value (LSB)															

This register reads the value in register $3A, see section 7.3.7 for details of bit functions.

7.3.12 RFPLL_FDIV1_RD - $CB

8-bit Read:

7	6	5	4	3	2	1	0
Main divider fractional value (MSB)							

This register reads the value in register $3B, see section 7.3.8 for details of bit functions.

7.4 IF PLL

7.4.1 IFPLL_NDIV - $3C

16-bit Write
Reset value: $0080

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		N Divider													

IFPLL_NDIV b15-b14
Reserved, clear to '0'.

IFPLL_NDIV b13-b0
Phase Locked Loop N divider value (must be greater than or equal to 25).

This register sets the N divider value for the PLL (Feedback divider). Note: To enable the PLL, b5 of the General Control Register ($31) also needs to be set.

7.4.2 IFPLL_RDIV - $3D

16-bit Write
Reset value: $0002

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved							R Divider								

IFPLL_R_DIV b15-b9
Reserved, clear to ‘0’.

IFPLL_R DIV b8-b0
Phase Locked Loop R divider value (must be greater than or equal to 2).

This register sets the R divider value for the PLL (Reference divider). Register updates can be asynchronous to the IFPLL phase detector clock.

7.4.3 IFPLL_CURRENT - $3E

8-bit Write
Reset value: $00

7	6	5	4	3	2	1	0
IF VCO Bias	*Reserved*			Charge pump current			

IFPLL_CURRENT b7: IF VCO Bias
IF VCO bias control for optimum phase noise performance. When cleared to ‘0’ (default), sets the IF VCO bias current to “low”, when set to 1 set bias current to high.
High current should be choosen for IF VCO oscillation frequencies greater than 700MHz.

IFPLL_CURRENT b6-b4
Reserved, clear to ‘0’.

IFPLL_CURRENT b3-b0: Charge pump current
Sets the value of the charge pump output current pulses. The value can be set in increments of 25µA, from 25µA (0000) to 400µA (1111).

7.4.4 IFPLL_NDIV_RD - $CC

16-bit Read

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		N Divider													

This register reads the value in register $3C, see section 7.4.1 for details of bit functions.

7.4.5 IFPLL_RDIV_RD - $CD

16-bit Read

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved							R Divider								

This register reads the value in register $3D, see section 7.4.2 for details of bit functions.

7.4.6 IFPLL_CURRENT_RD - $CE

8-bit Read

7	6	5	4	3	2	1	0
IF VCO Bias	*Reserved*			Charge pump current			

This register reads the value in register $3E, see section 7.4.3 for details of bit functions.

7.5 VCO Calibration

7.5.1 VCO_CAL_CTRL - $50

16-bit Write
Reset value: $1400

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MCLK FREQUENCY SET								*Reserved*					IFVCO Start	RFVCO Start	Bias Start

VCO_CAL_CTRL b15-b8
Value set to divide MCLK input clock (MHz rounded to the nearest integer, with a minimum value of 1) to provide a 1MHz clock, used as 1µs timing reference for the VCO Calibration ciurcuits. The default value of the MCLK_FREQ field is 20.

VCO_CAL_CTRL b7-b3
Reserved, clear to ‘0’.

VCO_CAL_CTRL b2
Writing a ‘1’ to this bit initiates IFVCO frequency calibration.

VCO_CAL_CTRL b1
Writing a ‘1’ to this bit initiates RFVCO frequency calibration.

VCO_CAL_CTRL b0
Writing a ‘1’ to this bit initiates BIAS calibration. The bias calibration should be initiated before frequency calibration.

For further details see section 6.3.4.

7.5.2 VCO_BIAS_CAL_WRITE - $51

8-bit Write
Reset value: $00

7	6	5	4	3	2	1	0
Reserved			VCO bias cal setting				

VCO_BIAS_CAL_WRITE b7-b5
Reserved, clear to ‘0’.

VCO_BIAS_CAL_WRITE b4-b0
VCO bias calibration setting.

For further details see section 6.3.4.

7.5.3 VCO_BIAS_CAL_TIME - $52

8-bit Write
Reset value: $06

7	6	5	4	3	2	1	0
Reserved		Bias cal settling period in µs					

VCO_BIAS_CAL_TIME b7-b6
Reserved, clear to ‘0’.

VCO_BIAS_CAL_TIME b5-b0
Bias calibration settling period in µs.
The minimum recommended value for VCO_BIAS_CAL_TIME = 6.

For further details see section 6.3.4.

7.5.4 RFVCO_CAL_WRITE - $53

16-bit Write
Reset value: $0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved							Calibration Code								

RFVCO_CAL_WRITE b15-b9
Reserved, clear to '0'.

RFVCO_CAL_WRITE b8-b0
Calibration Code.

For further details see section 6.3.4.

7.5.5 RFVCO_CAL_COUNT - $54

16-bit Write
Reset value: $015E

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						RF VCO open-loop calibration reference clock cycles									

Default RF VCO open-loop calibration reference clock cycles = 350.
The default value assumes a 3500MHz RF VCO operating frequency.
This value should be set to the RF VCO operating frequency in MHz divided by 10.

For further details see section 6.3.4.

7.5.6 RFVCO_CAL_TIME - $55

16-bit Write
Reset value: $0D06

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PLL settling time after closing loop x 8µs								Closed-loop calibration settling time x 8µs							

Default PLL settling time after closing loop = 104µs.
Default Closed-loop calibration settling time = 48µs.

For further details see section 6.3.4.

7.5.7 RFVCO_STARTUP_TIME - $56

16-bit Write
Reset value: $012C

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				RFVCO Start-up time in µs											

Default RF VCO start-up time = 300µs.

For further details see section 6.3.4.

7.5.8 IFVCO_CAL_WRITE - $57

16-bit Write
Reset value: $0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved							Calibration Code								

For further details see section 6.4.2.

7.5.9 IFVCO_CAL_COUNT - $58

16-bit Write
Reset value: $01C2

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						IF VCO open-loop calibration reference clock cycles									

Default IF VCO open-loop calibration reference clock cycles = 450.
The default value assumes a 900MHz IF VCO operating frequency.
This value should be set to the IF VCO operating frequency in MHz divided by 2.

For further details see section 6.4.2.

7.5.10 IFVCO_CAL_TIME - $59

16-bit Write
Reset value: $0D0D

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PLL settling time after closing loop x 8µs								Closed-loop calibration settling time x 8µs							

Default PLL settling time after closing loop = 104µs.
Default Closed-loop calibration settling time = 104µs.

For further details see section 6.4.2.

7.5.11 IFVCO_STARTUP_TIME - $5A

16-bit Write
Reset value: $0145

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				IFVCO Start-up time in µs											

Default IF VCO start-up time = 325µs. For further details see section 6.4.2.

7.5.12 VCO_BIAS_CAL_READ - $5B

8-bit Read
Reset value: $00
Only valid when VCO_CAL_STAT bit 0 is ‘0’.

7	6	5	4	3	2	1	0
Reserved			VCO bias cal setting				

This register reads the value in register $51, see section 7.5.2 for details of bit functions.

7.5.13 RFVCO_CAL_READ - $5C

16-bit Read
Reset value: $0000
Only valid when VCO_CAL_STAT bit 1 is ‘0’.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved							Calibration Code								

This register reads the value in register $53, see section 7.5.4 for details of bit functions.

7.5.14 IFVCO_CAL_READ - $5D

16-bit Read
Reset value: $0000
Only valid when VCO_CAL_STAT bit 2 is 0.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved							Calibration Code								

This register reads the value in register $57, see section 7.5.8 for details of bit functions.

7.5.15 VCO_CAL_STAT - $5E

8-bit Read
Reset value: $00

7	6	5	4	3	2	1	0
Reserved					IFVCO	RFVCO	BIAS

This register gives status information on calibration initiated in register $50, see section 7.5.1.

VCO_CAL_STAT b2
Read ‘0’ = Idle, ‘1’ = IF VCO Calibration in progress.

VCO_CAL_STAT b1
Read ‘0’ = Idle, ‘1’ = RF VCO Calibration in progress.

VCO_CAL_STAT b0
Read ‘0’ = Idle, ‘1’ = BIAS Calibration in progress.

7.6 LO Control

7.6.1 LO_CONTROL - $3F

8-bit Write
Reset value: $00
PLL Output Control Mode.

7	6	5	4	3	2	1	0
Reserved		IFPLLDIV		*Reserved*	LODIV		

LO_CONTROL b7-b6
Reserved, clear to ‘0’.

LO_CONTROL b5-b4: IFPLLDIV
The IFPLLDIV bits control the output divider, which drives the IFPLL signal onto the IFPLLOUT pin.

b5	b4	Function
0	0	Divide by 1
0	1	Divide by 4
1	0	Divide by 8
1	1	Divide by 16

LO_CONTROL b3
Reserved, clear to ‘0’.

LO_CONTROL b2-b0: LODIV
The LODIV bits control the LO divider, which is part of the LO output function.

b2	b1	b0	Function
1	1	1	Divide by 8
1	1	0	Illegal value, do not use
1	0	1	Divide by 6
1	0	0	Divide by 4
0	1	1	Illegal value, do not use
0	1	0	Divide by 2
0	0	1	Divide by 1
0	0	0	Divider off

7.6.2 LO_CONTROL_RD - $CF

8-bit Read

7	6	5	4	3	2	1	0
Reserved		IFPLLDIV		*Reserved*	LODIV		

This register reads the value in register $3F, see section 7.6.1 for details of bit functions.

7.7 Device Status Register

7.7.1 DEVICE_STATUS - $C4

8-bit Read

7	6	5	4	3	2	1	0
Clock Ready	RF VCO Calibrate HI	RF VCO Calibrate LO	IF VCO Calibrate HI	IF VCO Calibrate LO	IF and RF PLL Lock	IF PLL Lock	RF PLL Lock

If the corresponding bit in the IRQ_ENABLE register ($C5) is ‘0’, this register bit provides a real-time indication of the status at the time the register is read. See section 7.8.1.

If the corresponding bit in the IRQ_ENABLE register is ‘1’, this register bit is set to ‘1’ when a specific transition in the status is detected and an active low interrupt will be raised on the IRQN pin. The register bit is cleared to ‘0’ on reading the DEVICE_STATUS register.

The DEVICE_STATUS register bits require the PLL reference clock to be active. If neither PLL is enabled, the PLL reference clock will be disabled and the DEVICE_STATUS register bits will be automatically cleared.

DEVICE_STATUS b7: Clock Ready
If the corresponding bit in the IRQ_ENABLE register is ‘0’, this bit will reflect the status of the PLL reference clock:

0 = PLL reference clock is internally disabled or has not yet stabilised after being enabled and functions requiring this clock are prohibited.
1 = PLL reference clock has started successfully.

If the corresponding bit in the IRQ_ENABLE register is ‘1’, the bit will be set to ‘1’ on detecting a positive transition in the Clock Ready status.

DEVICE_STATUS b6: RF VCO Calibration HI
If the corresponding bit in the IRQ_ENABLE register is ‘0’, this bit will reflect the status of the RF VCO Calibration HI voltage comparator output:

0 = RF VCO tune voltage is below the HI voltage threshold.
1 = RF VCO tune voltage is above the HI voltage threshold indicating the RF VCO has drifted too low in frequency and requires recalibration, either by entering a larger calibration code directly or by performing a new auto-calibration routine as outlined in section 6.3.4.1. This bit may change during RF VCO calibration.

If the corresponding bit in the IRQ_ENABLE register is '1', the bit will be set to '1' on detecting a positive transition in the RF VCO Calibration HI status. This bit may change during RF VCO calibration and it is therefore recommended that the corresponding IRQ_ENABLE bit is only set after calibration has completed.

DEVICE_STATUS b5: RF VCO Calibration LO
If the corresponding bit in the IRQ_ENABLE register is '0', this bit will reflect the status of the RF VCO Calibration LO voltage comparator output:

0 = RF VCO tune voltage is above the LO voltage threshold.
1 = RF VCO tune voltage is below the LO voltage threshold indicating the RF VCO has drifted too high in frequency and requires recalibration, either by entering a smaller calibration code directly or by performing a new auto-calibration routine as outlined in section 6.3.4.1. This bit may change during RF VCO calibration.

If the corresponding bit in the IRQ_ENABLE register is '1', the bit will be set to '1' on detecting a positive transition in the RF VCO Calibration LO status.

DEVICE_STATUS b4: IF VCO Calibration HI
If the corresponding bit in the IRQ_ENABLE register is '0', this bit will reflect the status of the IF VCO Calibration HI voltage comparator output:

0 = IF VCO tune voltage is below the HI voltage threshold.
1 = IF VCO tune voltage is above the HI voltage threshold indicating the IF VCO has drifted too low in frequency and requires recalibration, either by entering a larger calibration code directly or by performing a new auto-calibration routine as outlined in section 6.3.4.1. This bit may change during IF VCO calibration.

If the corresponding bit in the IRQ_ENABLE register is '1', the bit will be set to '1' on detecting a positive transition in the IF VCO Calibration HI status. This bit may change during IF VCO calibration and it is therefore recommended that the corresponding IRQ_ENABLE bit is only set after calibration has completed.

DEVICE_STATUS b3: IF VCO Calibration LO
If the corresponding bit in the IRQ_ENABLE register is '0', this bit will reflect the status of the IF VCO Calibration LO voltage comparator output:

0 = IF VCO tune voltage is above the LO voltage threshold.
1 = IF VCO tune voltage is below the LO voltage threshold indicating the IF VCO has drifted too high in frequency and requires recalibration, either by entering a smaller calibration code directly or by performing a new auto-calibration routine as outlined in section 6.3.4.1. This bit may change during IF VCO calibration.

If the corresponding bit in the IRQ_ENABLE register is '1', the bit will be set to '1' on detecting a positive transition in the IF VCO Calibration LO status. This bit may change during IF VCO calibration and it is therefore recommended that the corresponding IRQ_ENABLE bit is only set after calibration has completed.

DEVICE_STATUS b2: IF and RF PLL Lock
If the corresponding bit in the IRQ_ENABLE register is '0', this bit reflects the PLLs lock status:

0 = IF PLL and RF PLL are not both locked.
1 = IF PLL and RF PLL are both locked.

If the corresponding bit in the IRQ_ENABLE register is '1', this bit will be set to '1' on detecting a negative transition in either PLL lock status. This indicates that either PLL has lost lock. Note, this is the opposite sense to the status indication.

DEVICE_STATUS b1: IF PLL Lock
If the corresponding bit in the IRQ_ENABLE register is '0', this bit reflects the IF PLL lock status:

0 = IF PLL is not locked.
1 = IF PLL is locked.

If the corresponding bit in the IRQ_ENABLE register is '1', this bit will be set to '1' on detecting a negative transition in the IF PLL lock status. This indicates the IF PLL has lost lock. Note, this is the opposite sense to the status indication.

DEVICE_STATUS b0: RF PLL Lock
If the corresponding bit in the IRQ_ENABLE register is '0', this bit reflects the RF PLL lock status:

0 = RF PLL is not locked.
1 = RF PLL is locked.

If the corresponding bit in the IRQ_ENABLE register is ‘1’, this bit will be set to ‘1’ on detecting a negative transition in the RF PLL lock status. This indicates the RF PLL has lost lock. Note, this is the opposite sense to the status indication.

7.8 Interrupt Enable Register

7.8.1 IRQ_ENABLE - $C5

8-bit Write
Reset value: $80

7	6	5	4	3	2	1	0
Clock Ready Interrupt Enable	RF VCO Comp HI Interrupt Enable	RF VCO Comp LO Interrupt Enable	IF VCO Comp HI Interrupt Enable	IF VCO Comp LO Interrupt Enable	IF & RF PLL Lock Interrupt Enable	IF PLL Lock Interrupt Enable	RF PLL Lock Interrupt Enable

IRQ Enable Register b7-b0 : Interrupt enables for DEVICE_STATUS bits

If the enable bit is ‘0’, the corresponding bit in the DEVICE_STATUS register provides a real-time indication of the status at the time the register is read. If the enable bit is ‘1’, the corresponding bit in the DEVICE_STATUS register is set to ‘1’ when a specific event is detected and an active low interrupt will be raised on the IRQN pin. The register bit is cleared to ‘0’ on reading the DEVICE_STATUS register.

7.9 Power Status Register

7.9.1 POWER_STATUS - $C6

8-bit Read

7	6	5	4	3	2	1	0
Reserved				Digital Ready	RF Functions Ready	IF PLL Ready	RF PLL Ready

Power Status Register b7-b4
Reserved, clear to ‘0’.

Power Status Register b3-b0
When the respective bit is set to ‘1’, the relevant power domain and bandgap is at its working level. There is a 15µs of delay between enabling an analogue block and the supplies being available for use.

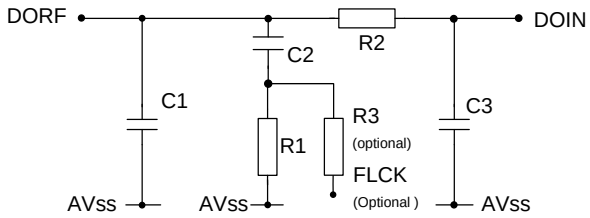
8 Application Notes

8.1 Loop Filter Design

The design of the loop filter for phase locked loops is relatively simple in principle but can be complex in practice. It is impossible in a datasheet to cover all aspects of loop filter design; for those interested in the detail please consult one of the many text books on phase locked loops. This datasheet provides some specific guidance for the CMX979 PLLdesign.

8.1.1 RF PLL (Fractional N)

The Loop Filter design is based upon the use of a passive 3rd order Loop Filter as shown below.



The loop filter can be considered as two pole filter (R1, C1, C2) with the addition of a single pole spur filter (R2,C3) added to attenuate spurs.

The two pole loop filter consists of a resistor R1 in series with a capacitor C2 and C1. The resistor provides the stabilizing zero to improve the phase margin and hence improve the transient response of the PLL. However, the resistor causes a ripple of value I_{CP} x R1 on the control voltage at the beginning of each phase detector pulse. At the end of the pulse, a ripple of equal value occurs in the opposite direction. This ripple modulates the VCO frequency and introduces excessive jitter in the output. A small capacitor C1 is added in parallel with the R1 and C2 network to suppress the glitch generated by the charge pump at every phase comparison instant, which in turn lowers the ripple on the control voltage the ripple and acts to suppress the induced jitter.

C1 should remain below C2 roughly by a factor of 10 so as to avoid underdamped settling. The choice of the loop parameters, R1, C2 and C1 can be determined by assuming a continuous time approximation. In a typical application the loop bandwidth, is set to between F_{Comp} /25 and F_{Comp} /100. This value is a compromise as a lower loop bandwidth helps to filter out reference or integer boundary spurs in the PLL output, but a higher loop bandwidth decreases lock time and helps reduce PLL jitter by filtering out noise (esp. flicker noise) within the loop bandwidth.

The frequency at which the PLL open loop phase margin is a maximum, should coincide with the chosen loop bandwidth. The resistor R1, in combination with C1 & C2 capacitors in the two pole loop filter, determines the frequency where the peak phase margin is achieved.

The important loop equations for the two pole filter are as follows:

(1) $C2 = I_{cp} K_{vco} / N (2\pi F_n)^2$
(2) $R1 = 2\xi\sqrt{(N/ I_{cp} K_{vco} C2)}$
(3) $C1 = C2/10$
(4) $BW = \pi F_n [\xi + (1/4 \xi)]$
(5) $\omega_n = 2\pi F_n$
(6) $PM \sim 100\xi$

where

Fref is the reference clock applied to the ICr
F_{Comp} is the phase detector comparison frequency (= Fref / N)
N is feedback divider value
I_{cp} is charge pump current (A/2πrad)
K_{vco} is vco gain (MHz/V)
F_n is the natural loop frequency
BW is the loop bandwidth
PM is the phase margin
ξ is the damping factor

Now looking at the single pole spur filter R2 and C3, the attenuation and time constant T3 can be defined as:

(7) Atten = 10log $[(2\pi F_{Comp} R2C3)^2 + 1]$ and

(8) T3 = R2C3.

Then in terms of the attenuation of the comparison frequency spurs added by the single pole filter we have:

(9) $T3 = \sqrt{[(10^{(Atten/10)} - 1)/(2\pi F_{Comp})^2]}$

The additional pole must be lower than the comparison frequency F_{Comp} in order to attenuate spurs, but should be at least 5 times greater than the loop bandwidth, otherwise the loop may become unstable.

In general C3 should be chosen to be ≤ C1/10 otherwise T3 will interact with the poles primary two pole filter, R2 should be chosen to be at least twice the value of R1.

Worked example:

VCO frequency = 3GHz, F_{Comp} = 4.8MHz, I_{cp} = 400uA, K_{vco} = 70MH/V, BW = 48kHz (F_{Comp} /100), Fn = 14kHz, Atten=13dB , ξ =0.707

a) N = 3e09 / 4.8e06 = 625
b) C2 = 5.78nF
c) R1 = 2.78kΩ
d) C1 = 579pF
e) T3 = 1.57e-07
f) Let R2 = 2R1, = 5.6kΩ
g) C3 = T3/R2 = 28pF

The choice should now be made of preferred values for R1, R2, C1, C2 and C3 using +/-1% on resistors and +/- 5% on capacitors, which would be C1 = 680pF, C2 = 5.6nF, C3 = 27pF, R1 = 2.2kΩ, R2 = 5.6kΩ.

The preferred values chosen should then be tested in the application and adjustment can then be made to optimise the loop response as required.

8.2 Phase Noise Performance

8.2.1 RF PLL

The RF PLL typical phase noise profiles are shown in Figure 14, Figure 15 and Figure 16. The effect of the divider is demonstrated in Figure 15.

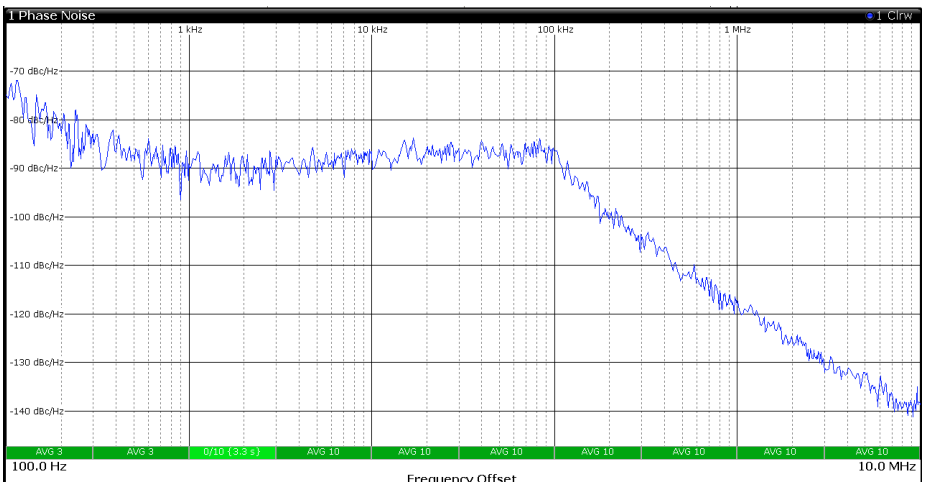


Figure 14 Phase noise plot of 3.6GHz RF PLL, Icp=400µA, F_{Comp} =38.4MHz, using internal VCO, 60kHz loop bandwidth, PLL type '1100'

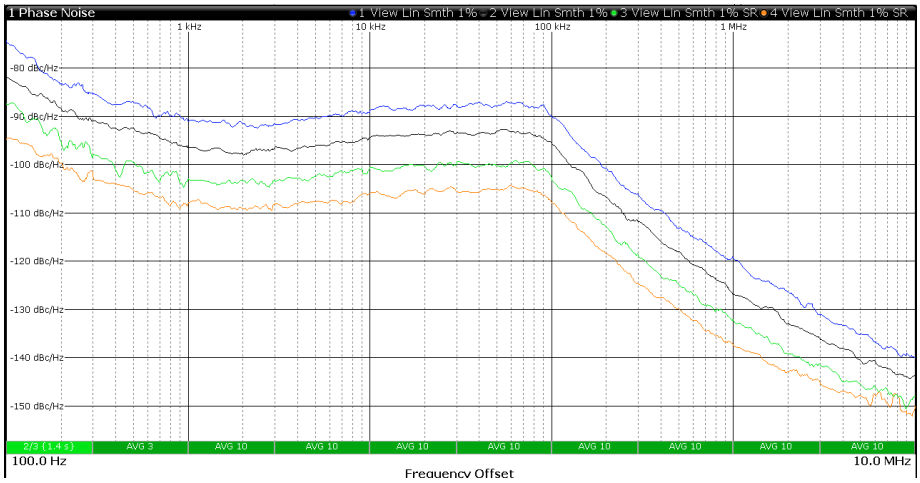


Figure 15 Phase noise plot of 3.201GHz RF PLL, Icp=400µA, F_{Comp} =38.4MHz, using internal VCO, 60kHz loop bandwidth, PLL type '1100' also showing output in /2 mode (1600MHz), /4 mode (800MHz) and /8 mode (400MHz)

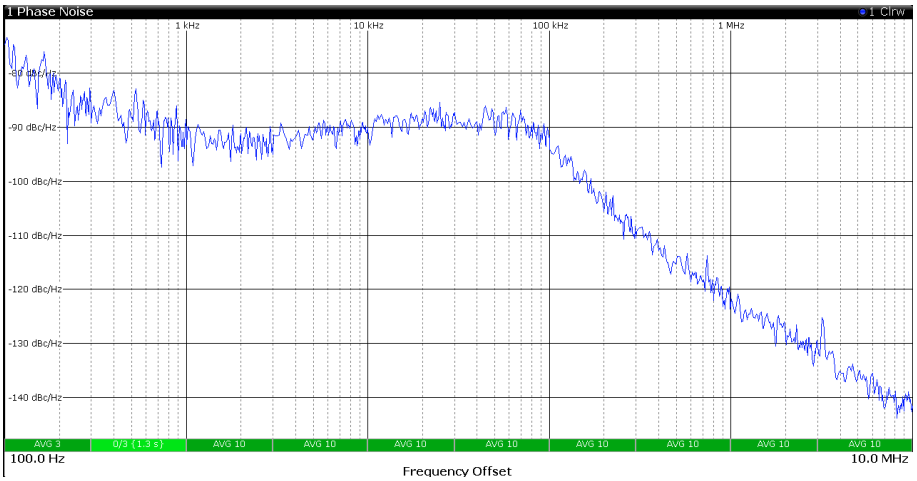


Figure 16 Phase noise plot of 2.8GHz RF PLL, Icp=400µA, F_{Comp} =38.4MHz, using internal VCO, 60kHz loop bandwidth, PLL type '1100'

8.2.2 IF PLL Phase Noise

The IF PLL has a typical phase noise profile as shown in Figure 17 for 900MHz using the internal IF_VCO.

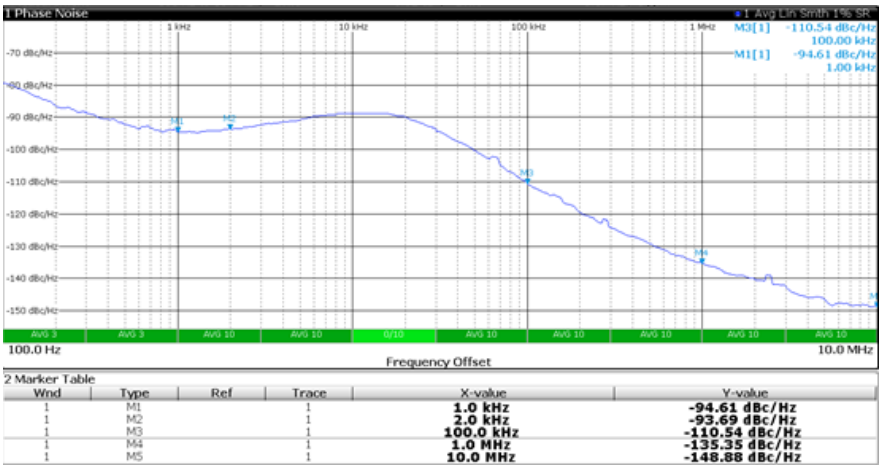


Figure 17 Phase noise plot of 900MHz IF PLL, Icp=400µA, F_{Comp} =1.2MHz, Kvco=10MHz/V

8.3 RF PLL Lock Time

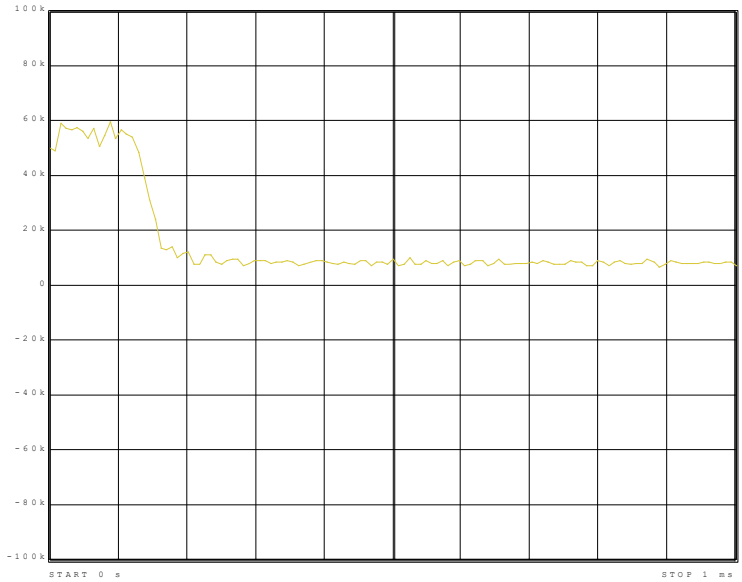


Figure 18 Lock time for frequency change 2.850GHz to 3.450GHz, Icp=400µA, F_{Comp} =19.2MHz, using internal VCO , 60 kHz loop bandwidth, PLL type '1100', without Fastlock function, Jump =300µs

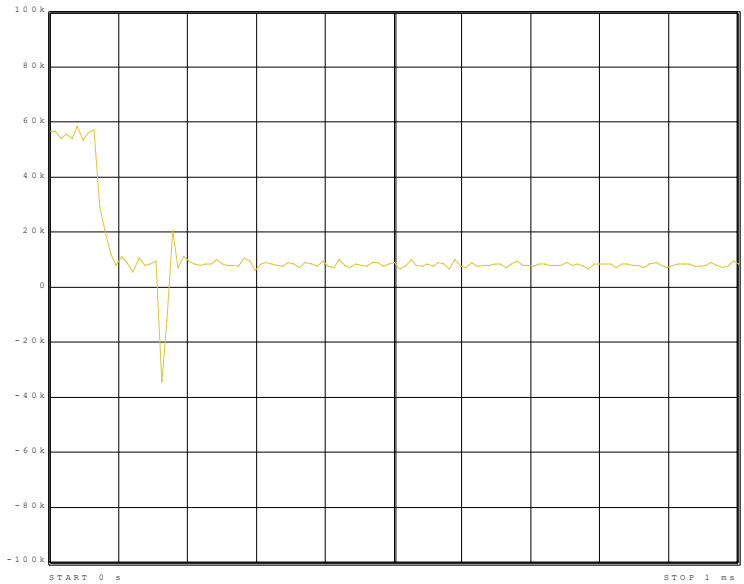


Figure 19 Lock time for frequency change 2.850GHz to 3.450GHz, Icp=400µA, F_{Comp} =19.2MHz, using internal VCO , 60kHz loop bandwidth, PLL type '1100', with Fastlock function (x12, 100µs), Jump =200µs

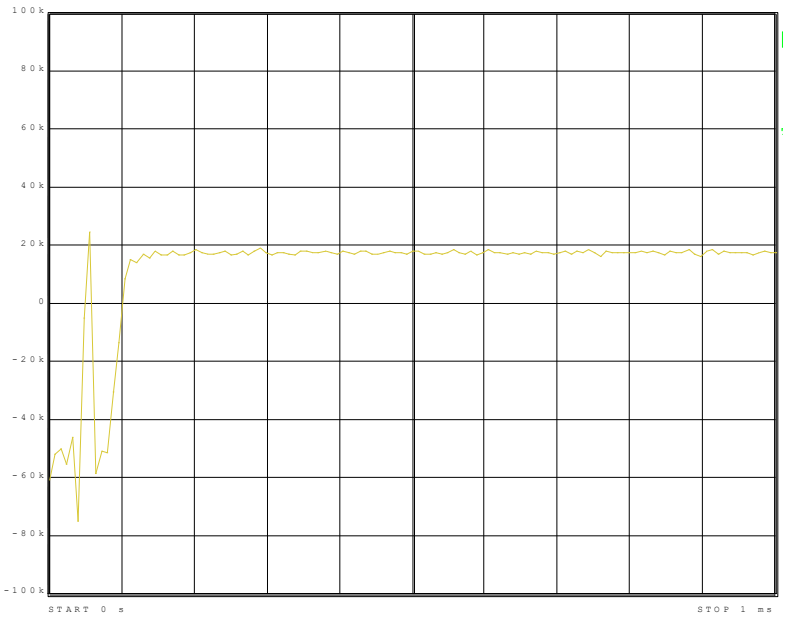


Figure 20 Lock time for frequency change 3.205 to 3.195GHz, Icp=400µA, F_{Comp} =19.2MHz, using internal VCO , 60kHz loop bandwidth, PLL type '1100', without Fastlock function, Jump = 150µs

8.4 RF PLL Spurious

8.4.1 Types of Spurious

Spurious signals (spurs for short) from a Fractional-N PLL can occur at offsets from the main output of:

- The input Master reference frequency (sidebands at +/- MCLK and harmonics)
- The loop comparison frequency (sidebands at +/- F_{Comp}, i.e. +/- MCLK/RDIV and harmonics)
- Frequencies offset from the integer-N frequency (e.g. at N x F_{Comp}, also referred to as 'Integer Boundary Spurs' or 'IBS'). These can be reduced by the action of the loop filter.
- Frequencies offset from simple fractions of the integer-N frequency (also referred to as 'high order boundary spurs'). These can be reduced by the action of the loop filter.

Frequency planning for the particular application, along with avoidance techniques, can be used to minimise some of these effects.
The spurs can also be reduced in level through use of the output frequency dividers (although other spurs can also be generated).

All of the above spur types can be observed in the CMX979.

8.4.2 MCLK Sidebands

Sidebands can occur at offsets of the input reference frequency (sidebands at +/- MCLK and harmonics). PCB Layout, decoupling, MCLK frequency and signal level, harmonic content and on-chip coupling can all have an effect on these levels. Fast MCLK edges are required for the lowest noise performance, but this can be at the detriment of spur level.

8.4.3 Comparison Frequency Sidebands

Sidebands can occur at offsets of the Comparison Frequency (sidebands at +/- F_{Comp} and harmonics). These spurs are largely reduced by the action of the loop filter.

If F_{Comp} = MCLK, the resulting spur levels may be higher than for the MCLK or F_{Comp} spur alone.

8.4.4 MCLK Boundaries

Spurs occur where F_{VCO} is close to N x MCLK, so a large MCLK frequency creates the lowest number of MCLK boundaries. For a given application, a frequency plan should avoid these where possible. A solution is to use two non-harmonically related MCLK sources and switch between them as appropriate.

8.4.5 FComp Boundaries

Spurs occur where F_{VCO} is close to N x F_{Comp}.

Mathematically, these spurs occur at frequencies of +/- the fractional component of N from the VCO frequency. If these are at a sufficiently large offset, then they are reduced by the action of the loop filter. A software routine can be used to determine if the fraction is sufficiently small to cause a problem (i.e. not be sufficiently attenuated by the loop filter).

One solution is to use two different RDIV values (e.g. divide by 4 or 5) and switch between them as appropriate.

If this is coupled with switching MCLK reference sources, many spurious can be avoided.

8.4.6 Higher Order Boundaries

These spurs occur at offsets from simple fractions. For example, if a frequency is programmed at say 10kHz from a 0.5 fraction, spurs can occur at +/- 20kHz and +/- 40kHz (i.e. at harmonics of 20kHz); if 10kHz from a 0.3333 fraction, spurs can occur at approximately +/- 30kHz; if a frequency is programmed at 10kHz from a 0.25 fraction, spurs occur at +/- 40kHz.

The amplitude of these reduce with order and offset from the 'simple fraction'. In practice, a fraction of 1/3 cannot be exactly determined digitally, so there will then be a strong fractional component at +/- (offset + FComp /(2^N)) where N is the number of fractional bits.

Frequency planning can predict where these occur, so again a different RDIV value could be used to avoid these. At small offsets from a 'simple fraction', these can land within the loop bandwidth.

Boundary spurious can also be reduced by applying a small value of bleed current (see section 7.3.2), however this will increase the level of the comparison frequency spurs.

8.5 IF PLL Spurious

The IF PLL has spurious products that occur at multiples of the MCLK reference frequency.

As an example, if a 19.2MHz MCLK is used, with IFPLL_RDIV = 0x0A (10 decimal) and IFPLL_NDIV = 0x01D5 (469 decimal), this gives a programmed VCO frequency of 900.48MHz.

A fixed spur will occur at 47 x MCLK (902.4MHz). In this instance, this will also coinside with a comparison frequency spur (+/- 1.92MHz) at typically -69 dBc.

If the programming is changed to IFPLL_NDIV = 0x01D4 (468 decimal), this gives a programmed VCO frequency of 898.56MHz. The comparison frequency spurs (+/- 1.92MHz) are typically -86 dBc, however a spur will still be present at 902.4MHz (and its image about the carrier) at around -76 dBc.

The spur continues to reduce with increasing separation from odd multiples of MCLK. The spur also occurs around even multiples, but at a lower level. This spur is independent of charge pump current setting.

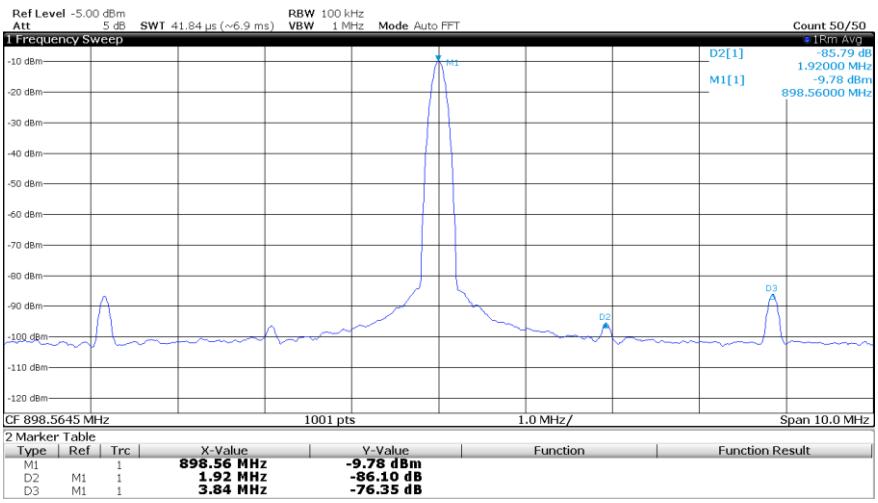
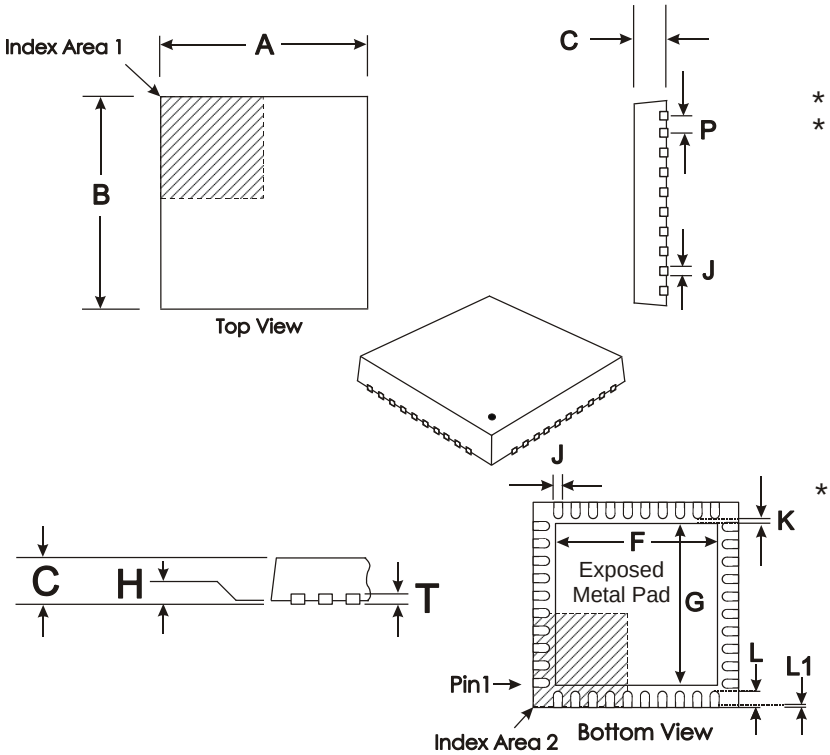


Figure 21 Reference spur plot of 900MHz IF PLL

9 Packaging

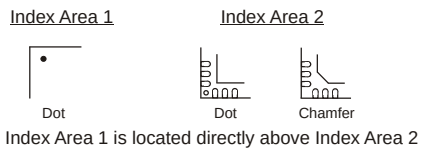


	DIM.	MIN.	TYP.	MAX.
*	A		6.00 BSC	
*	B		6.00 BSC	
	C	0.80	0.90	1.00
	F	3.95		4.30
	G	3.95		4.30
	H	0.00		0.05
	J	0.18	0.25	0.30
	K	0.20		
	L	0.30	0.40	0.50
	L1	0		0.15
	P		0.50	
	T		0.20	

NOTE :

* A & B are reference data and do not include mold deflash or protrusions.

All dimensions in mm
Angles are in degrees



Index Area 1 is located directly above Index Area 2

Depending on the method of lead termination at the edge of the package, pull back (L1) may be present.
L minus L1 to be equal to, or greater than 0.3mm
The underside of the package has an exposed metal pad which should ideally be soldered to the pcb to enhance the thermal conductivity and mechanical strength of the package fixing. Where advised, an electrical connection to this metal pad may also be required

Figure 22 Q4 Mechanical Outline

9.1 Ordering Information

Order as Part No. CMX979Q4

Handling precautions: This product includes input protection, however, precautions should be taken to prevent device damage from electro-static discharge. CML does not assume any responsibility for the use of any circuitry described. No IPR or circuit patent licences are implied. CML reserves the right at any time without notice to change the said circuitry and this product specification. CML has a policy of testing every product shipped using calibrated test equipment to ensure compliance with this product specification. Specific testing of all circuit parameters is not necessarily performed.

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