

# R1LV0216BSB

2Mb Advanced LPSRAM (128k word x 16bit)

R10DS0273EJ0101  
Rev.1.01  
2020.2.20

## Description

The R1LV0216BSB is a family of low voltage 2-Mbit static RAMs organized as 131,072-word by 16-bit, fabricated by Renesas's high-performance 0.15um CMOS and TFT technologies. The R1LV0216BSB has realized higher density, higher performance and low power consumption. The R1LV0216BSB is suitable for memory applications where a simple interfacing, battery operating and battery backup are the important design objectives. The R1LV0216BSB has been packaged in 44-pin TSOP.

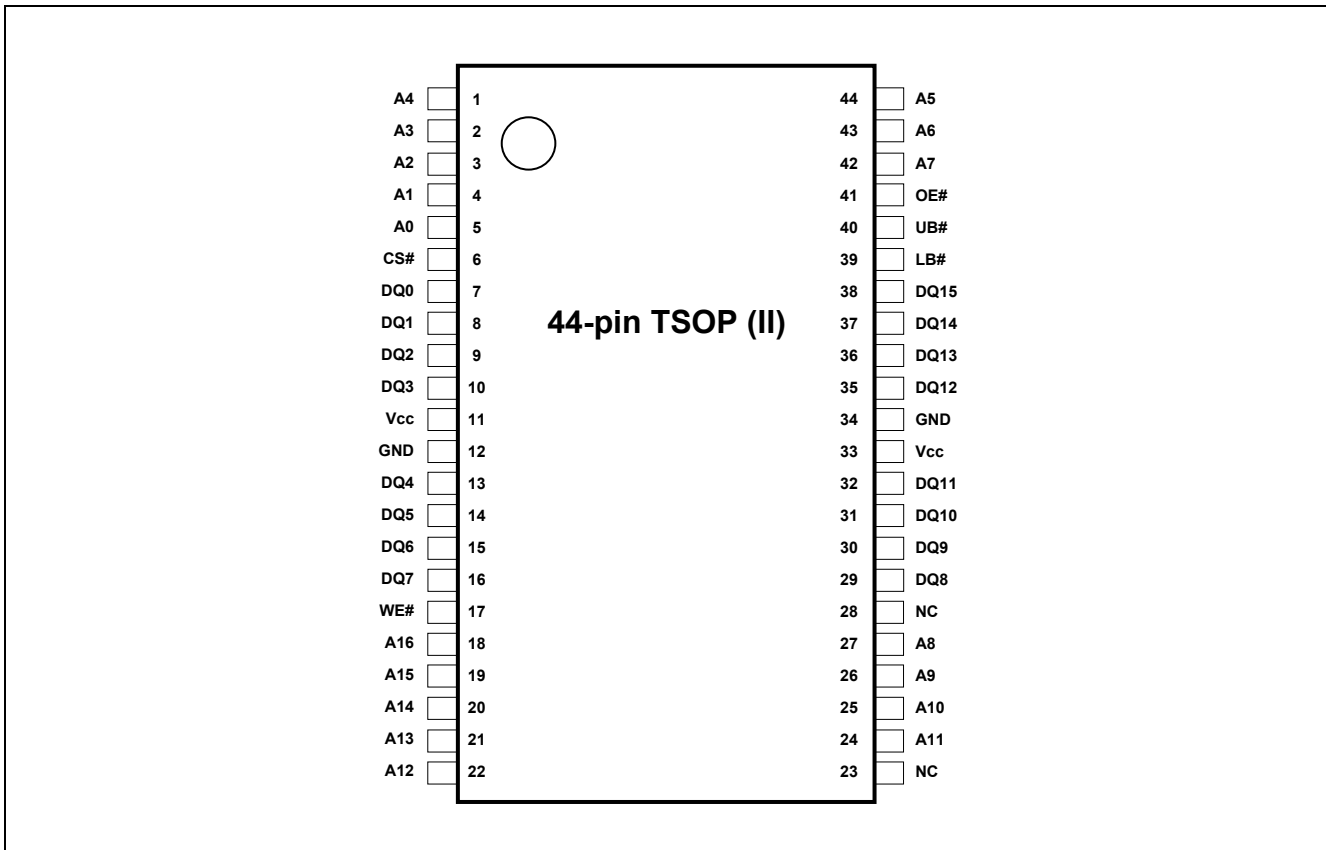
## Features

- Single 2.7V~3.6V power supply
- Small stand-by current: 1μA (3.0V, typical)
- No clocks, No refresh
- All inputs and outputs are TTL compatible.
- Easy memory expansion by CS#, LB# and UB#
- Common Data I/O
- Three-state outputs: OR-tie Capability
- OE# prevents data contention on the I/O bus

## Ordering Information

Orderable part name	Access time	Temperature range	Package	Shipping container
R1LV0216BSB-5SI#B1	55 ns	-40 ~ +85°C	400-mil 44pin plastic TSOP (II)	Tray
R1LV0216BSB-5SI#S1				Embossed tape

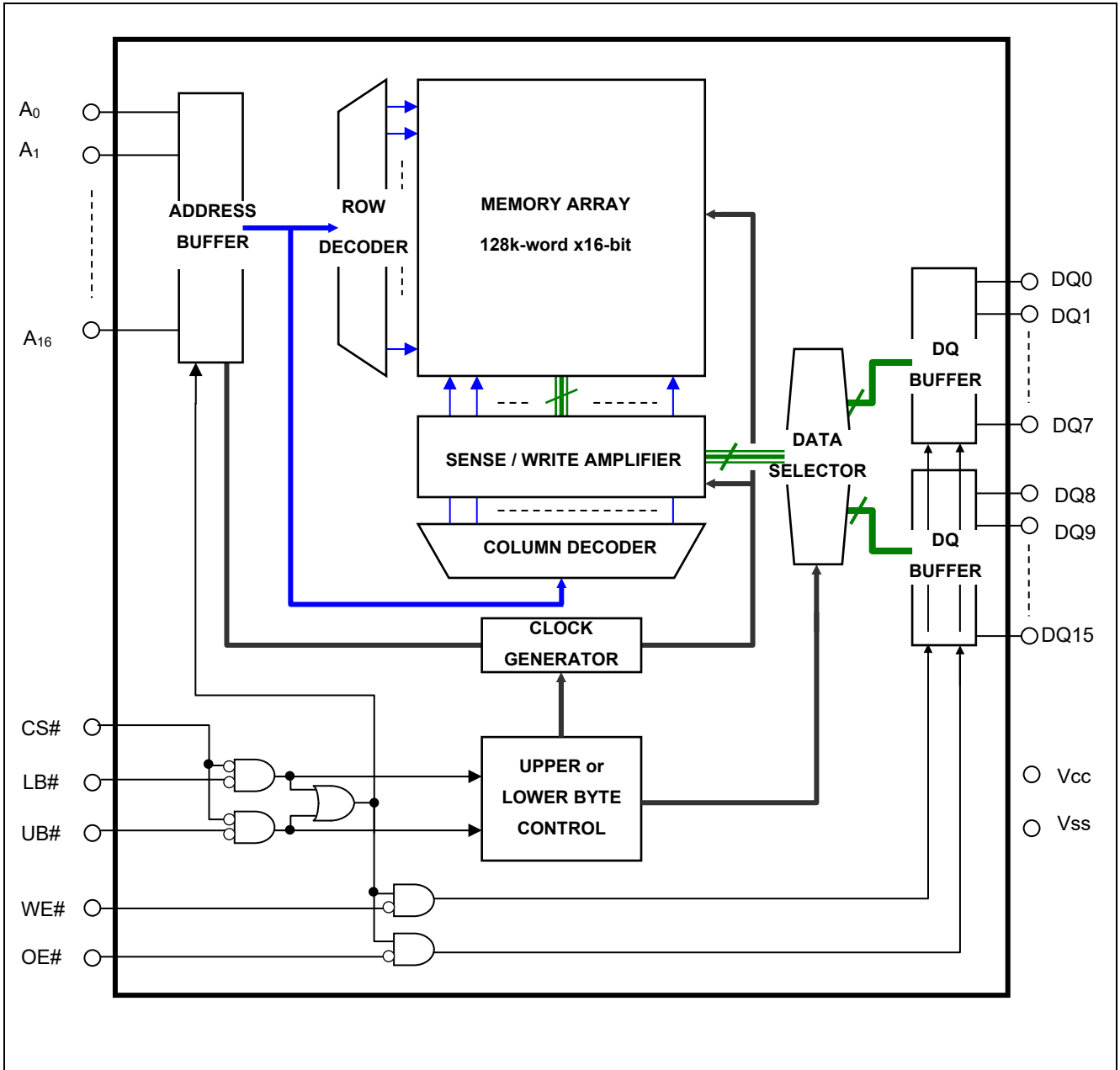
## Pin Arrangement



## Pin Description

Pin name	Function
Vcc	Power supply
Vss (GND)	Ground
A0 to A16	Address input
DQ0 to DQ15	Data input/output
CS#	Chip select
WE#	Write enable
OE#	Output enable
LB#	Lower byte enable
UB#	Upper byte enable
NC	Non connection

### Block Diagram



## Operation Table

CS#	LB#	UB#	WE#	OE#	DQ0~7	DQ8~15	Operation
H	X	X	X	X	High-Z	High-Z	Stand-by
X	H	H	X	X	High-Z	High-Z	Stand-by
L	L	H	L	X	Din	High-Z	Write in lower byte
L	L	H	H	L	Dout	High-Z	Read in lower byte
L	L	H	H	H	High-Z	High-Z	Output disable
L	H	L	L	X	High-Z	Din	Write in upper byte
L	H	L	H	L	High-Z	Dout	Read in upper byte
L	H	L	H	H	High-Z	High-Z	Output disable
L	L	L	L	X	Din	Din	Word write
L	L	L	H	L	Dout	Dout	Word read
L	L	L	H	H	High-Z	High-Z	Output disable

Note 1. H:  $V_{IH}$  L:  $V_{IL}$  X:  $V_{IH}$  or  $V_{IL}$

## Absolute Maximum

Parameter	Symbol	Value	unit
Power supply voltage relative to $V_{SS}$	$V_{CC}$	-0.5 to +4.6	V
Terminal voltage on any pin relative to $V_{SS}$	$V_T$	$-0.5^{*1}$ to $V_{CC}+0.5^{*2}$	V
Power dissipation	$P_T$	0.7	W
Operation temperature	$T_{opr}$	-40 to +85	°C
Storage temperature range	$T_{stg}$	-65 to 150	°C
Storage temperature range under bias	$T_{bias}$	-40 to +85	°C

Note 1. -3.0V for pulse  $\leq 30$ ns (full width at half maximum)  
 2. Maximum voltage is +4.6V.

## DC Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply voltage	V <sub>CC</sub>	2.7	3.0	3.6	V	
	V <sub>SS</sub>	0	0	0	V	
Input high voltage	V <sub>IH</sub>	2.2	-	V <sub>CC</sub> +0.3	V	
Input low voltage	V <sub>IL</sub>	-0.3	-	0.6	V	1
Ambient temperature range	T <sub>a</sub>	-40	-	+85	°C	

Note 1. -3.0V for pulse ≤ 30ns (full width at half maximum)

## DC Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions	
Input leakage current	I <sub>LI</sub>	-	-	1	μA	V <sub>in</sub> = V <sub>SS</sub> to V <sub>CC</sub>	
Output leakage current	I <sub>LO</sub>	-	-	1	μA	CS# = LB# = UB# = V <sub>IH</sub> or OE# = V <sub>IH</sub> , V <sub>I/O</sub> = V <sub>SS</sub> to V <sub>CC</sub>	
Average operating current	I <sub>CC1</sub>	-	15	25	mA	Min. cycle, duty = 100%, I <sub>I/O</sub> = 0mA, CS# = V <sub>IL</sub> , Others = V <sub>IH</sub> /V <sub>IL</sub>	
	I <sub>CC2</sub>	-	2	5	mA	Cycle = 1μs, duty = 100%, I <sub>I/O</sub> = 0mA, CS# ≤ 0.2V, V <sub>IH</sub> ≥ V <sub>CC</sub> -0.2V, V <sub>IL</sub> ≤ 0.2V	
Standby current	I <sub>SB</sub>	-	-	0.5	mA	(1) CS# = V <sub>IH</sub> , Others = V <sub>IH</sub> /V <sub>IL</sub> or (2) LB# = UB# = V <sub>IH</sub> , Others = V <sub>IH</sub> /V <sub>IL</sub>	
Standby current	I <sub>SB1</sub>	-	1 <sup>*1</sup>	2	μA	~+25°C	V <sub>in</sub> = V <sub>SS</sub> to V <sub>CC</sub> , (1) CS# ≥ V <sub>CC</sub> -0.2V or (2) LB# = UB# ≥ V <sub>CC</sub> -0.2V, CS# ≤ 0.2V
		-	-	3	μA	~+40°C	
		-	-	8	μA	~+70°C	
		-	-	10	μA	~+85°C	
Output high voltage	V <sub>OH</sub>	2.4	-	-	V	I <sub>OH</sub> = -0.5mA	
	V <sub>OH2</sub>	V <sub>CC</sub> - 0.5	-	-	V	I <sub>OH</sub> = -0.05mA	
Output low voltage	V <sub>OL</sub>	-	-	0.4	V	I <sub>OL</sub> = 2mA	

Note 1. Typical parameter indicates the value for the center of distribution at 3.0V (T<sub>a</sub> = 25°C), and not 100% tested.

## Capacitance

(V<sub>CC</sub> = 2.7V ~ 3.6V, f = 1MHz, T<sub>a</sub> = -40 ~ +85°C)

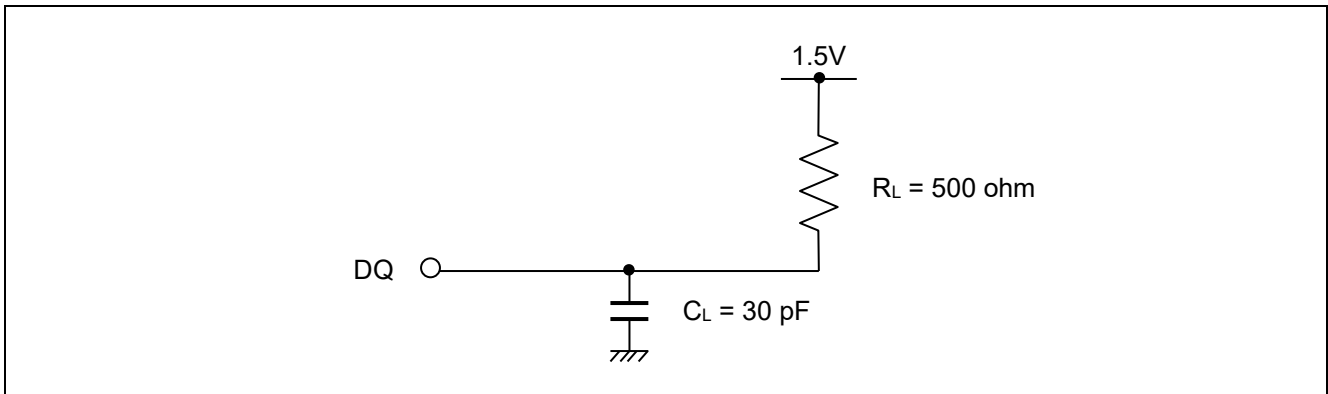
Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions	Note
Input capacitance	C <sub>in</sub>	-	-	8	pF	V <sub>in</sub> = 0V	1
Input / output capacitance	C <sub>I/O</sub>	-	-	10	pF	V <sub>I/O</sub> = 0V	1

Note 1. This parameter is sampled and not 100% tested.

## AC Characteristics

Test Conditions ( $V_{cc} = 2.7V \sim 3.6V$ ,  $T_a = -40 \sim +85^{\circ}C$ )

- Input pulse levels:  $V_{IL} = 0.4V$ ,  $V_{IH} = 2.4V$
- Input rise and fall time: 5ns
- Input and output timing reference level: 1.5V
- Output load: See figures (Including scope and jig)



**Read Cycle**

Parameter	Symbol	Min.	Max.	Unit	Note
Read cycle time	t <sub>RC</sub>	55	-	ns	
Address access time	t <sub>AA</sub>	-	55	ns	
Chip select access time	t <sub>ACS</sub>	-	55	ns	
Output enable to output valid	t <sub>OE</sub>	-	30	ns	
Output hold from address change	t <sub>OH</sub>	10	-	ns	
LB#, UB# access time	t <sub>BA</sub>	-	55	ns	
Chip select to output in low-Z	t <sub>CLZ</sub>	10	-	ns	2,3
LB#, UB# enable to low-Z	t <sub>BLZ</sub>	10	-	ns	2,3
Output enable to output in low-Z	t <sub>OLZ</sub>	5	-	ns	2,3
Chip deselect to output in high-Z	t <sub>CHZ</sub>	0	20	ns	1,2,3
LB#, UB# disable to high-Z	t <sub>BHZ</sub>	0	20	ns	1,2,3
Output disable to output in high-Z	t <sub>OHZ</sub>	0	20	ns	1,2,3

**Write Cycle**

Parameter	Symbol	Min.	Max.	Unit	Note
Write cycle time	t <sub>WC</sub>	55	-	ns	
Address valid to end of write	t <sub>AW</sub>	50	-	ns	
Chip select to end of write	t <sub>CW</sub>	50	-	ns	5
Write pulse width	t <sub>WP</sub>	45	-	ns	4
LB#, UB# valid to end of write	t <sub>BW</sub>	50	-	ns	
Address setup time	t <sub>AS</sub>	0	-	ns	6
Write recovery time	t <sub>WR</sub>	0	-	ns	7
Data to write time overlap	t <sub>DW</sub>	25	-	ns	
Data hold from write time	t <sub>DH</sub>	0	-	ns	
Output enable from end of write	t <sub>OW</sub>	5	-	ns	2
Output disable to output in high-Z	t <sub>OHZ</sub>	0	20	ns	1,2
Write to output in high-Z	t <sub>WHZ</sub>	0	20	ns	1,2

- Note
1. t<sub>CHZ</sub>, t<sub>OHZ</sub> and t<sub>WHZ</sub> are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.
  2. This parameter is sampled and not 100% tested.
  3. At any given temperature and voltage condition, t<sub>HZ</sub> max is less than t<sub>LZ</sub> min both for a given device and from device to device.
  4. A write occurs during the overlap of a low CS#, a low WE# and a low LB# or a low UB#.
 

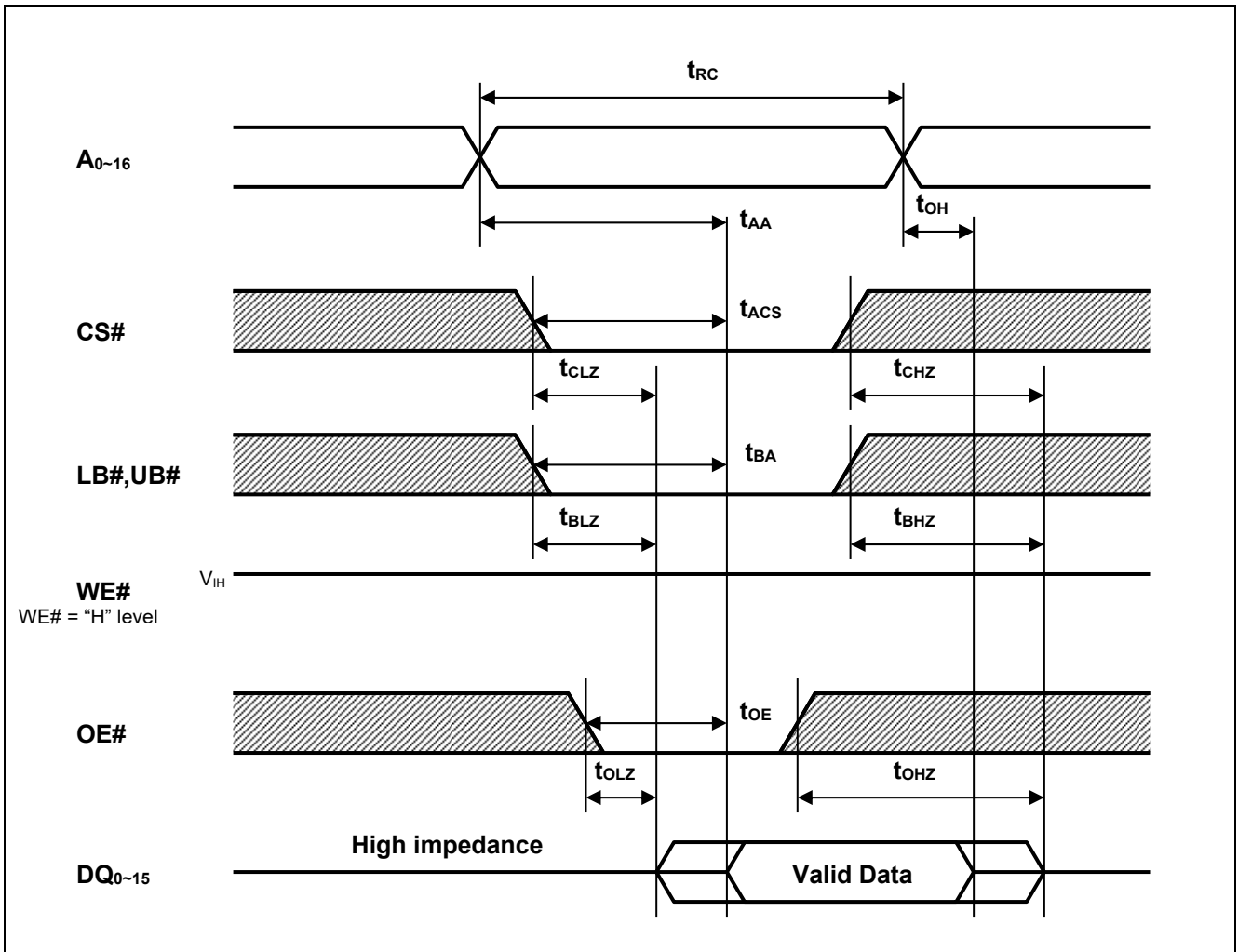
A write begins at the latest transition among CS# going low, WE# going low and LB# going low or UB# going low.

A write ends at the earliest transition among CS# going high, WE# going high and LB# going high or UB# going high.

t<sub>WP</sub> is measured from the beginning of write to the end of write.
  5. t<sub>CW</sub> is measured from the later of CS# going low to end of write.
  6. t<sub>AS</sub> is measured the address valid to the beginning of write.
  7. t<sub>WR</sub> is measured from the earliest of CS#, WE#, LB# or UB# going high to the end of write cycle.
  8. Don't apply inverted phase signal externally when DQ pin is output mode.

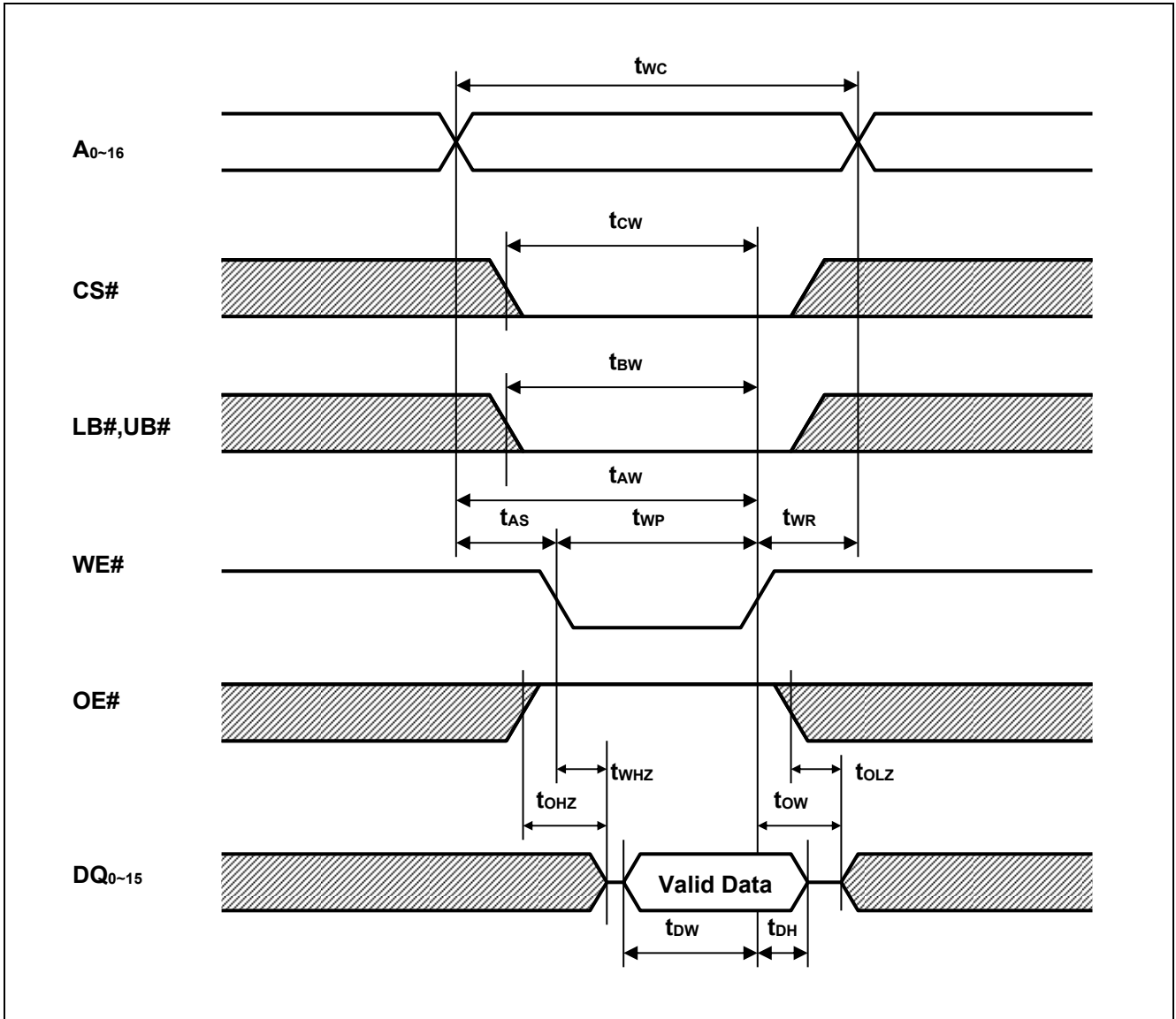
## Timing Waveforms

### Read Cycle

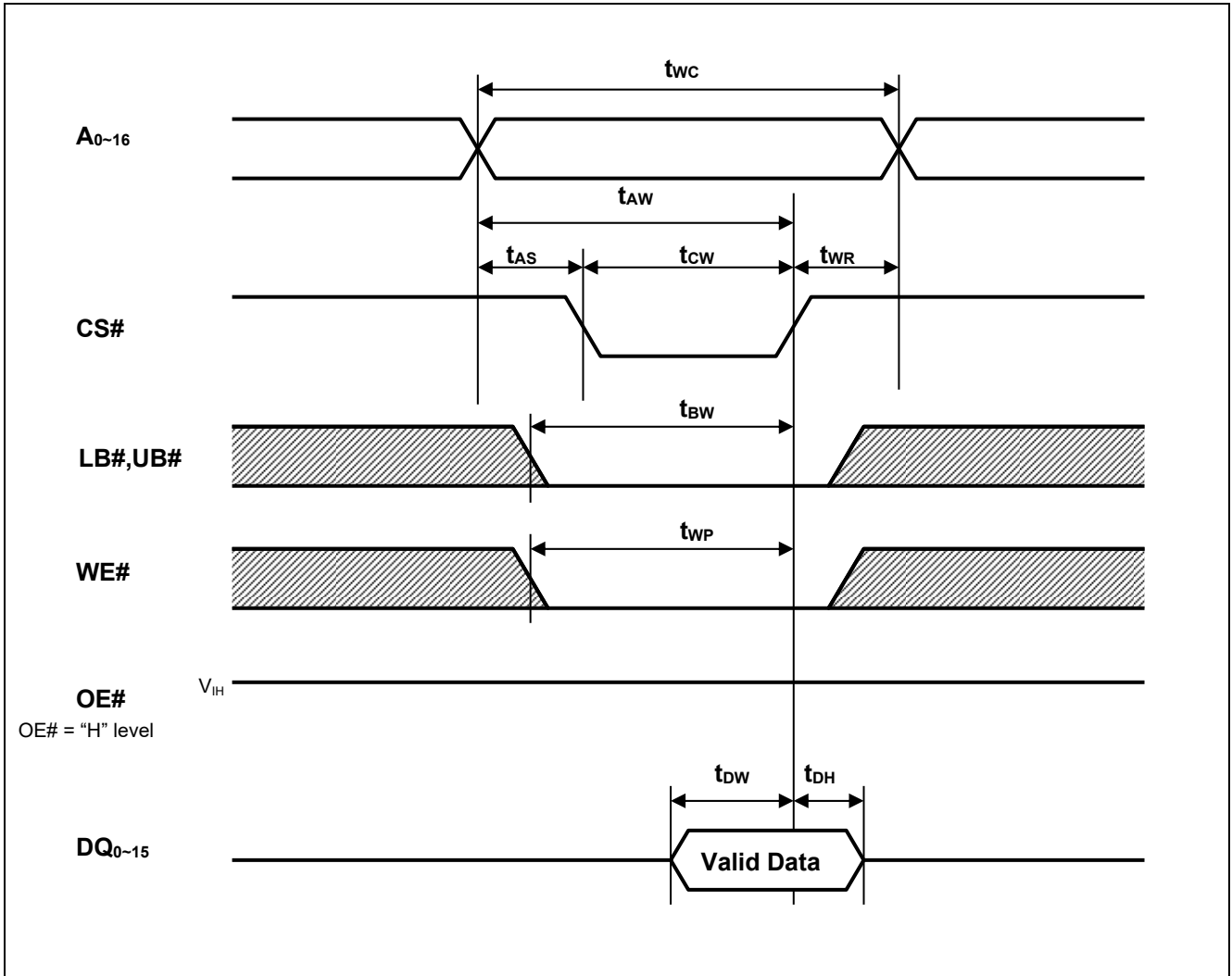




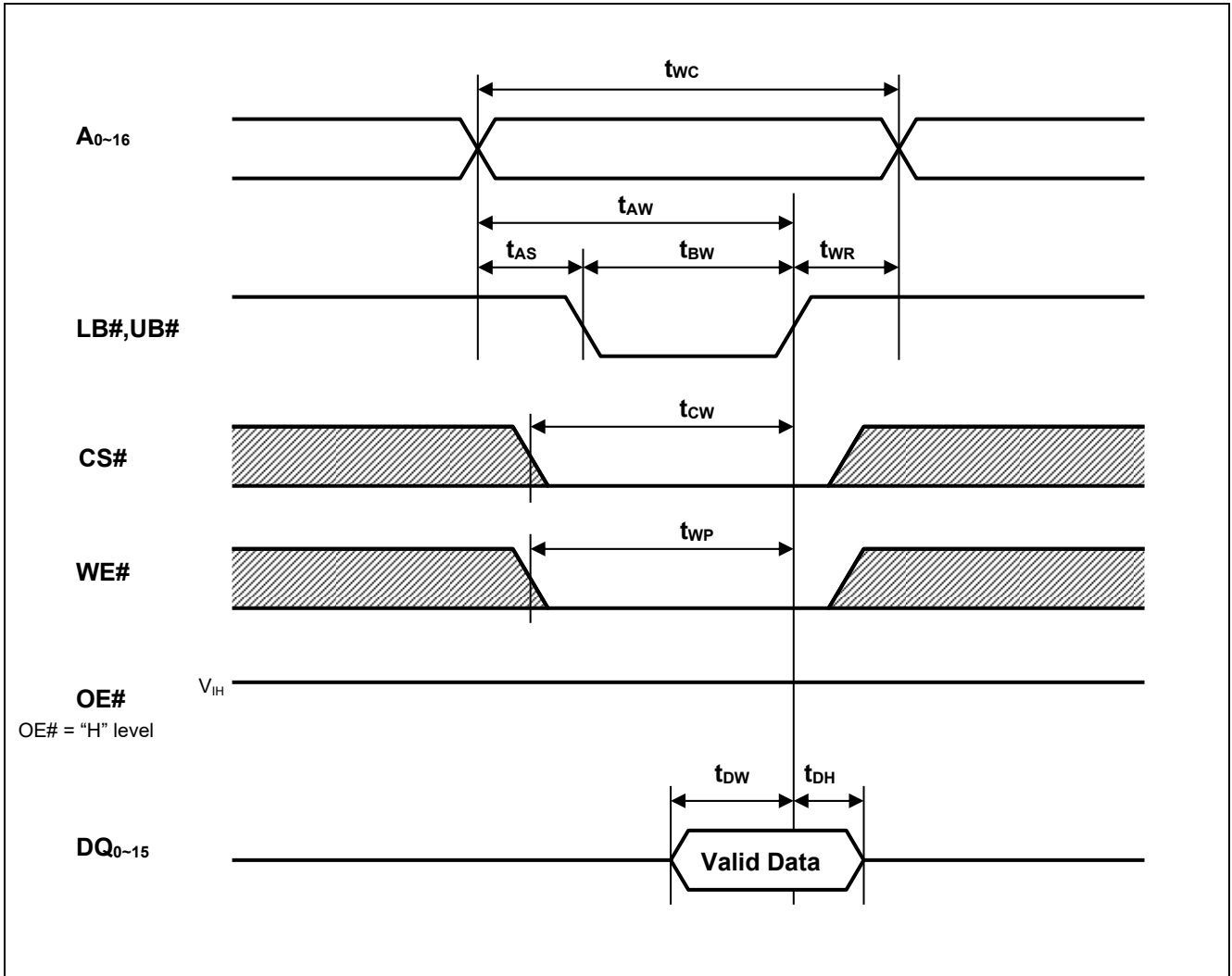
Write Cycle (1) (WE# CLOCK)



Write Cycle (2) (CS# CLOCK)



Write Cycle (3) (LB#, UB# CLOCK)



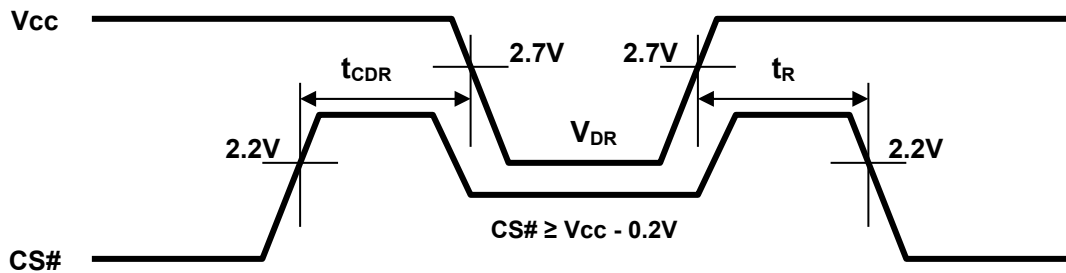
## Low Vcc Data Retention Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions <sup>2</sup>	
V <sub>CC</sub> for data retention	V <sub>DR</sub>	2.0	-	3.6	V	V <sub>in</sub> ≥ 0V, (1) CS# ≥ V <sub>CC</sub> -0.2V or (2) LB# = UB# ≥ V <sub>CC</sub> -0.2V, CS# ≤ 0.2V	
Data retention current	I <sub>CCDR</sub>	-	1 <sup>*1</sup>	2	μA	~+25°C	V <sub>CC</sub> =3.0V, V <sub>in</sub> ≥ 0V, (1) CS# ≥ V <sub>CC</sub> -0.2V or (2) LB# = UB# ≥ V <sub>CC</sub> -0.2V, CS# ≤ 0.2V
		-	-	3	μA	~+40°C	
		-	-	8	μA	~+70°C	
		-	-	10	μA	~+85°C	
Chip deselect time to data retention	t <sub>CDR</sub>	0	-	-	ns	See retention waveform.	
Operation recovery time	t <sub>R</sub>	5	-	-	ms		

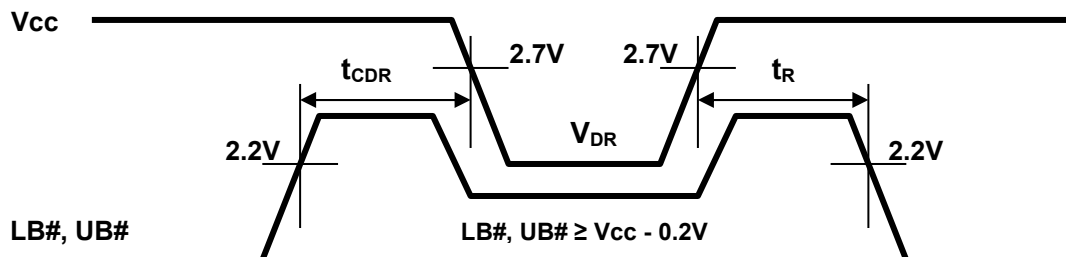
- Note
1. Typical parameter indicates the value for the center of distribution at 3.0V (T<sub>a</sub>= 25°C), and not 100% tested.
  2. CS# controls address buffer, WE# buffer, OE# buffer, LB# buffer, UB# buffer and Din buffer. If CS# controls data retention mode, V<sub>in</sub> levels (address, WE#, OE#, LB#, UB#, DQ) can be in the high impedance state.

### Low Vcc Data Retention Timing Waveforms

#### (1) CS# Controlled



#### (2) LB#, UB# Controlled



Revision History	R1LV0216BSB Data Sheet
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Rev.	Date	Description	
		Page	Summary
1.00	2017.1.27	-	First Edition issued
1.01	2020.2.20	Last page	Updated the Notice to the latest version

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