User's Guide

TPS3704Q1EVM Voltage Supervisor User Guide

Ben Chan

ABSTRACT

This user guide describes the operational use of the TPS3704Q1EVM evaluation module (EVM) as a reference design for engineering demonstration and evaluation of the TPS3704x-Q1. This guide contains the EVM schematic, bill of materials (BOM), assembly drawing, and top and bottom board layouts.

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1 Introduction

The TPS3704Q1EVM is an evaluation module (EVM) for the TPS37044-Q1 voltage supervisor. This EVM can be used with any TPS3704x-Q1 device variant in DDF package. Test points are provided to give the user additional access, if needed, for oscilloscope or multi-meter measurements.

The TPS3704Q1EVM comes pre-populated with TPS37044A7OHDDFRQ1. This option is capable of monitoring four distinct input voltage rails and outputting an active low $\overline{\text{RESET}}$ signal on $\overline{\text{RESET1}}$ and/or $\overline{\text{RESET2}}$ depending on the state of the input voltages. If users need a different option, the existing device must be removed from the board and replaced. The EVM board is designed to support all possible options by changing jumper configurations.

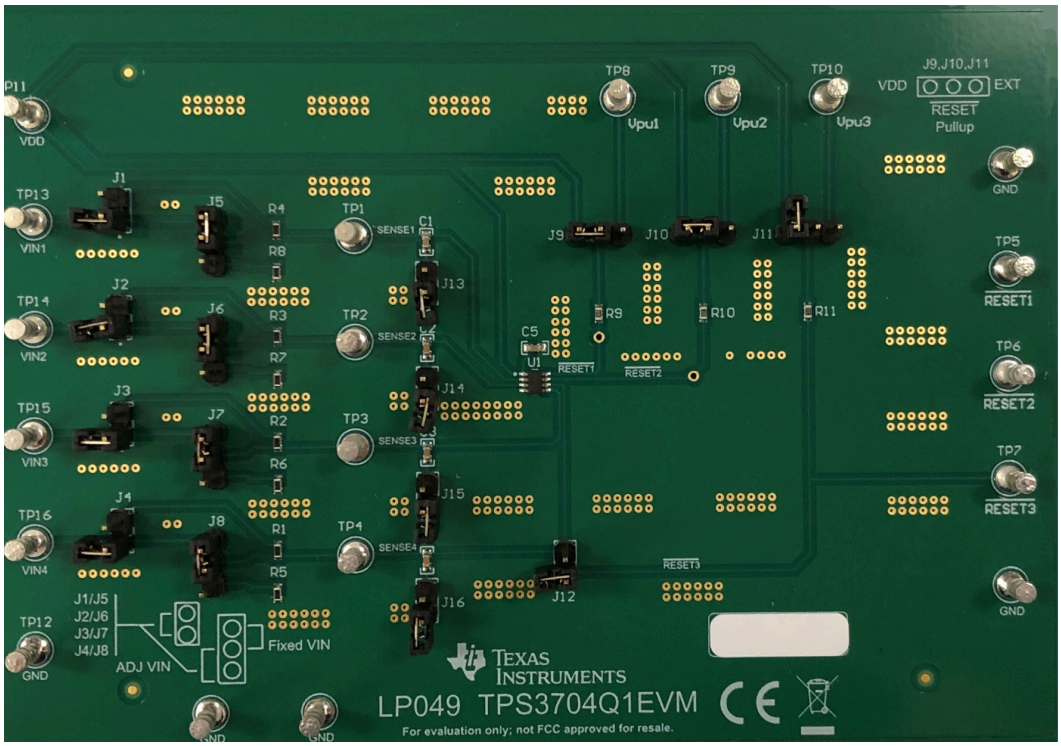


Figure 1-1. TPS3704Q1EVM Board Top

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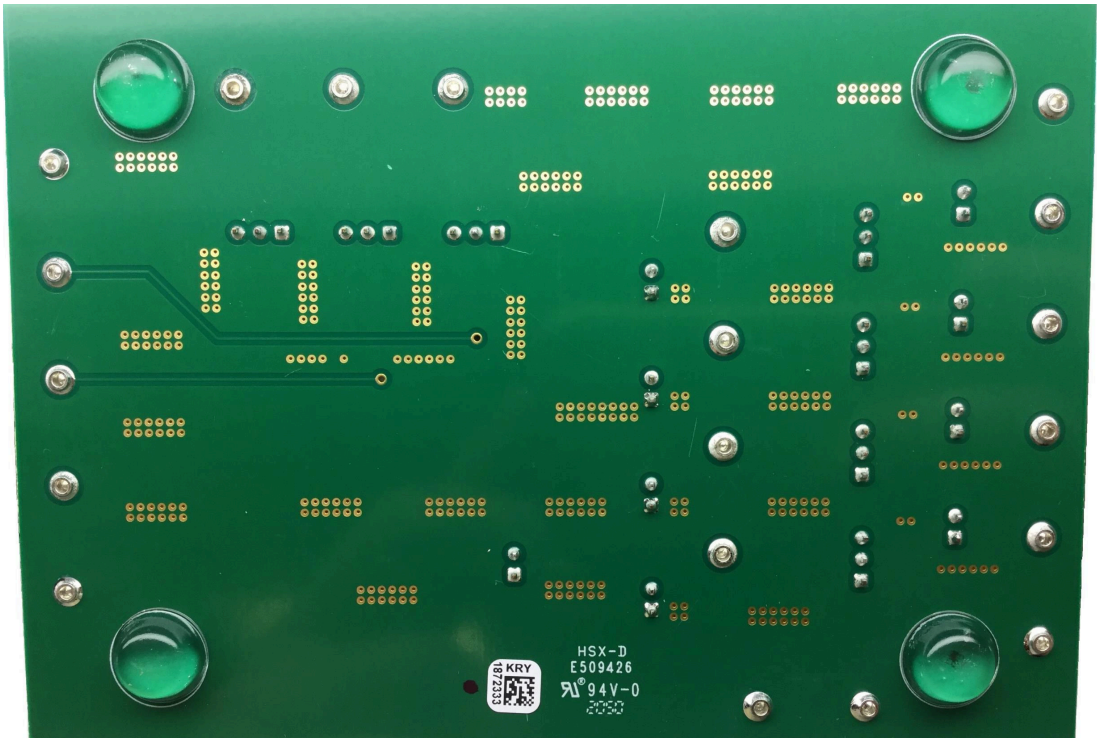


Figure 1-2. TPS3704Q1EVM Board Bottom

1.1 Related Documentation

Datasheet: *TPS3704x-Q1 Quad/Triple/Dual/Single Window/Standard Voltage Supervisor*

1.2 TPS3704x-Q1 Applications

- Advanced Driver Assistance System (ADAS)
- ADAS Domain Controller
- Automotive Infotainment & Cluster
- Digital cockpit
- HEV/EV

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2 Schematic, Bill of Materials, and Layout

This section provides a detailed description of the TPS3704Q1EVM schematic, bill of materials (BOM), and layout.

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2.1 TPS3704Q1EVM Schematic

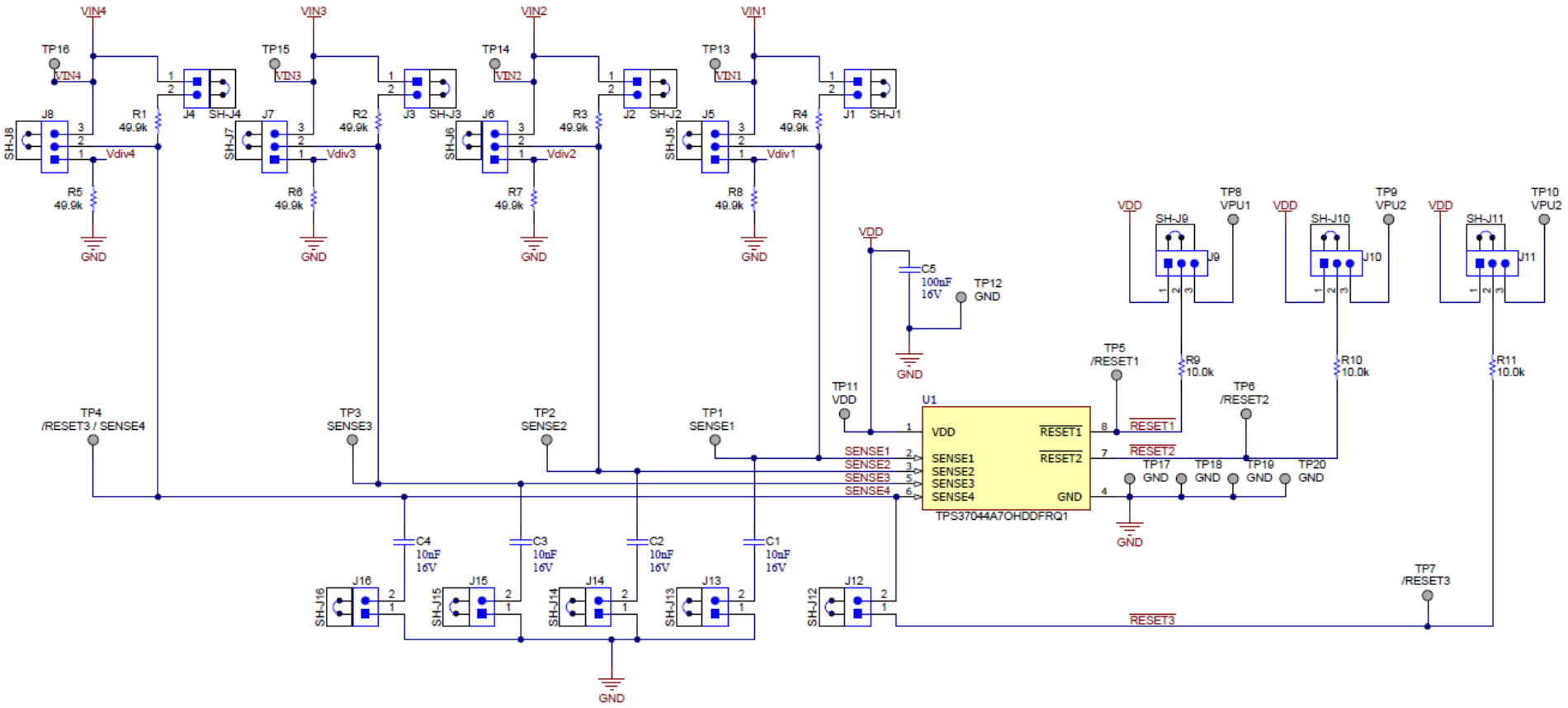


Figure 2-1. TPS3704Q1EVM Schematic

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2.2 TPS3704Q1EVM Bill of Materials

Table 2-1. BOM

DESIGNATOR	QTY	VALUE	DESCRIPTION	PACKAGE REFERENCE	PART NUMBER	MANUFACTURER
PCB	1		Printed Circuit Board		TPS3704Q1EVM	Any
C5	1	0.1 µF	CAP, CERM, 0.1 µF, 16 V, ± 10%, X7R, 0603	0603	C0603C104K4RACTU	Kemet
C1, C2, C3, C4	4	0.01 µF	CAP, CERM, 0.01 µF, 16 V, ± 10%, X7R, 0603	0603	C0603C103K4RACTU	Kemet
H9, H10, H11, H12	4		Bumpon, Hemisphere, 0.44 X 0.20, Clear	Transparent Bumpon	SJ-5303 (CLEAR)	3M
J1, J2, J3, J4, J12, J13, J14, J15, J16	9		Header, 100mil, 2x1, TH	Header, 2x1, 100mil, TH	TSW-102-07-G-S	Samtec
J5, J6, J7, J8, J9, J10, J11	7		Header, 100mil, 3x1, TH	Header, 3x1, 100mil, TH	TSW-103-07-G-S	Samtec
R1, R2, R3, R4, R5, R6, R7, R8	8	49.9k	RES, 47.5 k, 1%, 0.1 W, 0603	0603	RC0603FR-0749K9L	Yageo America
R9, R10, R11	3	10k	RES, 10.0 k, 1%, 0.1 W, 0603	0603	RC0603FR-0710KL	Yageo America
SH-J1, SH-J2, SH-J3, SH-J4, SH-J5, SH-J6, SH-J7, SH-J8, SH-J9, SH-J10, SH-J11, SH-J12, SH-J13, SH-J14, SH-J15, SH-J16	16		Shunt, 100mil, Tin plated, Black	Shunt Connector Black Open Top, 2x1	SNT-100-BK-G	Samtec
TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP14, TP15, TP16, TP17, TP18, TP19, TP20	20		Terminal, Turret, TH, Triple	Test Point, SMT	1598-2	Keystone
U1	1		Quad/Triple/Dual/Single Window/Standard Voltage Supervisor	DDF	TPS37044A7OHDDFRQ1	TI
FID1, FID2, FID3	0		Fiducial mark. There is nothing to buy or mount.	Fiducial	N/A	N/A

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2.3 Layout and Component Placement

Figure 2-2 and Figure 2-3 show the top and bottom assemblies of the printed circuit board (PCB) to show the component placement on the EVM.

Figure 2-4 and Figure 2-5 show the top and bottom layouts, Figure 2-6 and Figure 2-7 show the top and bottom layers, and Figure 2-8 shows the top solder mask of the EVM.

2.4 Layout

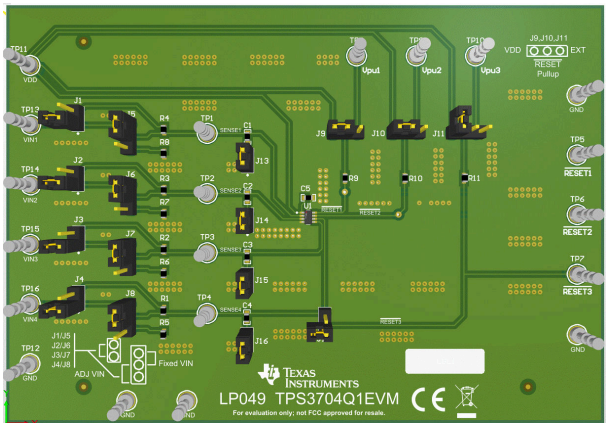


Figure 2-2. Component Placement—Top Assembly

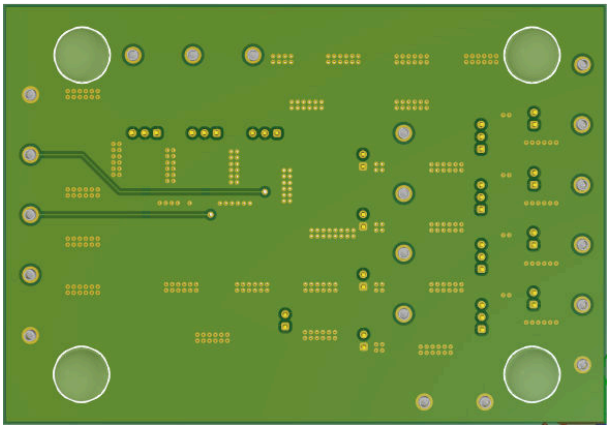


Figure 2-3. Component Placement—Bottom Assembly

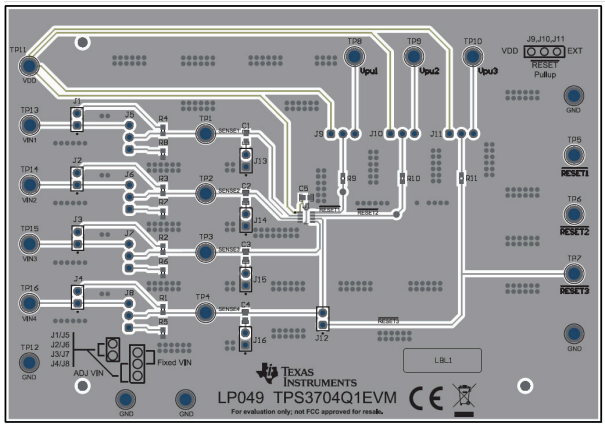


Figure 2-4. Layout—Top

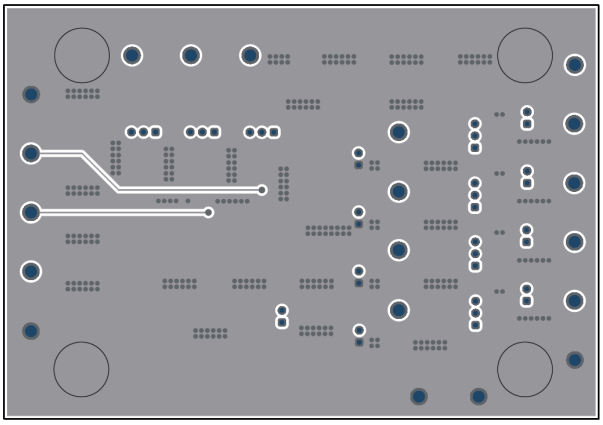


Figure 2-5. Layout—Bottom

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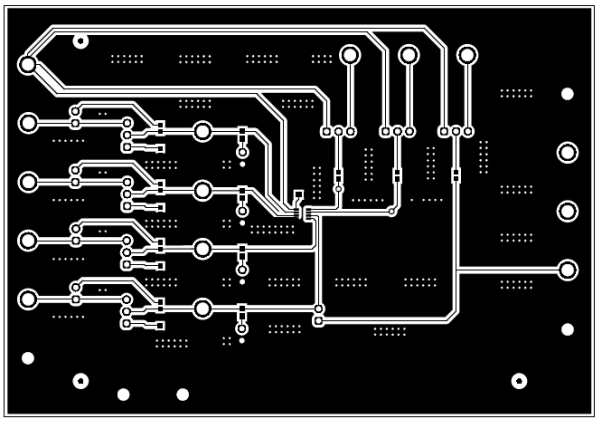


Figure 2-6. Top Layer

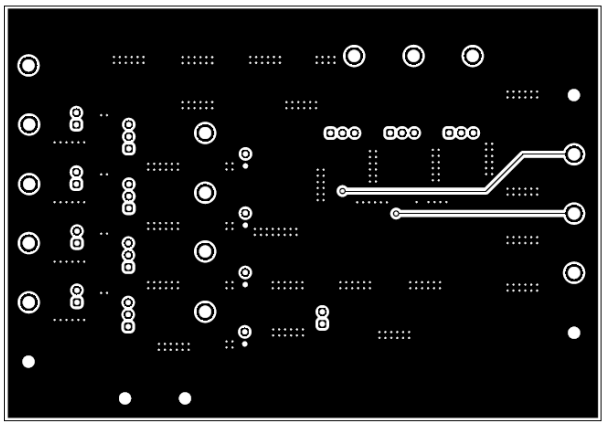


Figure 2-7. Bottom Layer

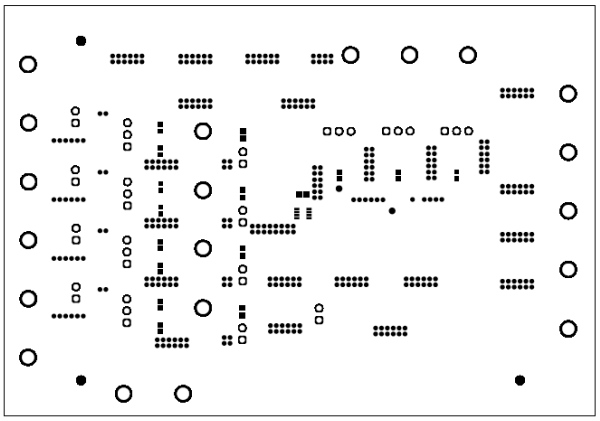


Figure 2-8. Top Solder Mask

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3 EVM Connectors

This section describes the connectors, jumpers, and test points on the EVM as well as how to connect, set up, and properly use the EVM. Each device has an independent supply connection, but all grounds are connected on the board.

3.1 EVM Test Points

Table 3-1 lists the EVM test points as well as their functional descriptions. All TPS3704x-Q1 pins have a corresponding test point on the EVM. These test points are located close to the pins for more accurate measurements. In addition to the test points listed below, the EVM also has four additional GND test points.

Table 3-1. Test Points

TEST POINT NUMBER	TEST POINT SILKSCREEN LABEL	FUNCTION	DESCRIPTION
TP1	SENSE1	Connection to SENSE1 pin	Allows the user to monitor the SENSE1 pin
TP2	SENSE2	Connection to SENSE2 pin	Allows the user to monitor the SENSE2 pin
TP3	SENSE3	Connection to SENSE3 pin	Allows the user to monitor the SENSE3 pin
TP4	SENSE4	Connection to SENSE4 pin	Allows the user to monitor the SENSE4 pin
TP5	$\overline{\text{RESET1}}$	Connection to $\overline{\text{RESET1}}$ pin	Allows the user to monitor the $\overline{\text{RESET1}}$ output
TP6	$\overline{\text{RESET2}}$	Connection to $\overline{\text{RESET2}}$ pin	Allows the user to monitor the $\overline{\text{RESET2}}$ output
TP7	$\overline{\text{RESET3}}$	Connection to $\overline{\text{RESET3}}$ pin	Allows the user to monitor the $\overline{\text{RESET3}}$ output
TP8	Vpu1	Pullup Voltage for $\overline{\text{RESET1}}$	Option for pullup voltage other than VDD
TP9	Vpu2	Pullup Voltage for $\overline{\text{RESET2}}$	Option for pullup voltage other than VDD
TP10	Vpu3	Pullup Voltage for $\overline{\text{RESET3}}$	Option for pullup voltage other than VDD
TP11	VDD	Supply voltage for EVM	Supply voltage for EVM
TP12	GND	GND for EVM	GND for EVM
TP13	VIN1	Input1 for Monitoring	Connect the input to be monitored
TP14	VIN2	Input2 for Monitoring	Connect the input to be monitored
TP15	VIN3	Input3 for Monitoring	Connect the input to be monitored
TP16	VIN4	Input4 for Monitoring	Connect the input to be monitored

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3.2 EVM Jumpers

Table 3-2 lists the jumpers on the TPS3704Q1EVM. As ordered, the EVM will have sixteen (16) jumpers installed. Figure 3-1 is provided as visual aid.

Table 3-2. List of Onboard Jumpers

JUMPER	JUMPER CONFIGUATION	DESCRIPTION
J1 & J5	J1-Open & J5-top position	For direct monitoring of VIN1. Default position.
J1 & J5	J1-Shunt & J5-bottom position	For monitoring of VIN1 via R4, R8 resistor divider (ADJ) version.
J2 & J6	J2-Open & J6-top position	For direct monitoring of VIN2. Default position.
J2 & J6	J2-Shunt & J6-bottom position	For monitoring of VIN2 via R3, R7 resistor divider (ADJ) version.
J3 & J7	J3-Open & J7-top position	For direct monitoring of VIN3. Default position.
J3 & J7	J3-Shunt & J7-bottom position	For monitoring of VIN3 via R2, R6 resistor divider (ADJ) version.
J4 & J8	J4-Open & J8-top position	For direct monitoring of VIN4. Default position.
J4 & J8	J4-Shunt & J8-bottom position	For monitoring of VIN4 via R1, R5 resistor divider (ADJ) version.
J9	Left or Right	Left for $\overline{\text{RESET1}}$ pull up to VDD, Right for pull up to Vpu1. Default position is Left.
J10	Left or Right	Left for $\overline{\text{RESET2}}$ pull up to VDD, Right for pull up to Vpu2. Default position is Left.
J11	Left or Right	Left for $\overline{\text{RESET3}}$ pull up to VDD, Right for pull up to Vpu3. Default position is Left.
J12	Open	SENSE4 testpoint (TP4) connects directly to SENSE4 pin of IC. Default position.
J12	Shunt	$\overline{\text{RESET3}}$ output pin of IC connected to $\overline{\text{RESET3}}$ test point (TP7). J4 & J8 must be left Open.Valid for TPS37043 device variants.
J13	Shunt	High frequency input capacitor placed in parallel with SENSE1 input pin to provide better noise immunity for noisy applicaitions. Default position is Open.
J14	Shunt	High frequency input capacitor placed in parallel with SENSE2 input pin to provide better noise immunity for noisy applicaitions. Default position is Open.
J15	Shunt	High frequency input capacitor placed in parallel with SENSE3 input pin to provide better noise immunity for noisy applicaitions. Default position is Open..
J16	Shunt	High frequency input capacitor placed in parallel with SENSE4 input pin to provide better noise immunity for noisy applicaitions. Default position is Open.

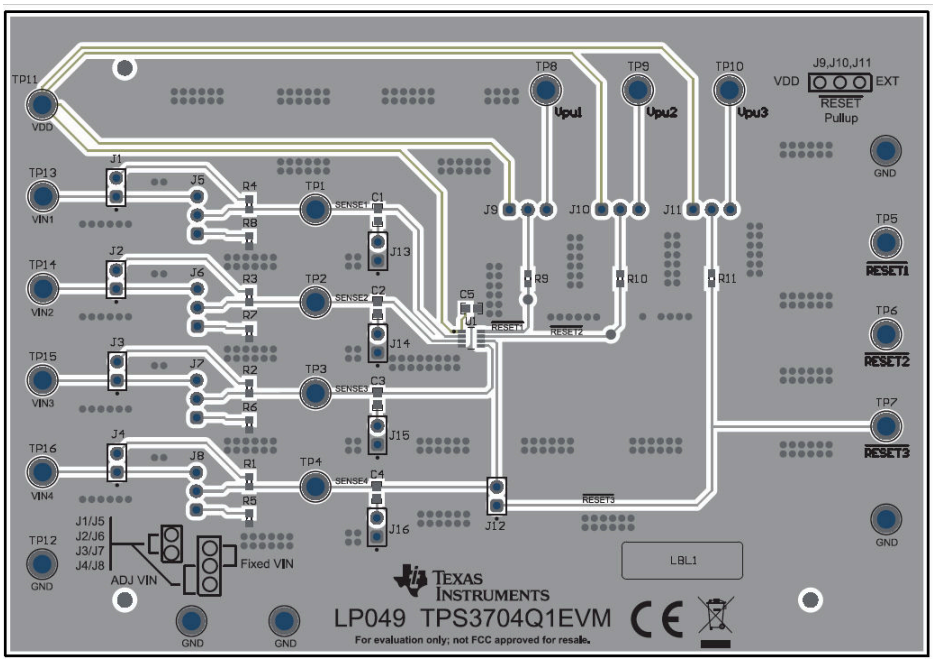


Figure 3-1. Layout—Top

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4 EVM Setup and Operation

This section describes the functionality and operation of the TPS3704Q1EVM. Refer to the TPS3704x-Q1 datasheet for details on the electrical characteristics of the device.

The TPS3704Q1EVM comes pre-populated with the TPS37044A7OHDDFRQ1 meaning the device is capable of monitoring four seperate voltage rails and outputting two active low $\overline{\text{RESET}}$ signals. The EVM is capable of many different configurations in order to fully evaluate the functionality of all the TPS3704x-Q1 device variants. The default configuration of the EVM is as follows:

- Jumpers J1 through J4 will be left open while J5 through J8 will be in the Fixed VIN position for direct monitoring of the input voltage.
- Jumpers J9 and J10 will be in the left position to allow $\overline{\text{RESET1}}$ and $\overline{\text{RESET2}}$ to pull up to VDD. J11 will be open because the default configuration does not support $\overline{\text{RESET3}}$.
- Jumper J12 will be open connecting TP4 directly to SENSE4 input pin of the device.
- Jumpers J13 through J16 will be open. Shunt these jumpers to connect high frequency bypass capaitors in parallel with the desired input line.

The TPS3704Q1EVM comes populated with 2:1 resistor dividers on each of the input lines. The user must choose appropriately sized resistors such that the divided voltage is within the voltage window of the sense pin to be used. Consult the Device Threshold Table in the datasheet to ensure proper resistor values.

The TPS3704Q1EVM also provides an option to apply a seperate pull-up voltage to any of the output pins by changing the position of jumpers J9, J10, and/or J11 to *EXT* and connecting the pull-up voltage to test points TP8, TP9, and/or TP10.

4.1 Supply Voltage (V_{DD})

Test point TP11 is used to supply VDD to the TPS3704x-Q1, this test point also supplies the pull-up voltage for $\overline{\text{RESET1}}$, $\overline{\text{RESET2}}$, and $\overline{\text{RESET3}}$ through jumpers J9, J10, and J11 respectively. The recommended VDD supply voltage range for the TPS3704x-Q1 is 1.7 V to 6 V. The absolute maximum ratings can be found in the device datasheet.

In the default EVM configuration, $\overline{\text{RESET1}}$ and $\overline{\text{RESET2}}$ will follow VDD as shown in Figure 4-1. The voltage blips seen on $\overline{\text{RESET2}}$ when VDD approaches zero are related to the power on reset voltage, V_{POR}, which is the minimum VDD voltage level for a controlled output state. The device datasheet should be consulted for more information on V_{POR} for this device. Figure 4-2 shows the reset delay time of $\overline{\text{RESET1}}$ and $\overline{\text{RESET2}}$ due to VDD while input voltages VIN1 through VIN4 are all held within their respective voltage window thresholds.

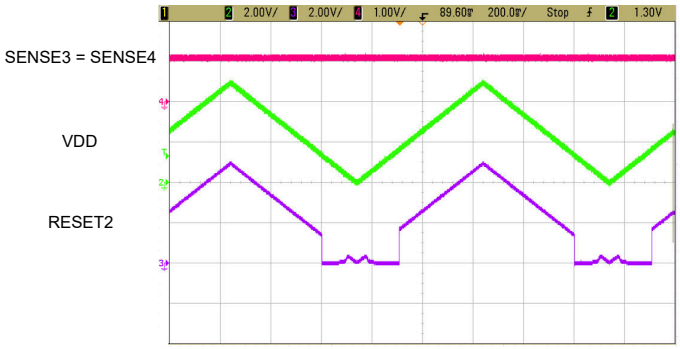


Figure 4-1. VDD Ramp

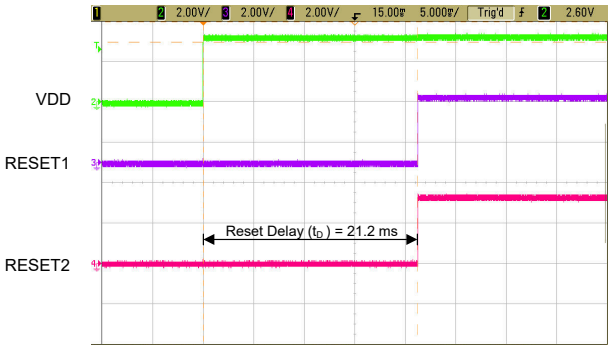


Figure 4-2. Reset Delay (t_D) due to VDD

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4.2 Monitoring Input Voltage

The TPS3704Q1EVM allows users to monitor between one and four input voltages depending on the device variant populating the board. The voltages to be monitored are referred to as VIN1, VIN2, VIN3, and VIN4 and are applied to test points TP13 through TP16 respectively. By using jumpers J1 through J8 the user can input either an adjustable or fixed voltage. When the adjustable voltage jumper configuration is used, the voltage measured at sense test points TP1 through TP4 will be scaled down versions of the input voltage applied to TP13 through TP16. The adjustable voltage option is useful when the input voltage to be monitored is higher than the maximum allowable pin voltage specified in the device datasheet.

The fixed input voltage jumper configuration is useful when the input voltage is expected within the voltage window of the sense pin used. For instance the TPS37044A7OHDDFRQ1, which comes populated on the board, has a threshold voltage of 3.3 V (±8%) on SENSE1 pin. Therefore, a 3.3 V rail could be monitored by connecting the rail to TP13 with the FIXED VIN jumper configuration as outlined in Table 3-2.

Figure 4-3, Figure 4-4, and Figure 4-5 show the OVLO and UVLO thresholds for $\overline{\text{RESET1}}$ and $\overline{\text{RESET2}}$ for the fixed input voltage jumper configuration. Note that in Figure 4-3 SENSE2 is held within the voltage threshold window, while in Figure 4-4 SENSE1 is held wihtin its voltage threshold window.

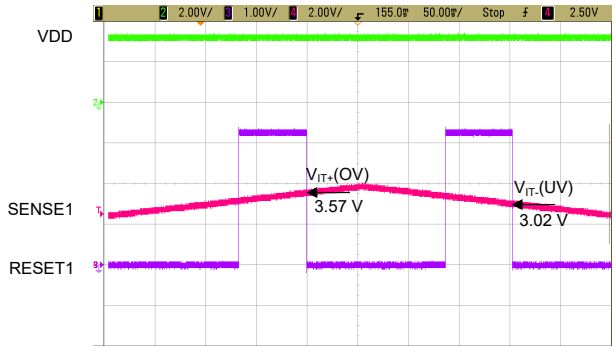


Figure 4-3. $\overline{\text{RESET1}}$ VIN1 OVLO (V_{IT+}) and UVLO (V_{IT-}) Thresholds

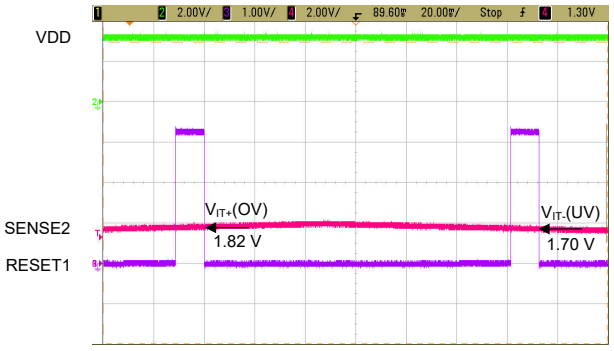


Figure 4-4. $\overline{\text{RESET1}}$ VIN2 OVLO (V_{IT+}) and UVLO (V_{IT-}) Thresholds

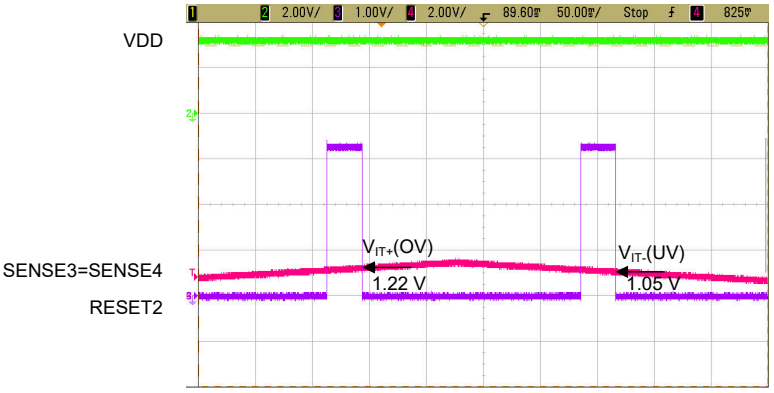


Figure 4-5. $\overline{\text{RESET2}}$ VIN3=VIN4 OVLO (V_{IT+}) and UVLO (V_{IT-}) Thresholds

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4.3 Default Reset Outputs ($\overline{\text{RESET1}}$ and $\overline{\text{RESET2}}$)

The TPS3704Q1EVM comes populated with the TPS37044A7OHDDFRQ1 device variant which has an open-drain, active-low output topology for the $\overline{\text{RESET1}}$ and $\overline{\text{RESET2}}$ pins. The other device variants provide different number of $\overline{\text{RESET}}$ output pins and can be used on this EVM. The TPS3704Q1EVM provides test points TP5 and TP6 that are connected directly to the $\overline{\text{RESET1}}$ and $\overline{\text{RESET2}}$ pins, respectively, for monitoring and/or interfacing to other devices.

For TPS37044-Q1 $\overline{\text{RESET1}}$ asserts when either SENSE1 or SENSE2 voltages fall outside of the overvoltage or undervoltage window threshold. $\overline{\text{RESET1}}$ stays asserted for the reset timeout period after both SENSE1 and SENSE2 voltages fall back within the window threshold. This is shown in Figure 4-6.

For all other device options, $\overline{\text{RESET1}}$ asserts when the voltage on SENSE1 falls outside of the overvoltage or undervoltage threshold window. $\overline{\text{RESET1}}$ stays asserted for the reset timeout period after SENSE1 voltage falls back within the window threshold.

For TPS37044-Q1 $\overline{\text{RESET2}}$ asserts when either SENSE3 or SENSE4 fall outside of the aformentioned window threshold. $\overline{\text{RESET2}}$ stays asserted for the reset timeout period after both SENSE3 and SENSE4 voltages fall back within the window threshold. This is shown in Figure 4-7.

For the two channel and three channel device options (TPS37042-Q1 and TPS37043-Q1 respectively) $\overline{\text{RESET2}}$ asserts when the voltage on SENSE2 falls outside of the overvoltage or undervoltage threshold window. $\overline{\text{RESET2}}$ stays asserted for the reset timeout period after SENSE2 voltage falls back within the window threshold.

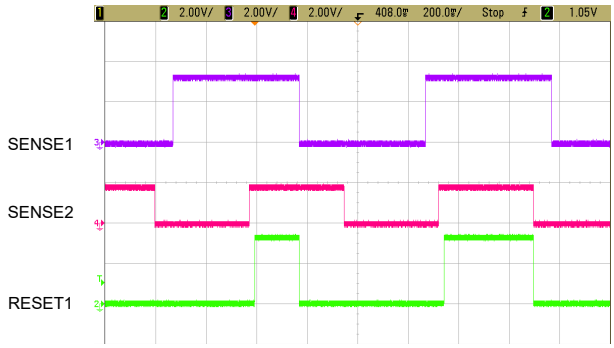


Figure 4-6. Default $\overline{\text{RESET1}}$ Output Logic

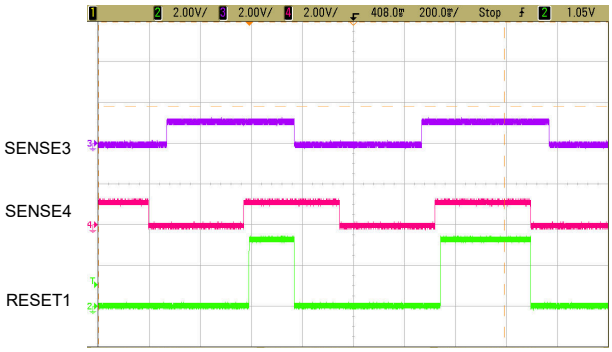


Figure 4-7. Default $\overline{\text{RESET2}}$ Output Logic

4.4 Optional Reset Output ($\overline{\text{RESET3}}$)

By default, the TPS3704Q1EVM does not support the $\overline{\text{RESET3}}$ output. In order to use this EVM to evaluate $\overline{\text{RESET3}}$ the TPS37044-Q1 option that is installed on the board must be replaced by a TPS37043-Q1 device. The TPS37043-Q1 device is capable of monitoring three voltage rails and outputing three active low reset signals. When evaluating this option, the following jumper configurations must be used:

- Jumper J12 must be shunted in order to connect the $\overline{\text{RESET3}}$ pin to the TP7 testpoint.
- Jumper J11 must be placed in either the left or the right position in order for the $\overline{\text{RESET3}}$ output to be pulled up to VDD or Vpu3 respectively.
- Jumpers J4 and J8 must be left open.

$\overline{\text{RESET3}}$ asserts when the voltage on SENSE3 falls outside of the overvoltage or undervoltage threshold window. $\overline{\text{RESET3}}$ stays asserted for the reset timeout period after SENSE3 falls back within the window threshold.

5 Revision History

DATE	REVISION	NOTE
February 2021	*	Initial Release

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