Datasheet

32

Renesas RA2A1 Group

Datasheet

32-Bit MCU

Renesas Advanced (RA) Family
Renesas RA2 Series

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Ultra-low power 48-MHz Arm® Cortex®-M23 core, up to 256-KB code flash memory, 32-KB SRAM, Capacitive Touch Sensing Unit, 16-bit A/D Converter, 24-bit sigma-delta A/D Converter, 12-bit D/A Converter, 8-bit D/A Converter, Operational Amplifier, security and safety features.

Features

■ Arm Cortex-M23 Core
- Armv8-M architecture
- Maximum operating frequency: 48 MHz
- Arm Memory Protection Unit (Arm MPU) with 8 regions
- Debug and Trace: DWT, FPB, and CoreSight™ MTB-M23
- CoreSight Debug Port: SW-DP

■ Memory
- Up to 256-KB code flash memory
- 8-KB data flash memory (100,000 program/erase (P/E) cycles)
- Up to 32-KB SRAM
- Flash Cache (FCACHE)
- Memory Protection Unit (MPU)
- Memory Mirror Function (MMF)
- 128-bit unique ID

■ Connectivity
- USB 2.0 Full-Speed (USBFS) module
  - On-chip transceiver with voltage regulator
  - Compliant with USB Battery Charging Specification 1.2
- Serial Communications Interface (SCI) × 3
  - UART
  - Simple IIC
  - Simple SPI
- Serial Peripheral Interface (SPI) × 2
- I^2C bus interface (IIC) × 2
- Controller Area Network (CAN) module

■ Analog
- 16-bit A/D Converter (ADC16)
  - 1.2 Msps
  - Differential input mode
  - Single-ended input mode
- 24-bit Sigma-Delta A/D Converter (SDADC24)
  - 15.6 ksps
  - Differential input mode
  - Single-ended input mode
- 12-bit D/A Converter (DAC12)
- 8-bit D/A Converter (DAC8) × 2
- High-Speed Analog Comparator (ACMPHS)
- Low-Power Analog Comparator (ACMPLP) × 2
- Operational Amplifier (OPAMP) × 3
- Temperature Sensor (TSN)

■ Timers
- General PWM Timer 32-bit (GPT32)
- General PWM Timer 16-bit (GPT16) × 6
- Asynchronous General-Purpose Timer (AGT) × 2
- Watchdog Timer (WDT)

■ Safety
- Error Correction Code (ECC) in SRAM
- SRAM parity error check
- Flash area protection
- ADC self-diagnosis function
- Clock Frequency Accuracy Measurement Circuit (CAC)
- Cyclic Redundancy Check (CRC) calculator
- Data Operation Circuit (DOC)
- Port Output Enable for GPT (POEG)
- Independent Watchdog Timer (IWDT)
- GPIO readback level detection
- Register write protection
- Main oscillator stop detection
- Illegal memory access

■ System and Power Management
- Low power modes
- Realtime Clock (RTC)
- Event Link Controller (ELC)
- Data Transfer Controller (DTC)
- Key Interrupt Function (KINT)
- Power-on reset
- Low Voltage Detection (LVD) with voltage settings

■ Security and Encryption
- AES128/256
- True Random Number Generator (TRNG)

■ Human Machine Interface (HMI)
- Capacitive Touch Sensing Unit (CTSU)

■ Multiple Clock Sources
- Main clock oscillator (MOSC)
  (1 to 20 MHz when VCC = 2.4 to 5.5 V)
  (1 to 8 MHz when VCC = 1.8 to 5.5 V)
  (1 to 4 MHz when VCC = 1.6 to 5.5 V)
- Sub-clock oscillator (SOSC) (32.768 kHz)
- High-speed on-chip oscillator (HOCO)
  (24, 32, 48, 64 MHz when VCC = 2.4 to 5.5 V)
  (24, 32, 48 MHz when VCC = 1.8 to 5.5 V)
  (24, 32 MHz when VCC = 1.6 to 5.5 V)
- Middle-speed on-chip oscillator (MOCO) (8 MHz)
- Low-speed on-chip oscillator (LOCO) (32.768 kHz)
- IWDT-dedicated on-chip oscillator (15 kHz)
- Clock trim function for HOCO/MOCO/LOCO
- Clock out support

■ General Purpose I/O Ports
- Up to 49 input/output pins
  - Up to 3 CMOS input
  - Up to 46 CMOS input/output
    - Up to 9 input/output 5 V tolerant
    - Up to 3 high current (20 mA)

■ Operating Voltage
- VCC: 1.6 to 5.5 V

■ Operating Temperature and Packages
- Ta = -40°C to +85°C
  - 36-pin BGA (5 mm × 5 mm, 0.8 mm pitch)
- Ta = -40°C to +105°C
  - 64-pin LQFP (10 mm × 10 mm, 0.5 mm pitch)
  - 32-pin LQFP (7 mm × 7 mm, 0.8 mm pitch)
  - 48-pin QFN (7 mm × 7 mm, 0.5 mm pitch)
  - 40-pin QFN (6 mm × 6 mm, 0.5 mm pitch)

1. Overview

The MCU integrates multiple series of software- and pin-compatible Arm®-based 32-bit cores that share a common set of Renesas peripherals to facilitate design scalability and efficient platform-based product development.

The MCU in this series incorporates an energy-efficient Arm Cortex®-M23 32-bit core that is particularly well suited for cost-sensitive and low-power applications, with the following features:

- Up to 256-KB code flash memory
- 32-KB SRAM
- 16-bit A/D Converter (ADC16)
- 24-bit Sigma-Delta A/D Converter (SDADC24)
- 12-bit D/A Converter (DAC12)
- 8-bit D/A Converter (DAC8)
- Operational Amplifier (OPAMP) with configurable switches
- Security features.

1.1 Function Outline

Table 1.1 Arm core

Feature	Functional description
Arm Cortex-M23 core	• Maximum operating frequency: up to 48 MHz • Arm Cortex-M23 core: - Revision: r1p0-00rel0 - Armv8-M architecture profile - Single-cycle integer multiplier - 17-cycle integer divider. • Arm Memory Protection Unit (Arm MPU): - Armv8 Protected Memory System Architecture - 8 protect regions. • SysTick timer: - Driven by SYSTICCLK (LOCO) or ICLK.

Table 1.2 Memory

Feature	Functional description
Code flash memory	256 KB of code flash memory. See section 43, Flash Memory in User's Manual.
Data flash memory	8 KB of data flash memory. See section 43, Flash Memory in User's Manual.
Memory Mirror Function (MMF)	The Memory Mirror Function (MMF) can be configured to mirror the desired application image load address in code flash memory to the application image link address in the 23-bit unused memory space (memory mirror space addresses). Your application code is developed and linked to run from this MMF destination address. Your application code does not need to know the load location where it is stored in code flash memory. See section 5, Memory Mirror Function (MMF) in User's Manual.
Option-setting memory	The option-setting memory determines the state of the MCU after a reset. See section 7, Option-Setting Memory in User's Manual.
SRAM	On-chip high-speed SRAM with either parity bit or Error Correction Code (ECC). See section 42, SRAM in User's Manual.

Table 1.3 System (1 of 2)

Feature	Functional description
Operating modes	Two operating modes: • Single-chip mode • SCI or USB boot mode. See section 3, Operating Modes in User's Manual.

Table 1.3 System (2 of 2)

Feature	Functional description
Resets	13 resets: • RES pin reset • Power-on reset • Independent watchdog timer reset • Watchdog timer reset • Voltage monitor 0 reset • Voltage monitor 1 reset • Voltage monitor 2 reset • SRAM parity error reset • SRAM ECC error reset • Bus master MPU error reset • Bus slave MPU error reset • CPU stack pointer error reset • Software reset. See section 6, Resets in User's Manual.
Low Voltage Detection (LVD)	The Low Voltage Detection (LVD) function monitors the voltage level input to the VCC pin and the detection level can be selected using a software program. See section 8, Low Voltage Detection (LVD) in User's Manual.
Clocks	• Main clock oscillator (MOSC) • Sub-clock oscillator (SOSC) • High-speed on-chip oscillator (HOCO) • Middle-speed on-chip oscillator (MOCO) • Low-speed on-chip oscillator (LOCO) • IWDT-dedicated on-chip oscillator • Clock out support. See section 9, Clock Generation Circuit in User's Manual.
Clock Frequency Accuracy Measurement Circuit (CAC)	The Clock Frequency Accuracy Measurement Circuit (CAC) counts pulses of the clock to be measured (measurement target clock) within the time generated by the clock to be used as a measurement reference (measurement reference clock), and determines the accuracy depending on whether the number of pulses is within the allowable range. When measurement is complete or the number of pulses within the time generated by the measurement reference clock is not within the allowable range, an interrupt request is generated. See section 10, Clock Frequency Accuracy Measurement Circuit (CAC) in User's Manual.
Interrupt Controller Unit (ICU)	The Interrupt Controller Unit (ICU) controls which event signals are linked to the NVIC/DTC module. The ICU also controls NMI interrupts. See section 13, Interrupt Controller Unit (ICU) in User's Manual.
Key Interrupt Function (KINT)	A key interrupt can be generated by setting the Key Return Mode Register (KRM) and inputting a rising or falling edge to the key interrupt input pins. See section 19, Key Interrupt Function (KINT) in User's Manual.
Low power modes	Power consumption can be reduced in multiple ways, such as by setting clock dividers, stopping modules, selecting power control mode in normal operation, and transitioning to low power modes. See section 11, Low Power Modes in User's Manual.
Register write protection	The register write protection function protects important registers from being overwritten due to software errors. See section 12, Register Write Protection in User's Manual.
Memory Protection Unit (MPU)	Four Memory Protection Units (MPUs) and a CPU stack pointer monitor function are provided for memory protection. See section 15, Memory Protection Unit (MPU) in User's Manual.
Watchdog Timer (WDT)	The Watchdog Timer (WDT) is a 14-bit down-counter that can be used to reset the MCU when the counter underflows because the system has run out of control and is unable to refresh the WDT. In addition, a non-maskable interrupt or interrupt can be generated by an underflow. A refresh-permitted period can be set to refresh the counter and used as the condition to detect when the system runs out of control. See section 24, Watchdog Timer (WDT) in User's Manual.
Independent Watchdog Timer (IWDT)	The Independent Watchdog Timer (IWDT) consists of a 14-bit down-counter that must be serviced periodically to prevent counter underflow. The IWDT provides functionality to reset the MCU or to generate a non-maskable interrupt/interrupt for a timer underflow. Because the timer operates with an independent, dedicated clock source, it is particularly useful in returning the MCU to a known state as a fail-safe mechanism when the system runs out of control. The IWDT can be triggered automatically on a reset, underflow, refresh error, or by a refresh of the count value in the registers. See section 25, Independent Watchdog Timer (IWDT) in User's Manual.

Table 1.4 Event Link

Feature	Functional description
Event Link Controller (ELC)	The Event Link Controller (ELC) uses the interrupt requests generated by various peripheral modules as event signals to connect them to different modules, enabling direct interaction between the modules without CPU intervention. See section 17, Event Link Controller (ELC) in User's Manual.

Table 1.5 Direct memory access

Feature	Functional description
Data Transfer Controller (DTC)	A Data Transfer Controller (DTC) module is provided for transferring data when activated by an interrupt request. See section 16, Data Transfer Controller (DTC) in User's Manual.

Table 1.6 Timers

Feature	Functional description
General PWM Timer (GPT)	The General PWM Timer (GPT) is a 32-bit timer with one channel and a 16-bit timer with six channels. PWM waveforms can be generated by controlling the up-counter, down-counter, or the up- and down-counter. In addition, PWM waveforms can be generated for controlling brushless DC motors. The GPT can also be used as a general-purpose timer. See section 21, General PWM Timer (GPT) in User's Manual.
Port Output Enable for GPT (POEG)	Use the Port Output Enable for GPT (POEG) function to place the General PWM Timer (GPT) output pins in the output disable state. See section 20, Port Output Enable for GPT (POEG) in User's Manual.
Asynchronous General Purpose Timer (AGT)	The Asynchronous General Purpose Timer (AGT) is a 16-bit timer that can be used for pulse output, external pulse width or period measurement, and counting external events. This 16-bit timer consists of a reload register and a down-counter. The reload register and the down-counter are allocated to the same address, and they can be accessed with the AGT register. See section 22, Asynchronous General Purpose Timer (AGT) in User's Manual.
Realtime Clock (RTC)	The Realtime Clock (RTC) has two counting modes, calendar count mode and binary count mode, that are controlled by the register settings. For calendar count mode, the RTC has a 100-year calendar from 2000 to 2099 and automatically adjusts dates for leap years. For binary count mode, the RTC counts seconds and retains the information as a serial value. Binary count mode can be used for calendars other than the Gregorian (Western) calendar. See section 23, Realtime Clock (RTC) in User's Manual.

Table 1.7 Communication interfaces (1 of 2)

Feature	Functional description
Serial Communications Interface (SCI)	The Serial Communication Interface (SCI) is configurable to five asynchronous and synchronous serial interfaces: • Asynchronous interfaces (UART and asynchronous communications interface adapter (ACIA)) • 8-bit clock synchronous interface • Simple IIC (master-only) • Simple SPI • Smart card interface. The smart card interface complies with the ISO/IEC 7816-3 standard for electronic signals and transmission protocol. SCI0 has FIFO buffers to enable continuous and full-duplex communication, and the data transfer speed can be configured independently using an on-chip baud rate generator. See section 27, Serial Communications Interface (SCI) in User's Manual.
I^2C bus interface (IIC)	The 2-channel I^2C bus interface (IIC) conforms with and provides a subset of the NXP I^2C (Inter-Integrated Circuit) bus interface functions. See section 28, I2C Bus Interface (IIC) in User's Manual.
Serial Peripheral Interface (SPI)	Two independent Serial Peripheral Interface (SPI) channels are capable of high-speed, full-duplex synchronous serial communications with multiple processors and peripheral devices. See section 30, Serial Peripheral Interface (SPI) in User's Manual.

Table 1.7 Communication interfaces (2 of 2)

Feature	Functional description
Controller Area Network (CAN) module	The Controller Area Network (CAN) module provides functionality to receive and transmit data using a message-based protocol between multiple slaves and masters in electromagnetically noisy applications. The CAN module complies with the ISO 11898-1 (CAN 2.0A/CAN 2.0B) standard and supports up to 32 mailboxes, which can be configured for transmission or reception in normal mailbox and FIFO modes. Both standard (11-bit) and extended (29-bit) messaging formats are supported. See section 29, Controller Area Network (CAN) Module in User's Manual.
USB 2.0 Full-Speed (USBFS) module	The USB 2.0 Full-Speed (USBFS) module can operate as a device controller. The module supports full-speed and low-speed transfer as defined in the Universal Serial Bus Specification 2.0. The module has an internal USB transceiver and supports all of the transfer types defined in the Universal Serial Bus Specification 2.0. The USB has buffer memory for data transfer, providing a maximum of five pipes. Pipe 0 and pipe 4 to pipe 7 can be assigned any endpoint number based on the peripheral devices used for communication or based on your system. The MCU supports Battery Charging Specification revision 1.2. Because the MCU can be powered at 5 V, the USB LDO regulator provides the internal USB transceiver power supply 3.3 V. See section 26, USB 2.0 Full-Speed Module (USBFS) in User's Manual.

Table 1.8 Analog (1 of 2)

Feature	Functional description
16-bit A/D Converter (ADC16)	A successive approximation 16-bit A/D Converter (ADC16) is provided. Up to 17 single-ended/ 4 differential analog input channels are selectable. Reference voltage of SDADC24, temperature sensor output, and internal reference voltage are selectable for conversion. The calibration function calculates capacitor array DAC and gain/offset correction values under the usage conditions to enable accurate A/D conversion. See section 32, 16-Bit A/D Converter (ADC16) in User's Manual.
24-bit Sigma-Delta A/D Converter (SDADC24)	A 24-bit Sigma-Delta A/D Converter (SDADC24) with a programmable gain instrumentation amplifier is provided. Up to 10 single-ended/5 differential analog input channels are selectable. The 2 single-ended/1 differential analog input channels of these analog input channels are inputs from internal OPAMP. Analog input multiplexer is input to the sigma-delta A/D converter by the programmable gain instrumentation amplifier (PGA). The A/D conversion result is filtered by the SINC3 digital filter, and then stored in an output register. The calibration function calculates gain error and offset error correction values under the usage conditions to enable accurate A/D conversion. See section 33, 24-Bit Sigma-Delta A/D Converter (SDADC24) in User's Manual.
12-bit D/A Converter (DAC12)	A 12-bit D/A Converter (DAC12) is provided. See section 34, 12-Bit D/A Converter (DAC12) in User's Manual.
8-bit D/A Converter (DAC8)	An 8-bit D/A Converter (DAC8) is provided. See section 35, 8-Bit D/A Converter (DAC8) in User's Manual.
Temperature Sensor (TSN)	The on-chip Temperature Sensor (TSN) determines and monitors the die temperature for reliable operation of the device. The sensor outputs a voltage directly proportional to the die temperature, and the relationship between the die temperature and the output voltage is linear. The output voltage is provided to the ADC16 for conversion and can be further used by the end application. See section 36, Temperature Sensor (TSN) in User's Manual.
High-Speed Analog Comparator (ACMPHS)	The High-Speed Analog Comparator (ACMPHS) compares a reference voltage with an analog input voltage. The comparison result can be read by software and also be output externally. The reference voltage can be selected from either an input to the IVREFi (i = 0 to 2) pin, an output from internal D/A converter, or from the internal reference voltage (Vref) generated internally in the MCU. Such flexibility is useful in applications that require go/no-go comparisons to be performed between analog signals without necessarily requiring A/D conversion. See section 38, High-Speed Analog Comparator (ACMPHS) in User's Manual.
Low-Power Analog Comparator (ACMPLP)	The Low-Power Analog Comparator (ACMPLP) compares a reference voltage with an analog input voltage. The comparison result can be read by software and also be output externally. The reference voltage can be selected from either an input to the CMPREFi (i = 0, 1) pin, an internal 8-bit D/A converter output, or the internal reference voltage (Vref) generated internally in the MCU. The ACMPLP response speed can be set before starting an operation. Setting high-speed mode decreases the response delay time, but increases current consumption. Setting low-speed mode increases the response delay time, but decreases current consumption. See section 39, Low-Power Analog Comparator (ACMPLP) in User's Manual.

Table 1.8 Analog (2 of 2)

Feature	Functional description
Operational Amplifier (OPAMP)	The Operational Amplifier (OPAMP) can be used to amplify small analog input voltages and output the amplified voltages. A total of three differential operational amplifier units with two input pins and one output pin are provided. All units have switches that can select input signals. Additionally, operational amplifier 0 has a switch that can select the output pin. See section 37, Operational Amplifier (OPAMP) in User's Manual.

Table 1.9 Human machine interfaces

Feature	Functional description
Capacitive Touch Sensing Unit (CTSU)	The Capacitive Touch Sensing Unit (CTSU) measures the electrostatic capacitance of the touch sensor. Changes in the electrostatic capacitance are determined by software, which enables the CTSU to detect whether a finger is in contact with the touch sensor. The electrode surface of the touch sensor is usually enclosed with an electrical insulator so that fingers do not come into direct contact with the electrodes. See section 40, Capacitive Touch Sensing Unit (CTSU) in User's Manual.

Table 1.10 Data processing

Feature	Functional description
Cyclic Redundancy Check (CRC) calculator	The Cyclic Redundancy Check (CRC) calculator generates CRC codes to detect errors in the data. The bit order of CRC calculation results can be switched for LSB-first or MSB-first communication. Additionally, various CRC-generating polynomials are available. The snoop function allows monitoring reads from and writes to specific addresses. This function is useful in applications that require CRC code to be generated automatically in certain events, such as monitoring writes to the serial transmit buffer and reads from the serial receive buffer. See section 31, Cyclic Redundancy Check (CRC) Calculator in User's Manual.
Data Operation Circuit (DOC)	The Data Operation Circuit (DOC) compares, adds, and subtracts 16-bit data. See section 41, Data Operation Circuit (DOC) in User's Manual.

Table 1.11 Security

Feature	Functional description
AES	See section 44, AES Engine in User's Manual.
True Random Number Generator (TRNG)	See section 45, True Random Number Generator (TRNG) in User's Manual.

1.2 Block Diagram

Figure 1.1 shows a block diagram of the MCU superset, some individual devices within the group have a subset of the features.

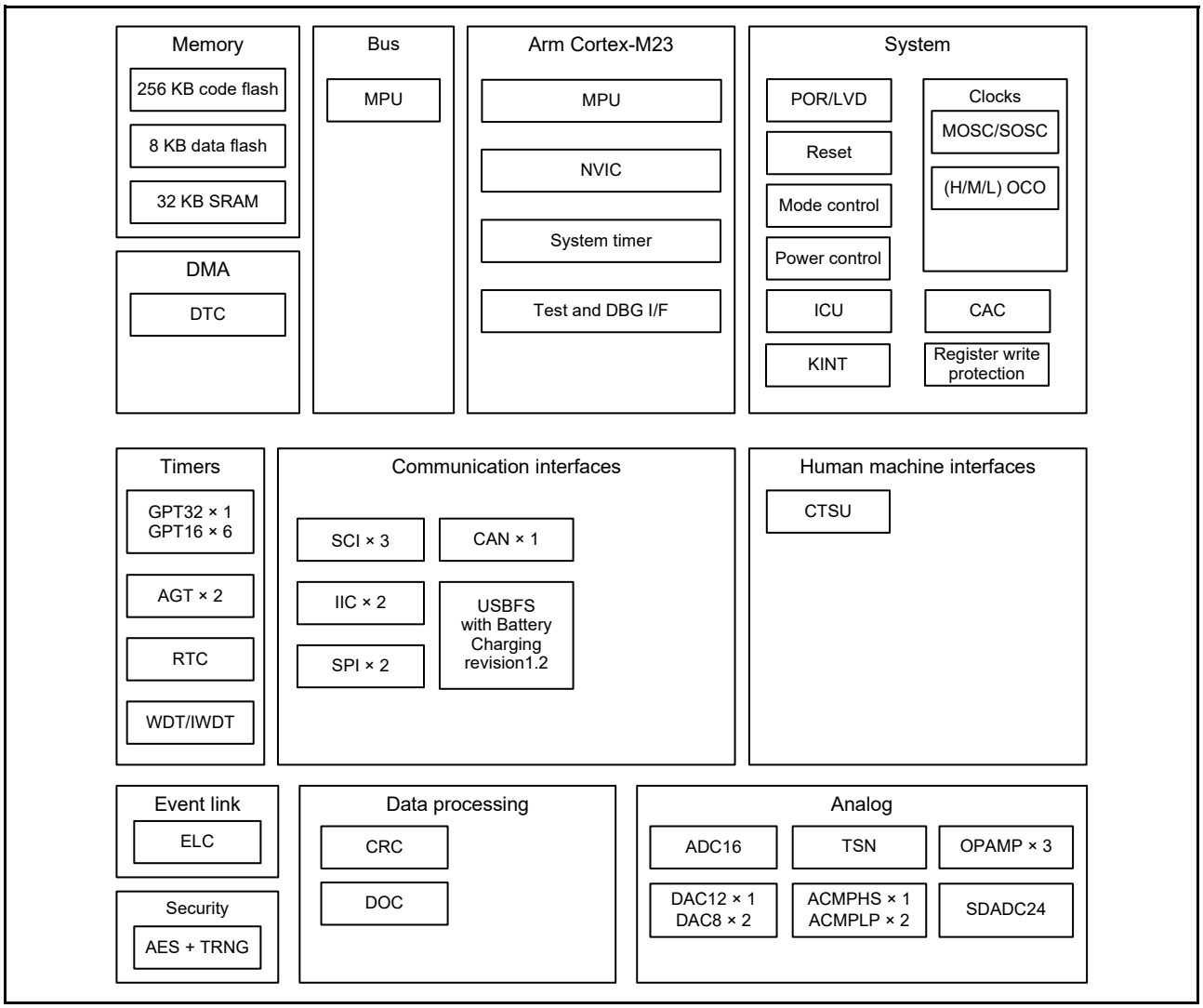


Figure 1.1 Block diagram

1.3 Part Numbering

Figure 1.2 shows the product part number information, including memory capacity and package type. Table 1.12 shows a list of products.

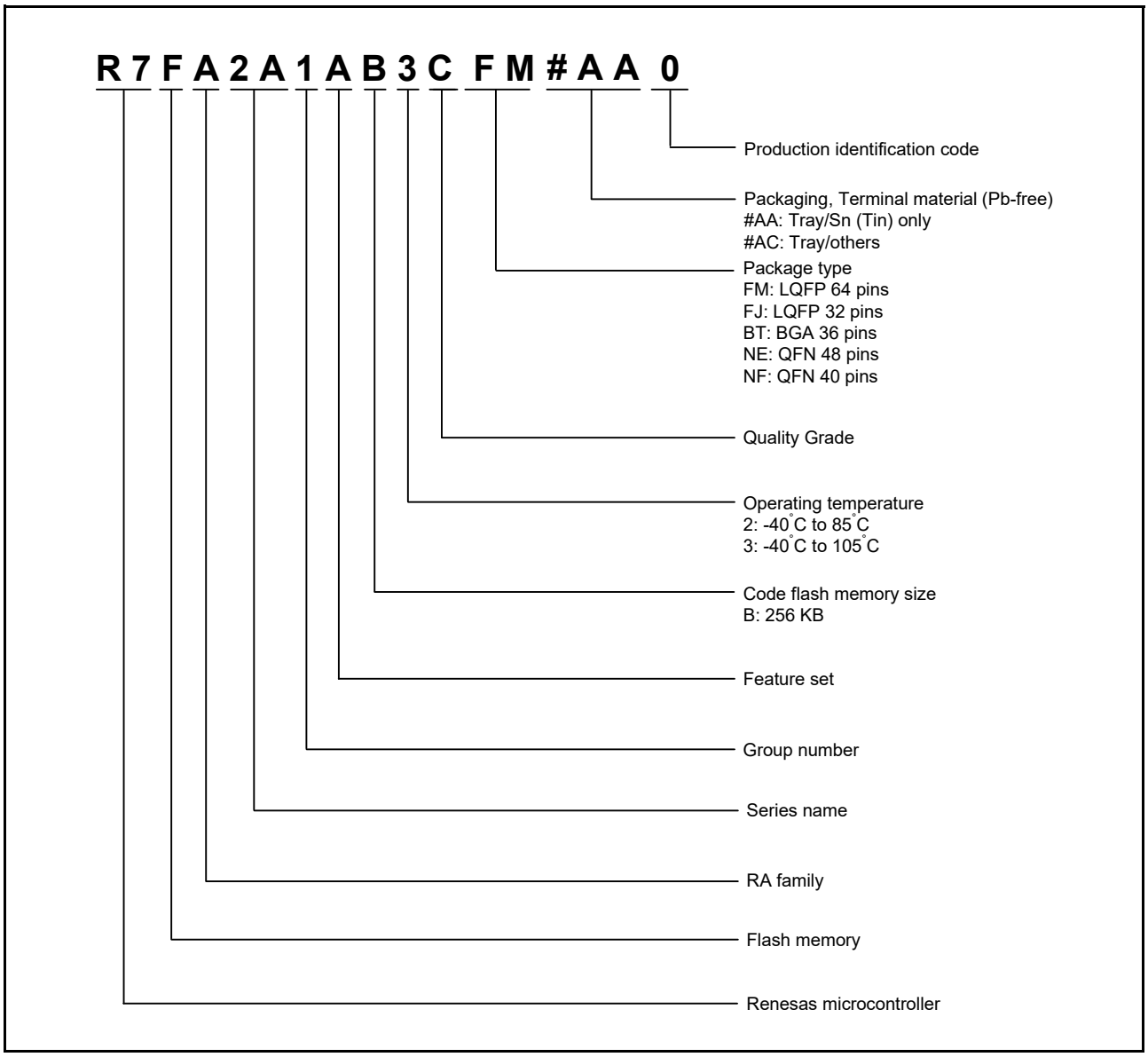


Figure 1.2 Part numbering scheme

Table 1.12 Product list

Product part number	Orderable part number	Package code	Code flash	Data flash	SRAM	Operating temperature
R7FA2A1AB3CFM	R7FA2A1AB3CFM#AA0	PLQP0064KB-C	256 KB	8 KB	32 KB	-40 to +105°C
R7FA2A1AB3CNE	R7FA2A1AB3CNE#AC0	PWQN0048KB-A				-40 to +105°C
R7FA2A1AB3CNF	R7FA2A1AB3CNF#AC0	PWQN0040KC-A				-40 to +105°C
R7FA2A1AB2CBT	R7FA2A1AB2CBT#AC0	PLBG0036GA-A				-40 to +85°C
R7FA2A1AB3CFJ	R7FA2A1AB3CFJ#AA0	PLQP0032GB-A				-40 to +105°C

1.4 Function Comparison

Table 1.13 Function comparison

Part numbers		R7FA2A1AB3CFM	R7FA2A1AB3CNE	R7FA2A1AB3CNF	R7FA2A1AB2CBT	R7FA2A1AB3CFJ
Pin count		64	48	40	36	32
Package		LQFP	QFN	QFN	BGA	LQFP
Code flash memory		256 KB				
Data flash memory		8 KB				
SRAM		32 KB				
	Parity	16 KB				
	ECC	16 KB				
System	CPU clock	48 MHz				
	Sub-clock oscillator	Yes				No
	ICU	Yes				
	KINT	8	6	4	4	3
Event control	ELC	Yes				
DMA	DTC	Yes				
Timers	GPT32	1				
	GPT16	6	6	4	3	4
	AGT	2				
	RTC	Yes				
	WDT/IWDT	Yes				
Communication	SCI	3				
	IIC	2				
	SPI	2			1	2
	CAN	Yes				
	USBFS	Yes				No
Analog	ADC16	17 (4*1)	12 (3*1)	8 (1*1)	5 (1*1)	5 (1*1)
	SDADC24	8 (4*1)	6 (3*1)	4 (2*1)	2 (1*1)	2 (1*1)
	DAC12	1				
	DAC8	2	2*2		2*3	
	ACMPHS	1				
	ACMPLP	2				
	OPAMP	3	2	1	1	1
	TSN	Yes				
HMI	CTSU	26	16	11	9	11
Data processing	CRC	Yes				
	DOC	Yes				
Security		AES and TRNG				

Note 1. The number of channels of the differential analog input.
Note 2. Pin output function of DA8_1 cannot be used.
Note 3. Pin output function of DA8_0 and DA8_1 cannot be used.

1.5 Pin Functions

Table 1.14 Pin functions (1 of 4)

Function	Signal	I/O	Description
Power supply	VCC	Input	Power supply pin. Connect this pin to the system power supply. Connect it to VSS by a 0.1-μF capacitor. Place the capacitor close to the pin.
	VCL	I/O	Connect this pin to VSS through a smoothing capacitor used to stabilize the internal power supply. Place the capacitor close to the pin.
	VSS	Input	Ground pin. Connect to the system power supply (0 V).
Clock	XTAL	Output	Pins for a crystal resonator. An external clock signal can be input through the EXTAL pin.
	EXTAL	Input	
	XCIN	Input	Input/output pins for the sub-clock oscillator. Connect a crystal resonator between XCOUT and XCIN.
	XCOUT	Output	
	CLKOUT	Output	Clock output pin
Operating mode control	MD	Input	Pins for setting the operating mode. The signal level on this pin must not be changed during operation mode transition on release from the reset state.
System control	RES	Input	Reset signal input pin. The MCU enters the reset state when this signal goes low.
CAC	CACREF	Input	Measurement reference clock input pin
On-chip debug	SWDIO	I/O	Serial wire debug data input/output pin
	SWCLK	Input	Serial wire clock pin
Interrupt	NMI	Input	Non-maskable interrupt request pin
	IRQ0 to IRQ7	Input	Maskable interrupt request pins
GPT	GTETRGA, GTETRGB	Input	External trigger input pin
	GTIOC0A to GTIOC6A, GTIOC0B to GTIOC6B	I/O	Input capture, output compare, or PWM output pin
	GTIU	Input	Hall sensor input pin U
	GTIV	Input	Hall sensor input pin V
	GTIW	Input	Hall sensor input pin W
	GTOUUP	Output	3-phase PWM output for BLDC motor control (positive U phase)
	GTOULO	Output	3-phase PWM output for BLDC motor control (negative U phase)
	GTOVUP	Output	3-phase PWM output for BLDC motor control (positive V phase)
	GTOVLO	Output	3-phase PWM output for BLDC motor control (negative V phase)
	GTOWUP	Output	3-phase PWM output for BLDC motor control (positive W phase)
	GTOWLO	Output	3-phase PWM output for BLDC motor control (negative W phase)
AGT	AGTEE0, AGTEE1	Input	External event input enable
	AGTIO0, AGTIO1	I/O	External event input and pulse output
	AGTO0, AGTO1	Output	Pulse output
	AGTOA0, AGTOA1	Output	Output compare match A output
	AGTOB0, AGTOB1	Output	Output compare match B output
RTC	RTCOUT	Output	Output pin for 1-Hz/64-Hz clock

Table 1.14 Pin functions (2 of 4)

Function	Signal	I/O	Description
SCI	SCK0, SCK1, SCK9	I/O	Input/output pins for the clock (clock synchronous mode)
	RXD0, RXD1, RXD9	Input	Input pins for received data (asynchronous mode/clock synchronous mode)
	TXD0, TXD1, TXD9	Output	Output pins for transmitted data (asynchronous mode/clock synchronous mode)
	CTS0_RTS0, CTS1_RTS1, CTS9_RTS9	I/O	Input/output pins for controlling the start of transmission and reception (asynchronous mode/clock synchronous mode), active-low
	SCL0, SCL1, SCL9	I/O	Input/output pins for the IIC clock (simple IIC)
	SDA0, SDA1, SDA9	I/O	Input/output pins for the IIC data (simple IIC)
	SCK0, SCK1, SCK9	I/O	Input/output pins for the clock (simple SPI)
	MISO0, MISO1, MISO9	I/O	Input/output pins for slave transmission of data (simple SPI)
	MOSI0, MOSI1, MOSI9	I/O	Input/output pins for master transmission of data (simple SPI)
	SS0, SS1, SS9	Input	Chip-select input pins (simple SPI), active-low
IIC	SCL0, SCL1	I/O	Input/output pins for clock
	SDA0, SDA1	I/O	Input/output pins for data
SPI	RSPCKA, RSPCKB	I/O	Clock input/output pin
	MOSIA, MOSIB	I/O	Inputs or outputs data output from the master
	MISOA, MISOB	I/O	Inputs or outputs data output from the slave
	SSLA0, SSLB0	I/O	Input or output pin for slave selection
	SSLA1 to SSLA3, SSLB1 to SSLB3	Output	Output pin for slave selection
CAN	CRX0	Input	Receive data
	CTX0	Output	Transmit data
USBFS	VSS_USB	Input	Ground pins
	VCC_USB_LDO	Input	Power supply pin for USB LDO regulator
	VCC_USB	I/O	Input: Power supply pin for USB transceiver. Output: USB LDO regulator output pin. This pin should be connected to an external capacitor.
	USB_DP	I/O	D+ I/O pin of the USB on-chip transceiver. This pin should be connected to the D+ pin of the USB bus.
	USB_DM	I/O	D- I/O pin of the USB on-chip transceiver. This pin should be connected to the D- pin of the USB bus.
	USB_VBUS	Input	USB cable connection monitor pin. This pin should be connected to VBUS of the USB bus. The VBUS pin status (connected or disconnected) can be detected when the USB module is operating as a device controller.

Table 1.14 Pin functions (3 of 4)

Function	Signal	I/O	Description
Analog power supply	AVCC0	Input	Analog voltage supply pin for the ADC16, DAC12, DAC8, ACMPHS, ACMPLP, and OPAMP
	AVSS0	Input	Analog ground pin for the ADC16, DAC12, DAC8, ACMPHS, ACMPLP, and OPAMP
	AVCC1	Input	Analog voltage supply pin for the SDADC24
	AVSS1	Input	Analog ground pin for the SDADC24
	VREFH0	Input	Analog reference voltage supply pin for the ADC16. Connect this pin to AVCC0 when not using the ADC16.
	VREFL0	Input	Analog reference ground pin for the ADC16. Connect this pin to AVSS0 when not using the ADC16.
	VREFH	Input	Analog reference voltage supply pin for the DAC12
	VREFL	Input	Analog reference ground pin for the DAC12
ADC16	AN000 to AN008, AN016 to AN023	Input	Input pins for the analog signals to be processed by the A/D converter
	ADTRG0	Input	Input pins for the external trigger signals that start the A/D conversion, active-low
SDADC24	ANSD0P to ANSD3P	Input	Input pins for the analog signals to be processed by the SDADC24
	ANSD0N to ANSD3N	Input	Input pins for the analog signals to be processed by the SDADC24
	ADREG	Output	Regulator capacitance for the SDADC24
	SBIAS	Output	Sensor power supply
	VREFI	Input	External reference voltage supply pin for the SDADC24
DAC12	DA12_0	Output	Output pin for the analog signals to be processed by the 12-bit D/A converter
DAC8	DA8_0, DA8_1	Output	Output pins for the analog signals to be processed by the 8-bit D/A converter
Comparator output	VCOUT	Output	Comparator output pin
ACMPHS	IVREF0 to IVREF2	Input	Reference voltage input pin
	IVCMP0 to IVCMP2	Input	Analog voltage input pin
ACMPLP	CMPREF0, CMPREF1	Input	Reference voltage input pins
	CMPIN0, CMPIN1	Input	Analog voltage input pins
OPAMP	AMP0+ to AMP2+	Input	Analog voltage input pins
	AMP0- to AMP2-	Input	Analog voltage input pins
	AMP0O to AMP2O	Output	Analog voltage output pins
CTSU	TS00 to TS25	Input	Capacitive touch detection pins (touch pins)
	TSCAP	-	Secondary power supply pin for the touch driver
KINT	KR00 to KR07	Input	Key interrupt input pins

Table 1.14 Pin functions (4 of 4)

Function	Signal	I/O	Description
I/O ports	P000 to P003, P012 to P015	I/O	General-purpose input/output pins
	P100 to P112	I/O	General-purpose input/output pins
	P200	Input	General-purpose input pin
	P201, P204 to P206, P212, P213	I/O	General-purpose input/output pins
	P214, P215	Input	General-purpose input pins
	P300 to P304	I/O	General-purpose input/output pins
	P400 to P403, P407 to P411	I/O	General-purpose input/output pins
	P500 to P502	I/O	General-purpose input/output pins
	P914, P915	I/O	General-purpose input/output pins

1.6 Pin Assignments

Figure 1.3 to Figure 1.7 show the pin assignments.

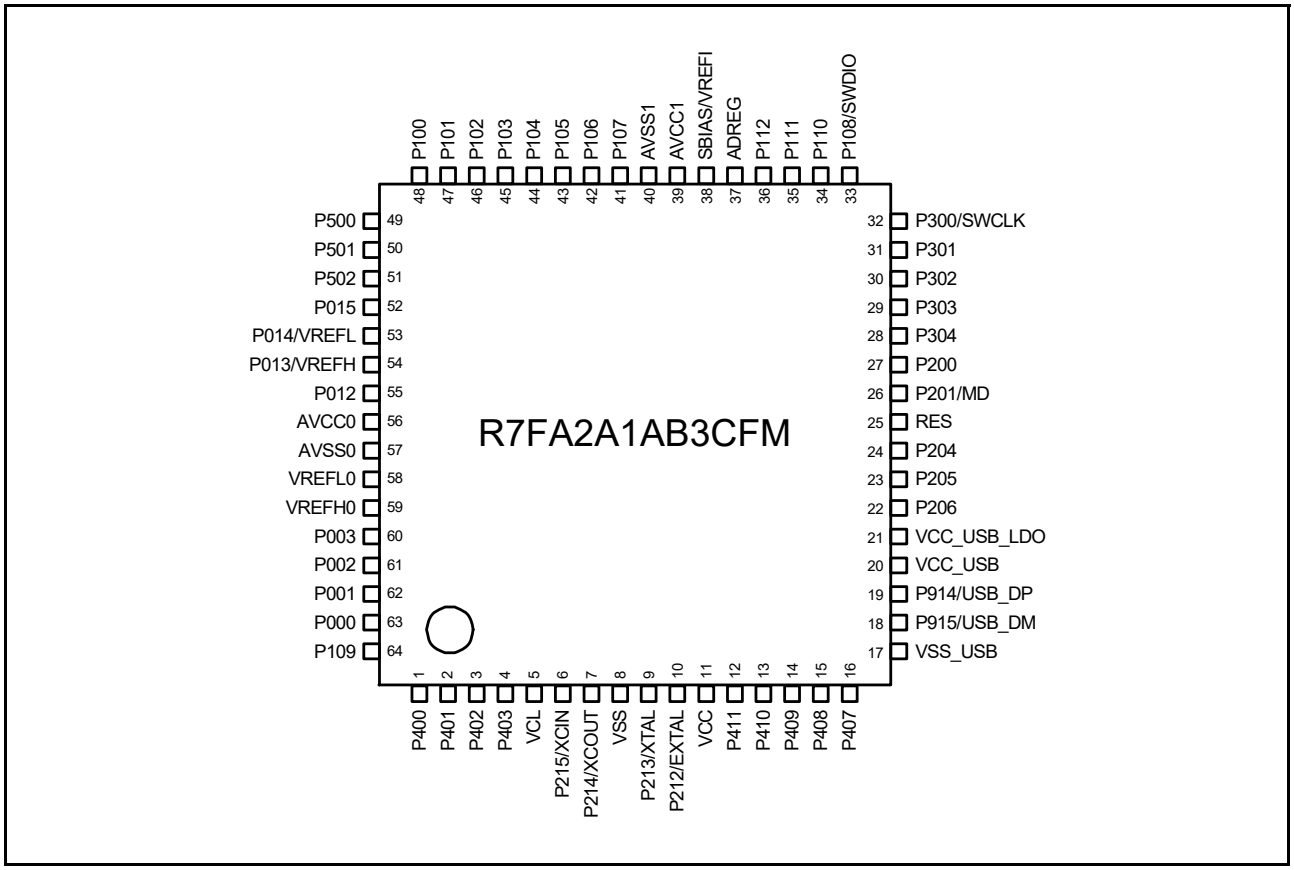


Figure 1.3 Pin assignment for LQFP 64-pin

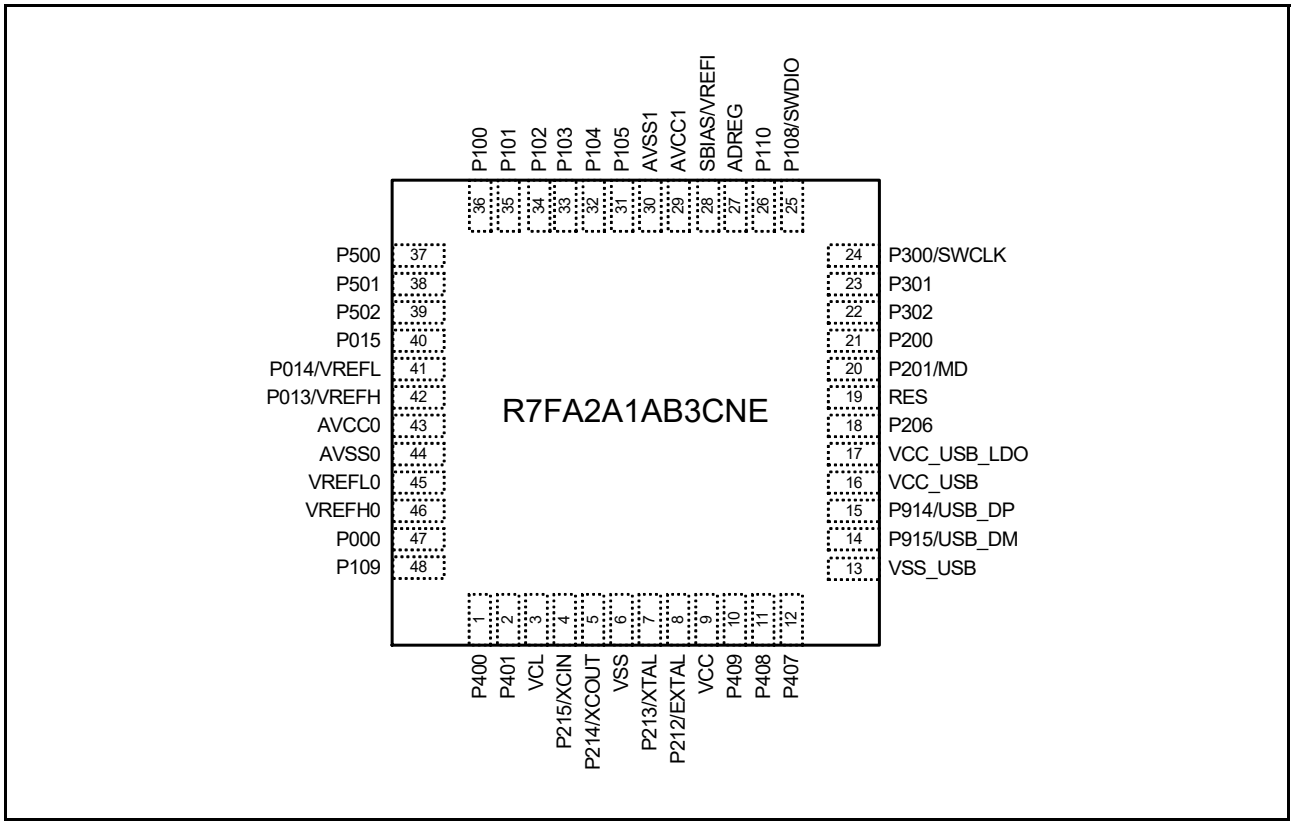


Figure 1.4 Pin assignment for QFN 48-pin

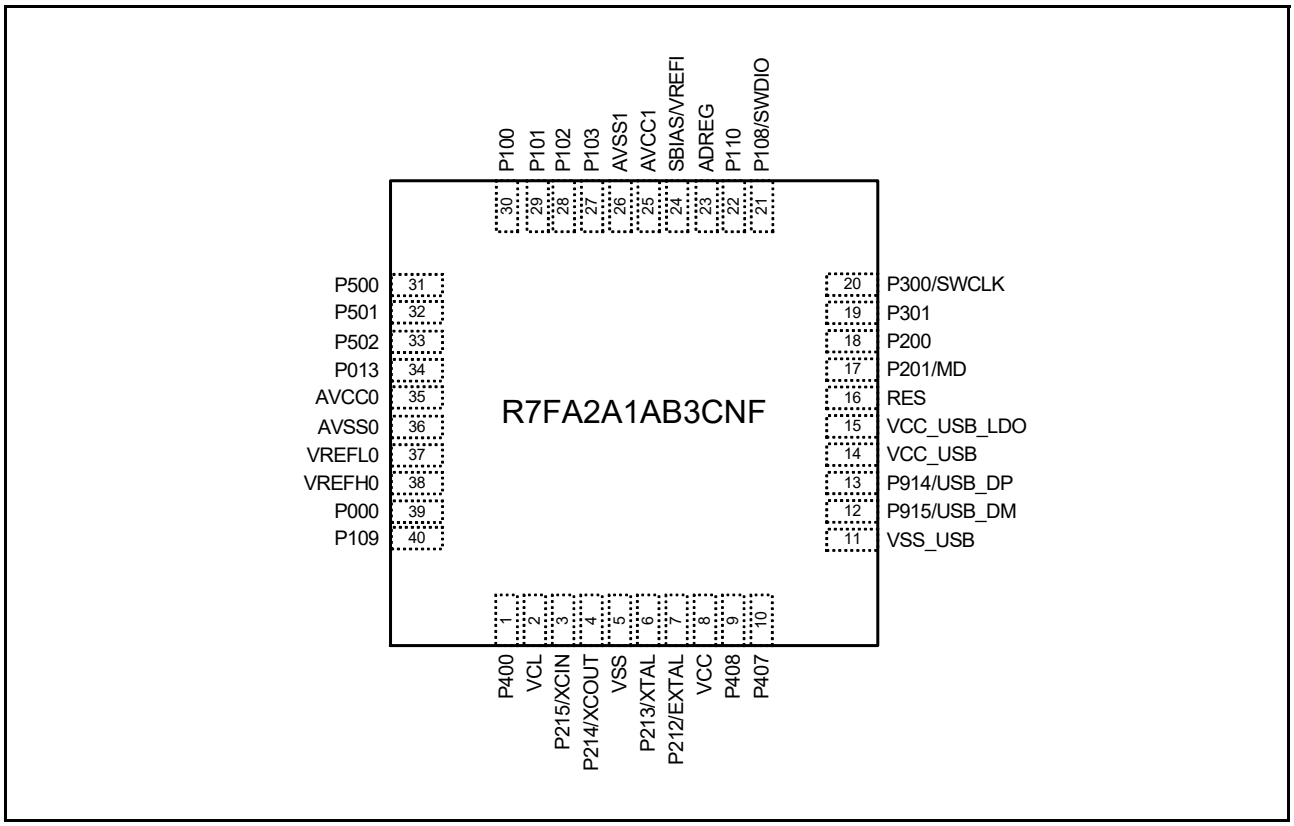


Figure 1.5 Pin assignment for QFN 40-pin

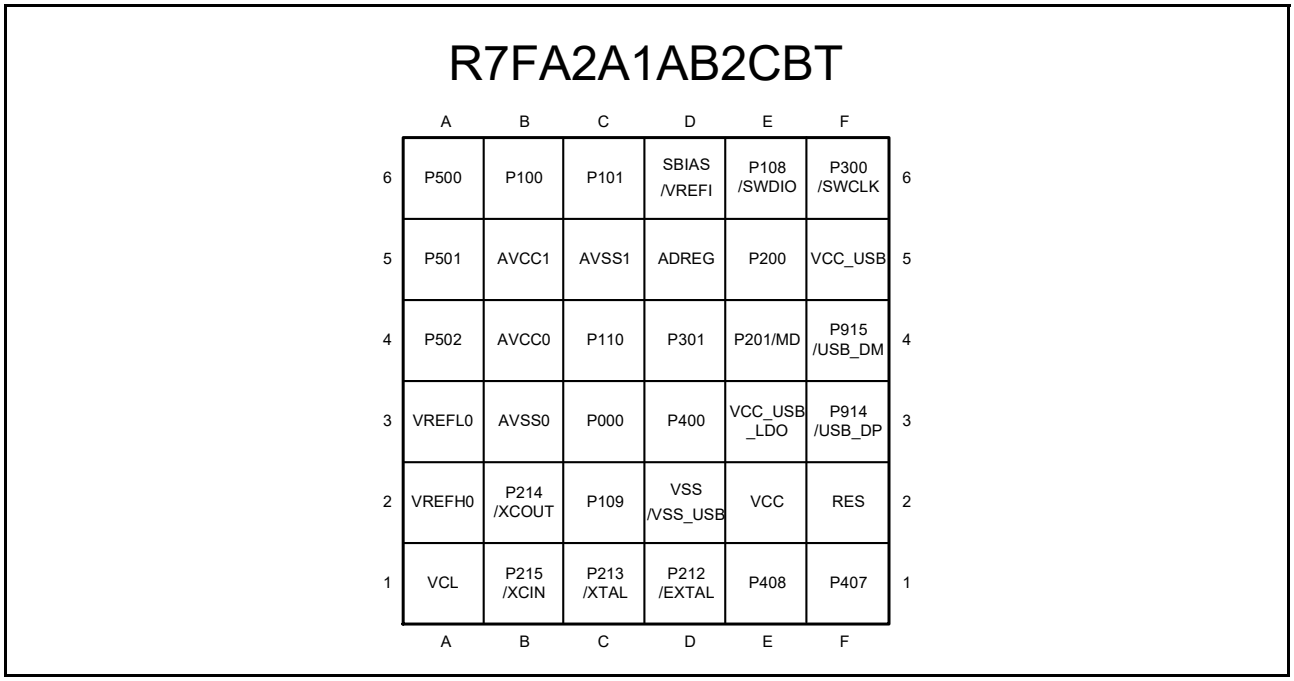


Figure 1.6 Pin assignment for BGA 36-pin (top view, pad side down)

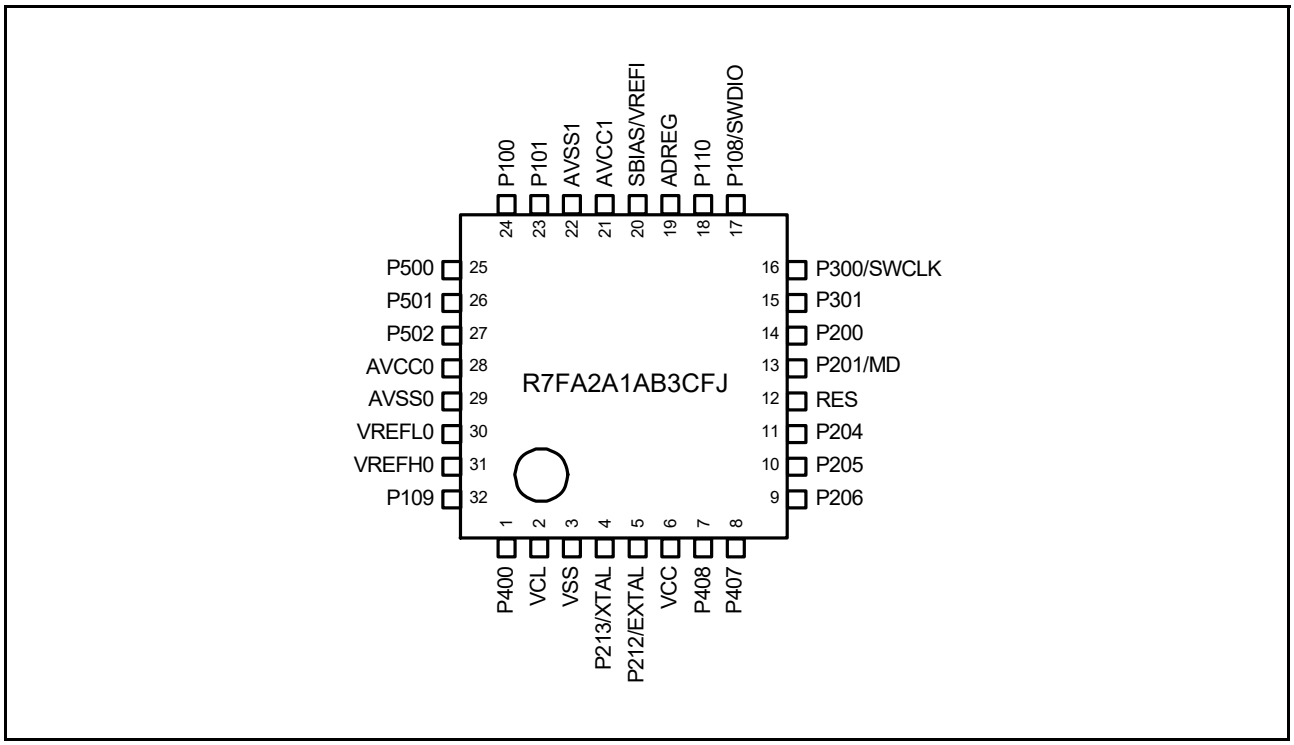


Figure 1.7 Pin assignment for LQFP 32-pin

1.7 Pin Lists

Pin number					Power, System, Clock, Debug, CAC	I/O ports	Timers				Communication Interfaces				Analogs					HMI	
LQFP64	QFN48	QFN40	BGA36	LQFP32			AGT	GPT_OPS, POEG	GPT	RTC	USBFS, CAN	SCI	IIC	SPI	ADC16	SDADC24	DAC12, DAC8	ACMPHS, ACMPLP	OPAMP	CTSU	Interrupt
1	1	1	D3	1		P400	AGTEE0_A	GTETRGA_A	GTIOC1A_A	RTCOUT_C		CTS0_RTS0_D/ SS0_D/ RXD1_C/ MISO1_C/ SCL1_C	SDA1_A	MOSIA_A				CMPIN0		TS00	KR02/ IRQ0_A
2	2	-	-	-		P401	AGTEE1_A	GTIU_A	GTIOC4A_A			SCK0_D/ SCK9_A	SDA0_C	SSLB1_A				VCOUT_B		TS01	KR03/ IRQ5_B
3	-	-	-	-		P402		GTIV_A	GTIOC0A_D			CTS9_RTS9_C/ SS9_C		SSLB2_A						TS02	
4	-	-	-	-		P403		GTIW_A	GTIOC0B_C			SCK1_B		SSLB3_A						TS03	
5	3	2	A1	2	VCL																
6	4	3	B1	-	XCIN	P215															
7	5	4	B2	-	XCOUT	P214															
8	6	5	D2	3	VSS																
9	7	6	C1	4	XTAL	P213	AGTEE1_B	GTETRGA_B	GTIOC0A_B			RXD1_D/ MISO1_D/ SCL1_D									IRQ2_B
10	8	7	D1	5	EXTAL	P212	AGTIO0_A	GTETRGB_B	GTIOC0B_B			TXD1_D/ MOSI1_D/ SDA1_D									IRQ3_B
11	9	8	E2	6	VCC																
12	-	-	-	-		P411			GTIOC5A_A			TXD0_F/ MOSI0_F/ SDA0_F/ RXD1_B/ MISO1_B/ SCL1_B		SSLA3_A						TS04	
13	-	-	-	-		P410			GTIOC5B_A			CTS0_RTS0_A/ SS0_A/ TXD1_B/ MOSI1_B/ SDA1_B		SSLA2_A						TS05	
14	10	-	-	-		P409	AGTO1_A		GTIOC0A_C		CTX0_B	SCK0_A/ CTS1_RTS1_B/ SS1_B	SCL0_B	SSLA1_A						TSCAP_E	IRQ7_A
15	11	9	E1	7		P408	AGTO0_A	GTOUUP_A	GTIOC0A_A		CRX0_B	RXD0_A/ MISO0_A/ SCL0_A/ TXD1_C/ MOSI1_C/ SDA1_C	SDA0_B	SSLA0_A				CMPIN1		TS06	IRQ1_A
16	12	10	F1	8	CACREF_B	P407	AGTIO0_C	GTOULO_A	GTIOC0B_A		USB_VBUS/ CTX0_D	TXD0_A/ MOSI0_A/ SDA0_A/ TXD9_A/ MOSI9_A/ SDA9_A	SCL0_A	RSPCKB_B						TSCAP_D	IRQ1_B
17	13	11	D2	-	VSS_USB																
18	14	12	F4	-		P915					USB_DM										
19	15	13	F3	-		P914					USB_DP										
20	16	14	F5	-	VCC_USB																
21	17	15	E3	-	VCC_USB_LDO																
22	18	-	-	9		P206	AGTIO0_B	GTOVUP_A	GTIOC3A_A			CTS0_RTS0_C/ SS0_C/ TXD1_A/ MOSI1_A/ SDA1_A	SCL1_B	SSLB0_A						TS07	IRQ6_A
23	-	-	-	10		P205		GTOVLO_A	GTIOC3B_A			TXD0_C/ MOSI0_C/ SDA0_C/ CTS1_RTS1_A/ SS1_A	SDA1_B	MISOB_B						TS08	IRQ0_C
24	-	-	-	11		P204						RXD0_C/ MISO0_C/ SCL0_C/ SCK9_B		MOSIB_B						TS09	
25	19	16	F2	12	RES																
26	20	17	E4	13	MD	P201															
27	21	18	E5	14		P200															NMI
28	-	-	-	-		P304			GTIOC6A_A		CTX0_A	SCK0_B/ TXD9_C/ MOSI9_C/ SDA9_C		MISOA_B						TS10	KR07
29	-	-	-	-		P303			GTIOC6B_A		CRX0_A	CTS0_RTS0_B/ SS0_B/ SCK1_A		MOSIA_B						TS11	KR06
30	22	-	-	-	CACREF_A	P302	AGTOA1_A	GTOVLO_B	GTIOC3B_B			TXD0_B/ MOSI0_B/ SDA0_B/ RXD1_A/ MISO1_A/ SCL1_A		RSPCKB_A						TS12	KR05/ IRQ4_B

Pin number					Power, System, Clock, Debug, CAC	I/O ports	Timers				Communication Interfaces				Analogs					HMI	
LQFP64	QFN48	QFN40	BGA36	LQFP32			AGT	GPT_OPS, POEG	GPT	RTC	USBFS, CAN	SCI	IIC	SPI	ADC16	SDADC24	DAC12, DAC8	ACMPHS, ACMPLP	OPAMP	CTSU	Interrupt
31	23	19	D4	15		P301	AGTOB1_A	GTOWUP_A	GTIOC2A_B	RTCOUT_A		RXD0_B/ MISO0_B/ SCL0_B/ CTS9_RTS9_B/ SS9_B	SDA0_A	MOSIB_A						TS13	KR04/ IRQ5_A
32	24	20	F6	16	SWCLK	P300															
33	25	21	E6	17	SWDIO	P108															
34	26	22	C4	18	CLKOUT_A	P110	AGTOB0_A	GTOWLO_A	GTIOC2B_B		CTX0_C	TXD0_D/ MOSI0_D/ SDA0_D/ RXD9_B/ MISO9_B/ SCL9_B	SDA1_D	RSPCKA_A	ADTRG0_A			CMPREF1		TSCAP_A	IRQ2_A
35	-	-	-	-		P111				RTCOUT_B			SCL1_C	RSPCKA_B						TS14	IRQ6_B
36	-	-	-	-	CLKOUT_B	P112							SDA1_C	SSLA0_B						TSCAP_B	IRQ7_B
37	27	23	D5	19	ADREG																
38	28	24	D6	20	SBIAS/ VREFI																
39	29	25	B5	21	AVCC1																
40	30	26	C5	22	AVSS1																
41	-	-	-	-		P107									AN023	ANSD3N					
42	-	-	-	-		P106									AN022	ANSD3P					
43	31	-	-	-		P105								MOSIB_C	AN021	ANSD2N				TS18	IRQ7_C
44	32	-	-	-		P104								MISOB_C	AN020	ANSD2P				TS19	IRQ6_C
45	33	27	-	-		P103			GTIOC6A_B					RSPCKB_C	AN019	ANSD1N				TS20	
46	34	28	-	-		P102			GTIOC6B_B			CTS9_RTS9_D/ SS9_D		SSLB0_C	AN018	ANSD1P				TS21	
47	35	29	C6	23		P101			GTIOC5A_B			RXD9_C/ MISO9_C/ SCL9_C			AN017	ANSD0N		IVREF2		TS22	IRQ5_C
48	36	30	B6	24		P100			GTIOC5B_B			TXD9_D/ MOSI9_D/ SDA9_D			AN016	ANSD0P		IVCMP2		TS23	IRQ4_C
49	37	31	A6	25		P500			GTIOC5A_C			RXD0_D/ MISO0_D/ SCL0_D			AN000		DA12_0	IVCMP0	AMP0+	TS24	IRQ3_C
50	38	32	A5	26		P501			GTIOC5B_C			TXD0_E/ MOSI0_E/ SDA0_E			AN001			IVREF0	AMP0-	TS25	IRQ2_C
51	39	33	A4	27		P502						CTS0_RTS0_E/ SS0_E			AN002				AMP0O		IRQ1_C
52	40	-	-	-		P015									AN003				AMP1O		
53	41	-	-	-	VREFL	P014			GTIOC6A_C						AN004			IVREF1	AMP1-		
54	42	34	-	-	VREFH	P013			GTIOC6B_C						AN005		DA8_0	IVCMP1	AMP1+		
55	-	-	-	-		P012									AN008				AMP2O		
56	43	35	B4	28	AVCC0																
57	44	36	B3	29	AVSS0																
58	45	37	A3	30	VREFL0																
59	46	38	A2	31	VREFH0																
60	-	-	-	-		P003									AN006				AMP2-		
61	-	-	-	-		P002									AN007		DA8_1		AMP2+		
62	-	-	-	-		P001				RTCOUT_D		CTS9_RTS9_A/ SS9_A		RSPCKB_D						TS15	IRQ0_B
63	47	39	C3	-		P000	AGTIO1_A		GTIOC4B_B			RXD9_A/ MISO9_A/ SCL9_A	SCL0_C	MISOB_A						TS16	KR00/ IRQ4_A
64	48	40	C2	32		P109	AGTOA0_A	GTETRGB_A	GTIOC1B_B			SCK0_C/ TXD9_B/ MOSI9_B/ SDA9_B	SCL1_A	MISOA_A	ADTRG0_B			CMPREF0/ VCOUT_A		TS17	KR01/ IRQ3_A

Note: Several pin names have the added suffix of _A, _B, _C, _D, _E and _F. The suffix can be ignored when assigning functionality.

2. Electrical Characteristics

Unless otherwise specified, the electrical characteristics of the MCU are defined under the following conditions:

- VCC*1 = AVCC0 = AVCC1 = VCC_USB*2 = VCC_USB_LDO*2 = 1.6 to 5.5 V
- VREFH = VREFH0 = 1.6 to AVCC0
- VSS = AVSS0 = AVSS1 = VREFL = VREFL0 = VSS_USB = 0 V
- Ta = T_{opr}.

Note 1. The typical condition is set to VCC = 3.3 V.
Note 2. When USBFS is not used.

Figure 2.1 shows the timing conditions.

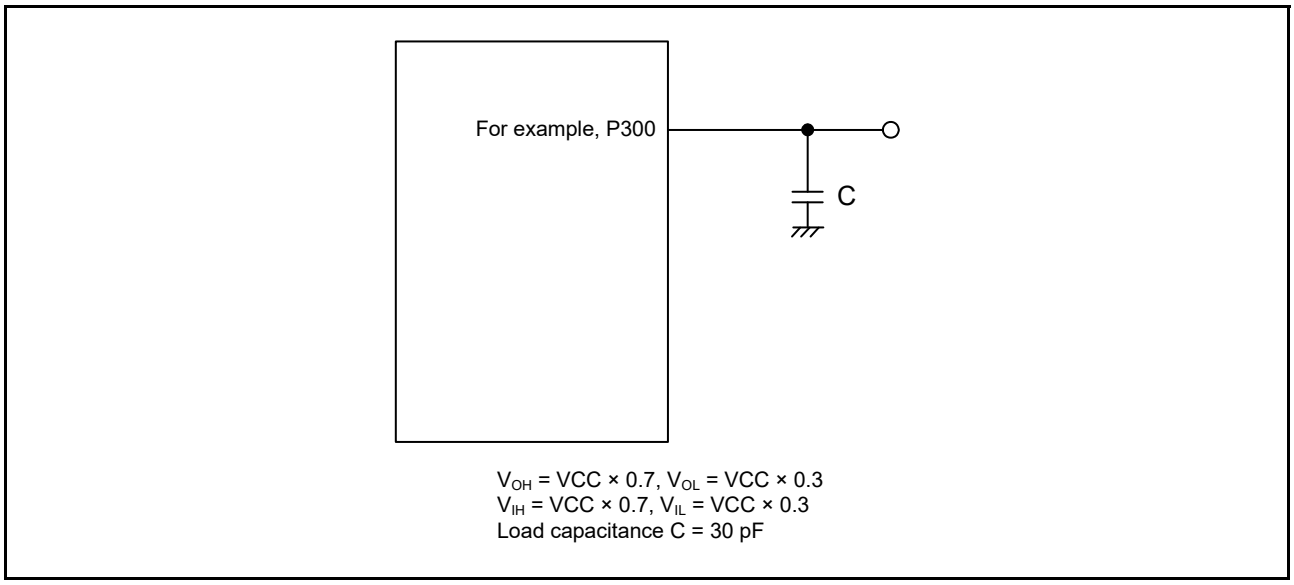


Figure 2.1 Input or output timing measurement conditions

The measurement conditions for the timing specifications of each peripheral are recommended for the best peripheral operation. However, make sure to adjust driving abilities of each pin to meet the conditions of your system.

Each function pin used for the same function must select the same drive ability. If the I/O drive ability of each function pin is mixed, the A/C specification of each function is not guaranteed.

2.1 Absolute Maximum Ratings

Table 2.1 Absolute maximum ratings (1 of 2)

Parameter		Symbol	Value	Unit
Power supply voltage		VCC	-0.5 to +6.5	V
Input voltage	5 V-tolerant ports*1	V_{in}	-0.3 to +6.5	V
	P002, P003, P012 to P015, P500 to P502	V_{in}	-0.3 to AVCC0 + 0.3	V
	P100 to P107	V_{in}	-0.3 to AVCC1 + 0.3	V
	Others	V_{in}	-0.3 to VCC + 0.3	V
Reference power supply voltage		VREFH0	-0.3 to +6.5	V
		VREFH	-0.3 to +6.5	V
		VREFI	-0.3 to AVCC1 + 0.3	V
Analog power supply voltage		AVCC0, AVCC1*5	-0.5 to +6.5	V

Table 2.1 Absolute maximum ratings (2 of 2)

Parameter		Symbol	Value	Unit
USB power supply voltage		VCC_USB	-0.5 to +6.5	V
		VCC_USB_LDO	-0.5 to +6.5	V
Analog input voltage	When AN000 to AN008 are used	V_{AN}	-0.3 to AVCC0 + 0.3	V
	When AN016 to AN023 are used		-0.3 to AVCC1 + 0.3	V
	When ANSD0P to ANSD3P and ANSD0N to ANSD3N are used		-0.3 to AVCC1 + 0.3	V
Operating temperature*2 *3 *4		T_{opr}	-40 to +85 -40 to +105	°C
Storage temperature		T_{stg}	-55 to +125	°C

Note 1. Ports P000, P111, P112, P205, P206, P301, P401, P407, and P409 are 5 V tolerant.
Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up might cause malfunction and the abnormal current that passes in the device at this time might cause degradation of internal elements.
Note 2. See section 2.2.1, Tj/Ta Definition.
Note 3. Contact Renesas Electronics sales office for information on derating operation when Ta = +85°C to +105°C. Derating is the systematic reduction of load for improved reliability.
Note 4. The upper limit of the operating temperature is 85°C or 105°C, depending on the product. For details, see section 1.3, Part Numbering.
Note 5. Use AVCC0 and AVCC1 under the same conditions:
AVCC0 = AVCC1

Caution: Permanent damage to the MCU may result if absolute maximum ratings are exceeded.
To preclude any malfunctions due to noise interference, insert capacitors with high frequency characteristics between the VCC and VSS pins, between the AVCC0 and AVSS0 pins, between the AVCC1 and AVSS1 pins, between the VCC_USB and VSS_USB pins, between the VREFH and VREFL pins, and between the VREFH0 and VREFL0 pins when VREFH0 is selected as the high potential reference voltage for the ADC16. Place capacitors of the following value as close as possible to every power supply pin and use the shortest and heaviest possible traces:
- VCC and VSS: about 0.1 µF
- AVCC0 and AVSS0: about 0.1 µF
- AVCC1 and AVSS1: about 0.1 µF
- VREFH and VREFL: about 0.1 µF
- VREFH0 and VREFL0: about 10 µF.
Also, connect capacitors as stabilization capacitance.
Connect the VCL pin to a VSS pin by a 4.7 µF capacitor. Connect the VREFH0 pin to a VREFL0 pin by 1 µF (-25% to +25%) capacitor when VREFADC is selected as the high potential reference voltage of the ADC16. Connect the ADREG pin to a AVSS1 pin by a 0.47 µF (-50% to +20%) capacitor. Connect the SBIAS/VREFI pin to a AVSS1 pin by a 0.22 µF (-20% to +20%) capacitor. Every capacitor must be placed close to the pin.

Table 2.2 Recommended operating conditions (1 of 2)

Parameter	Symbol	Value	Min	Typ	Max	Unit
Power supply voltages	VCC*1, *2	When USBFS is not used	1.6	-	5.5	V
		When USBFS is used USB Regulator Disable	VCC_USB	-	3.6	V
		When USBFS is used USB Regulator Enable	VCC_USB _LDO	-	5.5	V
	VSS		-	0	-	V

Table 2.2 Recommended operating conditions (2 of 2)

Parameter	Symbol	Value	Min	Typ	Max	Unit
USB power supply voltages	VCC_USB	When USBFS is not used	-	VCC	-	V
		When USBFS is used USB Regulator Disable (Input)	3.0	3.3	3.6	V
	VCC_USB_LDO	When USBFS is not used	-	VCC	-	V
		When USBFS is used USB Regulator Disable	-	VCC	-	V
		When USBFS is used USB Regulator Enable	3.8	-	5.5	V
	VSS_USB		-	0	-	V
Analog power supply voltages	AVCC0*1, *2		1.6	-	5.5	V
	AVSS0		-	0	-	V
	AVCC1*1, *2		-	AVCC0	-	V
	AVSS1		-	0	-	V
	VREFH0	When used as ADC16 Reference	1.7	-	AVCC0	V
	VREFL0		-	0	-	V
	VREFH	When used as DAC12 Reference	1.7	-	AVCC0	V
	VREFL		-	0	-	V
	VREFI	When used as SDADC24 Reference*3	0.8	-	2.4	V

Note 1. Use AVCC0, AVCC1, and VCC under the following conditions:
AVCC0, AVCC1, and VCC can be set individually within the operating range when VCC ≥ 2.2 V and AVCC0 = AVCC1 ≥ 2.2 V.
AVCC0 = AVCC1 = VCC when VCC < 2.2 V or AVCC0 = AVCC1 < 2.2 V.

Note 2. When powering on the VCC and AVCC0 and AVCC1 pins, power them on at the same time or the VCC pin first and then the AVCC0 and AVCC1 pins.

Note 3. The condition when using external input for the reference voltage of SDADC24.

2.2 DC Characteristics

2.2.1 Tj/Ta Definition

Table 2.3 DC characteristics

Conditions: Products with operating temperature (T_a) -40 to +105°C

Parameter	Symbol	Typ	Max	Unit	Test conditions
Permissible junction temperature	Tj	-	125	°C	High-speed mode Middle-speed mode Low-voltage mode Low-speed mode SubOSC-speed mode
			105*1		

Note: Make sure that Tj = T_a + θja × total power consumption (W), where total power consumption = (VCC - V_{OH}) × ΣI_{OH} + V_{OL} × ΣI_{OL} + I_{CC}max × VCC.

Note 1. The upper limit of operating temperature is 85°C or 105°C, depending on the product. For details, see section 1.3, Part Numbering. If the part number shows the operation temperature at 85°C, then the maximum value of Tj is 105°C, otherwise it is 125°C.

2.2.2 I/O V_{IH}, V_{IL}

Table 2.4 I/O V_{IH}, V_{IL}

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = VCC_USB_LDO = 1.6 to 5.5 V

Parameter		Symbol	Min	Typ	Max	Unit	Test Conditions
Schmitt trigger input voltage	IIC (except for SMBus)*1	V_{IH}	VCC × 0.7	-	5.8	V	-
		V_{IL}	-	-	VCC × 0.3		
		ΔV_T	VCC × 0.05	-	-		
	RES, NMI Other peripheral input pins excluding IIC	V_{IH}	VCC × 0.8	-	-		
		V_{IL}	-	-	VCC × 0.2		
		ΔV_T	VCC × 0.1	-	-		
Input voltage (except for Schmitt trigger input pin)	IIC (SMBus)*2	V_{IH}	2.2	-	-		VCC = 3.6 to 5.5 V
		V_{IH}	2.0	-	-		VCC =2.7 to 3.6 V
		V_{IL}	-	-	0.8		VCC = 2.7 to 5.5 V
	5 V-tolerant ports*3	V_{IH}	VCC × 0.8	-	5.8		-
		V_{IL}	-	-	VCC × 0.2		
	P002, P003, P012 to P015, P500 to P502	V_{IH}	AVCC0 × 0.8	-	-		
		V_{IL}	-	-	AVCC0 × 0.2		
	P100 to P107	V_{IH}	AVCC1 × 0.8	-	-		
		V_{IL}	-	-	AVCC1 × 0.2		
	P914, P915	V_{IH}	VCC_USB × 0.8	-	VCC_USB + 0.3		
		V_{IL}	-	-	VCC_USB × 0.2		
	EXTAL Input ports pins except for P002, P003, P012 to P015, P100 to P107, P500 to P502, P914, P915	V_{IH}	VCC × 0.8	-	-		
		V_{IL}	-	-	VCC × 0.2		

Note 1. SCL0_A, SCL0_B, SCL0_C, SDA0_A, SDA0_C, SCL1_B, SCL1_C, SDA1_B, SDA1_C (total 9 pins)
Note 2. SCL0_A, SCL0_B, SCL0_C, SDA0_A, SDA0_B, SDA0_C, SCL1_A, SCL1_B, SCL1_C, SDA1_A, SDA1_B, SDA1_C, SDA1_D (total 13 pins)
Note 3. P000, P111, P112, P205, P206, P301, P401, P407, P409 (total 9 pins)

2.2.3 I/O I_{OH}, I_{OL}

Table 2.5 I/O I_{OH}, I_{OL}
Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = VCC_USB_LDO = 1.6 to 5.5 V

Parameter			Symbol	Min	Typ	Max	Unit
Permissible output current (average value per pin)	Ports P212, P213	-	I_{OH}	-	-	-4.0	mA
			I_{OL}	-	-	4.0	mA
	Ports P407, P408, P409	Low drive*1	I_{OH}	-	-	-4.0	mA
			I_{OL}	-	-	4.0	mA
		Middle drive for IIC Fast mode and SPI*4	I_{OH}	-	-	-8.0	mA
			I_{OL}	-	-	8.0	mA
		Middle drive*2 VCC = 3.0 to 5.5 V	I_{OH}	-	-	-20.0	mA
			I_{OL}	-	-	20.0	mA
	Ports P914, P915		I_{OH}	-	-	-4.0	mA
			I_{OL}	-	-	4.0	mA
	Other output pins*3	Low drive*1	I_{OH}	-	-	-4.0	mA
			I_{OL}	-	-	4.0	mA
		Middle drive*2	I_{OH}	-	-	-8.0	mA
			I_{OL}	-	-	8.0	mA
Permissible output current (max value per pin)	Ports P212, P213	-	I_{OH}	-	-	-4.0	mA
			I_{OL}	-	-	4.0	mA
	Ports P407, P408, P409	Low drive*1	I_{OH}	-	-	-4.0	mA
			I_{OL}	-	-	4.0	mA
		Middle drive for IIC Fast mode and SPI*4	I_{OH}	-	-	-8.0	mA
			I_{OL}	-	-	8.0	mA
		Middle drive*2 VCC = 3.0 to 5.5 V	I_{OH}	-	-	-20.0	mA
			I_{OL}	-	-	20.0	mA
	Ports P914, P915		I_{OH}	-	-	-4.0	mA
			I_{OL}	-	-	4.0	mA
	Other output pins*3	Low drive*1	I_{OH}	-	-	-4.0	mA
			I_{OL}	-	-	4.0	mA
		Middle drive*2	I_{OH}	-	-	-8.0	mA
			I_{OL}	-	-	8.0	mA
Permissible output current (max value total pins)	Total of ports P002, P003, P012 to P015, P500 to P502		$\Sigma I_{OH\ (max)}$	-	-	-30	mA
			$\Sigma I_{OL\ (max)}$	-	-	30	mA
	Total of ports P100 to P107		$\Sigma I_{OH\ (max)}$	-	-	-30	mA
			$\Sigma I_{OL\ (max)}$	-	-	30	mA
	Total of ports P914, P915		ΣI_{OH}	-	-	-4.0	mA
			ΣI_{OL}	-	-	4.0	mA
	Total of all output pin*5		$\Sigma I_{OH\ (max)}$	-	-	-60	mA
			$\Sigma I_{OL\ (max)}$	-	-	60	mA

Note 1. This is the value when low driving ability is selected with the Port Drive Capability bit in the PmnPFS register.
Note 2. This is the value when middle driving ability is selected with the Port Drive Capability bit in the PmnPFS register.
Note 3. Except for Ports P200, P214, P215, which are input ports.
Note 4. This is the value when middle driving ability for IIC Fast mode and SPI is selected with the Port Drive Capability bit in PmnPFS register.
Note 5. For details on the permissible output current used with CTSU, see section 2.12, CTSU Characteristics.

Caution: To protect the reliability of the MCU, the output current values should not exceed the values in Table 2.5. The average output current indicates the average current value measured during 100 µs.

2.2.4 I/O V_{OH}, V_{OL}, and Other Characteristics

Table 2.6 I/O V_{OH}, V_{OL} (1)
Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = VCC_USB_LDO = 4.0 to 5.5 V

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Output voltage	IIC*1		V_{OL}	-	-	0.4	V	I_{OL} = 3.0 mA
			V_{OL}*2,*5	-	-	0.6		I_{OL} = 6.0 mA
	Ports P407, P408, P409	Low drive	V_{OH}	VCC - 0.8	-	-		I_{OH} = -2.0 mA
			V_{OL}	-	-	0.8		I_{OL} = 2.0 mA
		Middle drive for IIC Fast mode and SPI*5	V_{OH}	VCC - 0.8	-	-		I_{OH} = -4.0 mA
			V_{OL}	-	-	0.8		I_{OL} = 4.0 mA
		Middle drive*2,*3	V_{OH}	VCC - 1.0	-	-		I_{OH} = -20 mA
			V_{OL}	-	-	1.0		I_{OL} = 20 mA
	Ports P002, P003, P012 to P015, P500 to P502	Low drive	V_{OH}	AVCC0 - 0.8	-	-		I_{OH} = -2.0 mA
			V_{OL}	-	-	0.8		I_{OL} = 2.0 mA
		Middle drive	V_{OH}	AVCC0 - 0.8	-	-		I_{OH} = -4.0 mA
			V_{OL}	-	-	0.8		I_{OL} = 4.0 mA
	Ports P100 to P107	Low drive	V_{OH}	AVCC1 - 0.8	-	-		I_{OH} = -2.0 mA
			V_{OL}	-	-	0.8		I_{OL} = 2.0 mA
		Middle drive	V_{OH}	AVCC1 - 0.8	-	-		I_{OH} = -4.0 mA
			V_{OL}	-	-	0.8		I_{OL} = 4.0 mA
	Ports P914, P915		V_{OH}	VCC_USB - 0.8	-	-		I_{OH} = -2.0 mA
			V_{OL}	-	-	0.8		I_{OL} = 2.0 mA
	Other output pins*4	Low drive	V_{OH}	VCC - 0.8	-	-		I_{OH} = -2.0 mA
			V_{OL}	-	-	0.8		I_{OL} = 2.0 mA
		Middle drive*6	V_{OH}	VCC - 0.8	-	-		I_{OH} = -4.0 mA
			V_{OL}	-	-	0.8		I_{OL} = 4.0 mA

Note 1. SCL0_A, SCL0_B, SCL0_C, SDA0_A, SDA0_B, SDA0_C, SCL1_A, SCL1_B, SCL1_C, SDA1_A, SDA1_B, SDA1_C, SDA1_D (total 13 pins).
Note 2. This is the value when middle driving ability is selected with the Port Drive Capability bit in the PmnPFS register.
Note 3. Based on characterization data, not tested in production.
Note 4. Except for P200, P214, P215, which are input ports.
Note 5. This is the value when middle driving ability for IIC and SPI is selected with the Port Drive Capability bit in PmnPFS register for P407, P408, and P409.
Note 6. Except for P212, P213.

Table 2.7 I/O V_{OH}, V_{OL} (2)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = VCC_USB_LDO = 2.7 to 4.0 V

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Output voltage	IIC*1		V_{OL}	-	-	0.4	V	I_{OL} = 3.0 mA
			V_{OL}*2,*5	-	-	0.6		I_{OL} = 6.0 mA
	Ports P407, P408, P409	Low drive	V_{OH}	VCC - 0.5	-	-		I_{OH} = -1.0 mA
			V_{OL}	-	-	0.5		I_{OL} = 1.0 mA
		Middle drive for IIC Fast mode and SPI*5	V_{OH}	VCC - 0.5	-	-		I_{OH} = -2.0 mA
			V_{OL}	-	-	0.5		I_{OL} = 2.0 mA
		Middle drive*2,*3	V_{OH}	VCC - 1.0	-	-		I_{OH} = -20 mA VCC = 3.3 V
			V_{OL}	-	-	1.0		I_{OL} = 20 mA VCC = 3.3 V
	Ports P002, P003, P012 to P015, P500 to P502	Low drive	V_{OH}	AVCC0 - 0.5	-	-		I_{OH} = -1.0 mA
			V_{OL}	-	-	0.5		I_{OL} = 1.0 mA
		Middle drive	V_{OH}	AVCC0 - 0.5	-	-		I_{OH} = -2.0 mA
			V_{OL}	-	-	0.5		I_{OL} = 2.0 mA
	Ports P100 to P107	Low drive	V_{OH}	AVCC1 - 0.5	-	-		I_{OH} = -1.0 mA
			V_{OL}	-	-	0.5		I_{OL} = 1.0 mA
		Middle drive	V_{OH}	AVCC1 - 0.5	-	-		I_{OH} = -2.0 mA
			V_{OL}	-	-	0.5		I_{OL} = 2.0 mA
	Ports P914, P915		V_{OH}	VCC_USB - 0.5	-	-		I_{OH} = -1.0 mA
			V_{OL}	-	-	0.5		I_{OL} = 1.0 mA
	Other output pins*4	Low drive	V_{OH}	VCC - 0.5	-	-		I_{OH} = -1.0 mA
			V_{OL}	-	-	0.5		I_{OL} = 1.0 mA
		Middle drive*6	V_{OH}	VCC - 0.5	-	-		I_{OH} = -2.0 mA
			V_{OL}	-	-	0.5		I_{OL} = 2.0 mA

Note 1. SCL0_A, SCL0_B, SCL0_C, SDA0_A, SDA0_B, SDA0_C, SCL1_A, SCL1_B, SCL1_C, SDA1_A, SDA1_B, SDA1_C, SDA1_D (total 13 pins).
Note 2. This is the value when middle driving ability is selected with the Port Drive Capability bit in the PmnPFS register.
Note 3. Based on characterization data, not tested in production.
Note 4. Except for P200, P214, P215, which are input ports.
Note 5. This is the value when middle driving ability for IIC and SPI is selected with the Port Drive Capability bit in PmnPFS register for P407, P408, and P409.
Note 6. Except for P212, P213.

Table 2.8 I/O V_{OH}, V_{OL} (3)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = VCC_USB_LDO = 1.6 to 2.7 V

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Output voltage	Ports P407, P408, P409	Low drive	V_{OH}	VCC - 0.3	-	-	V	I_{OH} = -0.5 mA
			V_{OL}	-	-	0.3		I_{OL} = 0.5 mA
		Middle drive for IIC Fast mode and SPI*2	V_{OH}	VCC - 0.3	-	-		I_{OH} = -1.0 mA
			V_{OL}	-	-	0.3		I_{OL} = 1.0 mA
	Ports P002, P003, P012 to P015, P500 to P502	Low drive	V_{OH}	AVCC0 - 0.3	-	-		I_{OH} = -0.5 mA
			V_{OL}	-	-	0.3		I_{OL} = 0.5 mA
		Middle drive	V_{OH}	AVCC0 - 0.3	-	-		I_{OH} = -1.0 mA
			V_{OL}	-	-	0.3		I_{OL} = 1.0 mA
	Ports P100 to P107	Low drive	V_{OH}	AVCC0 - 0.3	-	-		I_{OH} = -0.5 mA
			V_{OL}	-	-	0.3		I_{OL} = 0.5 mA
		Middle drive	V_{OH}	AVCC0 - 0.3	-	-		I_{OH} = -1.0 mA
			V_{OL}	-	-	0.3		I_{OL} = 1.0 mA
	Ports P914, P915		V_{OH}	VCC_USB - 0.3	-	-		I_{OH} = -0.5 mA
			V_{OL}	-	-	0.3		I_{OL} = 0.5 mA
	Other output pins*1	Low drive	V_{OH}	VCC - 0.3	-	-		I_{OH} = -0.5 mA
			V_{OL}	-	-	0.3		I_{OL} = 0.5 mA
		Middle drive*3	V_{OH}	VCC - 0.3	-	-		I_{OH} = -1.0 mA
			V_{OL}	-	-	0.3		I_{OL} = 1.0 mA

Note 1. Except for ports P200, P214, P215, which are input ports.

Note 2. This is the value when middle driving ability for IIC and SPI is selected with the Port Drive Capability bit in the PmnPFS register for P407, P408, and P409.

Note 3. Except for P212, P213.

Table 2.9 I/O other characteristics

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = VCC_USB_LDO = 1.6 to 5.5 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	RES, ports P200, P214, P215	$\lvert I_{in} \rvert$	-	-	1.0	µA	V_{in} = 0 V V_{in} = VCC
Three-state leakage current (off state)	5 V-tolerant ports	$\lvert I_{TSI} \rvert$	-	-	1.0	µA	V_{in} = 0 V V_{in} = 5.8 V
	Other ports		-	-	1.0		V_{in} = 0 V V_{in} = VCC
Input pull-up resistor	All ports (except for P200, P214, P215, P914, P915)	R_U	10	20	50	kΩ	V_{in} = 0 V
Input capacitance	P012 to P015, P200, P502, P914, P915	C_{in}	-	-	30	pF	V_{in} = 0 V f = 1 MHz T_a = 25°C
	Other input pins		-	-	15		

2.2.5 Output Characteristics for I/O Pins (Low Drive Capacity)

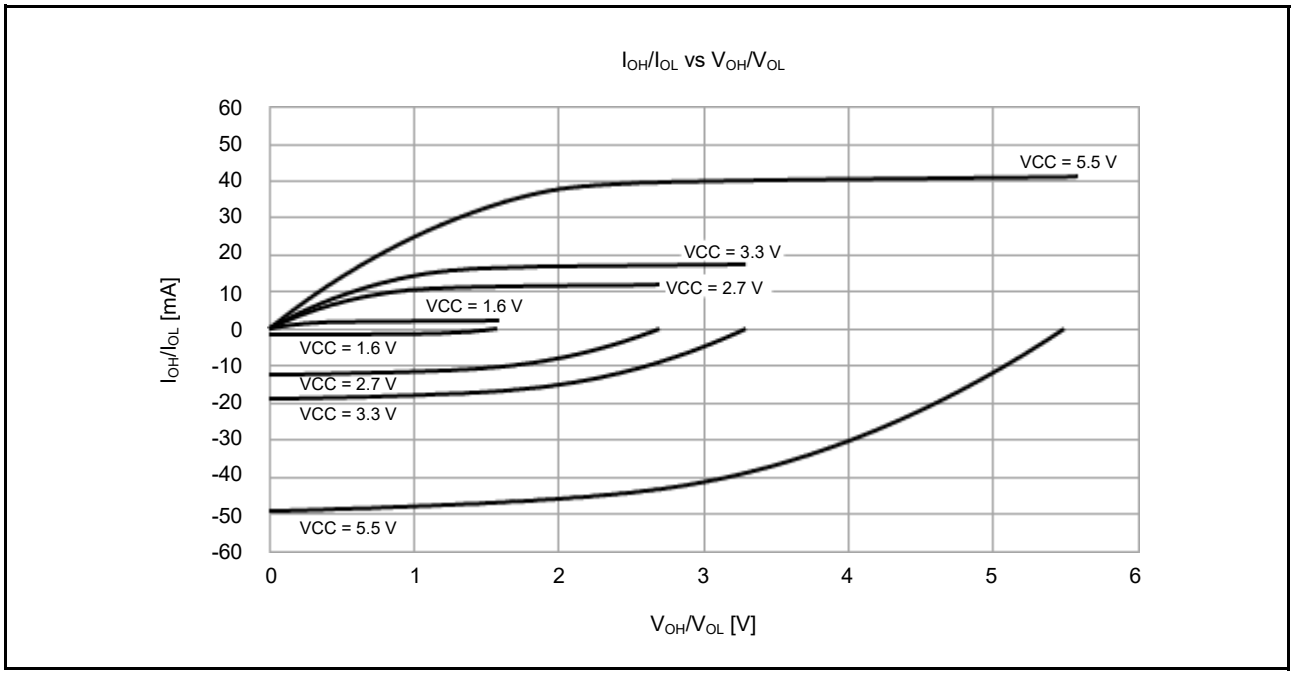


Figure 2.2 **V_{OH}/V_{OL} and I_{OH}/I_{OL} voltage characteristics at Ta = 25°C when low drive output is selected (reference data, except for P914 and P915)**

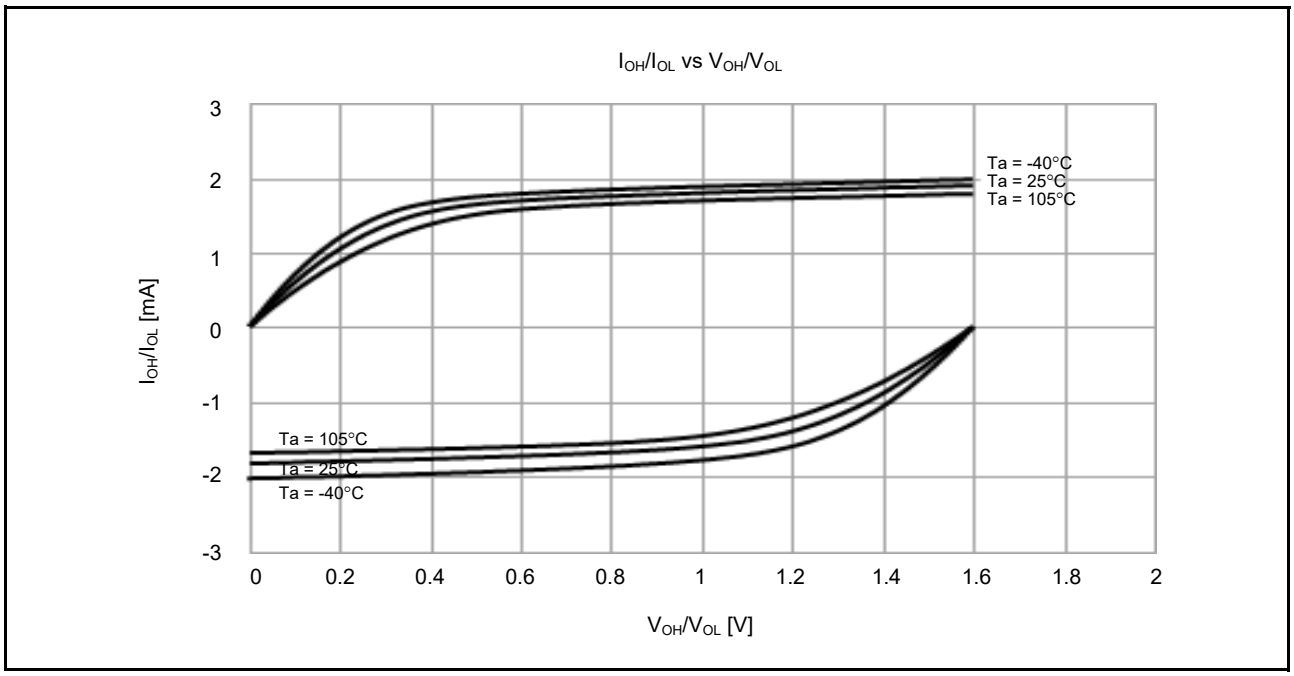


Figure 2.3 **V_{OH}/V_{OL} and I_{OH}/I_{OL} temperature characteristics at VCC = 1.6 V when low drive output is selected (reference data, except for P914 and P915)**

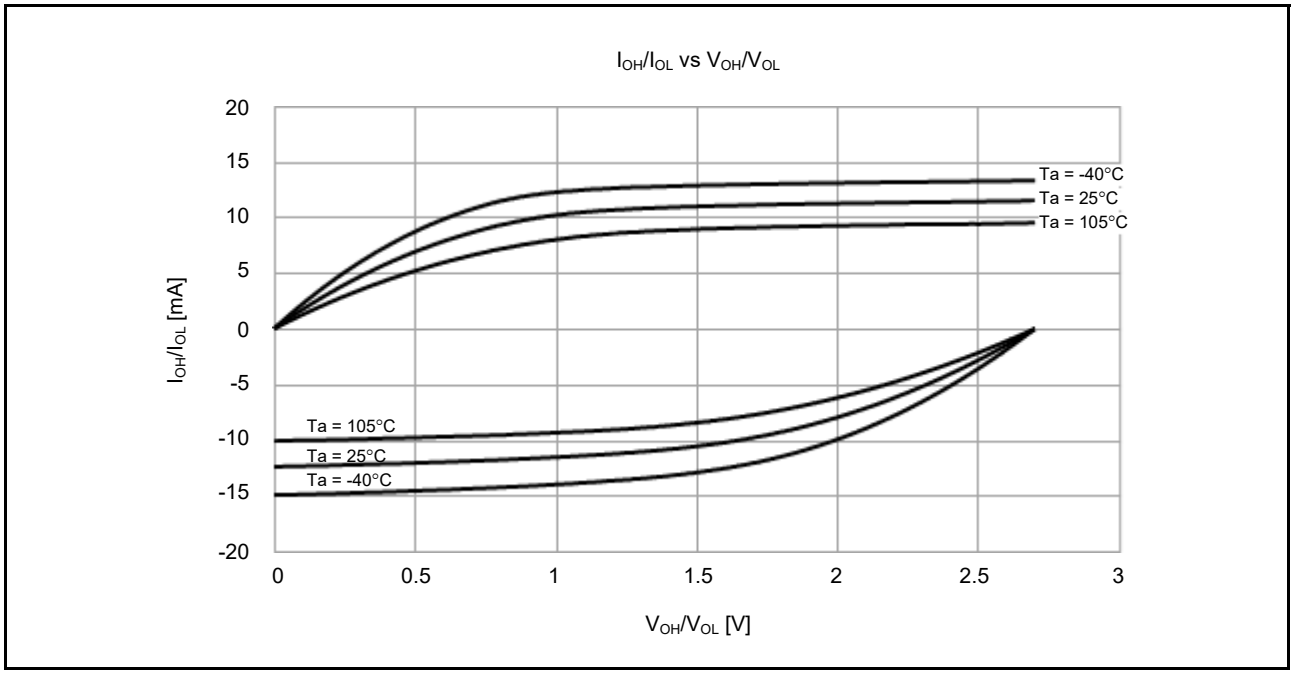


Figure 2.4 **V_{OH}/V_{OL} and I_{OH}/I_{OL} temperature characteristics at VCC = 2.7 V when low drive output is selected (reference data, except for P914 and P915)**

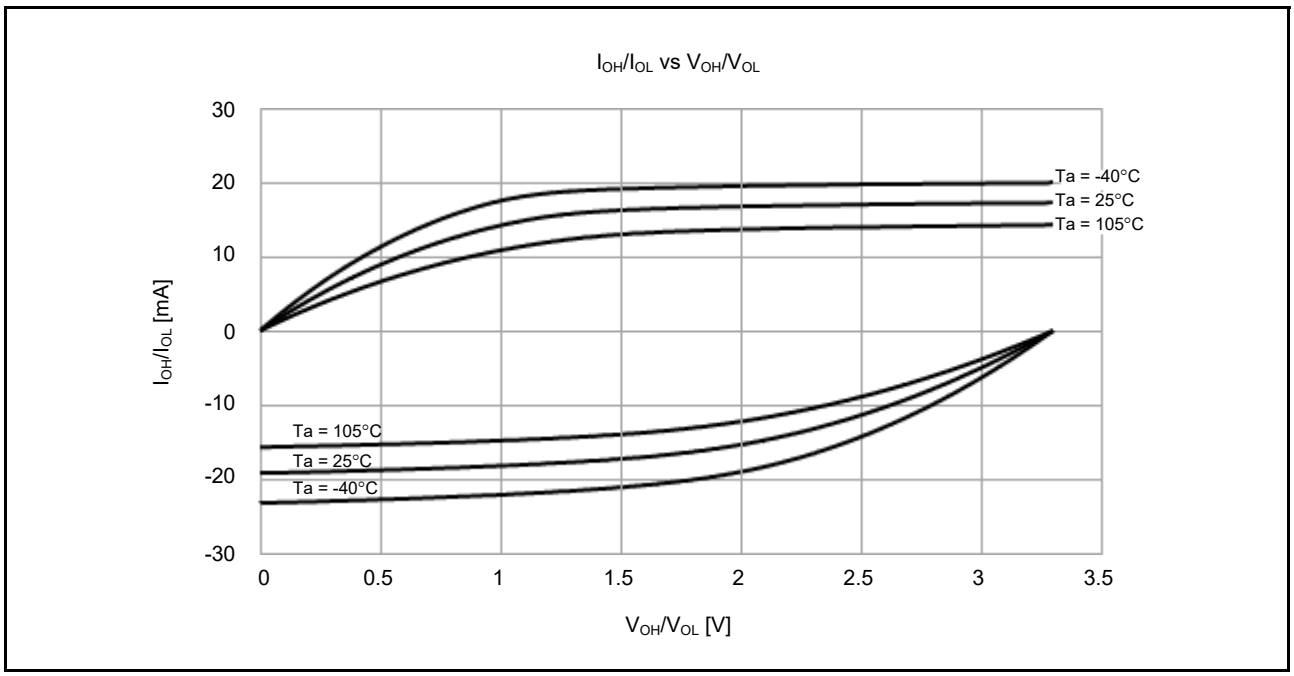


Figure 2.5 **V_{OH}/V_{OL} and I_{OH}/I_{OL} temperature characteristics at VCC = 3.3 V when low drive output is selected (reference data, except for P914 and P915)**

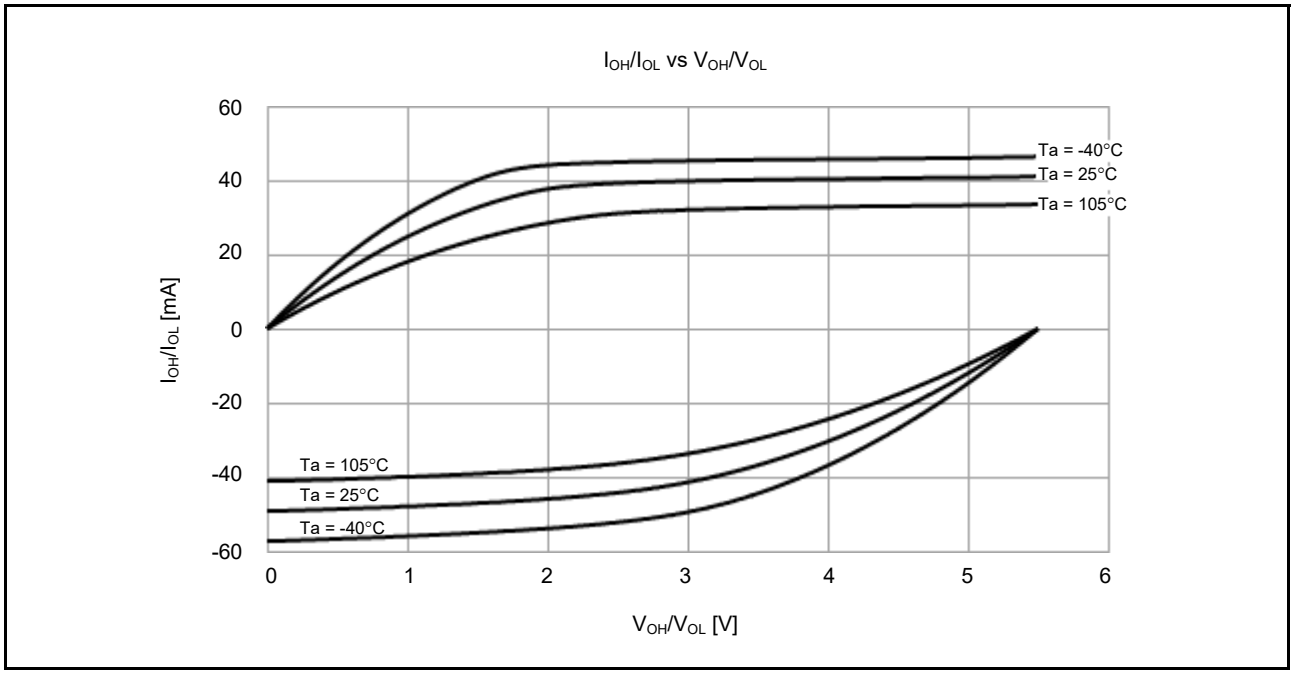


Figure 2.6 **V_{OH}/V_{OL} and I_{OH}/I_{OL} temperature characteristics at VCC = 5.5 V when low drive output is selected (reference data, except for P914 and P915)**

2.2.6 Output Characteristics for I/O Pins (Middle Drive Capacity)

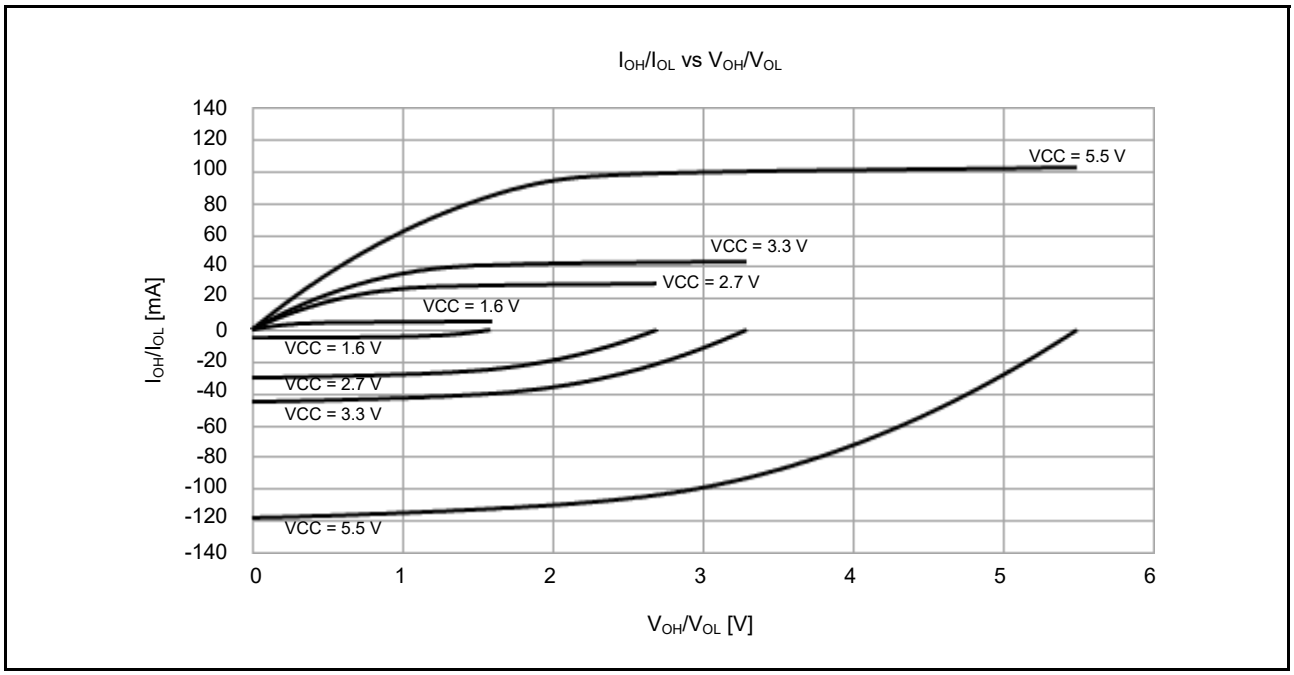


Figure 2.7 **V_{OH}/V_{OL} and I_{OH}/I_{OL} voltage characteristics at Ta = 25°C when middle drive output is selected (reference data, except for P914 and P915)**

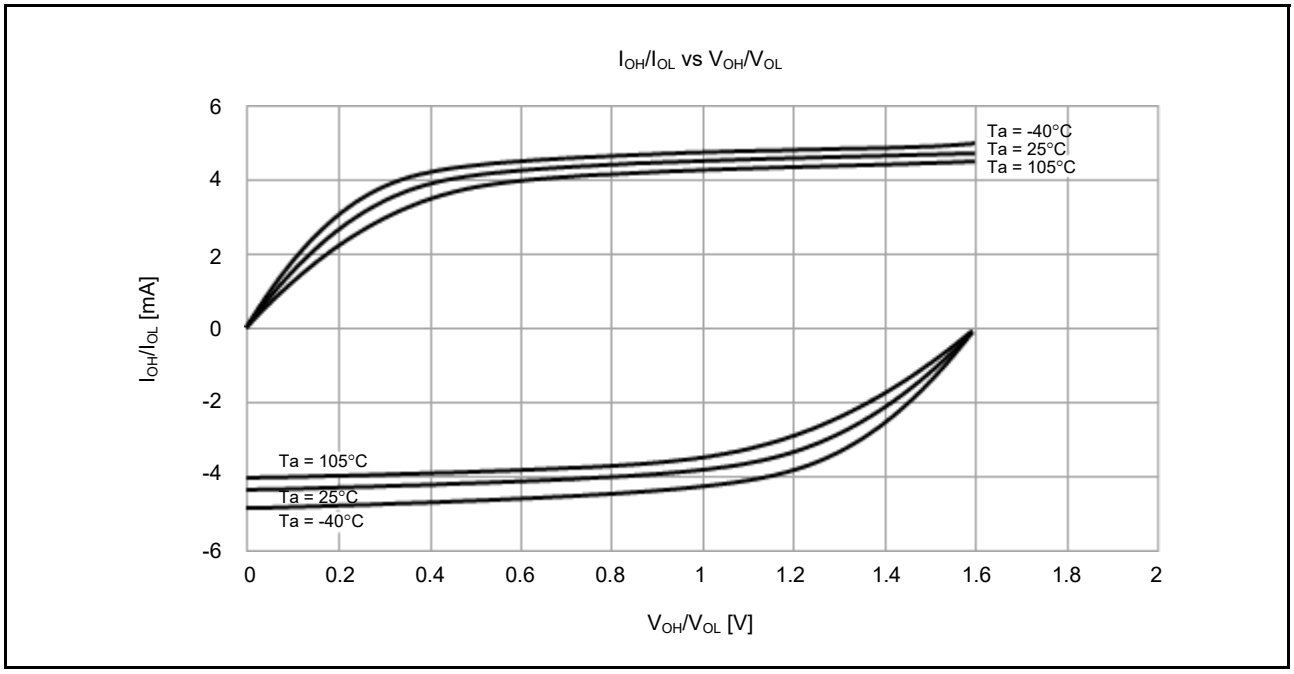


Figure 2.8 **V_{OH}/V_{OL} and I_{OH}/I_{OL} temperature characteristics at VCC = 1.6 V when middle drive output is selected (reference data, except for P914 and P915)**

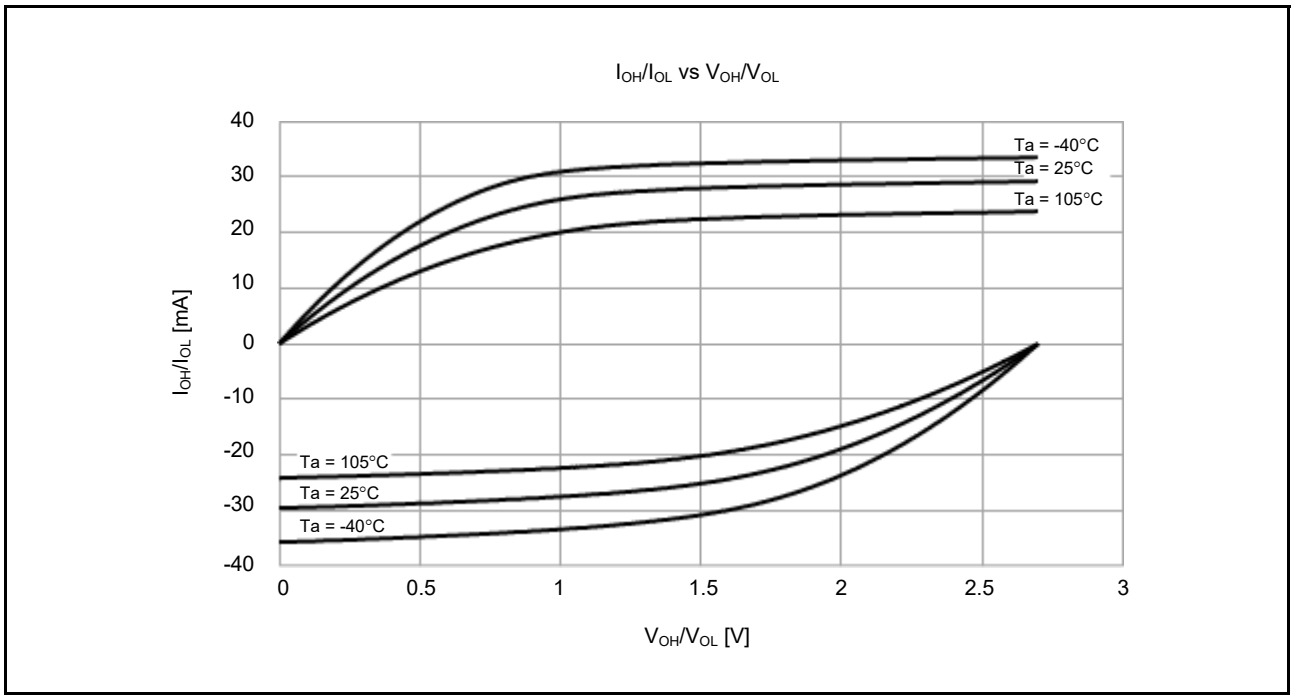


Figure 2.9 **V_{OH}/V_{OL} and I_{OH}/I_{OL} temperature characteristics at VCC = 2.7 V when middle drive output is selected (reference data, except for P914 and P915)**

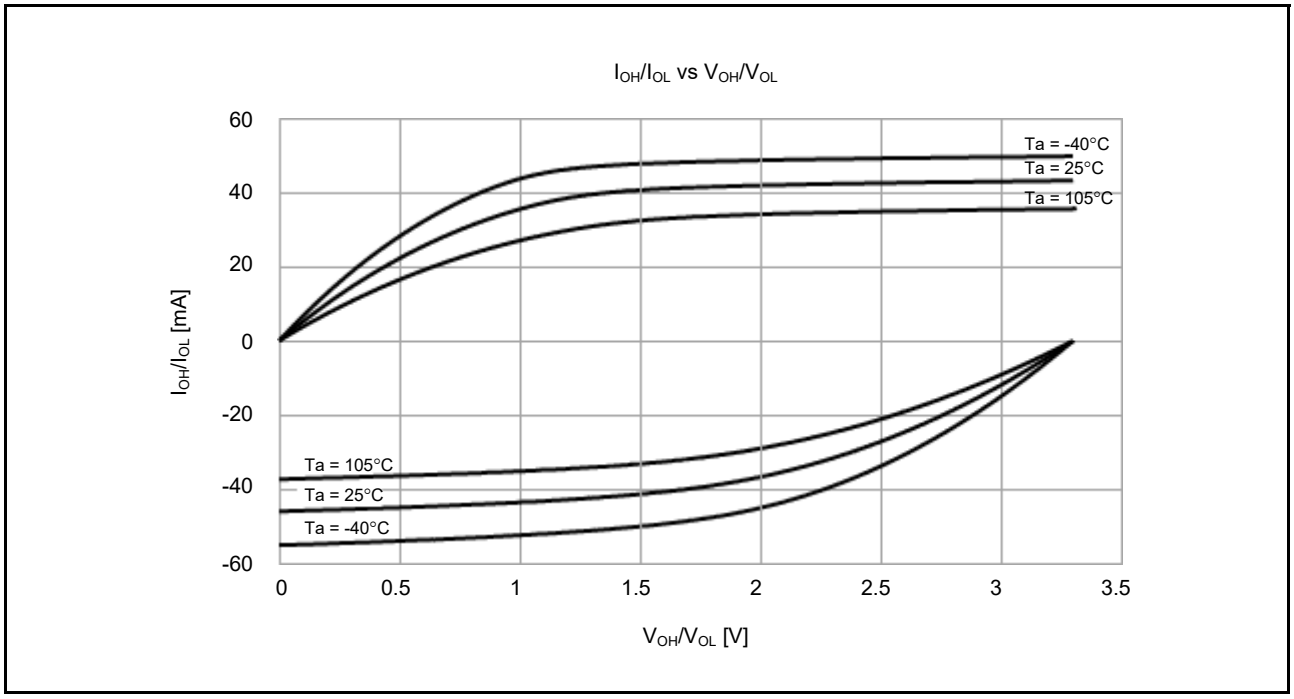


Figure 2.10 **V_{OH}/V_{OL} and I_{OH}/I_{OL} temperature characteristics at VCC = 3.3 V when middle drive output is selected (reference data, except for P914 and P915)**

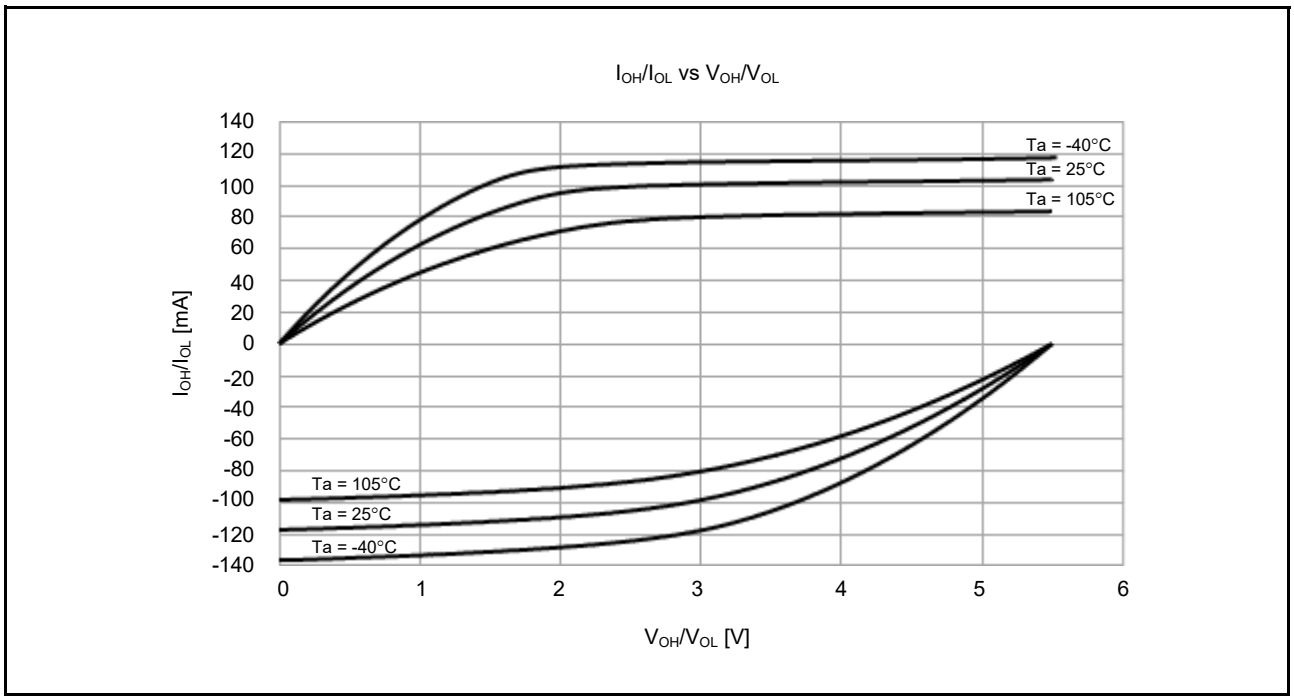


Figure 2.11 **V_{OH}/V_{OL} and I_{OH}/I_{OL} temperature characteristics at VCC = 5.5 V when middle drive output is selected (reference data, except for P914 and P915)**

2.2.7 Output Characteristics for P407, P408 and P409 I/O Pins (Middle Drive Capacity)

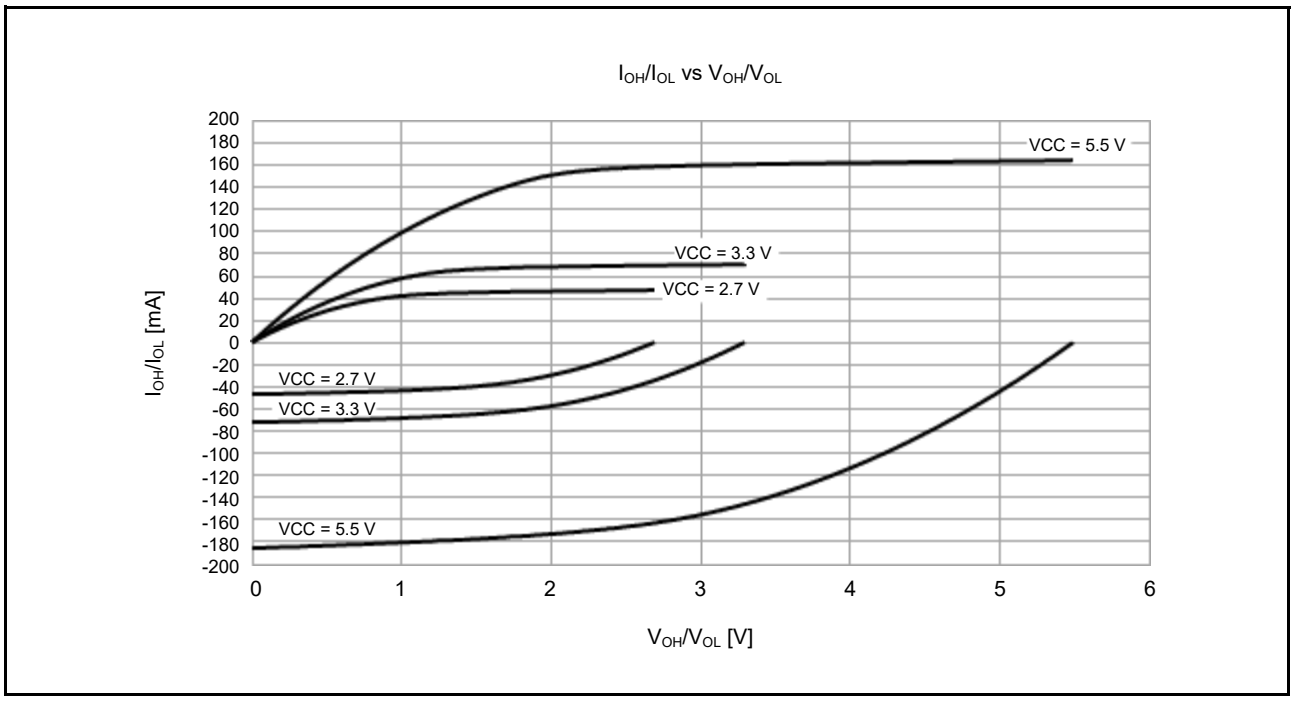


Figure 2.12 **V_{OH}/V_{OL} and I_{OH}/I_{OL} voltage characteristics at Ta = 25°C when middle drive output is selected (reference data)**

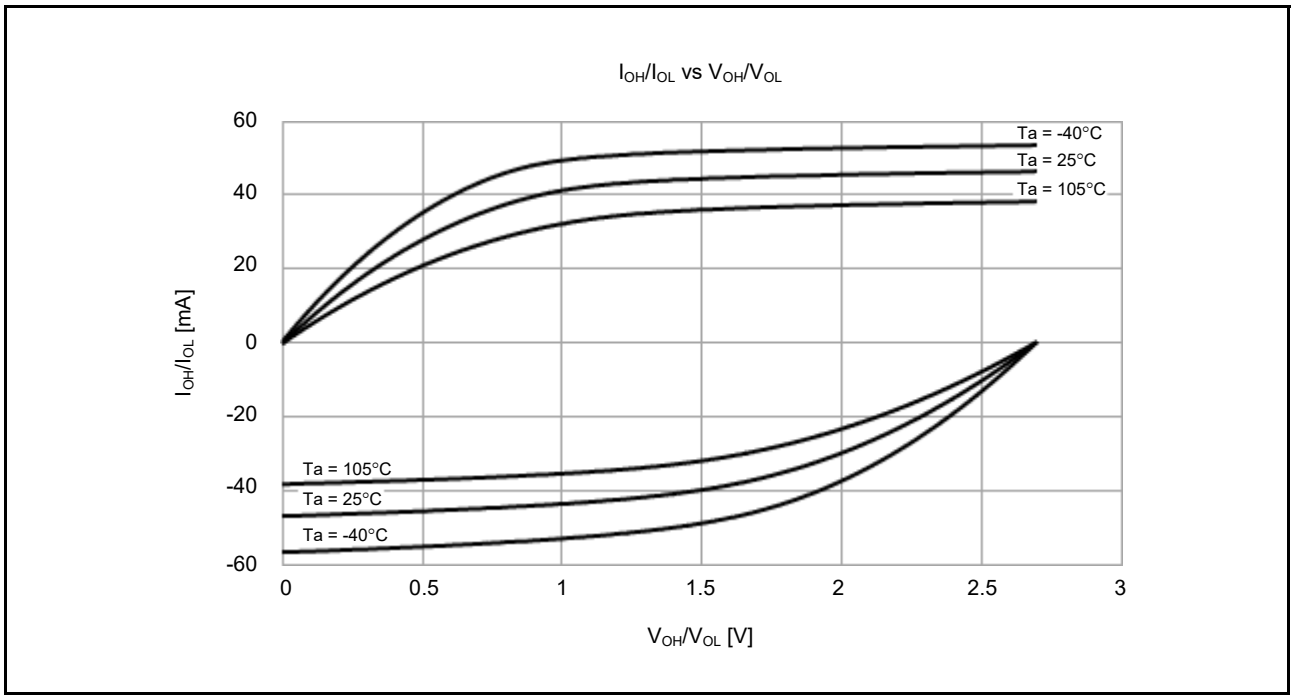


Figure 2.13 **V_{OH}/V_{OL} and I_{OH}/I_{OL} temperature characteristics at VCC = 2.7 V when middle drive output is selected (reference data)**

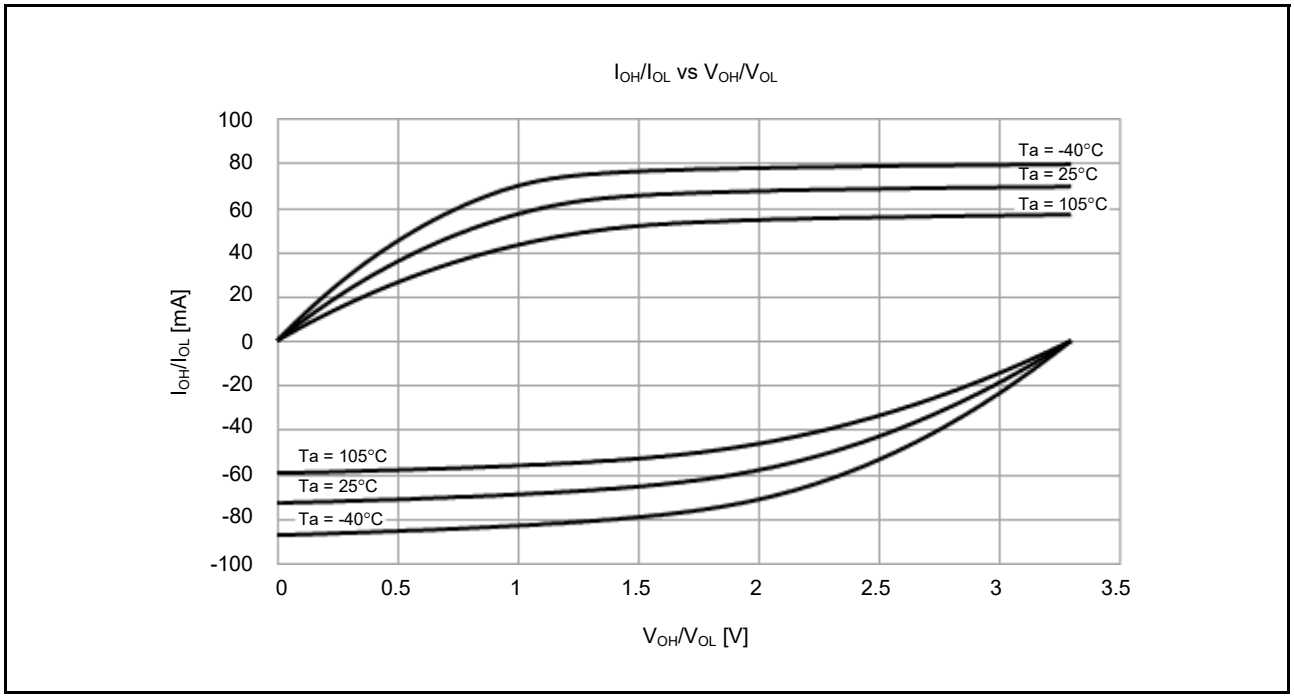


Figure 2.14 **V_{OH}/V_{OL} and I_{OH}/I_{OL} temperature characteristics at VCC = 3.3 V when middle drive output is selected (reference data)**

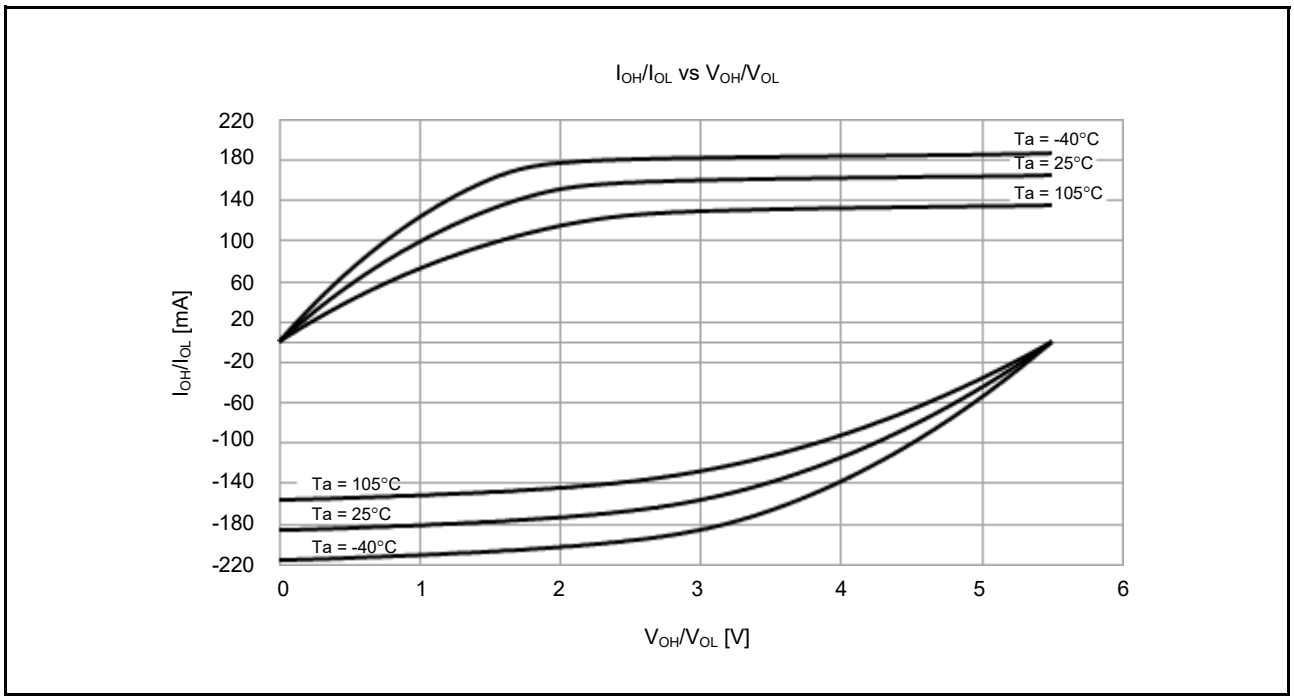


Figure 2.15 **V_{OH}/V_{OL} and I_{OH}/I_{OL} temperature characteristics at VCC = 5.5 V when middle drive output is selected (reference data)**

2.2.8 Output Characteristics for IIC I/O Pins

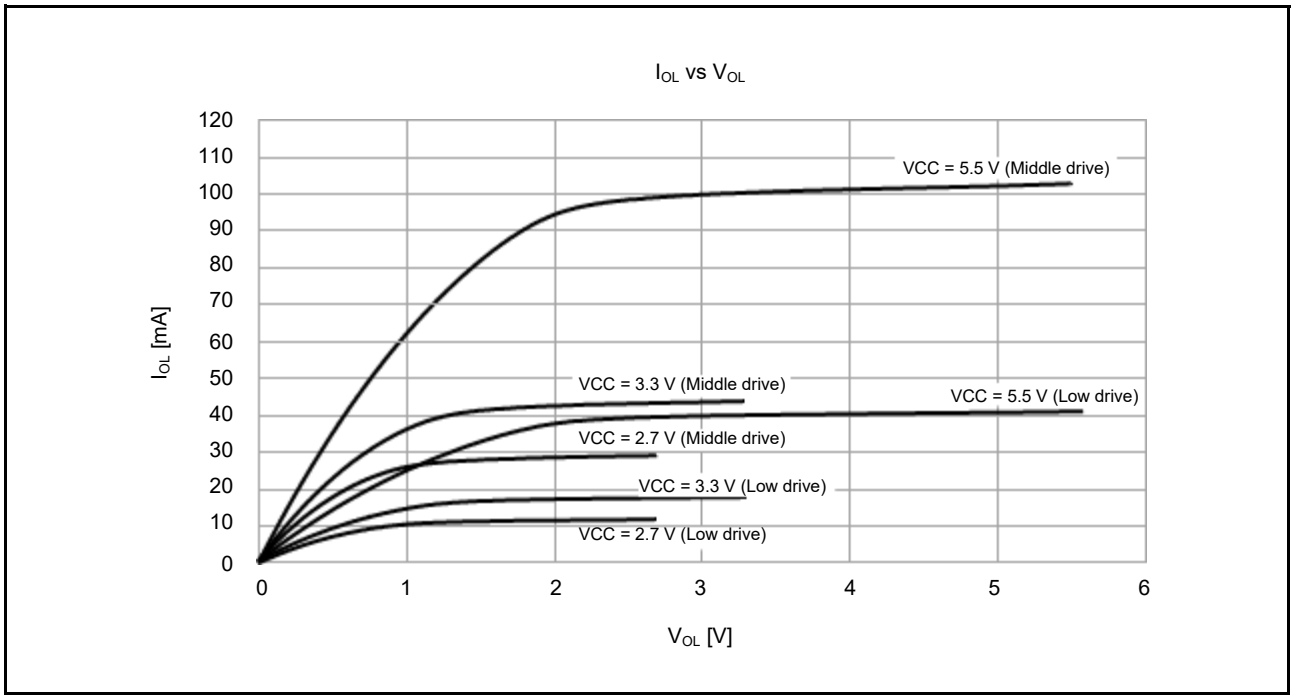


Figure 2.16 V_{OH}/V_{OL} and I_{OH}/I_{OL} voltage characteristics at Ta = 25°C

2.2.9 Operating and Standby Current

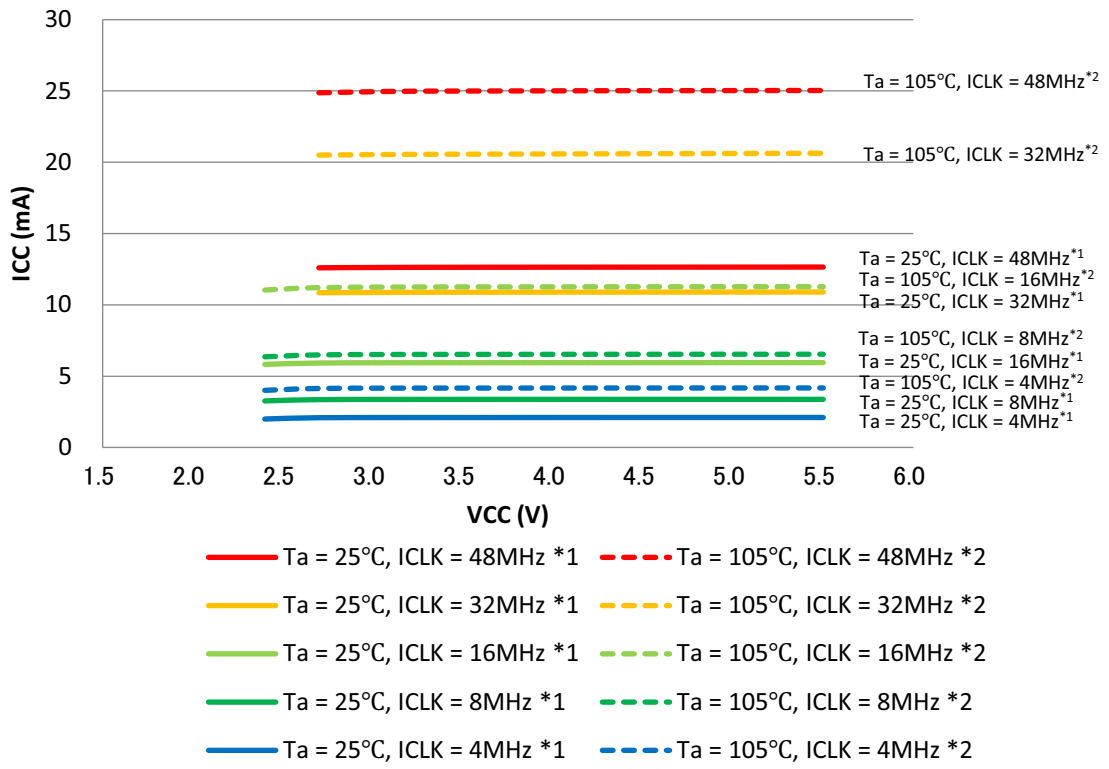
Table 2.10 Operating and standby current (1) (1 of 2)
Conditions: VCC = AVCC0 = AVCC1 = 1.6 to 5.5 V

Parameter					Symbol	Typ*10	Max	Unit	Test Conditions
Supply current*1	High-speed mode*2	Normal mode	All peripheral clocks disabled, while (1) code executing from flash*5	ICLK = 48 MHz	I_{CC}	5.2	-	mA	*7, *11
				ICLK = 32 MHz		3.8	-		
				ICLK = 16 MHz		2.3	-		
				ICLK = 8 MHz		1.6	-		
			All peripheral clocks disabled, CoreMark code executing from flash*5	ICLK = 48 MHz		12.1	-		
				ICLK = 32 MHz		8.3	-		
				ICLK = 16 MHz		4.6	-		
				ICLK = 8 MHz		2.8	-		
			All peripheral clocks enabled, while (1) code executing from flash*5	ICLK = 48 MHz		12.6	-		*9, *11
				ICLK = 32 MHz		10.9	-		*8, *11
				ICLK = 16 MHz		5.9	-		
				ICLK = 8 MHz		3.4	-		
			All peripheral clocks enabled, code executing from flash*5	ICLK = 48 MHz		-	28.5		*9, *11
		Sleep mode	All peripheral clocks disabled*5	ICLK = 48 MHz		2.7	-		*7
				ICLK = 32 MHz		2.1	-		
				ICLK = 16 MHz		1.5	-		
				ICLK = 8 MHz		1.1	-		
			All peripheral clocks enabled*5	ICLK = 48 MHz		9.8	-		*9
				ICLK = 32 MHz		8.9	-		*8
				ICLK = 16 MHz		5.0	-		
				ICLK = 8 MHz		2.9	-		
		Increase during BGO operation*6				2.5	-		-
	Middle-speed mode*2	Normal mode	All peripheral clocks disabled, while (1) code executing from flash*5	ICLK = 12 MHz	I_{CC}	1.6	-	mA	*7, *11
				ICLK = 8 MHz		1.3	-		
			All peripheral clocks disabled, CoreMark code executing from flash*5	ICLK = 12 MHz		3.4	-		
				ICLK = 8 MHz		2.6	-		
			All peripheral clocks enabled, while (1) code executing from flash*5	ICLK = 12 MHz		4.3	-		*8, *11
				ICLK = 8 MHz		3.1	-		
			All peripheral clocks enabled, code executing from flash*5	ICLK = 12 MHz		-	12.6		
		Sleep mode	All peripheral clocks disabled*5	ICLK = 12 MHz		1.0	-		*7
				ICLK = 8 MHz		0.9	-		
			All peripheral clocks enabled*5	ICLK = 12 MHz		3.6	-		*8
				ICLK = 8 MHz		2.7	-		
		Increase during BGO operation*6				2.5	-		-

Table 2.10 Operating and standby current (1) (2 of 2)
Conditions: VCC = AVCC0 = AVCC1 = 1.6 to 5.5 V

Parameter					Symbol	Typ*10	Max	Unit	Test Conditions
Supply current*1	Low-speed mode*3	Normal mode	All peripheral clocks disabled, while (1) code executing from flash*5	ICLK = 1 MHz	I_{CC}	0.3	-	mA	*7, *11
			All peripheral clocks disabled, CoreMark code executing from flash*5	ICLK = 1 MHz		0.4	-		
			All peripheral clocks enabled, while (1) code executing from flash*5	ICLK = 1 MHz		0.5	-		*8, *11
			All peripheral clocks enabled, code executing from flash*5	ICLK = 1 MHz		-	2.5		
		Sleep mode	All peripheral clocks disabled*5	ICLK = 1 MHz		0.2	-		*7
			All peripheral clocks enabled*5	ICLK = 1 MHz		0.4	-		*8
	Low-voltage mode*3	Normal mode	All peripheral clocks disabled, while (1) code executing from flash*5	ICLK = 4 MHz	I_{CC}	1.5	-	mA	*7, *11
			All peripheral clocks disabled, CoreMark code executing from flash*5	ICLK = 4 MHz		2.2	-		
			All peripheral clocks enabled, while (1) code executing from flash*5	ICLK = 4 MHz		2.5	-		*8, *11
			All peripheral clocks enabled, code executing from flash*5	ICLK = 4 MHz		-	7.0		
		Sleep mode	All peripheral clocks disabled*5	ICLK = 4 MHz		1.3	-		*7
			All peripheral clocks enabled*5	ICLK = 4 MHz		2.3	-		*8
	Subosc-speed mode*4	Normal mode	All peripheral clocks disabled, while (1) code executing from flash*5	ICLK = 32.768 kHz	I_{CC}	6.5	-	µA	*8, *11
			All peripheral clocks enabled, while (1) code executing from flash*5	ICLK = 32.768 kHz		12.1	-		
			All peripheral clocks enabled, code executing from flash*5	ICLK = 32.768 kHz		-	190.0		
		Sleep mode	All peripheral clocks disabled*5	ICLK = 32.768 kHz		4.5	-		*8
			All peripheral clocks enabled*5	ICLK = 32.768 kHz		10.2	-		*8

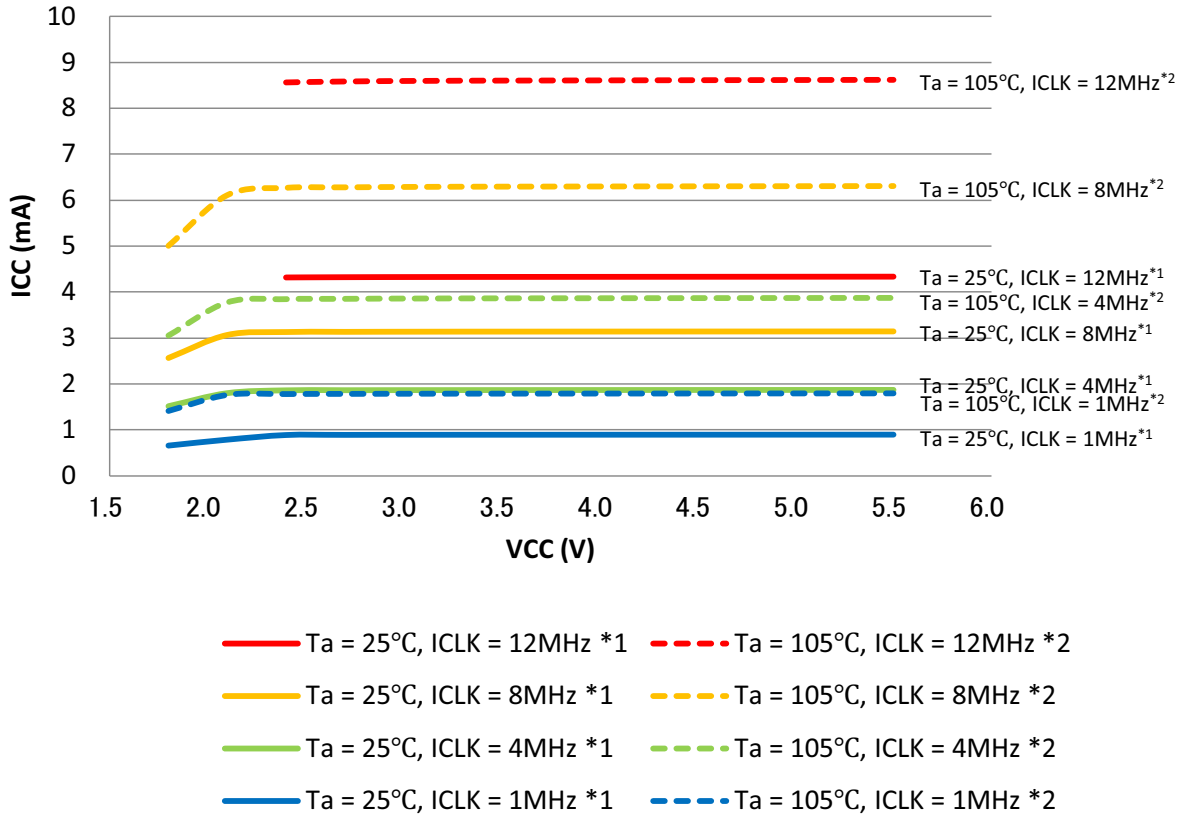
Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.
Note 2. The clock source is HOCO.
Note 3. The clock source is MOCO.
Note 4. The clock source is the sub-clock oscillator.
Note 5. This does not include BGO operation.
Note 6. This is the increase for programming or erasure of the flash memory for data storage during program execution.
Note 7. FCLK, PCLKB, and PCLKD are set to divided by 64.
Note 8. FCLK, PCLKB, and PCLKD are the same frequency as that of ICLK.
Note 9. FCLK and PCLKB are set to be divided by 2 and PCLKD is the same frequency as that of ICLK.
Note 10. VCC = 3.3 V.
Note 11. The flash cache is operating.



Note 1. All peripheral operations except any BGO operation are operating normally. This is the average of the actual measurements of the sample cores during product evaluation.

Note 2. All peripheral operations except any BGO operation are operating at maximum. This is the average of the actual measurements for the upper limit samples during product evaluation.

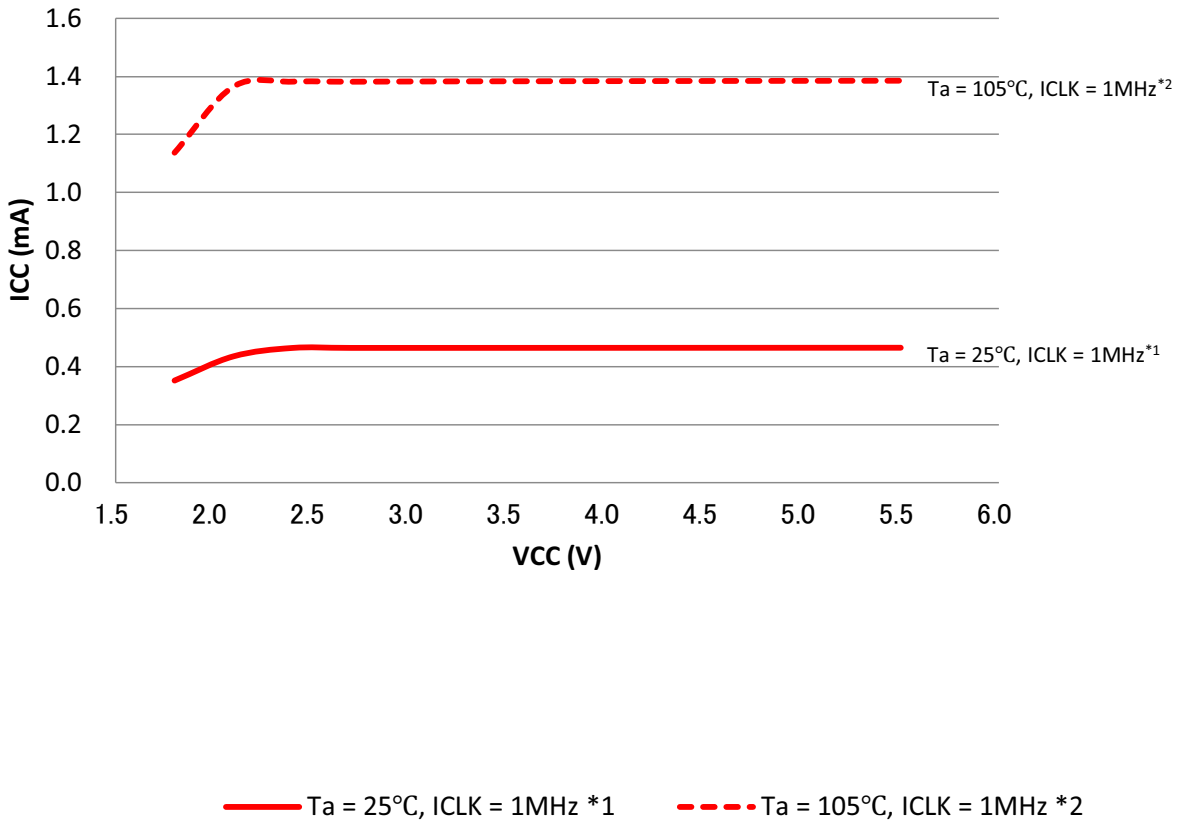
Figure 2.17 Voltage dependency in high-speed operating mode (reference data)



Note 1. All peripheral operations except any BGO operation are operating normally. This is the average of the actual measurements of the sample cores during product evaluation.

Note 2. All peripheral operations except any BGO operation are operating at maximum. This is the average of the actual measurements for the upper limit samples during product evaluation.

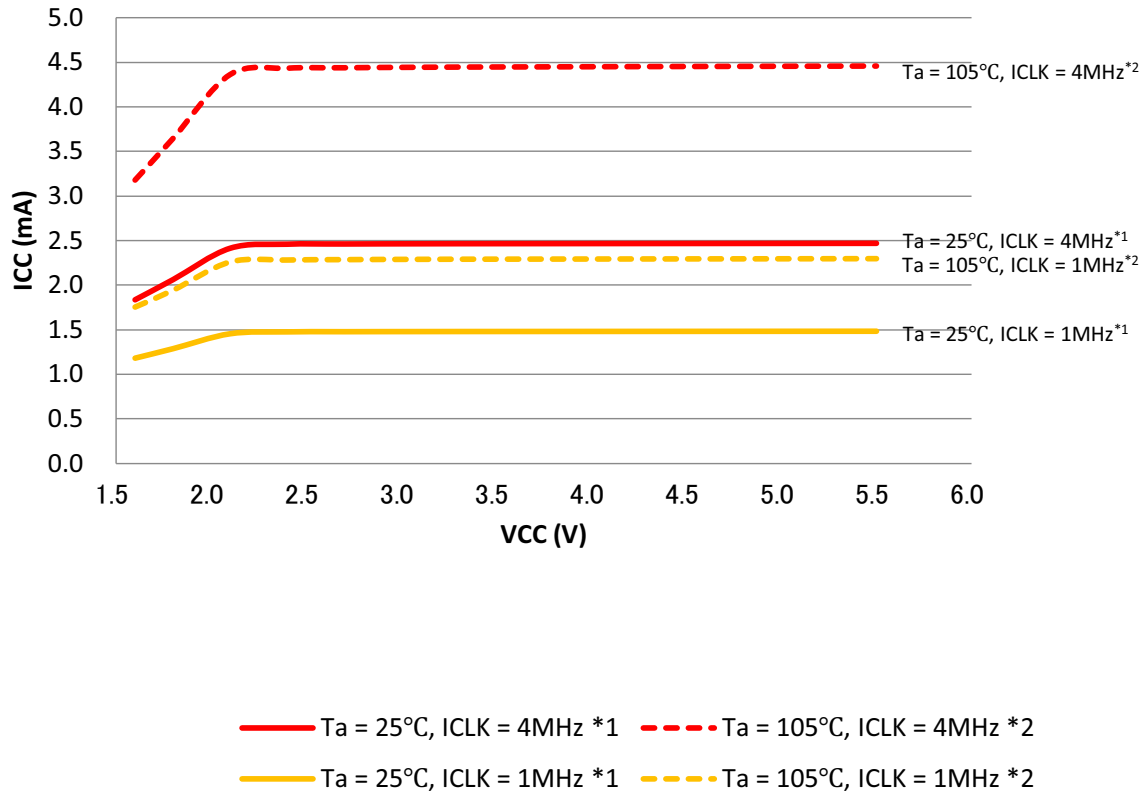
Figure 2.18 Voltage dependency in middle-speed operating mode (reference data)



Note 1. All peripheral operations except any BGO operation are operating normally. This is the average of the actual measurements of the sample cores during product evaluation.

Note 2. All peripheral operations except any BGO operation are operating at maximum. This is the average of the actual measurements for the upper limit samples during product evaluation.

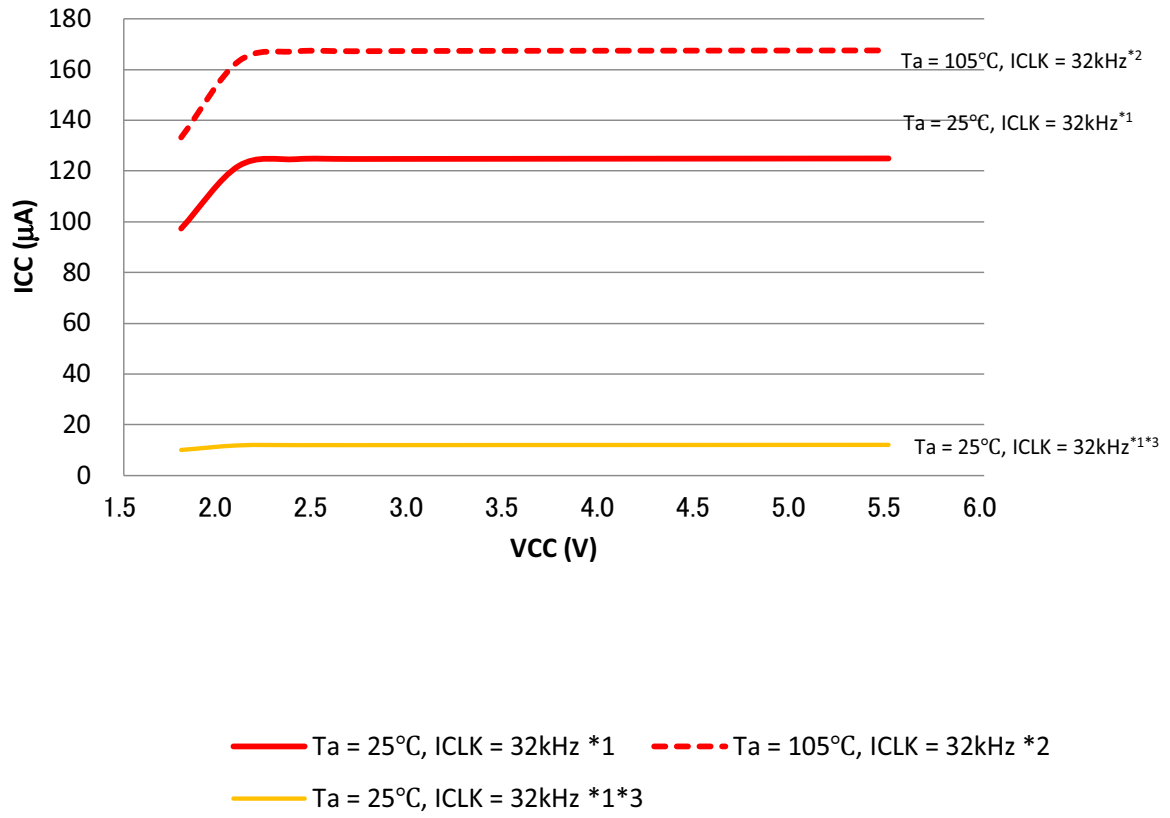
Figure 2.19 Voltage dependency in low-speed operating mode (reference data)



Note 1. All peripheral operations except any BGO operation are operating normally. This is the average of the actual measurements of the sample cores during product evaluation.

Note 2. All peripheral operations except any BGO operation are operating at maximum. This is the average of the actual measurements for the upper limit samples during product evaluation.

Figure 2.20 Voltage dependency in low-voltage operating mode (reference data)



Note 1. All peripheral operations except any BGO operation are operating normally. This is the average of the actual measurements of the sample cores during product evaluation.
Note 2. All peripheral operations except any BGO operation are operating at maximum. This is the average of the actual measurements for the upper limit samples during product evaluation.
Note 3. MOCO and DAC are stopped.

Figure 2.21 Voltage dependency in subosc-speed operating mode (reference data)

Table 2.11 Operating and standby current (2)
Conditions: VCC = AVCC0 = AVCC1 = 1.6 to 5.5 V

Parameter			Symbol	Typ*3	Max	Unit	Test conditions
Supply current*1	Software Standby mode*2	T_a = 25°C	I_{CC}	0.5	2.0	µA	-
		T_a = 55°C		0.8	7.0		
		T_a = 85°C		1.8	17.0		
		T_a = 105°C		4.4	45.0		
	Increment for RTC operation with low-speed on-chip oscillator*4			0.4	-		-
	Increment for RTC operation with sub-clock oscillator*4			0.5	-		SOMCR.SODRV[1:0] are 11b (Low power mode 3)
				1.3	-		SOMCR.SODRV[1:0] are 00b (normal mode)

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOS transistors are in the off state.
Note 2. The IWDT and LVD are not operating.
Note 3. VCC = 3.3 V.
Note 4. Includes the low-speed on-chip oscillator or sub-oscillation circuit current.

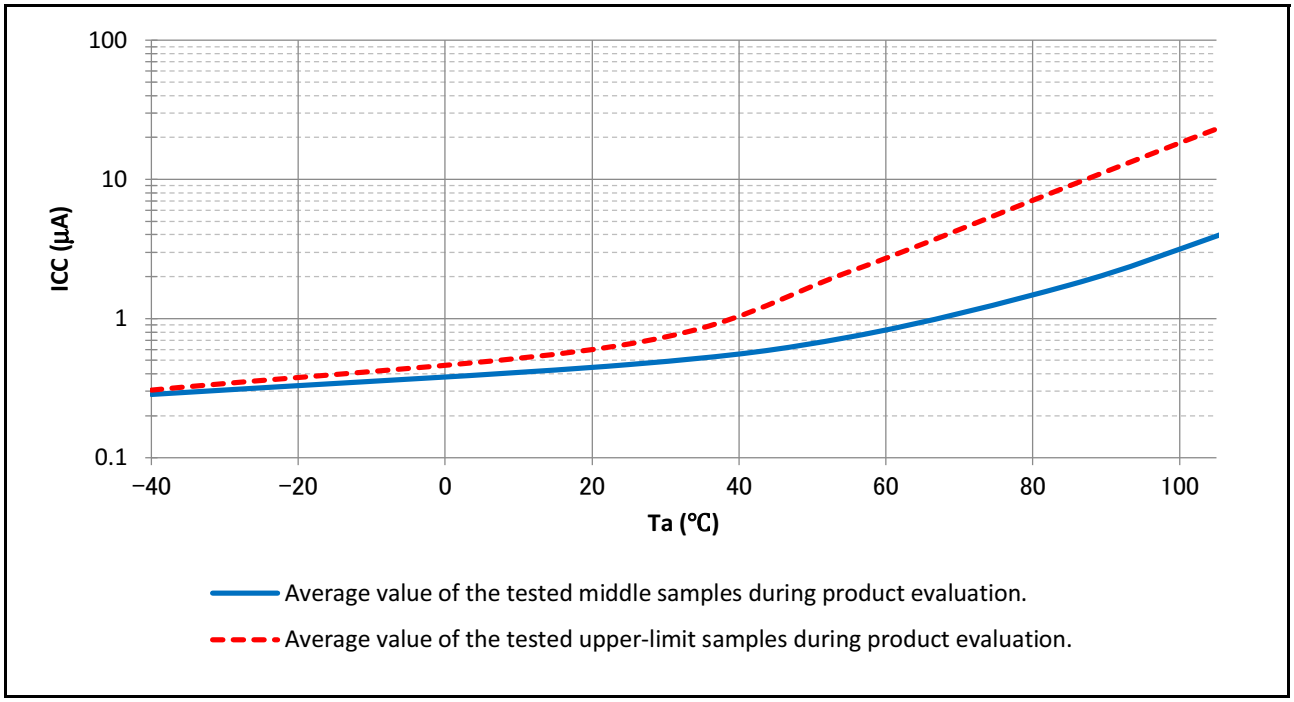
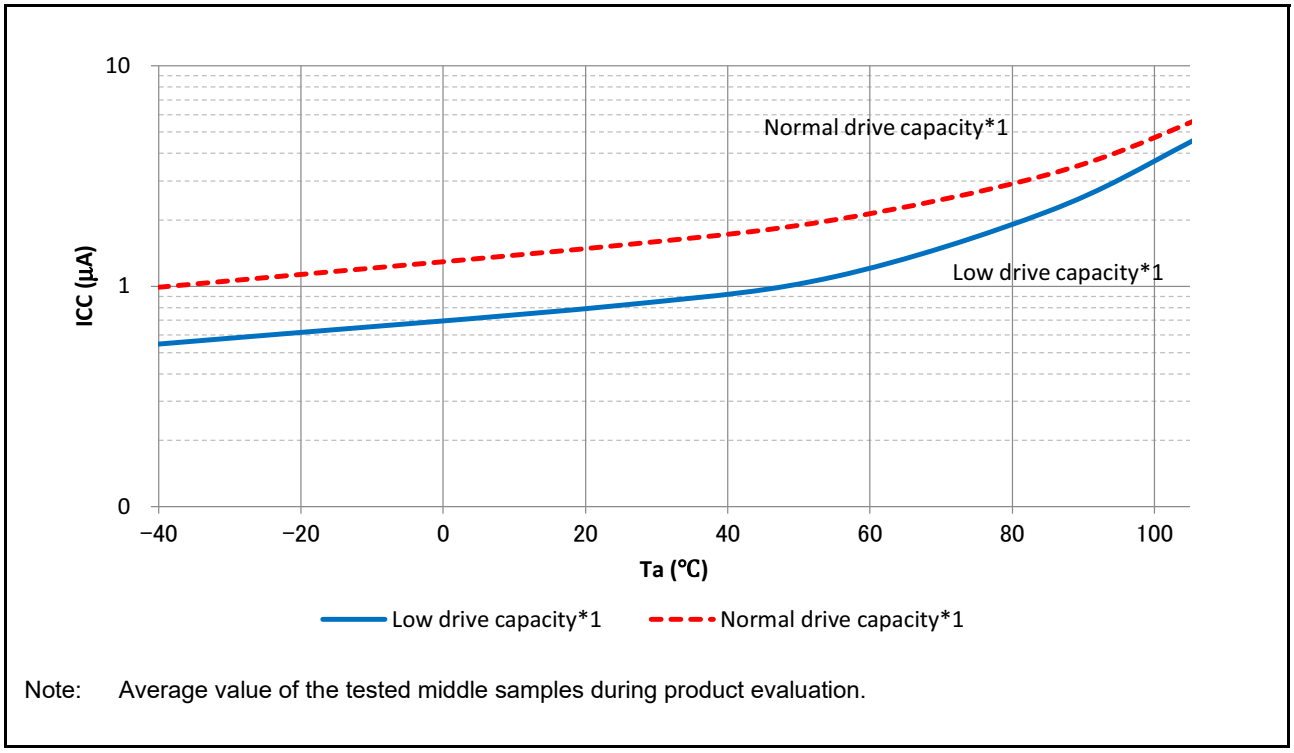


Figure 2.22 Temperature dependency in Software Standby mode (reference data)



Note: Average value of the tested middle samples during product evaluation.

Figure 2.23 Temperature dependency of RTC operation (reference data)

Table 2.12 Operating and standby current (3)
Conditions: VCC = AVCC0 = AVCC1 = 1.6 to 5.5 V

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Analog power supply current	During 16-bit A/D conversion		I_{AVCC0}	-	-	1.5	mA	-
	During 8-bit D/A conversion (per channel) *1			-	-	1.6	mA	-
	During 12-bit D/A conversion (per channel) *1			-	-	0.9	mA	-
	Waiting for 16-bit A/D, 8-bit D/A and 12-bit D/A conversion (all units) *5			-	-	2.0	µA	-
	During 24-bit sigma-delta A/D conversion (at normal mode)		I_{AVCC1}	-	-	1.29	mA	-
	During 24-bit sigma-delta A/D conversion (at low-power conversion)			-	-	1.06	mA	G_{SET1} = 8, or G_{TOTAL} = 24,32
				-	-	0.9	mA	G_{SET1}, G_{TOTAL} = the others
	Waiting for 24-bit sigma-delta A/D conversion*6			-	-	1.0	µA	-
Reference power supply current	During 16-bit A/D conversion		I_{REFH0}	-	-	80	µA	-
	Waiting for 16-bit A/D conversion			-	-	60	nA	-
	During 12-bit D/A conversion		I_{REFH}	-	-	650	µA	-
	Waiting for 12-bit D/A conversion			-	-	100	nA	-
	During 24-bit sigma-delta A/D conversion		I_{REFI}	-	-	30	µA	External VREF mode
Temperature Sensor (TSN) operating current			I_{TNS}	-	75	-	µA	-
Low-power Analog Comparator (ACMPLP) operating current	Window comparator (high-speed mode)		I_{CMPLP}	-	15	-	µA	-
	Comparator (high-speed mode)			-	10	-	µA	-
	Comparator (low-speed mode)			-	2	-	µA	-
High-speed analog comparator (ACMPHS) operating current			I_{CPMHS}	-	70	100	µA	AVCC0 ≥ 2.7 V
Operational Amplifier (OPAMP) operating current	Low power mode	1 unit operating	I_{AMP}	-	10	16	µA	-
		2 unit operating		-	19	30	µA	-
		3 unit operating		-	28	44	µA	-
	Middle speed mode	1 unit operating		-	280	360	µA	-
		2 unit operating		-	530	690	µA	-
		3 unit operating		-	770	1020	µA	-
	High speed mode	1 unit operating		-	0.74	0.91	mA	-
		2 unit operating		-	1.41	1.74	mA	-
		3 unit operating		-	2.07	2.57	mA	-
Internal reference voltage for ADC16 operating current			$I_{VREFADC}$	-	65	130	µA	-
USBFS operating current	During USB communication under the following settings and conditions: • Function controller is in Full-Speed mode and - Bulk OUT transfer is (64 bytes) × 1 - Bulk IN transfer is (64 bytes) × 1 • Host device is connected by a 1-meter USB cable from the USB port.		I_{USBF}*2	-	3.6 (VCC) 1.1 (VCC_USB)*4	-	mA	-
	During suspended state under the following setting and conditions: • Function controller is in Full-Speed mode (the USB_DP pin is pulled up) • Software Standby mode • Host device is connected through a 1-meter USB cable from the USB port.		I_{SUSP}*3	-	0.35 (VCC) 170 (VCC_USB)*4	-	µA	-

Note 1. The reference power supply current is included in the power supply current value for D/A conversion.
Note 2. Current is consumed only by the USBFS.
Note 3. Includes the current supplied from the pull-up resistor of the USB_DP pin to the pull-down resistor of the host device, in addition to the current consumed by the MCU in the suspended state.
Note 4. When VCC = VCC_USB = 3.3 V.
Note 5. When the MCU is in Software Standby mode or the MSTPCRD.MSTPD16 (ADC160 module-stop bit) is in the module-stop

state.

Note 6. When the MCU is in the MSTPCRD.MSTPD17 (SDADC24 module-stop bit) is in the module-stop state.

2.2.10 VCC Rise and Fall Gradient and Ripple Frequency

Table 2.13 Rise and fall gradient characteristics

Conditions: VCC = AVCC0 = AVCC1 = 0 to 5.5 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Power-on VCC rising gradient	Voltage monitor 0 reset disabled at startup	SrVCC	0.02	-	2	ms/V	-
	Voltage monitor 0 reset enabled at startup*1, *2				-		
	SCI/USB boot mode*2				2		

Note 1. When OFS1.LVDAS = 0.

Note 2. At boot mode, the reset from voltage monitor 0 is disabled regardless of the value of OFS1.LVDAS bit.

Table 2.14 Rising and falling gradient and ripple frequency characteristics

Conditions: VCC = AVCC0 = AVCC1 = 1.6 to 5.5 V

The ripple voltage must meet the allowable ripple frequency $f_{r(VCC)}$ within the range between the VCC upper limit (5.5 V) and lower limit (1.6 V).

When the VCC change exceeds VCC ± 10%, the allowable voltage change rising and falling gradient dt/dVCC must be met.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Allowable ripple frequency	$f_{r(VCC)}$	-	-	10	kHz	Figure 2.24 $V_{r\ (VCC)} \leq VCC \times 0.2$
		-	-	1	MHz	Figure 2.24 $V_{r\ (VCC)} \leq VCC \times 0.08$
		-	-	10	MHz	Figure 2.24 $V_{r\ (VCC)} \leq VCC \times 0.06$
Allowable voltage change rising and falling gradient	dt/dVCC	1.0	-	-	ms/V	When VCC change exceeds VCC ± 10%

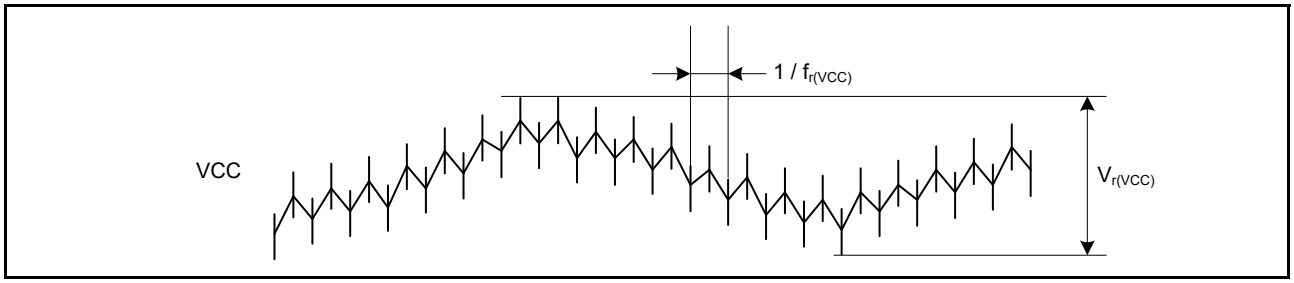


Figure 2.24 Ripple waveform

2.3 AC Characteristics

2.3.1 Frequency

Table 2.15 Operation frequency in high-speed operating mode
Conditions: VCC = AVCC0 = AVCC1 = 2.4 to 5.5 V

Parameter			Symbol	Min	Typ	Max*7	Unit
Operation frequency	System clock (ICLK)*6	2.7 to 5.5 V	f	0.032768	-	48	MHz
		2.4 to 2.7 V		0.032768	-	16	
	FlashIF clock (FCLK)*1,*2,*6	2.7 to 5.5 V		0.032768	-	32	
		2.4 to 2.7 V		0.032768	-	16	
	Peripheral module clock (PCLKB)*5,*6	2.7 to 5.5 V		-	-	32	
		2.4 to 2.7 V		-	-	16	
	Peripheral module clock (PCLKD)*3,*6	2.7 to 5.5 V		-	-	64*4	
		2.4 to 2.7 V		-	-	16	

Note 1. The lower-limit frequency of FCLK is 1 MHz while programming or erasing the flash memory. When using FCLK for programming or erasing the flash memory at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note 2. The frequency accuracy of FCLK must be ± 3.5% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.
Note 3. The lower-limit frequency of PCLKD is 1 MHz when the ADC16 is in use.
Note 4. The upper-limit frequency of PCLKD is 32 MHz when the ADC16 is in use.
Note 5. The lower-limit frequency of PCLKB is 1 MHz when the SDADC24 is in use.
Note 6. See section 9, Clock Generation Circuit in User's Manual for the relationship of frequencies between ICLK, PCLKB, PCLKD, and FCLK.
Note 7. The maximum value of operation frequency does not include internal oscillator errors. For details on the range for guaranteed operation, see Table 2.20, Clock timing.

Table 2.16 Operation frequency in middle-speed mode
Conditions: VCC = AVCC0 = AVCC1 = 1.8 to 5.5 V

Parameter			Symbol	Min	Typ	Max*6	Unit
Operation frequency	System clock (ICLK)*5	2.7 to 5.5 V	f	0.032768	-	12	MHz
		2.4 to 2.7 V		0.032768	-	12	
		1.8 to 2.4 V		0.032768	-	8	
	FlashIF clock (FCLK)*1,*2,*5	2.7 to 5.5 V		0.032768	-	12	
		2.4 to 2.7 V		0.032768	-	12	
		1.8 to 2.4 V		0.032768	-	8	
	Peripheral module clock (PCLKB)*4,*5	2.7 to 5.5 V		-	-	12	
		2.4 to 2.7 V		-	-	12	
		1.8 to 2.4 V		-	-	8	
	Peripheral module clock (PCLKD)*3,*5	2.7 to 5.5 V		-	-	12	
		2.4 to 2.7 V		-	-	12	
		1.8 to 2.4 V		-	-	8	

Note 1. The lower-limit frequency of FCLK is 1 MHz while programming or erasing the flash memory. When using FCLK for programming or erasing the flash memory at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note 2. The frequency accuracy of FCLK must be ± 3.5% while programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.
Note 3. The lower-limit frequency of PCLKD is 1 MHz when the ADC16 is in use.
Note 4. The lower-limit frequency of PCLKB is 1 MHz when the SDADC24 is in use.
Note 5. See section 9, Clock Generation Circuit in User's Manual for the relationship of frequencies between ICLK,

PCLKB, PCLKD, and FCLK.

Note 6. The maximum value of operation frequency does not include internal oscillator errors. For details on the range for guaranteed operation, see Table 2.20, Clock timing.

Table 2.17 Operation frequency in low-speed mode

Conditions: VCC = AVCC0 = AVCC1 = 1.8 to 5.5 V

Parameter			Symbol	Min	Typ	Max*6	Unit
Operation frequency	System clock (ICLK)*5	1.8 to 5.5 V	f	0.032768	-	1	MHz
	FlashIF clock (FCLK) *1,*2,*5	1.8 to 5.5 V		0.032768	-	1	
	Peripheral module clock (PCLKB)*4,*5	1.8 to 5.5 V		-	-	1	
	Peripheral module clock (PCLKD)*3,*5	1.8 to 5.5 V		-	-	1	

Note 1. The lower-limit frequency of FCLK is 1 MHz while programming or erasing the flash memory.
Note 2. The frequency accuracy of FCLK must be ± 3.5% while programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.
Note 3. The lower-limit frequency of PCLKD is 1 MHz when the ADC16 is in use.
Note 4. The lower-limit frequency of PCLKB is 1 MHz when the SDADC24 is in use.
Note 5. See section 9, Clock Generation Circuit in User's Manual for the relationship of frequencies between ICLK, PCLKB, PCLKD, and FCLK.
Note 6. The maximum value of operation frequency does not include internal oscillator errors. For details on the range for guaranteed operation, see Table 2.20, Clock timing.

Table 2.18 Operation frequency in low-voltage mode

Conditions: VCC = AVCC0 = AVCC1 = 1.6 to 5.5 V

Parameter			Symbol	Min	Typ	Max*6	Unit
Operation frequency	System clock (ICLK)*5	1.6 to 5.5 V	f	0.032768	-	4	MHz
	FlashIF clock (FCLK)*1,*2,*5	1.6 to 5.5 V		0.032768	-	4	
	Peripheral module clock (PCLKB)*4,*5	1.6 to 5.5 V		-	-	4	
	Peripheral module clock (PCLKD)*3,*5	1.6 to 5.5 V		-	-	4	

Note 1. The lower-limit frequency of FCLK is 1 MHz while programming or erasing the flash memory. When using FCLK for programming or erasing the flash memory at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note 2. The frequency accuracy of FCLK must be ± 3.5% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.
Note 3. The lower-limit frequency of PCLKD is 1 MHz when the ADC16 is in use.
Note 4. The lower-limit frequency of PCLKB is 1 MHz when the SDADC24 is in use.
Note 5. See section 9, Clock Generation Circuit in User's Manual for the relationship of frequencies between ICLK, PCLKB, PCLKD, and FCLK.
Note 6. The maximum value of operation frequency does not include internal oscillator errors. For details on the range for guaranteed operation, see Table 2.20, Clock timing.

Table 2.19 Operation frequency in Subosc-speed mode

Conditions: VCC = AVCC0 = AVCC1 = 1.8 to 5.5 V

Parameter			Symbol	Min	Typ	Max	Unit
Operation frequency	System clock (ICLK)*4	1.8 to 5.5 V	f	27.8528	32.768	37.6832	kHz
	FlashIF clock (FCLK)*1,*4	1.8 to 5.5 V		27.8528	32.768	37.6832	
	Peripheral module clock (PCLKB)*3,*4	1.8 to 5.5 V		-	-	37.6832	
	Peripheral module clock (PCLKD)*2,*4	1.8 to 5.5 V		-	-	37.6832	

Note 1. Programming and erasing the flash memory is not possible.
Note 2. The ADC16 cannot be used.
Note 3. The SDADC24 cannot be used.
Note 4. See section 9, Clock Generation Circuit in User's Manual for the relationship of frequencies between ICLK, PCLKB, PCLKD, and FCLK.

2.3.2 Clock Timing

Table 2.20 Clock timing (1 of 2)

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
EXTAL external clock input cycle time		t_{Xcyc}	50	-	-	ns	Figure 2.25
EXTAL external clock input high pulse width		t_{XH}	20	-	-	ns	
EXTAL external clock input low pulse width		t_{XL}	20	-	-	ns	
EXTAL external clock rising time		t_{Xr}	-	-	5	ns	
EXTAL external clock falling time		t_{Xf}	-	-	5	ns	
EXTAL external clock input wait time*1		t_{EXWT}	0.3	-	-	μs	-
EXTAL external clock input frequency		f_{EXTAL}	-	-	20	MHz	2.4 ≤ VCC ≤ 5.5
			-	-	8		1.8 ≤ VCC < 2.4
			-	-	1		1.6 ≤ VCC < 1.8
Main clock oscillator oscillation frequency		f_{MAIN}	1	-	20	MHz	2.4 ≤ VCC ≤ 5.5
			1	-	8		1.8 ≤ VCC < 2.4
			1	-	4		1.6 ≤ VCC < 1.8
LOCO clock oscillation frequency		f_{LOCO}	27.8528	32.768	37.6832	kHz	-
LOCO clock oscillation stabilization time		t_{LOCO}	-	-	100	μs	Figure 2.26
IWDT-dedicated clock oscillation frequency		f_{ILOCO}	12.75	15	17.25	kHz	-
MOCO clock oscillation frequency		f_{MOCO}	6.8	8	9.2	MHz	-
MOCO clock oscillation stabilization time		t_{MOCO}	-	-	1	μs	-
HOCO clock oscillation frequency		f_{HOCO24}	23.64	24	24.36	MHz	Ta = -40 to -20°C 1.8 ≤ VCC ≤ 5.5
			22.68	24	25.32		Ta = -40 to 85°C 1.6 ≤ VCC < 1.8
			23.76	24	24.24		Ta = -20 to 85°C 1.8 ≤ VCC ≤ 5.5
			23.52	24	24.48		Ta = 85 to 105°C 2.4 ≤ VCC ≤ 5.5
		f_{HOCO32}	31.52	32	32.48		Ta = -40 to -20°C 1.8 ≤ VCC ≤ 5.5
			30.24	32	33.76		Ta = -40 to 85°C 1.6 ≤ VCC < 1.8
			31.68	32	32.32		Ta = -20 to 85°C 1.8 ≤ VCC ≤ 5.5
			31.36	32	32.64		Ta = 85 to 105°C 2.4 ≤ VCC ≤ 5.5
		f_{HOCO48}*3	47.28	48	48.72		Ta = -40 to -20°C 1.8 ≤ VCC ≤ 5.5
			47.52	48	48.48		Ta = -20 to 85°C 1.8 ≤ VCC ≤ 5.5
			47.04	48	48.96		Ta = 85 to 105°C 2.4 ≤ VCC ≤ 5.5
		f_{HOCO64}*4	63.04	64	64.96		Ta = -40 to -20°C 2.4 ≤ VCC ≤ 5.5
			63.36	64	64.64		Ta = -20 to 85°C 2.4 ≤ VCC ≤ 5.5
			62.72	64	65.28		Ta = 85 to 105°C 2.4 ≤ VCC ≤ 5.5
HOCO clock oscillation stabilization time*5, *6	Except low-voltage mode	t_{HOCO24} t_{HOCO32}	-	-	37.1	μs	Figure 2.27
		t_{HOCO48}	-	-	43.3		
		t_{HOCO64}	-	-	80.6		
	Low-voltage mode	t_{HOCO24} t_{HOCO32} t_{HOCO48} t_{HOCO64}	-	-	100.9		
Sub-clock oscillator oscillation frequency		f_{SUB}	-	32.768	-	kHz	-

Table 2.20 Clock timing (2 of 2)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Sub-clock oscillation stabilization time*2	t_{SUBOSC}	-	0.5	-	s	Figure 2.28

Note 1. Time until the clock can be used after the Main Clock Oscillator stop bit (MOSCCR.MOSTP) is set to 0 (operating) when the external clock is stable.
Note 2. After changing the setting of the SOSCCR.SOSTP bit to start sub-clock oscillator operation, only start using the sub-clock oscillator after the sub-clock oscillation stabilization wait time elapsed. Use the oscillator wait time value recommended by the oscillator manufacturer.
Note 3. The 48-MHz HOCO can be used within a VCC range of 1.8 V to 5.5 V.
Note 4. The 64-MHz HOCO can be used within a VCC range of 2.4 V to 5.5 V.
Note 5. This is a characteristic when the HOCOCR.HCSTP bit is cleared to 0 (oscillation) in the MOCO stop state.
When the HOCOCR.HCSTP bit is set to 0 (oscillation) during MOCO oscillation, this specification is shortened by 1 µs.
Note 6. Check OSCSF.HOCOSF to confirm whether stabilization time has elapsed.

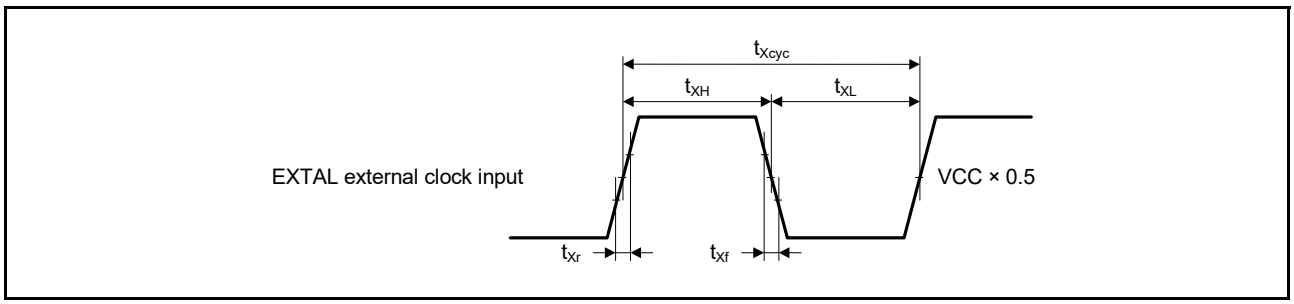


Figure 2.25 EXTAL external clock input timing

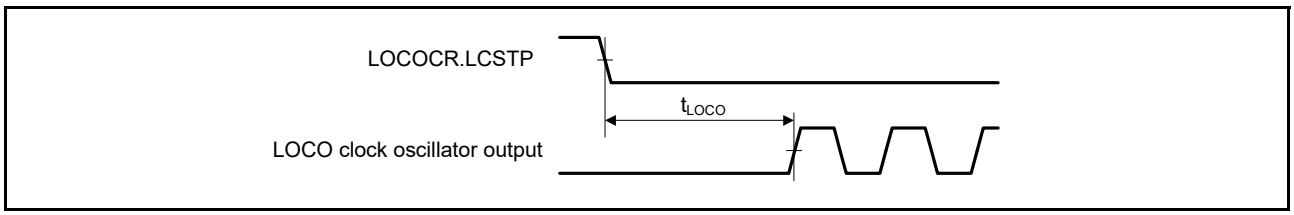


Figure 2.26 LOCO clock oscillation start timing

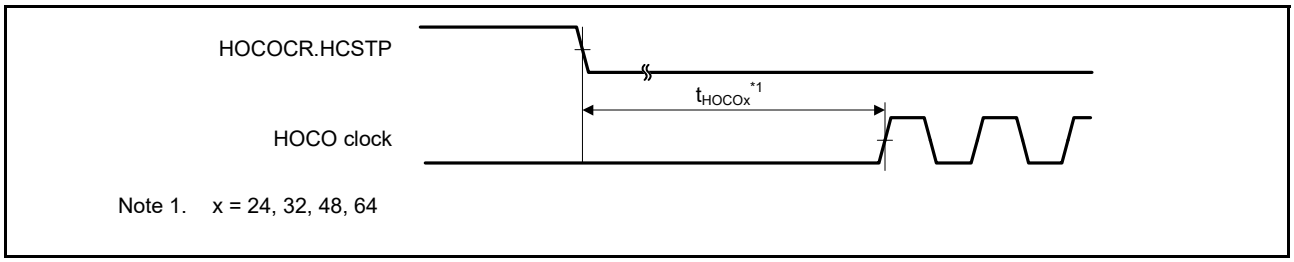


Figure 2.27 HOCO clock oscillation start timing (started by setting the HOCOCR.HCSTP bit)

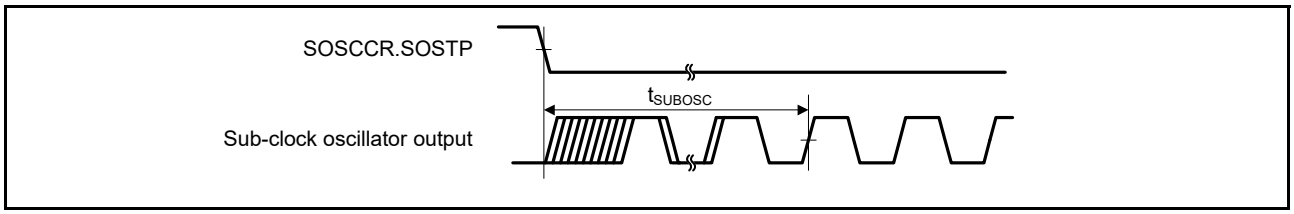


Figure 2.28 Sub-clock oscillation start timing

2.3.3 Reset Timing

Table 2.21 Reset timing

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
RES pulse width	At power-on	t_{RESWP}	3	-	-	ms	Figure 2.29
	Not at power-on	t_{RESW}	30	-	-	µs	Figure 2.30
Wait time after RES cancellation (at power-on)	LVD0 enabled*1	t_{RESWT}	-	0.7	-	ms	Figure 2.29
	LVD0 disabled*2		-	0.3	-		
Wait time after RES cancellation (during powered-on state)	LVD0 enabled*1	t_{RESWT2}	-	0.5	-	ms	Figure 2.30
	LVD0 disabled*2		-	0.1	-		
Wait time after internal reset cancellation (Watchdog timer reset, SRAM parity error reset, SRAM ECC error reset, bus master MPU error reset, bus slave MPU error reset, stack pointer error reset, software reset)	LVD0 enabled*1	t_{RESWT3}	-	0.6	-	ms	Figure 2.31
	LVD0 disabled*2		-	0.15	-		

Note 1. When OFS1.LVDAS = 0.
Note 2. When OFS1.LVDAS = 1.

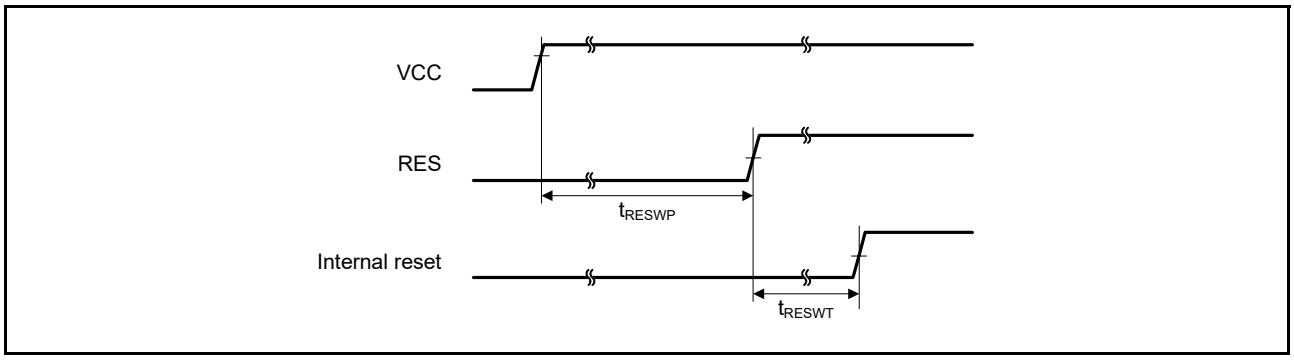


Figure 2.29 Reset input timing at power-on

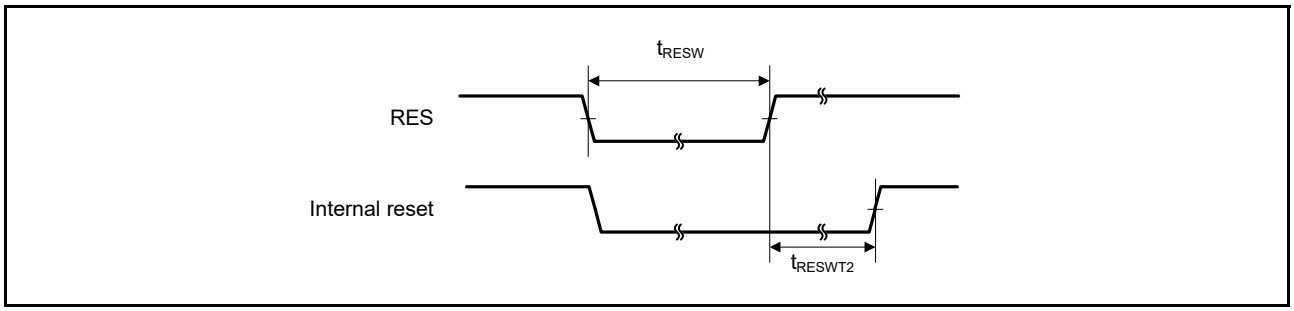


Figure 2.30 Reset input timing (1)

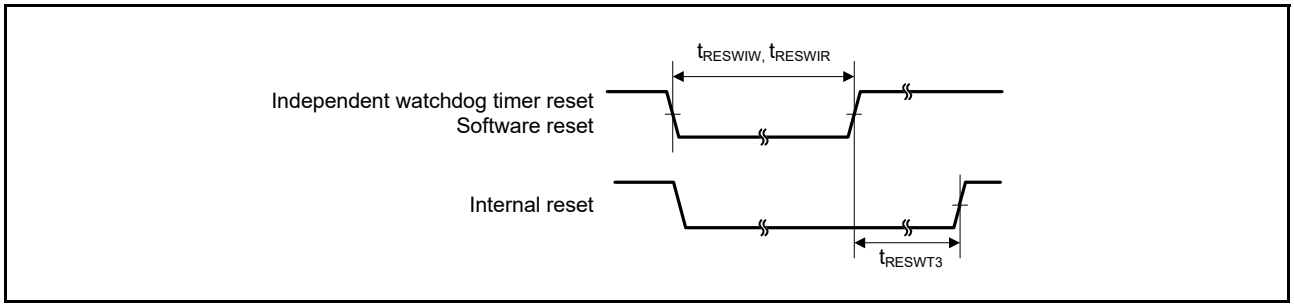


Figure 2.31 Reset input timing (2)

2.3.4 Wakeup Time

Table 2.22 Timing of recovery from low power modes (1)

Parameter				Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	High-speed mode	Crystal resonator connected to main clock oscillator	System clock source is main clock oscillator (20 MHz)*2	t_{SBYMC}	-	2	3	ms	Figure 2.32
		External clock input to main clock oscillator	System clock source is main clock oscillator (20 MHz)*3	t_{SBYEX}	-	14	25	µs	
		System clock source is HOCO*4 (HOCO clock is 32 MHz)		t_{SBYHO}	-	43	52	µs	
		System clock source is HOCO*4 (HOCO clock is 48 MHz)		t_{SBYHO}	-	44	52	µs	
		System clock source is HOCO*5 (HOCO clock is 64 MHz)		t_{SBYHO}	-	82	110	µs	
		System clock source is MOCO		t_{SBYMO}	-	16	25	µs	

Note 1. The division ratio of ICK, FCK, and PCKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source.
Note 2. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 05h.
Note 3. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 00h.
Note 4. The HOCO Clock Wait Control Register (HOCOWTCR) is set to 05h.
Note 5. The HOCO Clock Wait Control Register (HOCOWTCR) is set to 06h.

Table 2.23 Timing of recovery from low power modes (2)

Parameter				Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	Middle-speed mode	Crystal resonator connected to main clock oscillator	System clock source is main clock oscillator (12 MHz)*2	t_{SBYMC}	-	2	3	ms	Figure 2.32
		External clock input to main clock oscillator	System clock source is main clock oscillator (12 MHz)*3	t_{SBYEX}	-	2.9	10	µs	
		System clock source is HOCO*4		t_{SBYHO}	-	38	50	µs	
		System clock source is MOCO (8 MHz)		t_{SBYMO}	-	3.5	5.5	µs	

Note 1. The division ratio of ICK, FCK, and PCKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source.
Note 2. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 05h.
Note 3. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 00h.
Note 4. The system clock is 12 MHz.

Table 2.24 Timing of recovery from low power modes (3)

Parameter				Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	Low-speed mode	Crystal resonator connected to main clock oscillator	System clock source is main clock oscillator (1 MHz)*2	t_{SBYMC}	-	2	3	ms	Figure 2.32
		External clock input to main clock oscillator	System clock source is main clock oscillator (1 MHz)*3	t_{SBYEX}	-	28	50	µs	
		System clock source is MOCO (1 MHz)		t_{SBYMO}	-	25	35	µs	

Note 1. The division ratio of ICK, FCK, and PCKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source.
Note 2. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 05h.
Note 3. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 00h.

Table 2.25 Timing of recovery from low power modes (4)

Parameter				Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	Low-voltage mode	Crystal resonator connected to main clock oscillator	System clock source is main clock oscillator (4 MHz)*2	t_{SBYMC}	-	2	3	ms	Figure 2.32
		External clock input to main clock oscillator	System clock source is main clock oscillator (4 MHz)*3	t_{SBYEX}	-	108	130	µs	
		System clock source is HOCO (4 MHz)		t_{SBYHO}	-	108	130	µs	

Note 1. The division ratio of ICK, FCK, and PCKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source.
Note 2. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 05h.
Note 3. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 00h.

Table 2.26 Timing of recovery from low power modes (5)

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	Subosc-speed mode	System clock source is sub-clock oscillator (32.768 kHz)	t_{SBYSC}	-	0.85	1	ms	Figure 2.32
		System clock source is LOCO (32.768 kHz)	t_{SBYLO}	-	0.85	1.2	ms	

Note 1. The sub-clock oscillator or LOCO itself continues oscillating in Software Standby mode during Subosc-speed mode.

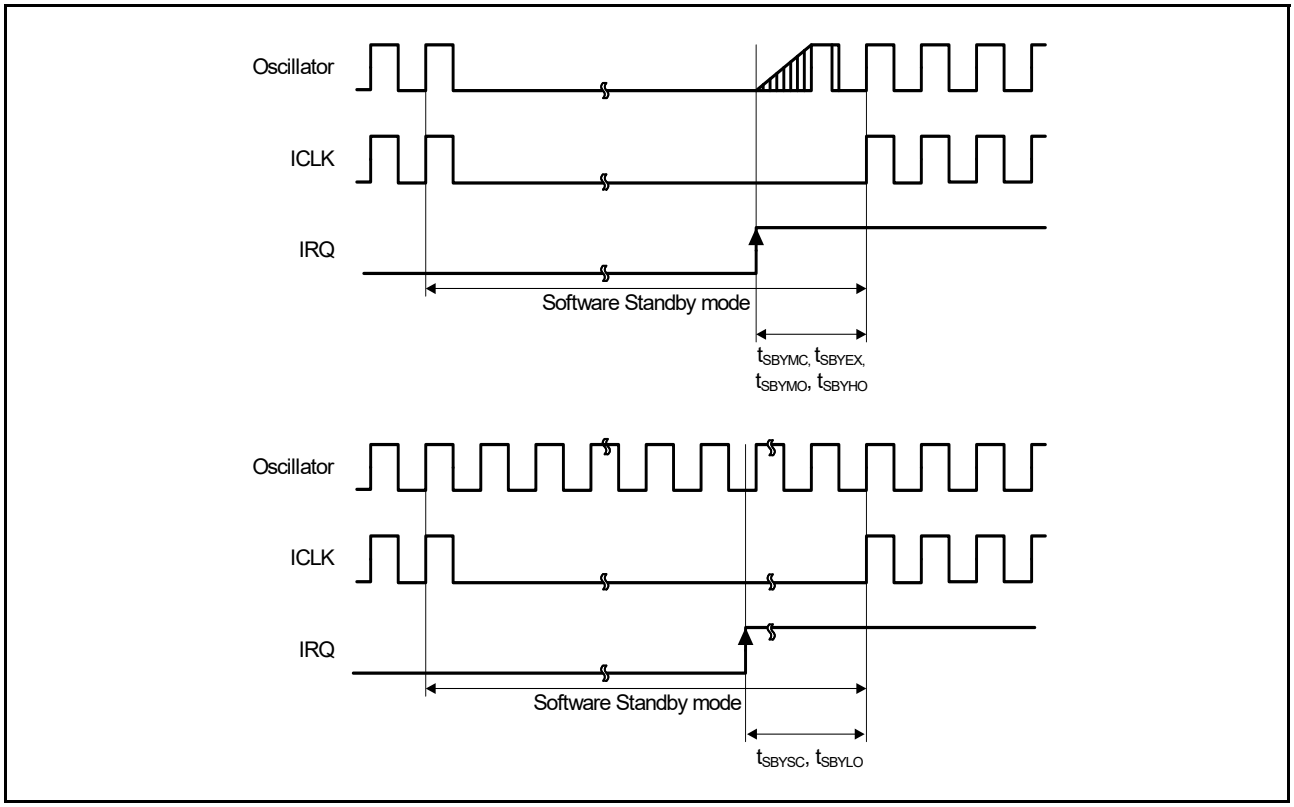
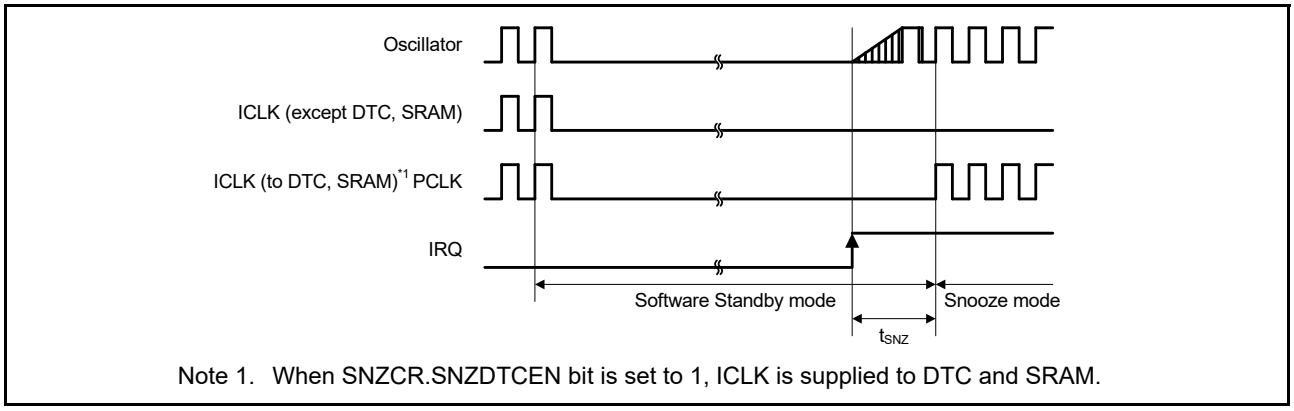


Figure 2.32 Software Standby mode cancellation timing

Table 2.27 Timing of recovery from low power modes (6)

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode to Snooze mode	High-speed mode System clock source is HOCO	t_{SNZ}	-	36	45	µs	Figure 2.33
	Middle-speed mode System clock source is MOCO (8 MHz)	t_{SNZ}	-	1.3	3.6	µs	
	Low-speed mode System clock source is MOCO (1 MHz)	t_{SNZ}	-	10	13	µs	
	Low-voltage mode System clock source is HOCO (4 MHz)	t_{SNZ}	-	87	110	µs	



Note 1. When SNZCR.SNZDTCEN bit is set to 1, ICLK is supplied to DTC and SRAM.

Figure 2.33 Recovery timing from Software Standby mode to Snooze mode

2.3.5 NMI and IRQ Noise Filter

Table 2.28 NMI and IRQ noise filter

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	
NMI pulse width	t_{NMIW}	200	-	-	ns	NMI digital filter disabled	$t_{Pcyc} \times 2 \leq 200$ ns
		$t_{Pcyc} \times 2$*1	-	-			$t_{Pcyc} \times 2 > 200$ ns
		200	-	-		NMI digital filter enabled	$t_{NMICK} \times 3 \leq 200$ ns
		$t_{NMICK} \times 3.5$*2	-	-			$t_{NMICK} \times 3 > 200$ ns
IRQ pulse width	t_{IRQW}	200	-	-	ns	IRQ digital filter disabled	$t_{Pcyc} \times 2 \leq 200$ ns
		$t_{Pcyc} \times 2$*1	-	-			$t_{Pcyc} \times 2 > 200$ ns
		200	-	-		IRQ digital filter enabled	$t_{IRQCK} \times 3 \leq 200$ ns
		$t_{IRQCK} \times 3.5$*3	-	-			$t_{IRQCK} \times 3 > 200$ ns

Note: 200 ns minimum in Software Standby mode.
Note: If the clock source is switched, add 4 clock cycles of the switched source.
Note 1. t_{Pcyc} indicates the PCLKB cycle.
Note 2. t_{NMICK} indicates the cycle of the NMI digital filter sampling clock.
Note 3. t_{IRQCK} indicates the cycle of the IRQi digital filter sampling clock (i = 0 to 7).

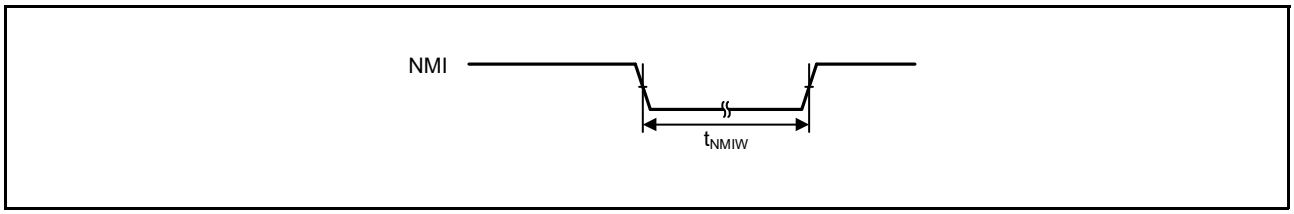


Figure 2.34 NMI interrupt input timing

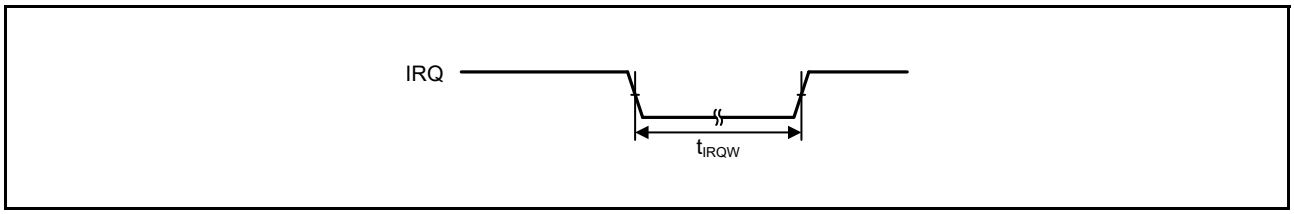


Figure 2.35 IRQ interrupt input timing

2.3.6 I/O Ports, POEG, GPT, AGT, KINT, and ADC16 Trigger Timing

Note:

Table 2.29 I/O Ports, POEG, GPT, AGT, KINT, and ADC16 trigger timing

Parameter			Symbol	Min	Max	Unit	Test conditions
I/O Ports	Input data pulse width		t_{PRW}	1.5	-	t_{Pcyc}	Figure 2.36
POEG	POEG input trigger pulse width		t_{POEW}	3	-	t_{Pcyc}	Figure 2.37
GPT	Input capture pulse width	Single edge	t_{GTICW}	1.5	-	t_{PDcyc}	Figure 2.38
		Dual edge		2.5	-		
AGT	AGTIO, AGTEE input cycle	2.7 V ≤ VCC ≤ 5.5 V	t_{ACYC}*1	250	-	ns	Figure 2.39
		2.4 V ≤ VCC < 2.7 V		500	-	ns	
		1.8 V ≤ VCC < 2.4 V		1000	-	ns	
		1.6 V ≤ VCC < 1.8 V		2000	-	ns	
	AGTIO, AGTEE input high-level width, low-level width	2.7 V ≤ VCC ≤ 5.5 V	t_{ACKWH}, t_{ACKWL}	100	-	ns	
		2.4 V ≤ VCC < 2.7 V		200	-	ns	
		1.8 V ≤ VCC < 2.4 V		400	-	ns	
		1.6 V ≤ VCC < 1.8 V		800	-	ns	
	AGTIO, AGTO, AGTOA, AGTOB output cycle	2.7 V ≤ VCC ≤ 5.5 V	t_{ACYC2}	62.5	-	ns	Figure 2.39
		2.4 V ≤ VCC < 2.7 V		125	-	ns	
		1.8 V ≤ VCC < 2.4 V		250	-	ns	
		1.6 V ≤ VCC < 1.8 V		500	-	ns	
ADC16	16-bit A/D converter trigger input pulse width		t_{TRGW}	1.5	-	t_{Pcyc}	Figure 2.40
KINT	KRn (n = 00 to 07) pulse width		t_{KR}	250	-	ns	Figure 2.41

Note: t_{Pcyc}: PCLKB cycle, t_{PDcyc}: PCLKD cycle.

Note 1. Constraints on input cycle:
When not switching the source clock: $t_{Pcyc} \times 2 < t_{ACYC}$ should be satisfied.
When switching the source clock: $t_{Pcyc} \times 6 < t_{ACYC}$ should be satisfied.

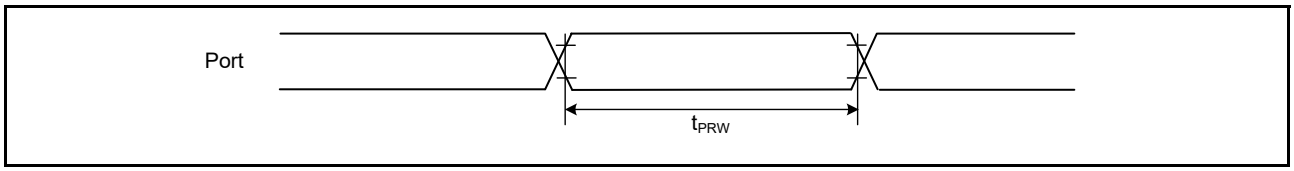


Figure 2.36 I/O ports input timing

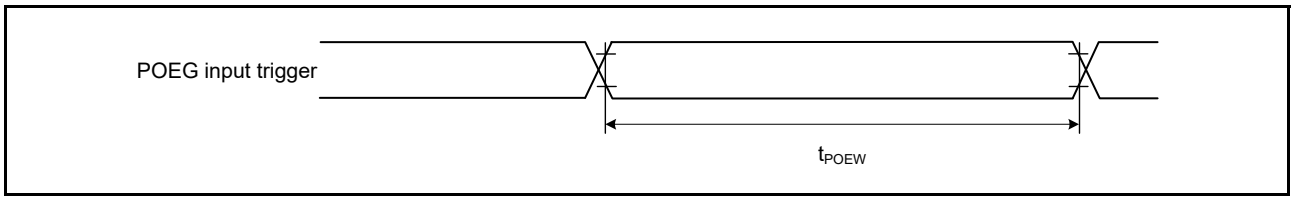


Figure 2.37 POEG input trigger timing

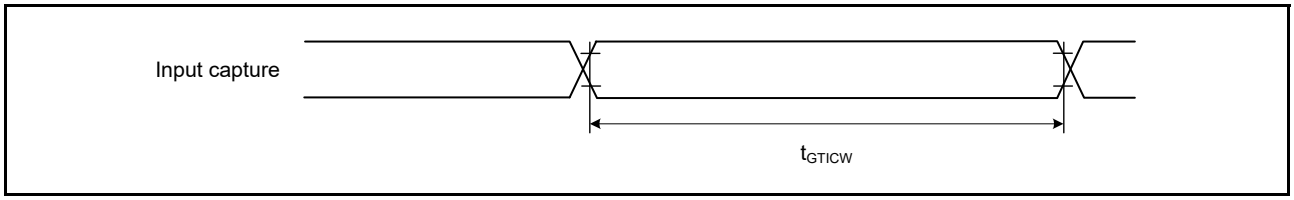


Figure 2.38 GPT input capture timing

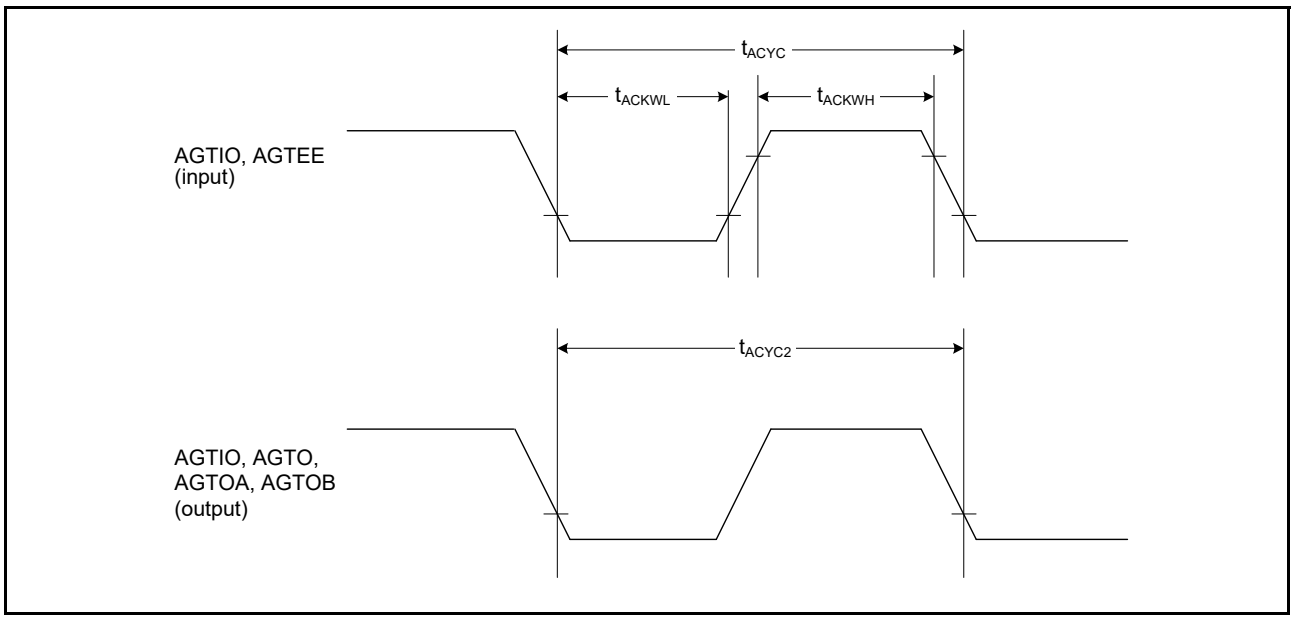


Figure 2.39 AGT I/O timing

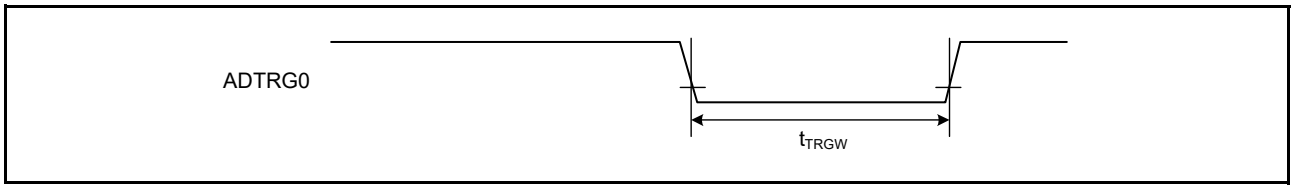


Figure 2.40 ADC16 trigger input timing

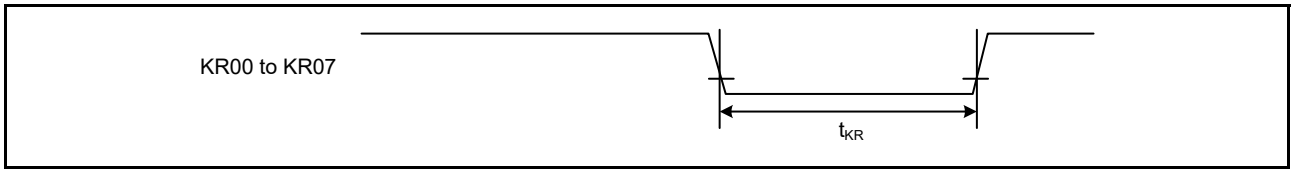


Figure 2.41 Key interrupt input timing

2.3.7 CAC Timing

Table 2.30 CAC timing
Conditions: VCC = AVCC0 = AVCC1 = 1.6 to 5.5 V

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
CAC	CACREF input pulse width	t_{Pcyc} *1 ≤ t_{cac}*2	t_{CACREF}	4.5 × t_{cac} + 3 × t_{Pcyc}	-	-	ns	-
		t_{Pcyc}*1 > t_{cac}*2		5 × t_{cac} + 6.5 × t_{Pcyc}	-	-	ns	

Note 1. t_{Pcyc}: PCLKB cycle.

Note 2. t_{cac}: CAC count clock source cycle.

2.3.8 SCI Timing

Table 2.31 SCI timing (1)
Conditions: VCC = AVCC0 = AVCC1 = 1.6 to 5.5 V

Parameter				Symbol	Min	Max	Unit*1	Test conditions
SCI	Input clock cycle	Asynchronous		t_{Scyc}	4	-	t_{Pcyc}	Figure 2.42
		Clock synchronous			6	-		
	Input clock pulse width			t_{SCKW}	0.4	0.6	t_{Scyc}	
	Input clock rise time			t_{SCKr}	-	20	ns	
	Input clock fall time			t_{SCKf}	-	20	ns	
	Output clock cycle	Asynchronous		t_{Scyc}	6	-	t_{Pcyc}	
		Clock synchronous			4	-		
	Output clock pulse width			t_{SCKW}	0.4	0.6	t_{Scyc}	
	Output clock rise time		1.8 V ≤ VCC ≤ 5.5 V	t_{SCKr}	-	20	ns	
			1.6 V ≤ VCC < 1.8 V		-	30		
	Output clock fall time		1.8 V ≤ VCC ≤ 5.5 V	t_{SCKf}	-	20	ns	
			1.6 V ≤ VCC < 1.8 V		-	30		
	Transmit data delay (master)	Clock synchronous	1.8 V ≤ VCC ≤ 5.5 V	t_{TXD}	-	40	ns	Figure 2.43
			1.6 V ≤ VCC < 1.8 V		-	45		
	Transmit data delay (slave)	Clock synchronous	2.7 V ≤ VCC ≤ 5.5 V		-	55	ns	
			2.4 V ≤ VCC < 2.7 V		-	60		
			1.8 V ≤ VCC < 2.4 V		-	100		
			1.6 V ≤ VCC < 1.8 V		-	125		
	Receive data setup time (master)	Clock synchronous	2.7 V ≤ VCC ≤ 5.5 V	t_{RXS}	45	-	ns	
			2.4 V ≤ VCC < 2.7 V		55	-		
			1.8 V ≤ VCC < 2.4 V		90	-		
			1.6 V ≤ VCC < 1.8 V		110	-		
	Receive data setup time (slave)	Clock synchronous	2.7 V ≤ VCC ≤ 5.5 V		40	-	ns	
			1.6 V ≤ VCC < 2.7 V		45	-		
	Receive data hold time (master)	Clock synchronous		t_{RXH}	5	-	ns	
	Receive data hold time (slave)	Clock synchronous		t_{RXH}	40	-	ns	

Note 1. t_{Pcyc}: PCLKB cycle.

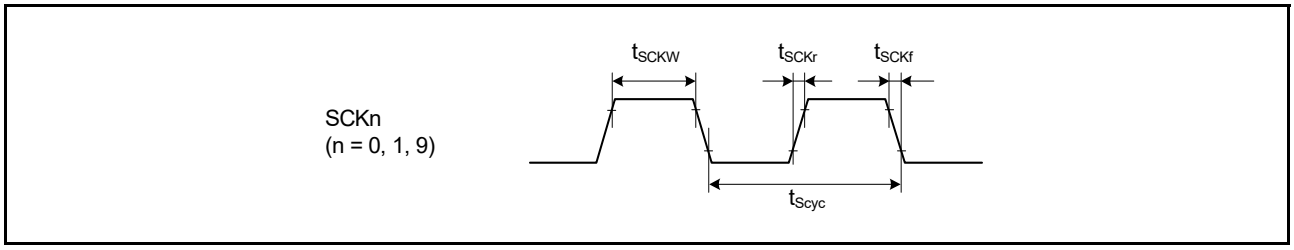


Figure 2.42 SCK clock input timing

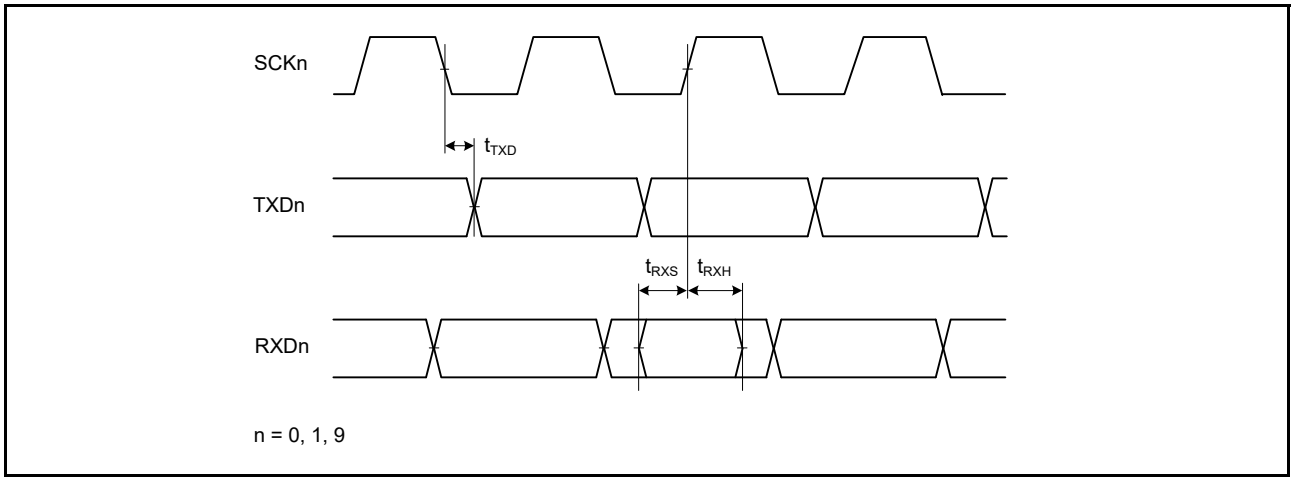


Figure 2.43 SCI input/output timing in clock synchronous mode

Table 2.32 SCI timing (2)

Conditions: VCC = AVCC0 = AVCC1 = 1.6 to 5.5 V

Parameter				Symbol	Min	Max	Unit*1	Test conditions
Simple SPI	SCK clock cycle output (master)			t_{SPcyc}	4	65536	t_{Pcyc}	Figure 2.44
	SCK clock cycle input (slave)				6	65536		
	SCK clock high pulse width			t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK clock low pulse width			t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK clock rise and fall time		1.8 V ≤ VCC ≤ 5.5 V	t_{SPCKr}, t_{SPCKf}	-	20	ns	
			1.6 V ≤ VCC < 1.8 V		-	30		
	Data input setup time	Master	2.7 V ≤ VCC ≤ 5.5 V	t_{SU}	45	-	ns	Figure 2.45 to Figure 2.48
			2.4 V ≤ VCC < 2.7 V		55	-		
			1.8 V ≤ VCC < 2.4 V		80	-		
			1.6 V ≤ VCC < 1.8 V		110	-		
		Slave	2.7 V ≤ VCC ≤ 5.5 V		40	-		
			1.6 V ≤ VCC < 2.7 V		45	-		
	Data input hold time	Master		t_{H}	33.3	-	ns	
		Slave			40	-		
	SS input setup time			t_{LEAD}	1	-	t_{SPcyc}	
	SS input hold time			t_{LAG}	1	-	t_{SPcyc}	
	Data output delay	Master	1.8 V ≤ VCC ≤ 5.5 V	t_{OD}	-	40	ns	
			1.6 V ≤ VCC < 1.8 V		-	50		
		Slave	2.4 V ≤ VCC ≤ 5.5 V		-	65		
			1.8 V ≤ VCC < 2.4 V		-	100		
			1.6 V ≤ VCC < 1.8 V		-	125		
	Data output hold time	Master	2.7 V ≤ VCC ≤ 5.5 V	t_{OH}	-10	-	ns	
			2.4 V ≤ VCC < 2.7 V		-20	-		
			1.8 V ≤ VCC < 2.4 V		-30	-		
			1.6 V ≤ VCC < 1.8 V		-40	-		
		Slave			-10	-		
	Data rise and fall time	Master	1.8 V ≤ VCC ≤ 5.5 V	t_{Dr}, t_{Df}	-	20	ns	
			1.6 V ≤ VCC < 1.8 V		-	30		
		Slave	1.8 V ≤ VCC ≤ 5.5 V		-	20		
			1.6 V ≤ VCC < 1.8 V		-	30		
Simple SPI	Slave access time			t_{SA}	-	6	t_{Pcyc}	Figure 2.48
	Slave output release time			t_{REL}	-	6	t_{Pcyc}	

Note 1. t_{Pcyc}: PCLKB cycle.

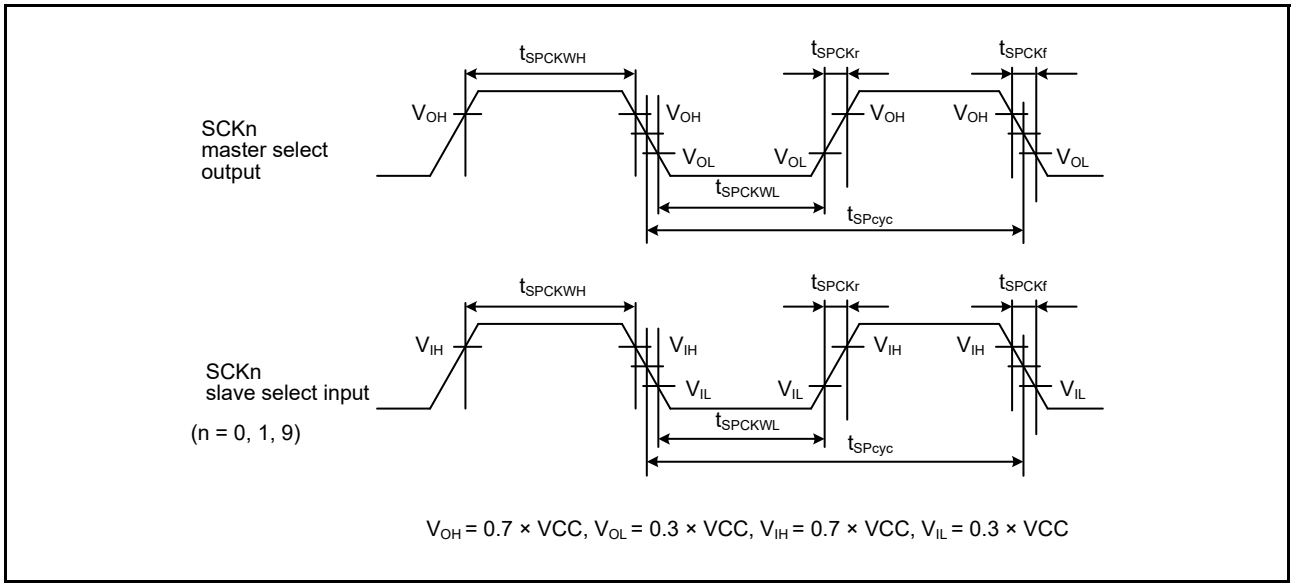


Figure 2.44 SCI simple SPI mode clock timing

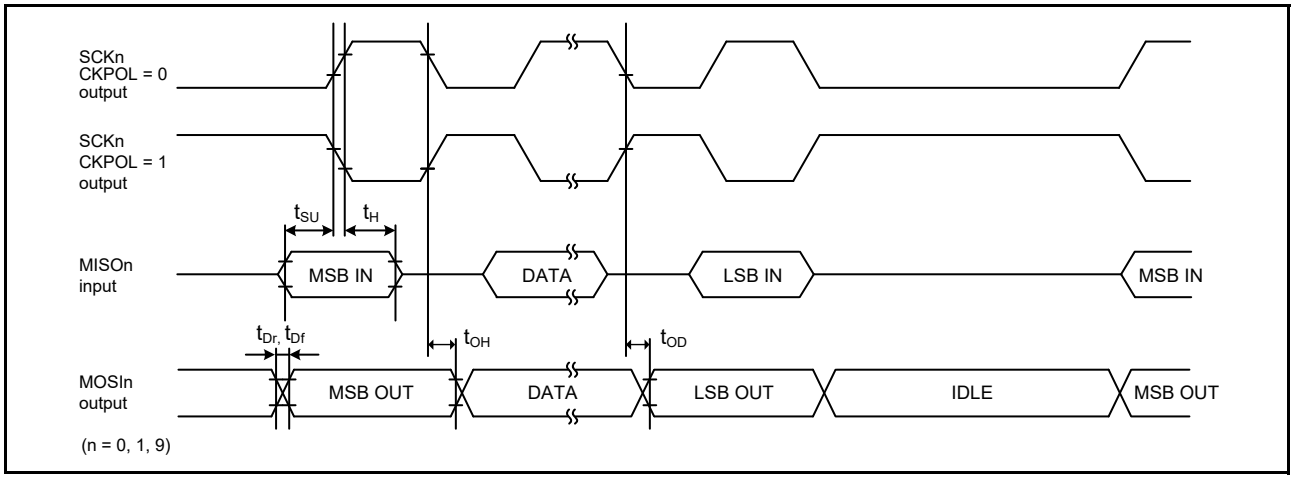


Figure 2.45 SCI simple SPI mode timing (master, CKPH = 1)

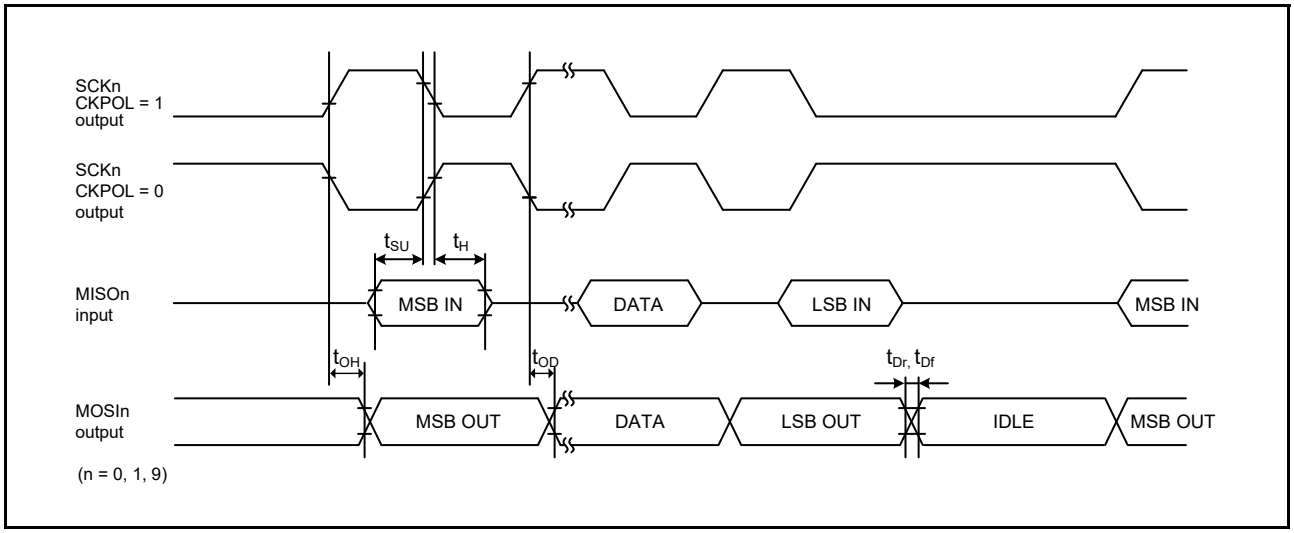


Figure 2.46 SCI simple SPI mode timing (master, CKPH = 0)

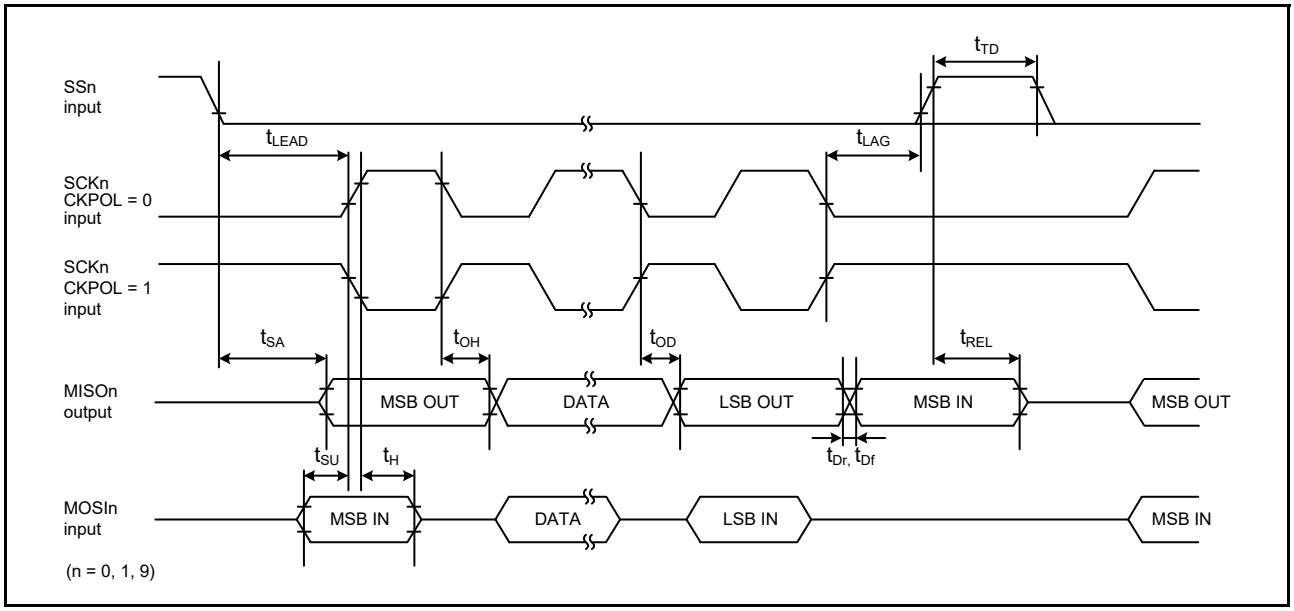


Figure 2.47 SCI simple SPI mode timing (slave, CKPH = 1)

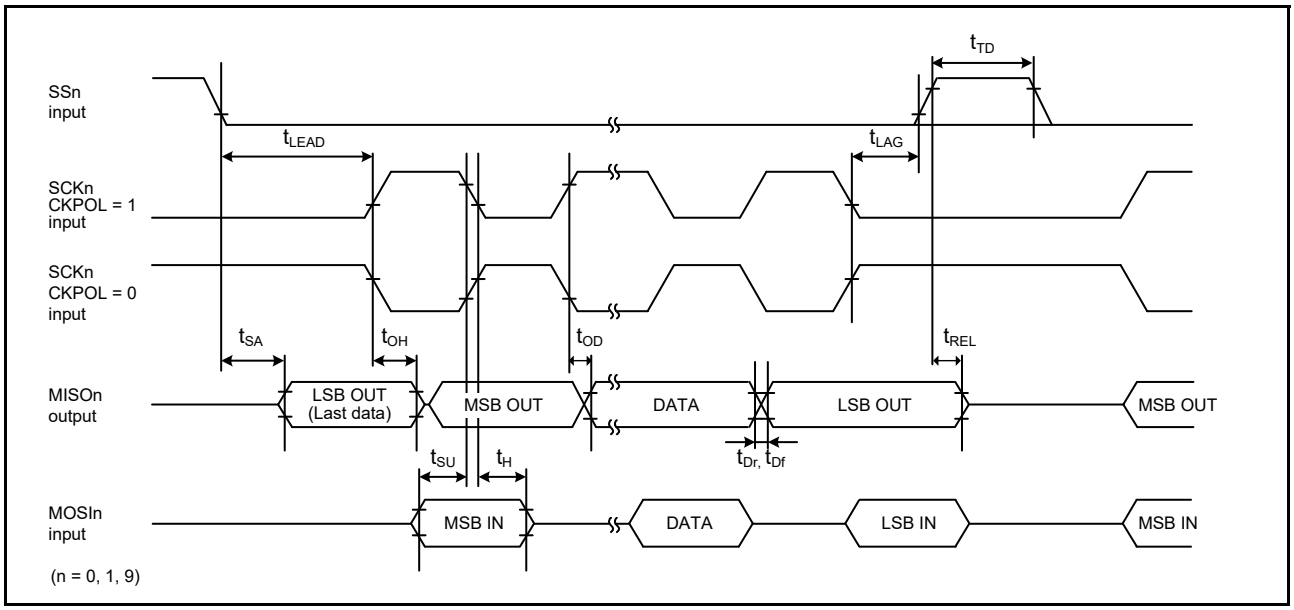


Figure 2.48 SCI simple SPI mode timing (slave, CKPH = 0)

Table 2.33 SCI timing (3)

Conditions: VCC = AVCC0 = AVCC1 = 2.7 to 5.5 V

Parameter		Symbol	Min	Max	Unit	Test conditions
Simple IIC (Standard mode)	SDA input rise time	t_{Sr}	-	1000	ns	Figure 2.49
	SDA input fall time	t_{Sf}	-	300	ns	
	SDA input spike pulse removal time	t_{SP}	0	4 × t_{IICcyc}*1	ns	
	Data input setup time	t_{SDAS}	250	-	ns	
	Data input hold time	t_{SDAH}	0	-	ns	
	SCL, SDA capacitive load	C_b*2	-	400	pF	

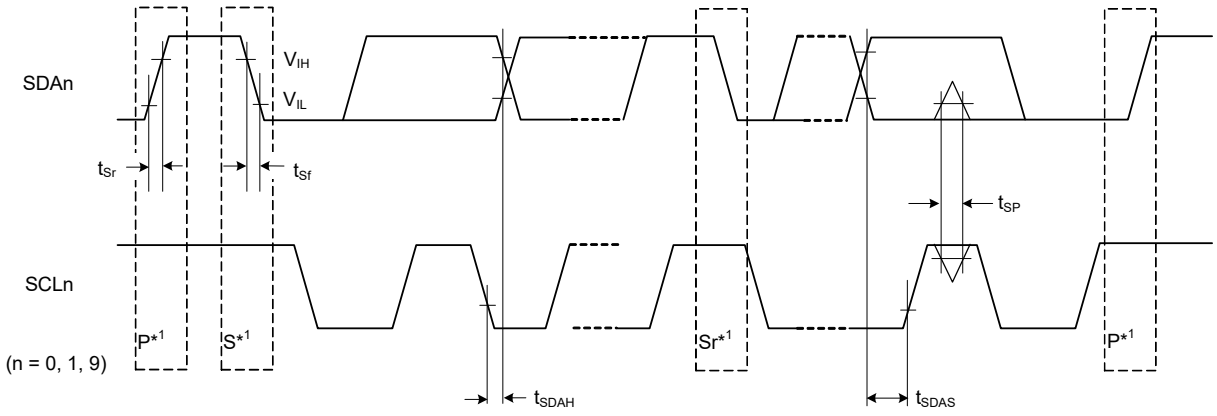
Table 2.33 SCI timing (3)

Conditions: VCC = AVCC0 = AVCC1 = 2.7 to 5.5 V

Parameter		Symbol	Min	Max	Unit	Test conditions
Simple IIC (Fast mode)	SDA input rise time	t_{Sr}	-	300	ns	Figure 2.49
	SDA input fall time	t_{Sf}	-	300	ns	
	SDA input spike pulse removal time	t_{SP}	0	4 × t_{IICcyc}*1	ns	
	Data input setup time	t_{SDAS}	100	-	ns	
	Data input hold time	t_{SDAH}	0	-	ns	
	SCL, SDA capacitive load	C_b*2	-	400	pF	

Note 1. t_{IICcyc}: Clock cycle selected by the SMR.CKS[1:0] bits.

Note 2. C_b indicates the total capacity of the bus line.



Note 1. S, P, and Sr indicate the following conditions:
S: Start condition
P: Stop condition
Sr: Restart condition

Figure 2.49 SCI simple IIC mode timing

2.3.9 SPI Timing

Table 2.34 SPI timing (1 of 2)

Conditions: Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter				Symbol	Min	Max	Unit*1	Test conditions
SPI	RSPCK clock cycle	Master		t_{SPcyc}	2	4096	t_{Pcyc}	Figure 2.50 C = 30 pF
		Slave			6	4096		
	RSPCK clock high pulse width	Master		t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3$	-	ns	
		Slave			$3 \times t_{Pcyc}$	-		
	RSPCK clock low pulse width	Master		t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3$	-	ns	
		Slave			$3 \times t_{Pcyc}$	-		
	RSPCK clock rise and fall time	Output	2.7 V ≤ VCC ≤ 5.5 V	t_{SPCKr}, t_{SPCKf}	-	10	ns	
			2.4 V ≤ VCC < 2.7 V		-	15		
			1.8 V ≤ VCC ≤ 2.4 V		-	20		
			1.6 V ≤ VCC < 1.8 V		-	30		
		Input			-	1	µs	
	Data input setup time	Master		t_{SU}	10	-	ns	Figure 2.51 to Figure 2.56 C = 30 pF
		Slave	2.4 V ≤ VCC ≤ 5.5 V		10	-		
			1.8 V ≤ VCC < 2.4 V		15	-		
			1.6 V ≤ VCC < 1.8 V		20	-		
	Data input hold time	Master (RSPCK is PCLKB/2)		t_{HF}	0	-	ns	
		Master (RSPCK is not PCLKB/2)		t_{H}	t_{Pcyc}	-		
		Slave		t_{H}	20	-		
	SSL setup time	Master	1.8 V ≤ VCC ≤ 5.5 V	t_{LEAD}	$-30 + N \times t_{Spcyc}$*2	-	ns	
			1.6 V ≤ VCC < 1.8 V		$-50 + N \times t_{Spcyc}$*2	-		
		Slave			$6 \times t_{Pcyc}$	-	ns	
	SSL hold time	Master		t_{LAG}	$-30 + N \times t_{Spcyc}$*3	-	ns	
		Slave			$6 \times t_{Pcyc}$	-	ns	
	Data output delay	Master	2.7 V ≤ VCC ≤ 5.5 V	t_{OD}	-	14	ns	
			2.4 V ≤ VCC < 2.7 V		-	20		
			1.8 V ≤ VCC < 2.4 V		-	25		
			1.6 V ≤ VCC < 1.8 V		-	30		
		Slave	2.7 V ≤ VCC ≤ 5.5 V		-	50		
			2.4 V ≤ VCC < 2.7 V		-	60		
			1.8 V ≤ VCC < 2.4 V		-	85		
			1.6 V ≤ VCC < 1.8 V		-	110		
	Data output hold time	Master		t_{OH}	0	-	ns	
		Slave			0	-		
	Successive transmission delay	Master		t_{TD}	$t_{SPcyc} + 2 \times t_{Pcyc}$	$8 \times t_{SPcyc} + 2 \times t_{Pcyc}$	ns	
		Slave			$6 \times t_{Pcyc}$	-		

Table 2.34 SPI timing (2 of 2)

Conditions: Middle drive output is selected in the Port Drive Capability bit in the PmnPFS register.

Parameter				Symbol	Min	Max	Unit*1	Test conditions
SPI	MOSI and MISO rise and fall time	Output	2.7 V ≤ VCC ≤ 5.5 V	t_{Dr}, t_{Df}	-	10	ns	Figure 2.51 to Figure 2.56 C = 30 pF
			2.4 V ≤ VCC < 2.7 V		-	15		
			1.8 V ≤ VCC < 2.4 V		-	20		
			1.6 V ≤ VCC < 1.8 V		-	30		
		Input			-	1	µs	
	SSL rise and fall time	Output	2.7 V ≤ VCC ≤ 5.5 V	t_{SSLr}, t_{SSLf}	-	10	ns	
			2.4 V ≤ VCC < 2.7 V		-	15		
			1.8 V ≤ VCC < 2.4 V		-	20		
			1.6 V ≤ VCC < 1.8 V		-	30		
		Input			-	1	µs	
	Slave access time		2.4 V ≤ VCC ≤ 5.5 V	t_{SA}	-	2 × t_{Pcyc} + 100	ns	Figure 2.55 and Figure 2.56 C = 30 pF
			1.8 V ≤ VCC < 2.4 V		-	2 × t_{Pcyc} + 140		
			1.6 V ≤ VCC < 1.8 V		-	2 × t_{Pcyc} + 180		
	Slave output release time		2.4 V ≤ VCC ≤ 5.5 V	t_{REL}	-	2 × t_{Pcyc} + 100	ns	
			1.8 V ≤ VCC < 2.4 V		-	2 × t_{Pcyc} + 140		
			1.6 V ≤ VCC < 1.8 V		-	2 × t_{Pcyc} + 180		

Note 1. t_{Pcyc}: PCLKB cycle.
Note 2. N is set as an integer from 1 to 8 by the SPCKD register.
Note 3. N is set as an integer from 1 to 8 by the SSLND register.

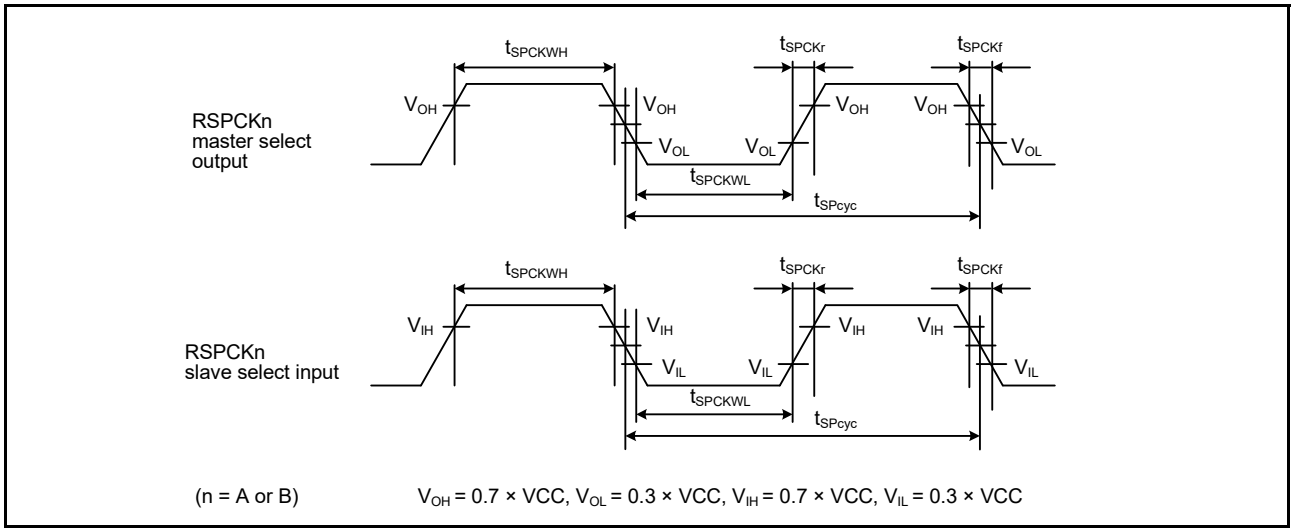


Figure 2.50 SPI clock timing

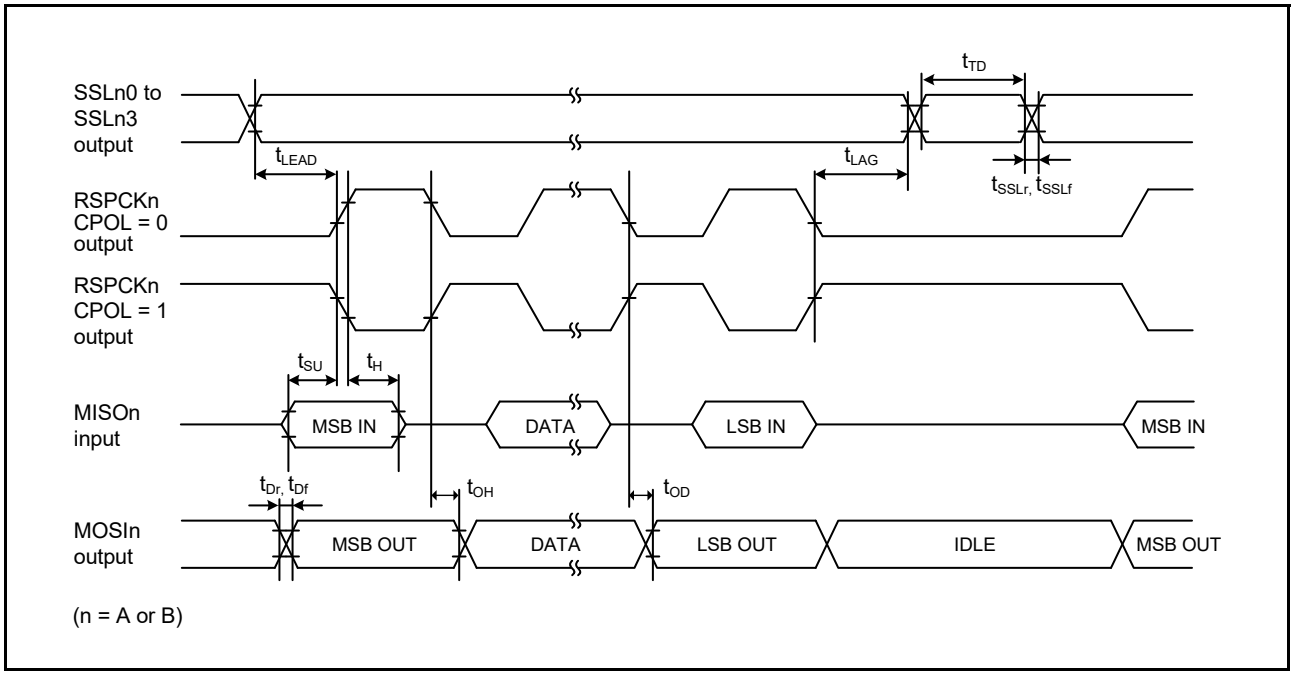


Figure 2.51 SPI timing (master, CPHA = 0) (bit rate: PCLKB division ratio is set to any value other than 1/2)

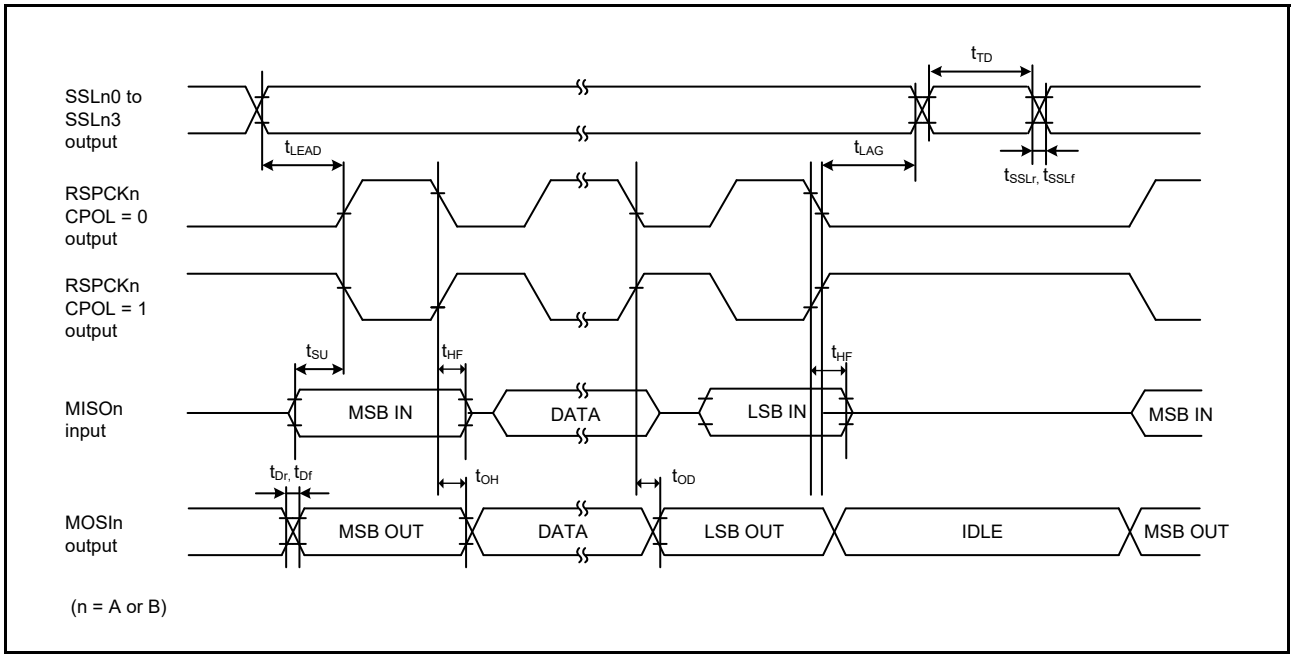


Figure 2.52 SPI timing (master, CPHA = 0) (bit rate: PCLKB division ratio is set to 1/2)

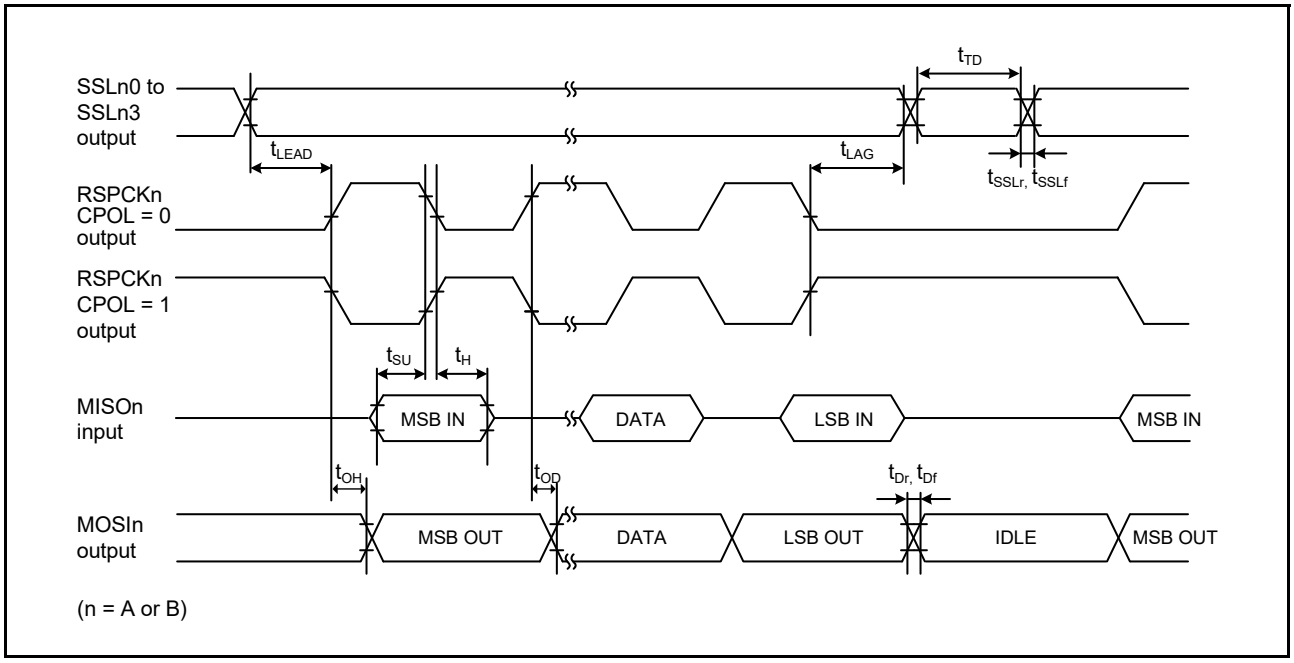


Figure 2.53 SPI timing (master, CPHA = 1) (bit rate: PCLKB division ratio is set to any value other than 1/2)

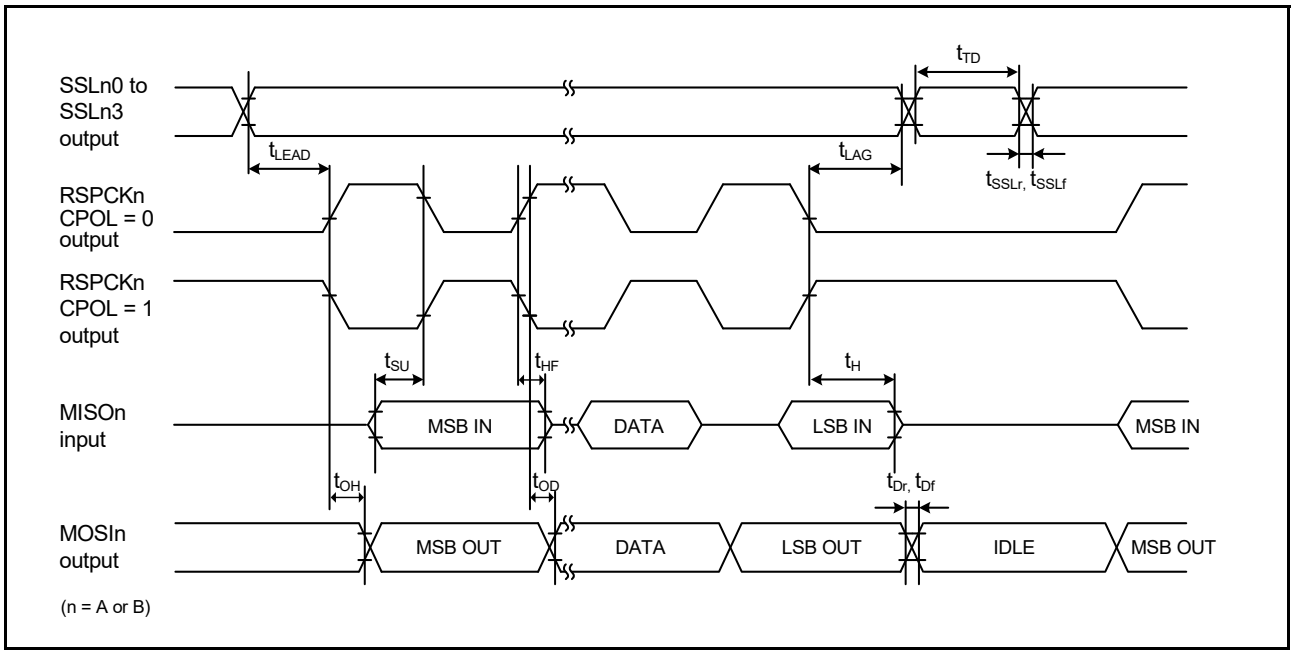


Figure 2.54 SPI timing (master, CPHA = 1) (bit rate: PCLKB division ratio is set to 1/2)

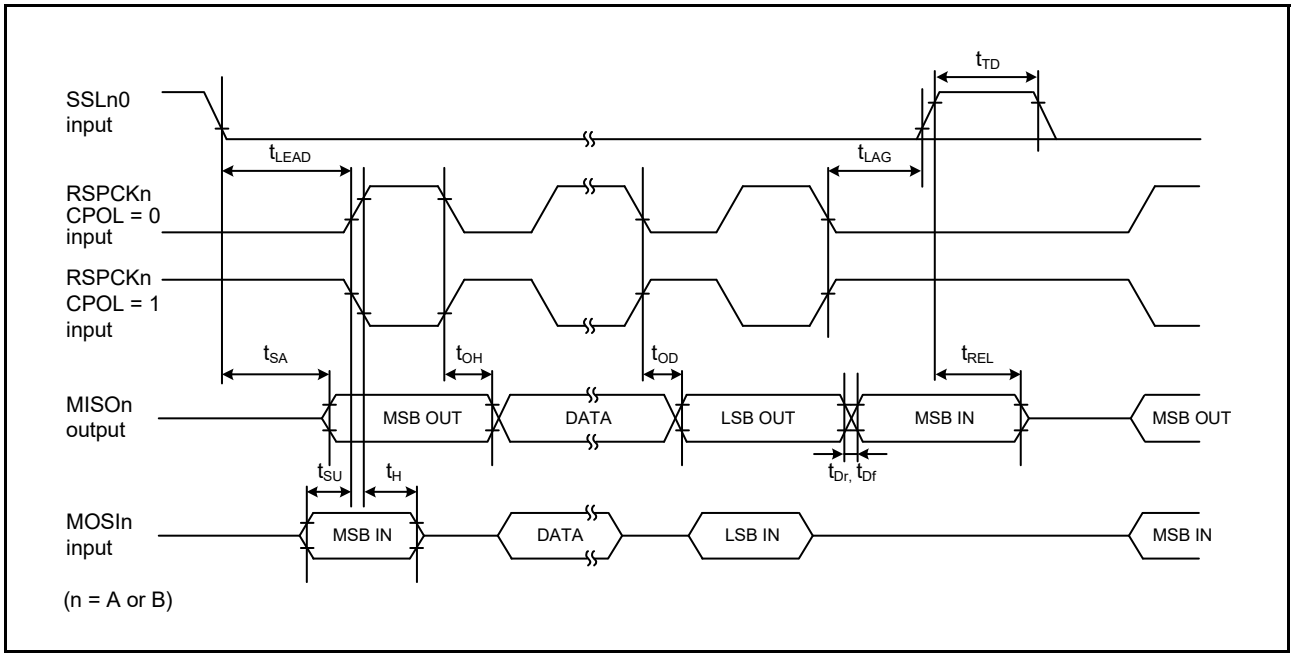


Figure 2.55 SPI timing (slave, CPHA = 0)

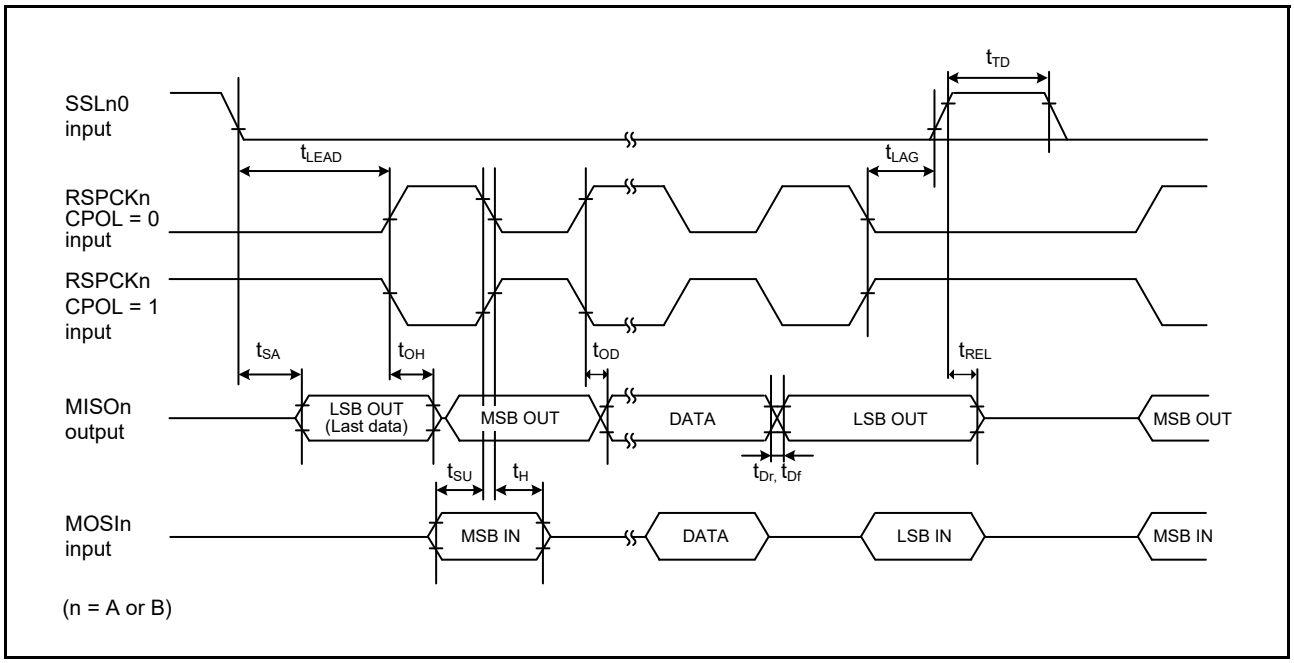


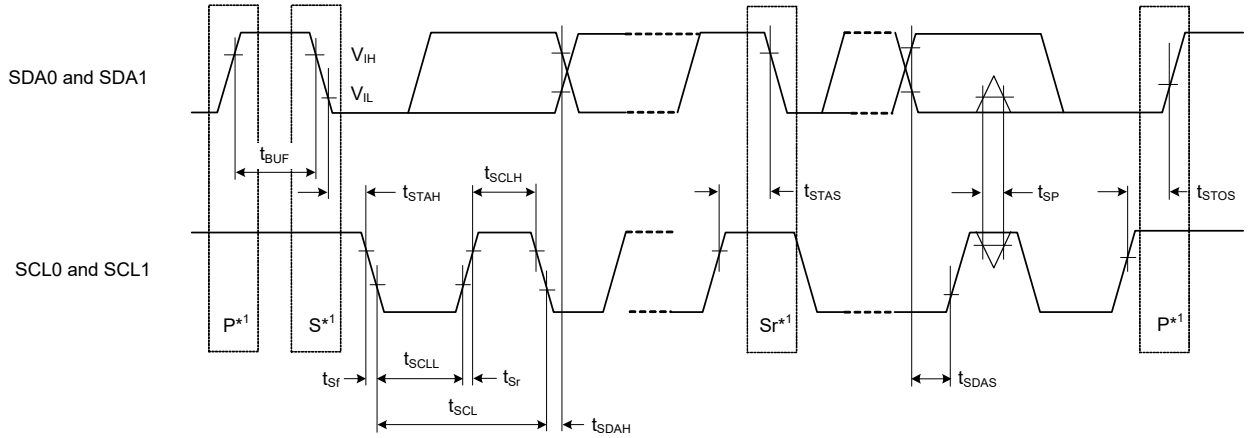
Figure 2.56 SPI timing (slave, CPHA = 1)

2.3.10 IIC Timing

Table 2.35 IIC timing
Conditions: VCC = AVCC0 = AVCC1 = 2.7 to 5.5 V

Parameter		Symbol	Min*1	Max	Unit	Test conditions
IIC (Standard mode, SMBus)	SCL input cycle time	t_{SCL}	6 (12) × t_{IICcyc} + 1300	-	ns	Figure 2.57
	SCL input high pulse width	t_{SCLH}	3 (6) × t_{IICcyc} + 300	-	ns	
	SCL input low pulse width	t_{SCLL}	3 (6) × t_{IICcyc} + 300	-	ns	
	SCL, SDA input rise time	t_{Sr}	-	1000	ns	
	SCL, SDA input fall time	t_{Sf}	-	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA input bus free time (when wakeup function is disabled)	t_{BUF}	3 (6) × t_{IICcyc} + 300	-	ns	
	SDA input bus free time (when wakeup function is enabled)	t_{BUF}	3 (6) × t_{IICcyc} + 4 × t_{Pcyc} + 300	-	ns	
	START condition input hold time (when wakeup function is disabled)	t_{STAH}	t_{IICcyc} + 300	-	ns	
	START condition input hold time (when wakeup function is enabled)	t_{STAH}	1 (5) × t_{IICcyc} + t_{Pcyc} + 300	-	ns	
	Repeated START condition input setup time	t_{STAS}	1000	-	ns	
	STOP condition input setup time	t_{STOS}	1000	-	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	-	ns	
	Data input hold time	t_{SDAH}	0	-	ns	
	SCL, SDA capacitive load	C_b	-	400	pF	
IIC (Fast mode)	SCL input cycle time	t_{SCL}	6 (12) × t_{IICcyc} + 600	-	ns	Figure 2.57
	SCL input high pulse width	t_{SCLH}	3 (6) × t_{IICcyc} + 300	-	ns	
	SCL input low pulse width	t_{SCLL}	3 (6) × t_{IICcyc} + 300	-	ns	
	SCL, SDA input rise time	t_{Sr}	-	300	ns	
	SCL, SDA input fall time	t_{Sf}	-	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA input bus free time (When wakeup function is disabled)	t_{BUF}	3 (6) × t_{IICcyc} + 300	-	ns	
	SDA input bus free time (When wakeup function is enabled)	t_{BUF}	3 (6) × t_{IICcyc} + 4 × t_{Pcyc} + 300	-	ns	
	START condition input hold time (When wakeup function is disabled)	t_{STAH}	t_{IICcyc} + 300	-	ns	
	START condition input hold time (When wakeup function is enabled)	t_{STAH}	1 (5) × t_{IICcyc} + t_{Pcyc} + 300	-	ns	
	Repeated START condition input setup time	t_{STAS}	300	-	ns	
	STOP condition input setup time	t_{STOS}	300	-	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	-	ns	
	Data input hold time	t_{SDAH}	0	-	ns	
	SCL, SDA capacitive load	C_b	-	400	pF	

Note: t_{IICcyc}: IIC internal reference clock (IICφ) cycle, t_{Pcyc}: PCLKB cycle
Note 1. Values in parentheses apply when ICMR3.NF[1:0] is set to 11b while the digital filter is enabled with ICFER.NFE set to 1.



Note 1. S, P, and Sr indicate the following conditions:
S: Start condition
P: Stop condition
Sr: Restart condition

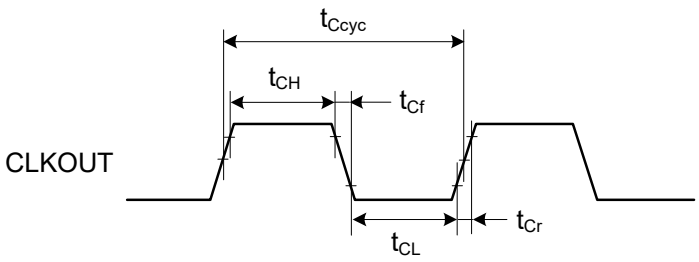
Figure 2.57 I²C bus interface input/output timing

2.3.11 CLKOUT Timing

Table 2.36 CLKOUT timing

Parameter			Symbol	Min	Max	Unit	Test conditions
CLKOUT	CLKOUT pin output cycle*1	2.7 V ≤ VCC ≤ 5.5 V	t_{Ccyc}	62.5	-	ns	Figure 2.58
		1.8 V ≤ VCC < 2.7 V		125	-		
		1.6 V ≤ VCC < 1.8 V		250	-		
	CLKOUT pin high pulse width*2	2.7 V ≤ VCC ≤ 5.5 V	t_{CH}	15	-	ns	
		1.8 V ≤ VCC < 2.7 V		30	-		
		1.6 V ≤ VCC < 1.8 V		150	-		
	CLKOUT pin low pulse width*2	2.7 V ≤ VCC ≤ 5.5 V	t_{CL}	15	-	ns	
		1.8 V ≤ VCC < 2.7 V		30	-		
		1.6 V ≤ VCC < 1.8 V		150	-		
	CLKOUT pin output rise time	2.7 V ≤ VCC ≤ 5.5 V	t_{Cr}	-	12	ns	
		1.8 V ≤ VCC < 2.7 V		-	25		
		1.6 V ≤ VCC < 1.8 V		-	50		
	CLKOUT pin output fall time	2.7 V ≤ VCC ≤ 5.5 V	t_{Cf}	-	12	ns	
		1.8 V ≤ VCC < 2.7 V		-	25		
		1.6 V ≤ VCC < 1.8 V		-	50		

Note 1. When the EXTAL external clock input or an oscillator is used with division by 1 (the CKOCR.CKOSEL[2:0] bits are 011b and the CKOCR.CKODIV[2:0] bits are 000b) to output from CLKOUT, specifications in Table 2.36 should be satisfied with 45% to 55% of input duty cycle.
Note 2. When MOCO is selected as the clock output source (the CKOCR.CKOSEL[2:0] bits are 001b), set the clock output division ratio to be divided by 2 (the CKOCR.CKODIV[2:0] bits are 001b).



Test conditions: V_{OH} = VCC × 0.7, V_{OL} = VCC × 0.3, I_{OH} = -1.0 mA, I_{OL} = 1.0 mA, C = 30 pF

Figure 2.58 CLKOUT output timing

2.4 USB Characteristics

2.4.1 USBFS Timing

Table 2.37 USB characteristics

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = 3.0 to 3.6 V, Ta = -20 to +85°C

Parameter			Symbol	Min	Max	Unit	Test conditions
Input characteristics	Input high level voltage		V_{IH}	2.0	-	V	-
	Input low level voltage		V_{IL}	-	0.8	V	-
	Differential input sensitivity		V_{DI}	0.2	-	V	| USB_DP - USB_DM |
	Differential common mode range		V_{CM}	0.8	2.5	V	-
Output characteristics	Output high level voltage		V_{OH}	2.8	VCC_USB	V	I_{OH} = -200 µA
	Output low level voltage		V_{OL}	0.0	0.3	V	I_{OL} = 2 mA
	Cross-over voltage		V_{CRS}	1.3	2.0	V	Figure 2.59, Figure 2.60, Figure 2.61
	Rise time	FS	t_r	4	20	ns	
		LS		75	300		
	Fall time	FS	t_f	4	20	ns	
		LS		75	300		
	Rise/fall time ratio	FS	t_r/t_f	90	111.11	%	
		LS		80	125		
	Output resistance		Z_{DRV}	28	44	Ω	(Adjusting the resistance of external elements is not required.)
VBUS characteristics	VBUS input voltage		V_{IH}	VCC × 0.8	-	V	-
			V_{IL}	-	VCC × 0.2	V	-
Pull-up, pull-down	Pull-down resistor		R_{PD}	14.25	24.80	kΩ	-
	Pull-up resistor		R_{PUI}	0.9	1.575	kΩ	During idle state
			R_{PUA}	1.425	3.09	kΩ	During reception
Battery charging specification version 1.2	D+ sink current		I_{DP_SINK}	25	175	µA	-
	D- sink current		I_{DM_SINK}	25	175	µA	-
	DCD source current		I_{DP_SRC}	7	13	µA	-
	Data detection voltage		V_{DAT_REF}	0.25	0.4	V	-
	D+ source voltage		V_{DP_SRC}	0.5	0.7	V	Output current = 250 µA
	D- source voltage		V_{DM_SRC}	0.5	0.7	V	Output current = 250 µA

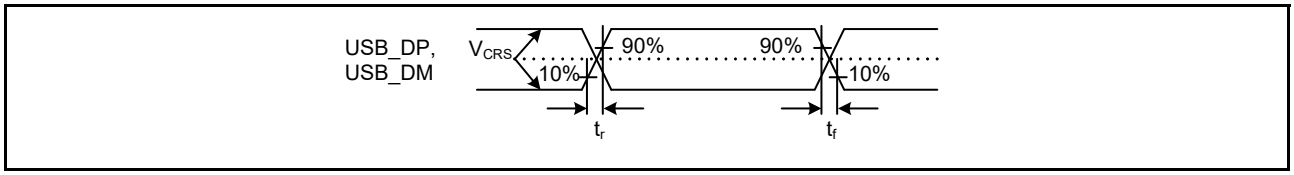


Figure 2.59 USB_DP and USB_DM output timing

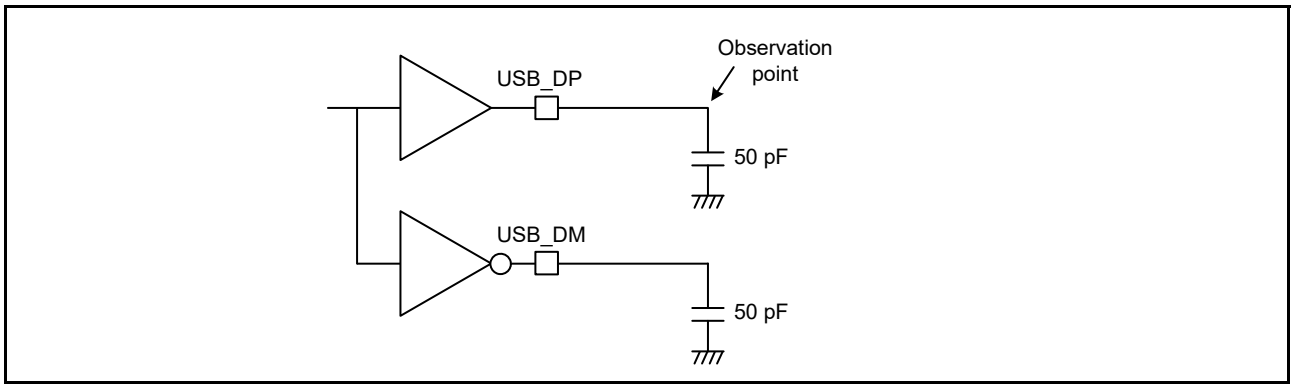


Figure 2.60 Test circuit for Full-Speed (FS) connection

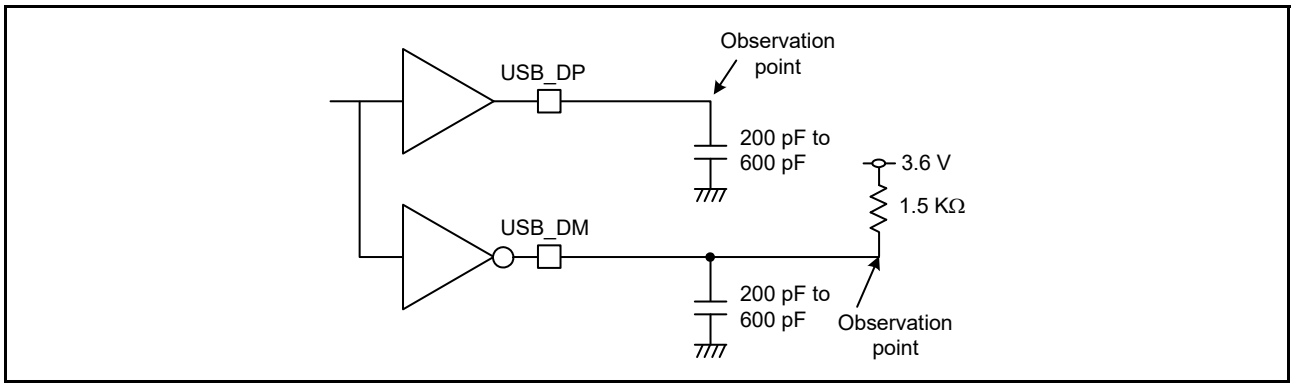


Figure 2.61 Test circuit for Low-Speed (LS) connection

2.4.2 USB External Supply

Table 2.38 USB regulator

Parameter		Min	Typ	Max	Unit	Test conditions
VCC_USB supply current	3.8 V ≤ VCC_USB_LDO < 4.5 V	-	-	50	mA	-
	4.5 V ≤ VCC_USB_LDO ≤ 5.5 V	-	-	100	mA	-
VCC_USB supply voltage		3.0	-	3.6	V	-

2.5 ADC16 Characteristics

Table 2.39 16-bit A/D conversion, power supply, and input range conditions
Conditions: VCC = AVCC0 = AVCC1 = 1.7 to 5.5 V, VREFH0 = 1.7 to 5.5 V, VSS = AVSS0 = AVSS1 = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test conditions
High-potential reference voltage		1.5	3.3	AVCC0	V	-
Low-potential reference voltage		-	AVSS0	-	V	-
Analog input voltage range		0	-	VREFH0	V	-
Input common-mode range	Acm	0	VREFH0/2	VREFH0	V	Differential analog input
Analog input capacitance*2	Cs	-	-	4.3	pF	-
Analog input resistance*1	Rs	-	-	0.7	kΩ	High-precision channel 2.7 V ≤ AVCC0 ≤ 5.5 V
		-	-	1.5		High-precision channel 1.7 V ≤ AVCC0 < 2.7 V
		-	-	2.5		Normal-precision channel 2.7 V ≤ AVCC0 ≤ 5.5 V
		-	-	3.8		Normal-precision channel 1.7 V ≤ AVCC0 < 2.7 V

Note 1. These values are based on simulation. They are not production tested.
Note 2. Except for I/O input capacitance (Cin), see section 2.2.4, I/O VOH, VOL, and Other Characteristics.

Figure 2.62 shows the equivalent circuit for analog input.

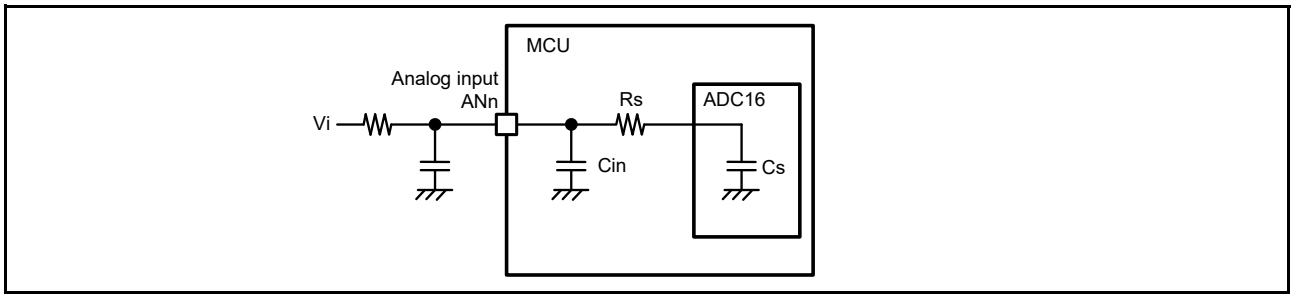


Figure 2.62 Equivalent circuit for analog input

Table 2.40 16-bit A/D conversion, timing parameters (1 of 2)
Conditions: VCC = AVCC0 = AVCC1 = 1.7 to 5.5 V, VREFH0 = 1.7 to 5.5 V, VSS = AVSS0 = AVSS1 = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Frequency	ADCLK	1	-	32	MHz	3.0 V ≤ AVCC0 ≤ 5.5 V, 3.0 V ≤ VREFH0
		1	-	24		2.7 V ≤ AVCC0 ≤ 5.5 V, 2.7 V ≤ VREFH0
		1	-	16		2.4 ≤ AVCC0 ≤ 5.5 V, 1.5 V ≤ VREFH0
		1	-	8		1.8 V ≤ AVCC0 ≤ 5.5 V, 1.5 V ≤ VREFH0
		1	-	4		1.7 V ≤ AVCC0 ≤ 5.5 V, 1.5 V ≤ VREFH0
Conversion rate	Fs	-	-	1 / (t_{SPL} + 18 / ADCLK)	S/s	-

Table 2.40 16-bit A/D conversion, timing parameters (2 of 2)
Conditions: VCC = AVCC0 = AVCC1 = 1.7 to 5.5 V, VREFH0 = 1.7 to 5.5 V, VSS = AVSS0 = AVSS1 = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Sampling time*1	Permissible signal source impedance Max = 0.5 kΩ	tSPL	0.25	-	-	µs	High-precision channel 2.7 V ≤ AVCC0 ≤ 5.5 V
			3	-	-		High-precision channel 1.7 V ≤ AVCC0 < 2.7 V
			3	-	-		Normal-precision channel 2.7 V ≤ AVCC0 ≤ 5.5 V
			10	-	-		Normal-precision channel 1.7 V ≤ AVCC0 < 2.7 V
Settling time*1		tSTART	-	-	1	µs	2.7 V ≤ AVCC0 ≤ 5.5 V
			-	-	3.2		1.8 V ≤ AVCC0 < 2.7 V
			-	-	8.9		1.7 V ≤ AVCC0 < 1.8 V

Note 1. These values are based on simulation. They are not production tested.

Table 2.41 16-bit A/D conversion, linearity parameters
Conditions: VCC = AVCC0 = AVCC1 = 1.7 to 5.5 V, VREFH0 = 1.7 to 5.5 V, VSS = AVSS0 = AVSS1 = VREFL0 = 0 V
External clock input used. Reference voltage range applied to the VREFH0 and VREFL0.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Resolution	-	-	16	-	Bit	-
Integral non-linearity *1	INL	-	± 4	± 8	LSB	2.7 V ≤ AVCC0 ≤ 5.5 V, 2.7 V ≤ VREFH0
		-		± 16		1.7 V ≤ AVCC0 < 2.7 V
Differential non-linearity*1	DNL	-	-1 to +2	-	LSB	-
Offset error*1	Ofst	-	± 4	-	LSB	-
Gain error*1	Gerr	-	-	±0.1	%	2.7 V ≤ VREFH0

Note: The characteristics apply when no pin functions other than 16-bit A/D converter input are used. Offset error, full-scale error, DNL differential non-linearity error, and INL integral non-linearity error do not include quantization errors.
Note 1. These values are based on simulation. They are not production tested.

Table 2.42 16-bit A/D conversion, dynamic parameters (1) (1 of 2)
Conditions: VCC = AVCC0 = AVCC1 = 1.7 to 5.5 V, VREFH0 = 1.7 to 5.5 V, VSS = AVSS0 = AVSS1 = VREFL0 = 0 V
External clock input used. Reference voltage range applied to VREFH0 and VREFL0.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Signal-to-noise and distortion*2	SINAD	67	81	-	dB	Differential input, Fin = 1 kHz, VREFH0 = 1.7 V to 5.5 V, AVCC0 = 1.7 V to 5.5 V
		78	81	-		Differential input, Fin = 1 kHz, VREFH0 = 3.3 V, AVCC0 = 3.3 V
		-	92	-		Differential input, Fin = 1 kHz, VREFH0 = 3.3 V, AVCC0 = 3.3 V, ADADC.ADC[2:0] = 101b
		61	75	-		Single input, Fin = 1 kHz, VREFH0 = 1.7 V to 5.5 V, AVCC0 = 1.7 V to 5.5 V
		72	75	-		Single input, Fin = 1 kHz, VREFH0 = 3.3 V, AVCC0 = 3.3 V

Table 2.42 16-bit A/D conversion, dynamic parameters (1) (2 of 2)

Conditions: VCC = AVCC0 = AVCC1 = 1.7 to 5.5 V, VREFH0 = 1.7 to 5.5 V, VSS = AVSS0 = AVSS1 = VREFL0 = 0 V
External clock input used. Reference voltage range applied to VREFH0 and VREFL0.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Effective number of bits*2	ENOB	11	13.2	-	bit	Differential input, Fin = 1 kHz, VREFH0 = 1.7 V to 5.5 V, AVCC0 = 1.7 V to 5.5 V
		12.7	13.2	-		Differential input, Fin = 1 kHz, VREFH0 = 3.3 V, AVCC0 = 3.3 V
		-	15	-		Differential input, Fin = 1 kHz, VREFH0 = 3.3 V, AVCC0 = 3.3 V, ADADC.ADC[2:0] = 101b
		10	12.2	-		Single input, Fin = 1 kHz, VREFH0 = 1.7 V to 5.5 V, AVCC0 = 1.7 V to 5.5 V
		11.7	12.2	-		Single input, Fin = 1 kHz, VREFH0 = 3.3 V, AVCC0 = 3.3 V
Total harmonic distortion*1, *2	THD	-	-100	-	dB	Differential input, Fin = 1 kHz, AVCC0 = 3.3 V
		-	-90	-		Single input, Fin = 1 kHz, AVCC0 = 3.3 V
Common mode rejection ratio*2	CMRR	-	100	-	dB	Differential input, Acm = 0 to VREFH0 at 1 kHz, AVCC0 = 3.3 V

Note: The characteristics apply when no pin functions other than 16-bit A/D converter input are used.
Note 1. THD = HD2 + HD3 + HD4 + HD5.
Note 2. These values are based on simulation. They are not production tested.

Table 2.43 16-bit A/D conversion, dynamic parameters (2)

Conditions: VCC = AVCC0 = AVCC1 = 1.7 to 5.5 V, VSS = AVSS0 = AVSS1 = VREFL0 = 0 V
External clock input used.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Signal-to-noise and distortion*1	SINAD	-	78.6	-	dB	Differential input, Fin = 1 kHz, AVCC0 = 3.3 V, VREFADC output = 2.5 V
		-	76.6	-		Differential input, Fin = 1 kHz, AVCC0 = 3.3 V, VREFADC output = 2.0 V
		-	74.2	-		Differential input, Fin = 1 kHz, AVCC0 = 3.3 V, VREFADC output = 1.5 V
Effective number of bits*1	ENOB	-	12.8	-	bit	Differential input, Fin = 1 kHz, AVCC0 = 3.3 V, VREFADC output = 2.5 V
		-	12.4	-		Differential input, Fin = 1 kHz, AVCC0 = 3.3 V, VREFADC output = 2.0 V
		-	12.0	-		Differential input, Fin = 1 kHz, AVCC0 = 3.3 V, VREFADC output = 1.5 V

Note: The characteristics apply when no pin functions other than 16-bit A/D converter input are used.
Note 1. These values are based on simulation. They are not production tested.

Table 2.44 16-bit A/D converter channel classification

Classification	Channel	Conditions
High-precision channel	AN000 to AN008	AVCC0 = 1.7 to 5.5 V
Normal-precision channel	AN016 to AN023	
Internal reference voltage input channel	Internal reference voltage	AVCC0 = 2.0 to 5.5 V
Temperature sensor input channel	Temperature sensor output	AVCC0 = 2.0 to 5.5 V

Table 2.45 Internal reference voltage for 16-bit ADC (VREFADC) characteristics
Conditions: VCC = AVCC0 = AVCC1 = 1.7 V to 5.5 V, VSS = AVSS0 = AVSS1 = VREFL0 = 0 V

Parameter	Min	Typ	Max	Unit	Test conditions
Output voltage range	1.41	1.5	1.59	V	VREFAMPCNT.VREFADCG[1:0] = 00b AVCC0 ≥ 1.7 V
	1.88	2	2.12		VREFAMPCNT.VREFADCG[1:0] = 10b AVCC0 ≥ 2.2 V
	2.35	2.5	2.65		VREFAMPCNT.VREFADCG[1:0] = 11b AVCC0 ≥ 2.7 V
BGR stabilization time*2 (after BGR is enabled)	-	-	150	µs	VREFAMPCNT.BGREN = 1
VREF AMP stabilization time*2 (after VREFAMP is enabled)	-	-	1500	µs	VREFAMPCNT.VREFADCEN = 1
Detect over current*2	-	20	40	mA	-
Load capacitance*1	0.75	1	1.25	µF	-

Note 1. Connect capacitors as stabilization capacitance between the VREFH0 and VREFL0 pins when VREFADC is used.
Note 2. These values are based on simulation. They are not production tested.

Table 2.46 A/D internal reference voltage characteristics
Conditions: VCC = AVCC0 = AVCC1 = VREFH0 = 2.0 to 5.5 V*1

Parameter	Min	Typ	Max	Unit	Test conditions
Internal reference voltage input channel*2	1.36	1.43	1.50	V	-
Sampling time*3	5.0	-	-	µs	-

Note 1. The internal reference voltage cannot be selected for input channels when AVCC0 < 2.0 V.
Note 2. The 16-bit A/D internal reference voltage indicates the voltage when the internal reference voltage is input to the 16-bit A/D converter.
Note 3. This is a parameter for ADC16 when the internal reference voltage is selected for an analog input channel in ADC16.

2.6 SDADC24 Characteristics

Table 2.47 Analog inputs characteristics (1 of 2)
Conditions: VCC = AVCC0 = AVCC1 = 2.7 to 5.5 V, VSS = AVSS0 = AVSS1 = 0 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Full-scale range		F_{SR}	-	± 0.8 / G_{TOTAL}	-	V	-
Analog input in differential input mode	Differential input voltage range	V_{ID}	-0.8 / G_{TOTAL}	-	0.8 / G_{TOTAL}	V	V_{ID} = ANSDnP - ANSDnN, or AMP0O - AMP1O (n = 0 to 3), d_{OFR} = 0 mV
	Input voltage range	V_I	0.2	-	1.8	V	V_I = ANSDnP, ANSDnN, AMP0O, or AMP1O (n = 0 to 3)
	Common mode Input voltage range	V_{COM}	0.2 + (|V_{ID}| × G_{SET1}) / 2	1.0	1.8 - (|V_{ID}| × G_{SET1}) / 2	V	d_{OFR} = 0 mV

Table 2.47 Analog inputs characteristics (2 of 2)
Conditions: VCC = AVCC0 = AVCC1 = 2.7 to 5.5 V, VSS = AVSS0 = AVSS1 = 0 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Analog Input in single-ended input mode	Input voltage range*1	V_I	0.2	-	1.8	V	V_I = ANSDnP, ANSDnN, AMP0O, or AMP1O (n = 0 to 3), V_{COM} = 1.0 V, d_{OFR} = 0 mV, G_{SET1} = 1, G_{SET2} = 1, OSR = 256

Note 1. The single-ended input mode supports only d_{OFR} = 0 mV, G_{SET1} = 1, G_{SET2} = 1 and OSR = 256.

Table 2.48 Programmable gain instrumentation amplifier and sigma-delta A/D converter (1)
Conditions: VCC = AVCC0 = AVCC1 = 2.7 to 5.5 V, VSS = AVSS0 = AVSS1 = 0 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Resolution		RES	-	24	-	bits	-
Over sampling frequency	Normal A/D conversion mode	Fos	-	1	-	MHz	-
	Low-power A/D conversion mode		-	0.125	-		
Output data rate		f_{DATA1}	0.48828	-	15.625	ksps	Normal A/D conversion mode
		f_{DATA2}	61.03615	-	1953.125	sps	Low-power A/D conversion mode
Gain Setting range		G_{TOTAL}	1	-	32	V/V	$G_{TOTAL} = G_{SET1} \times G_{SET2}$
1st Gain Setting range		G_{SET1}	-	1, 2, 3, 4, 8	-	V/V	-
2nd Gain Setting range		G_{SET2}	-	1, 2, 4, 8	-	V/V	-
Offset adjust bit range		d_{OFB}	-	5	-	bits	-
Offset adjust range		d_{OFR}	-164.06 / G_{SET1}	-	+164.06 / G_{SET1}	mV	Referred to input
Offset adjust step		d_{OFS}	-	350 / 32 / G_{SET1}	-	mV	Referred to input

Table 2.49 Programmable gain instrumentation amplifier and sigma-delta A/D converter (2)
Conditions: VCC = AVCC0 = AVCC1 = 2.7 to 5.5 V, VSS = AVSS0 = AVSS1 = 0 V
The electrical specifications are applied at differential input mode, external clock input used, F_{OS} = 1 MHz, dOFR = 0 mV, unless otherwise specified.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	
Signal to Noise Ratio*1,*3 V_{ID} = 0 V	SNR	83	86	-	dB	G_{SET1} = 1, G_{SET2} = 1	OSR = 256
		81	84	-	dB	G_{SET1} = 8, G_{SET2} = 4	OSR = 1024
Signal to Noise and Distortion Ratio*1, *2,*3 fin = 50 Hz	SINAD	82	85	-	dB	G_{SET1} = 1, G_{SET2} = 1	OSR = 256
		79	82	-	dB	G_{SET1} = 8, G_{SET2} = 4	OSR = 1024
		74	80	-	dB	G_{SET1} = 1, G_{SET2} = 1	OSR = 256, Single-ended input mode

Note: The characteristics apply when no pin functions other than 24-bit sigma-delta A/D converter input are used.
Note 1. SNR and SINAD are the ratio to Full-Scale Range (FSR) of analog inputs. These do not include the noise of analog inputs.
Note 2. When V_{ID} is equal to ± 0.8 / G_{TOTAL} actually, the digital output may overflow due to Gain Error (E_G), Offset Error (E_{OS}), and so forth. As a result, SINAD is degraded. See Table 33.7 of 24-Bit Sigma-Delta A/D Converter (SDADC24) in User's Manual for the relation between analog input and digital output.
Note 3. Not production tested but is guaranteed by the design and characterization.

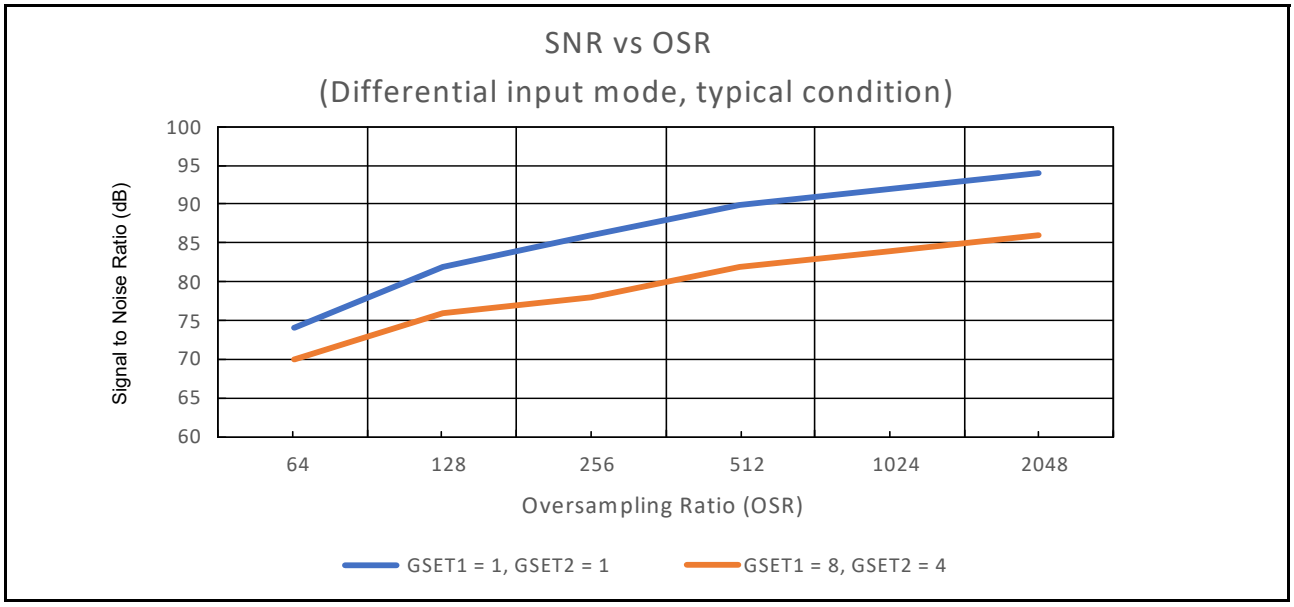


Figure 2.63 SNR vs. OSR (reference data)

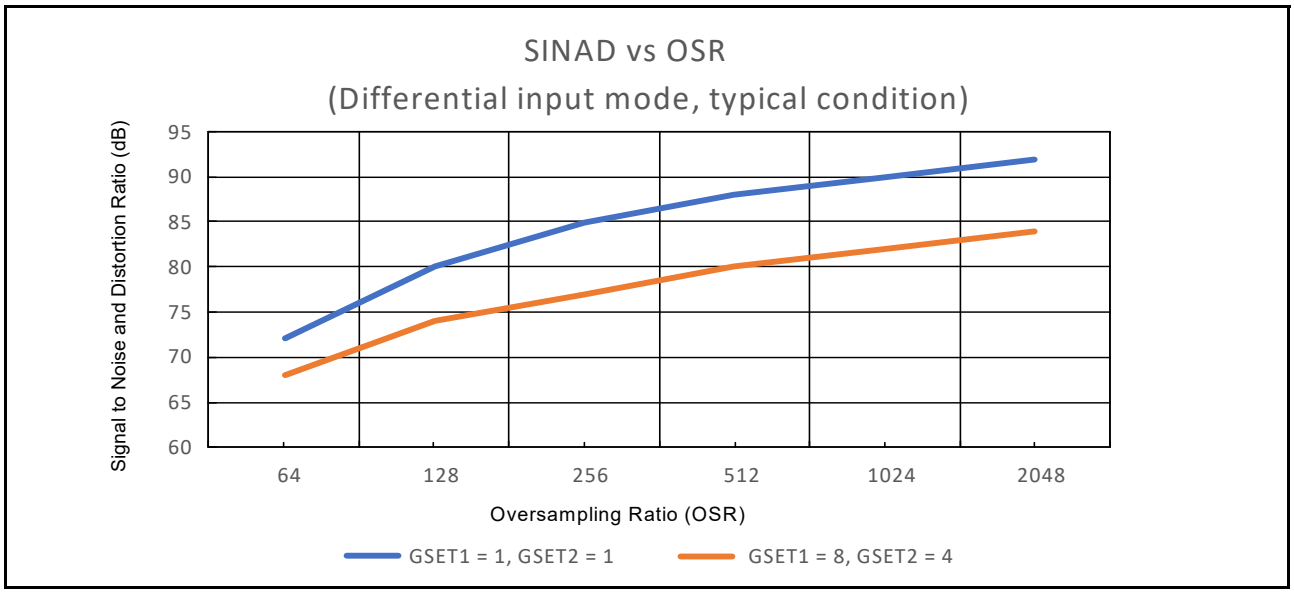


Figure 2.64 SINAD vs. OSR (reference data)

Table 2.50 Programmable gain instrumentation amplifier and sigma-delta A/D converter (3) (1 of 2)

Conditions: VCC = AVCC0 = AVCC1 = 2.7 to 5.5 V, VSS = AVSS0 = AVSS1 = 0 V
The electrical specifications are applied at the differential input mode, with external clock input used, Fos = 1 MHz, OSR = 256, and d_{OFR} = 0 mV, unless otherwise specified.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Gain error*2 (excluding SINC3 frequency response characteristic)	E_G	-0.5	-	0.5	%	After internal calibration, excluding SBIAS error or VREFI error, G_{SET1} = 1, G_{SET2} = 1
		-3	-	3		Single-ended input mode, excluding SBIAS error or VREFI error, G_{SET1} = 1, G_{SET2} = 1

Table 2.50 Programmable gain instrumentation amplifier and sigma-delta A/D converter (3) (2 of 2)
Conditions: VCC = AVCC0 = AVCC1 = 2.7 to 5.5 V, VSS = AVSS0 = AVSS1 = 0 V
The electrical specifications are applied at the differential input mode, with external clock input used, Fos = 1 MHz, OSR = 256, and d_{OFR} = 0 mV, unless otherwise specified.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Gain drift*1, *2	dE_G	-	6	22	ppm/°C	Excluding SBIAS error or VREFI error, G_{SET1} = 1, G_{SET2} = 1
Offset error*2	E_{OS}	-1	-	1	mV	After internal calibration, G_{SET1} = 1, G_{SET2} = 1, referred to input
		-50	-	50		Single-ended input mode, including SBIAS error, G_{SET1} = 1, G_{SET2} = 1, referred to input
Offset drift*1, *2	dE_{OS}	-	2	6	µV/°C	Referred to input
		-	-	120		Single-ended input mode, including SBIAS error, G_{SET1} = 1, G_{SET2} = 1
Integral non-linearity*2	INL	-	15	-	ppm of FSR	Input = DC, OSR = 2048
Common mode Rejection ratio*2	CMRR	-	80	-	dB	V_{COM} = 1.0 ± 0.8 V, f_{in} = 50 Hz, G_{SET1} = 1, G_{SET2} = 1
Power supply Rejection ratio*2	PSRR	-	70	-	dB	AVCC1 = 5.0 V + 0.1 V_{pp_ripple}, f_{in} = 50 Hz, G_{SET1} = 1, G_{SET2} = 1, excluding SBIAS error or VREFI error
Input absolute current*2	I_{IN}	-	2	-	nA	V_I = 1 V
Input offset current*2	I_{INOFR}	-	1	-	nA	V_{ID} = 0 V, V_{COM} = 1 V
Input impedance*2	Z_{IN}	-	500	-	Mohm	V_{ID} = 1 V, V_{COM} = 1 V
Offset adjust gain error*2	d_{OFGE}	-5	-	5	%	Including SBIAS error, d_{OFR} ≠ 0 mV
Offset adjust integral non-linearity*2	dOFINL	-0.5	-	0.5	LSB	d_{OFR} ≠ 0 mV

Note: The characteristics apply when no pin functions other than 24-bit sigma-delta A/D converter input are used.
Note 1. Gain drift is calculated by (Max (EG (T (-40°C) to T (125°C))) - Min (EG (T (-40°C) to T (125°C)))) / (125°C - (-40°C))
Offset drift is calculated by (Max (EOS (T (-40°C) to T (125°C))) - Min (EOS (T (-40°C) to T (125°C)))) / (125°C - (-40°C)).
Note 2. Not production tested but is guaranteed by the design and characterization.

Table 2.51 2.1 V LDO linear regulator for ADC (ADREG) characteristics
Conditions: VCC = AVCC0 = AVCC1 = 2.7 to 5.5 V, VSS = AVSS0 = AVSS1 = 0 V
Connect the ADREG pin to a AVSS1 pin by a 0.47 µF (-50% to +20%) capacitor.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
ADREG output voltage	V_{ADREG}	-	2.1	-	V	-

Table 2.52 ADC external reference voltage (VREFI) characteristics
Conditions: VCC = AVCC0 = AVCC1 = 2.7 to 5.5 V, VSS = AVSS0 = AVSS1 = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
External reference voltage range*1	VREFI	0.8	-	2.4	V	SDADCSTC1.VREFSEL = 1
External reference voltage step	VR_{STEP}	-	0.2	-	V	SDADCSTC1.VREFSEL = 1
External reference voltage accuracy	VR_A	-3	-	3	%	SDADCSTC1.VREFSEL = 1

Note 1. Select the reference voltage input value with STC1.VSBIAS[3:0].

Table 2.53 Sensor bias (SBIAS) characteristics
Conditions: VCC = AVCC0 = AVCC1 = 2.7 to 5.5 V, VSS = AVSS0 = AVSS1 = 0 V
Connect the SBIAS/VREFI pin to a AVSS1 pin by a 0.22 µF (-20% to +20%)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Output voltage range*2	SBIAS	0.8	-	2.2	V	-
Output voltage step	SV_{STEP}	-	0.2	-	V	-
Output voltage accuracy*1	SV_A	-3	-	3	%	SI_{OUT} = 1 mA
Output current*1	SI_{OUT}	-	-	10	mA	-
Short current*1	SI_{SHORT}	-	35	65	mA	SBIAS = 0 V
Load regulation*1	SL_R	-	-	15	mV	1 mA ≤ SI_{OUT} ≤ 5 mA
		-	-	20	mV	1 mA ≤ SI_{OUT} ≤ 10 mA
Power supply rejection ratio*1	SPSRR	-	50	-	dB	AVCC1 = 5.0 V + 0.1 V_{pp_ripple}, f = 100 Hz, SI_{OUT} = 2.5 mA
Transition time of one step*1,*3	ST_{TS}	-	-	80	µs	SBIAS < SV_A ± 3%
						1 mA ≤ SI_{OUT} ≤ SI_{OUT_MAX}

Note 1. Not production tested but is guaranteed by the design and characterization.
Note 2. Select the reference voltage output value for the sensor with STC1.VSBIAS[3:0].
Note 3. The load current of more than 1 mA is required because the output stage of SBIAS is Pch open drain. When the original load current is small, additional external load resistance is required.

2.7 DAC12 Characteristics

Table 2.54 12-bit D/A conversion characteristics
Conditions: VCC = AVCC0 = AVCC1 = 1.7 V to 5.5 V, VREFH = 1.7 V to 5.5 V, VSS = AVSS0 = AVSS1 = VREFL = 0 V

Parameter		Min	Typ	Max	Unit	Test conditions
Resolution		-	-	12	bit	-
Charge pump stabilization time*1		-	-	100	µs	-
SW stabilization time*1		-	-	50	µs	-
Conversion time*1	DAC Ref. = AVCC or VREFH ≥ 2.7 V	-	-	1.0	µs	Cload = 38 pF, @ 1 LSB step Cload = 8 pF, @ full range
	DAC Ref. = AVCC or VREFH < 2.7 V	-	-	1.2		-
Wake-up time*1		-	-	1.0	µs	-
Absolute accuracy		-	-	± 12	LSB	2-MΩ resistive load
DNL differential non-linearity error	DAC Ref. = AVCC or VREFH ≥ 2.7 V	-	-	±1.0	LSB	-
	DAC Ref. = AVCC or VREFH < 2.7 V	-	-	±2.0		-
INL integral non-linearity error		-	-	±7.0	LSB	-
RO output resistance		-	3.5	-	kΩ	-
Load resistance		2	2	-	MΩ	-
Load capacitance	1 LSB step	-	38	-	pF	-
	Full range	-	8	-		-

Note 1. These values are based on simulation. They are not production tested.

2.8 DAC8 Characteristics

Table 2.55 8-bit D/A conversion characteristics (1 of 2)
Conditions: VCC = AVCC0 = AVCC1 = 1.7 V to 5.5 V, VSS = AVSS0 = AVSS1 = 0 V

Parameter	Min	Typ	Max	Unit	Test conditions
Resolution	-	-	8	bit	-
Charge pump stabilization time*1	-	-	100	µs	-

Table 2.55 8-bit D/A conversion characteristics (2 of 2)
Conditions: VCC = AVCC0 = AVCC1 = 1.7 V to 5.5 V, VSS = AVSS0 = AVSS1 = 0 V

Parameter		Min	Typ	Max	Unit	Test conditions
Switch stabilization time*1		-	-	50	µs	-
Conversion time*1	AVCC0 = 2.7 to 5.5 V	-	-	3.0	µs	35-pF capacitive load
	AVCC0 = 1.7 to 2.7 V	-	-	6.0	µs	
Absolute accuracy	AVCC0 = 2.7 to 5.5 V	-	-	± 3.0	LSB	2-MΩ resistive load
	AVCC0 = 1.7 to 2.7 V	-	-	± 3.5		
	AVCC0 = 2.7 to 5.5 V	-	-	± 2.0	LSB	4-MΩ resistive load
	AVCC0 = 1.7 to 2.7 V	-	-	± 2.5		
RO output resistance		-	7.4	-	kΩ	-

Note 1. These values are based on simulation. They are not production tested.

2.9 TSN Characteristics

Table 2.56 TSN characteristics
Conditions: VCC = AVCC0 = AVCC1 = 2.0 to 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Relative accuracy	-	-	± 1.5	-	°C	2.4 V or above
		-	± 2.0	-	°C	Below 2.4 V
Temperature slope	-	-	-3.65	-	mV/°C	-
Output voltage (at 25°C)	-	-	1.05	-	V	VCC = 3.3 V
Temperature sensor start time	t_{START}	-	-	5	µs	-
Sampling time	-	5	-	-	µs	

2.10 OSC Stop Detect Characteristics

Table 2.57 Oscillation stop detection circuit characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Detection time	t_{dr}	-	-	1	ms	Figure 2.65

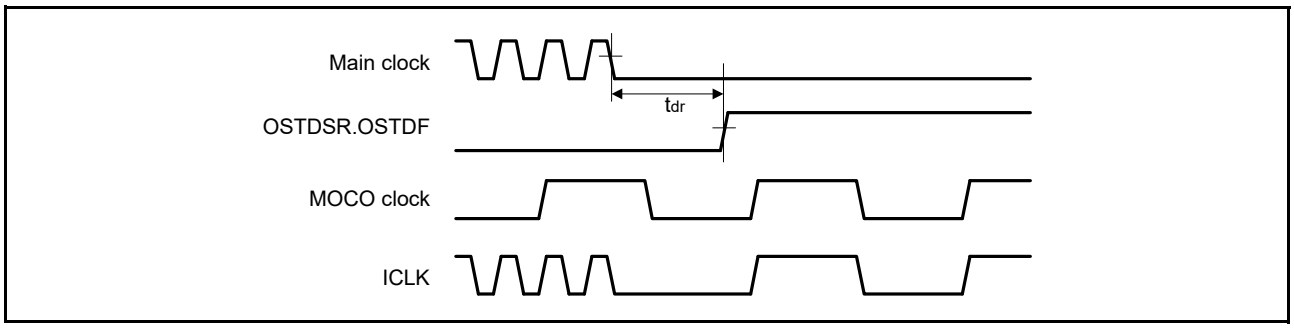


Figure 2.65 Oscillation stop detection timing

2.11 POR and LVD Characteristics

Table 2.58 Power-on reset circuit and voltage detection circuit characteristics (1)

Parameter		Symbol	Min	Typ	Max	Unit	Test Conditions
Voltage detection level*1	Power-on reset (POR)	V_{POR}	1.27	1.42	1.57	V	Figure 2.66, Figure 2.67
	Voltage detection circuit (LVD0)*2	V_{det0_0}	3.68	3.85	4.00	V	Figure 2.68 At falling edge VCC
		V_{det0_1}	2.68	2.85	2.96		
		V_{det0_2}	2.38	2.53	2.64		
		V_{det0_3}	1.78	1.90	2.02		
		V_{det0_4}	1.60	1.69	1.82		
	Voltage detection circuit (LVD1)*3	V_{det1_0}	4.13	4.29	4.45	V	Figure 2.69 At falling edge VCC
		V_{det1_1}	3.98	4.16	4.30		
		V_{det1_2}	3.86	4.03	4.18		
		V_{det1_3}	3.68	3.86	4.00		
		V_{det1_4}	2.98	3.10	3.22		
		V_{det1_5}	2.89	3.00	3.11		
		V_{det1_6}	2.79	2.90	3.01		
		V_{det1_7}	2.68	2.79	2.90		
		V_{det1_8}	2.58	2.68	2.78		
		V_{det1_9}	2.48	2.58	2.68		
		V_{det1_A}	2.38	2.48	2.58		
		V_{det1_B}	2.10	2.20	2.30		
		V_{det1_C}	1.84	1.96	2.05		
		V_{det1_D}	1.74	1.86	1.95		
		V_{det1_E}	1.63	1.75	1.84		
		V_{det1_F}	1.60	1.65	1.73		
	Voltage detection circuit (LVD2)*4	V_{det2_0}	4.11	4.31	4.48	V	Figure 2.70 At falling edge VCC
		V_{det2_1}	3.97	4.17	4.34		
		V_{det2_2}	3.83	4.03	4.20		
		V_{det2_3}	3.64	3.84	4.01		

Note 1. These characteristics apply when noise is not superimposed on the power supply. When a setting causes this voltage detection level to overlap with that of the voltage detection circuit, it cannot be specified whether LVD1 or LVD2 is used for voltage detection.

Note 2. # in the symbol $V_{det0_\#}$ denotes the value of the OFS1.VDSEL1[2:0] bits.

Note 3. # in the symbol $V_{det1_\#}$ denotes the value of the LVDLVLR.LVD1LVL[4:0] bits.

Note 4. # in the symbol $V_{det2_\#}$ denotes the value of the LVDLVLR.LVD2LVL[2:0] bits.

Table 2.59 Power-on reset circuit and voltage detection circuit characteristics (2)

Parameter		Symbol	Min	Typ	Max	Unit	Test Conditions
Wait time after power-on reset cancellation	LVD0: enable	t_{POR}	-	1.7	-	ms	-
	LVD0: disable	t_{POR}	-	1.3	-	ms	-
Wait time after voltage monitor 0,1,2 reset cancellation	LVD0: enable*1	$t_{LVD0,1,2}$	-	0.6	-	ms	-
	LVD0: disable*2	$t_{LVD1,2}$	-	0.2	-	ms	-
Response delay*3		t_{det}	-	-	350	µs	Figure 2.66, Figure 2.67
Minimum VCC down time		t_{VOFF}	450	-	-	µs	Figure 2.66, VCC = 1.0 V or above
Power-on reset enable time		$t_{W (POR)}$	1	-	-	ms	Figure 2.67, VCC = below 1.0 V
LVD operation stabilization time (after LVD is enabled)		$T_{d (E-A)}$	-	-	300	µs	Figure 2.69, Figure 2.70
Hysteresis width (POR)		V_{PORH}	-	110	-	mV	-
Hysteresis width (LVD0, LVD1 and LVD2)		V_{LVH}	-	60	-	mV	LVD0 selected
			-	100	-		V_{det1_0} to V_{det1_2} selected
			-	60	-		V_{det1_3} to V_{det1_9} selected
			-	50	-		V_{det1_A} to V_{det1_B} selected
			-	40	-		V_{det1_C} to V_{det1_F} selected
			-	60	-		LVD2 selected

Note 1. When OFS1.LVDAS = 0.
Note 2. When OFS1.LVDAS = 1.
Note 3. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR}, V_{det0}, V_{det1}, and V_{det2} for the POR/LVD.

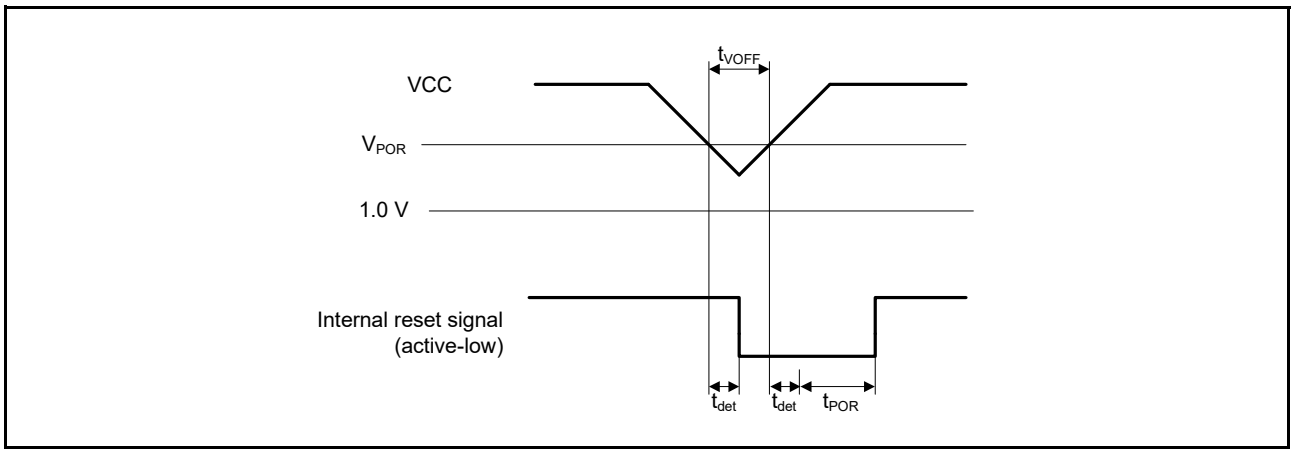
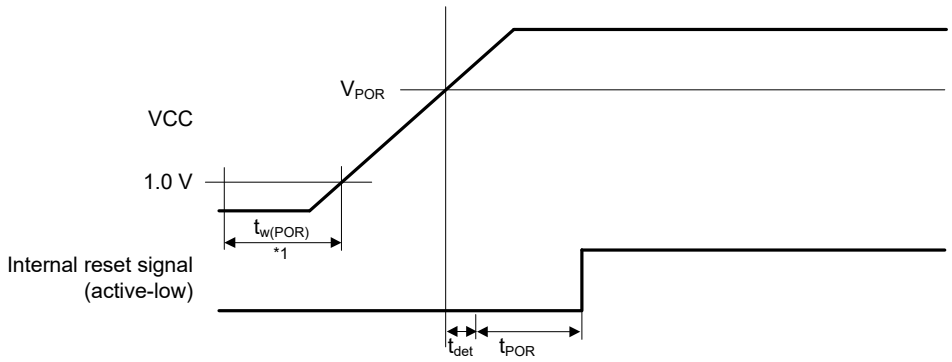


Figure 2.66 Voltage detection reset timing



Note 1. $t_{w(POR)}$ is the time required for a power-on reset to be enabled while the external power VCC is being held below the valid voltage (1.0 V).
When VCC turns on, maintain $t_{w(POR)}$ for 1.0 ms or more.

Figure 2.67 Power-on reset timing

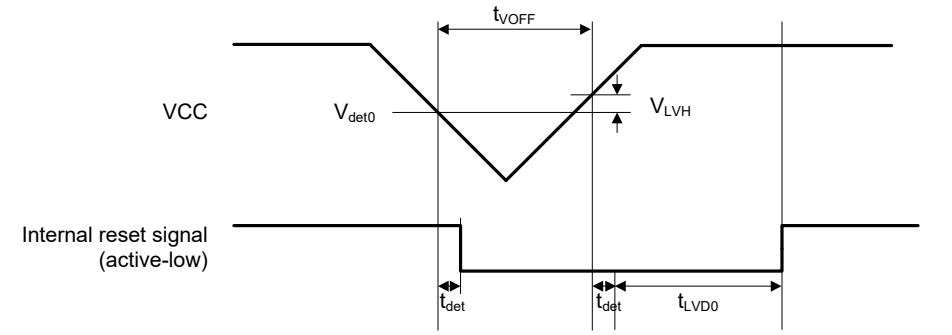


Figure 2.68 Voltage detection circuit timing (V_{det0})

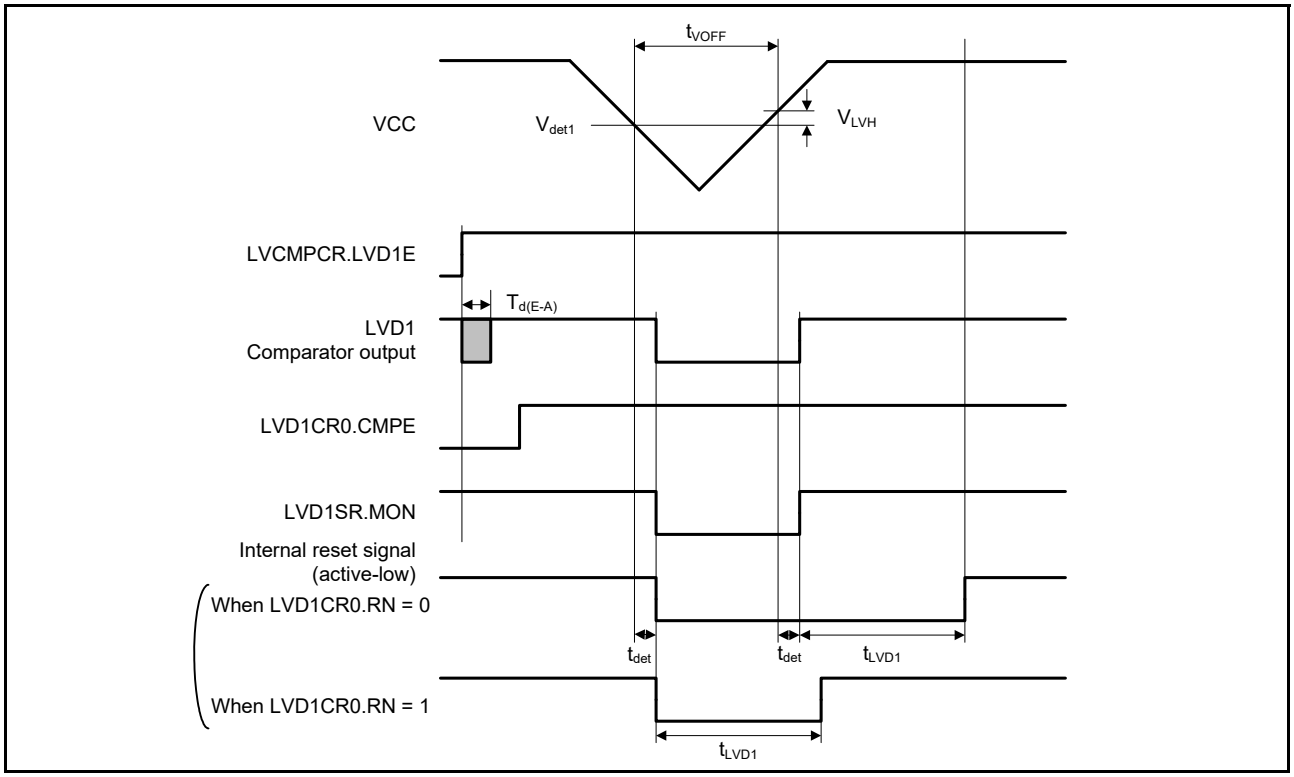


Figure 2.69 Voltage detection circuit timing (V_{det1})

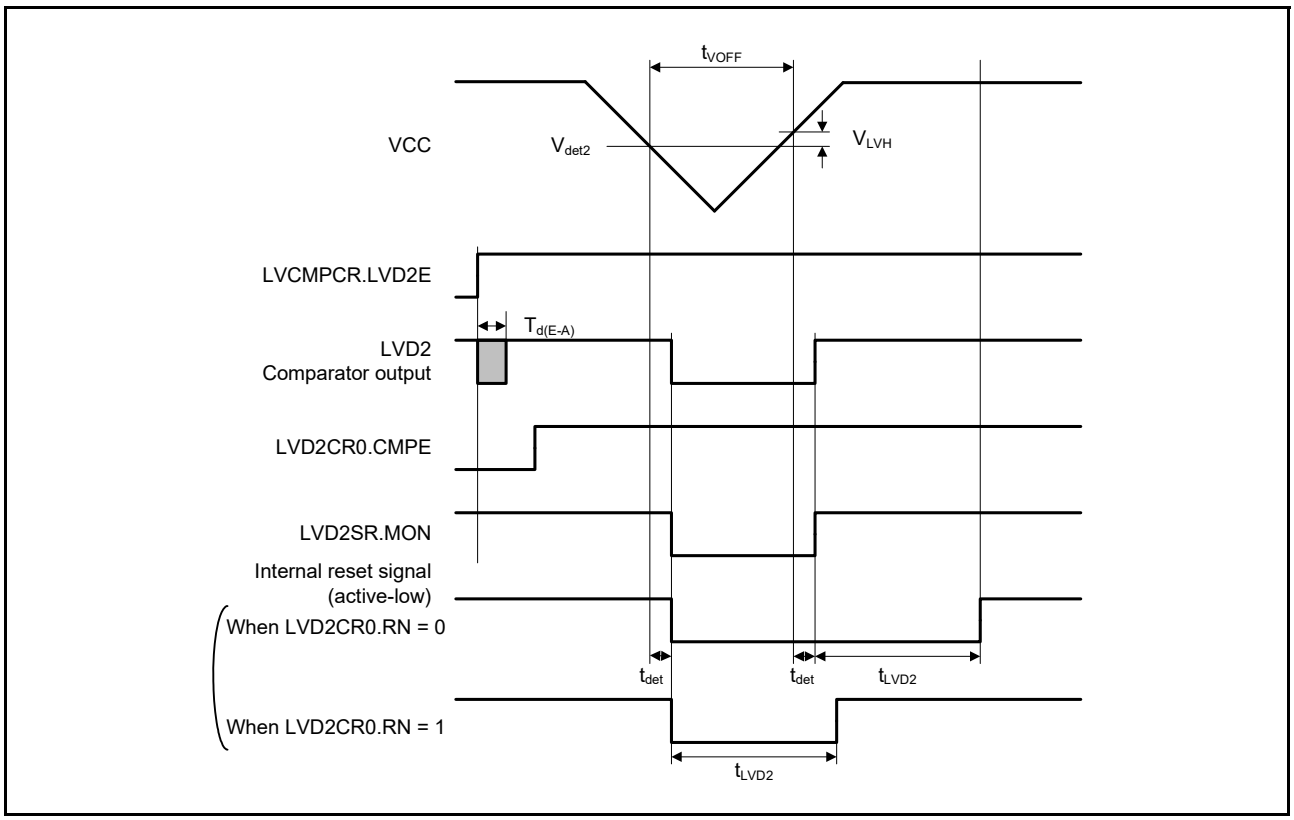


Figure 2.70 Voltage detection circuit timing (V_{det2})

2.12 CTSU Characteristics

Table 2.60 CTSU characteristics
Conditions: VCC = AVCC0 = AVCC1 = 1.8 to 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
External capacitance connected to TSCAP pin	C_{tscap}	9	10	11	nF	-
TS pin capacitive load	C_{base}	-	-	50	pF	-
Permissible output high current	ΣI_{OH}	-	-	-24	mA	When the mutual capacitance method is applied and TS07 to TS14 are not used for transmit channel
		-	-	-14		When the mutual capacitance method is applied and TS07 to TS14 are used for transmit channel

2.13 Comparator Characteristics

Table 2.61 ACMPHS characteristics
Conditions: VCC = AVCC0 = AVCC1 = 2.7 to 5.5 V, VSS = AVSS0 = AVSS1 = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input offset voltage	V_{IOCMP}	-	± 5	± 40	mV	-
Input voltage range	V_{ICPM}	0	-	AVCC0	V	-
Internal reference voltage input*3	Vref	1.36	1.43	1.50	V	AVCC0 ≥ 2.0 V
Input signal cycle	t_{PCMP}	10	-	-	µs	-
Output delay time	T_d	-	50	100	ns	Input amplitude ± 100 mV
Stabilization wait time during input channel switching*1	T_{WAIT}	300	-	-	ns	Input amplitude ± 100 mV
Operation stabilization wait time*2	T_{cmp}	1	-	-	µs	3.3 V ≤ AVCC0 ≤ 5.5 V
		3	-	-	µs	2.7 V ≤ AVCC0 < 3.3 V

Note 1. Period from when the comparator input channel is switched until the switched result reflects in its output.
Note 2. Period from when comparator operation is enabled (CPMCTL.HCMPON = 1) until the comparator satisfies the DC/AC characteristics.
Note 3. The internal reference voltage cannot be selected for input channels when AVCC0 < 2.0 V.

Table 2.62 ACMPLP characteristics
Conditions: VCC = AVCC0 = AVCC1 = 1.8 to 5.5 V, VSS = AVSS0 = AVSS1 = 0 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Input voltage range	IVREF0	V_{REF}	0	-	VCC - 1.4*1	V	-
	IVREF1 (Standard mode)		0	-	VCC - 1.4	V	
	IVREF1 (Window mode)		1.4*1	-	VCC	V	
	IVCMP0, IVCMP1	V_I	0	-	VCC	V	
Internal reference voltage*2		-	1.36	1.43	1.50	V	VCC ≥ 2.0 V
Output delay	Comparator high-speed mode (Standard mode)	T_d	-	-	1.2	µs	VCC = 3.0 V Slew rate of input signal > 50 mV/µs
	Comparator high-speed mode (Window mode)		-	-	2.0	µs	
	Comparator low-speed mode (Standard mode)		-	-	5.0	µs	

Table 2.62 ACMPLP characteristics
Conditions: VCC = AVCC0 = AVCC1 = 1.8 to 5.5 V, VSS = AVSS0 = AVSS1 = 0 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Offset voltage	Comparator high-speed mode (Standard mode)	-	-	-	50	mV	-
	Comparator high-speed mode (Window mode)		-	-	60	mV	
	Comparator low-speed mode (Standard mode)		-	-	40	mV	
Operation stabilization wait time		T_{cmp}	100	-	-	µs	-

Note 1. In window mode, be sure to satisfy the following condition: $V_{IVREF1} - V_{IVREF0} \geq 0.2$ V.
Note 2. The internal reference voltage cannot be selected for input channels when VCC < 2.0 V.

2.14 OPAMP Characteristics

Table 2.63 OPAMP characteristics (1 of 3)
Conditions: VCC = AVCC0 = AVCC1 = 1.7 V to 5.5 V, VSS = AVSS0 = AVSS1 = 0 V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage range	AVCC0	Low power mode	1.7	-	5.5	V
		Middle-speed mode	2.1	-	5.5	V
		High-speed mode	2.4	-	5.5	V
Charge pump stabilization time*1	-	-	-	-	100	µs
SW stabilization time*1	-	-	-	-	50	µs
Input voltage range	V_{icm1}	Low power mode	AVSS0	-	AVCC0	V
	V_{icm2}	Middle-speed mode				
	V_{icm3}	High-speed mode				
Output voltage range	V_{olh1}	Low power mode, Ilode = 100 µA	AVSS0	-	AVCC0	V
	V_{olh2}	Middle-speed mode, Iload = 100 µA				
	V_{olh3}	High-speed mode, Iload = 100 µA				
Input offset trimming range*1	$V_{offadj2l}$	Middle-speed mode, Vin = 0.1 V, Tj = 25°C	-3	-	3	mV
	$V_{offadj2h}$	Middle-speed mode, Vin = AVCC0 - 0.1 V, Tj = 25°C				
	$V_{offadj3l}$	High-speed mode, Vin = 0.1 V, Tj = 25°C				
	$V_{offadj3h}$	High-speed mode, Vin = AVCC0 - 0.1 V, Tj = 25°C				

Table 2.63 OPAMP characteristics (2 of 3)
Conditions: VCC = AVCC0 = AVCC1 = 1.7 V to 5.5 V, VSS = AVSS0 = AVSS1 = 0 V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input offset*1	V_{ioff1a}	Low power mode, Vin < AVCC0 - 1.0 V	-5.0	-	5.0	mV
	V_{ioff1b}	Low power mode, Vin ≥ AVCC0 - 1.0 V	-8.0	-	8.0	
	V_{ioff2a}	Middle-speed mode, Vin < AVCC0 - 1.2 V	-3.0	-	3.0	
	V_{ioff2b}	Middle-speed mode, Vin ≥ AVCC0 - 1.2 V	-3.0	-	3.0	
	V_{ioff3a}	High-speed mode, Vin < AVCC0 - 1.2 V	-2.5	-	2.5	
	V_{ioff3b}	High-speed mode, Vin ≥ AVCC0 - 1.2 V	-2.5	-	2.5	
Offset drift*1	Drift1a	Low power mode, Vin < AVCC0 - 1.0 V	-70	-	70	µV/°C
	Drift1b	Low power mode, Vin ≥ AVCC0 - 1.0 V	-70	-	70	
	Drift2a	Middle-speed mode, Vin < AVCC0 - 1.2 V	-30	-	30	
	Drift2b	Middle-speed mode, Vin ≥ AVCC0 - 1.2 V	-30	-	30	
	Drift3a	High-speed mode, Vin < AVCC0 - 1.2 V	-30	-	30	
	Drift3b	High-speed mode, Vin ≥ AVCC0 - 1.2 V	-30	-	30	
Open gain*1	Av1	Low power mode	70	130	-	dB
	Av2	Middle-speed mode	70	120	-	
	Av3	High-speed mode	60	130	-	
Gain bandwidth product*1	GBW1	Low power mode	-	90	-	kHz
	GBW2	Middle-speed mode	-	2	-	MHz
	GBW3	High-speed mode	-	4.8	-	MHz
Phase margin*1	PM1	Low power mode	35	-	-	deg
	PM2	Middle-speed mode	35	-	-	
	PM3	High-speed mode	35	-	-	
Gain margin*1	GM1	Low power mode	10	-	-	dB
	GM2	Middle-speed mode	10	-	-	
	GM3	High-speed mode	10	-	-	
Input noise density*1	V_{ind11}	Low power mode, f = 10 Hz	-	860	-	nV/√Hz
	V_{ind12}	Low power mode, f = 1 kHz	-	260	-	
	V_{ind21}	Middle-speed mode, f = 1 kHz	-	50	-	
	V_{ind22}	Middle-speed mode, f = 100 kHz	-	30	-	
	V_{ind31}	High-speed mode, f = 1 kHz	-	40	-	
	V_{ind32}	High-speed mode, f = 100 kHz	-	20	-	

Table 2.63 OPAMP characteristics (3 of 3)
Conditions: VCC = AVCC0 = AVCC1 = 1.7 V to 5.5 V, VSS = AVSS0 = AVSS1 = 0 V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Power supply rejection ratio*1	PSRR1	Low power mode	-	90	-	dB
	PSRR2	Middle-speed mode	-	90	-	
	PSRR3	High-speed mode	-	90	-	
Common mode rejection ratio*1	CMRR1	Low power mode	-	90	-	dB
	CMRR2	Middle-speed mode	-	90	-	
	CMRR3	High-speed mode	-	90	-	
Settling time*1	T_{set1}	Low power mode	-	70	200	µS
	T_{set2}	Middle-speed mode	-	2.8	8	
	T_{set3}	High-speed mode	-	1.2	3.2	
Slew rate*1	SR1	Low power mode	0.02	0.05	-	V/µS
	SR2	Middle-speed mode	0.8	1.3	-	
	SR3	High-speed mode	1.8	3.0	-	
Turn on time*1	T_{turn1}	Low power mode, AMPENx = 0 → 1, IREFEN = 0 → 1	-	80	220	µS
	T_{turn2}	Middle-speed mode, AMPENx = 0 → 1, IREFEN = 0 → 1	-	3	10	
	T_{turn3}	High-speed mode, AMPENx = 0 → 1, IREFEN = 0 → 1	-	1.3	4	
Input offset trimming step*1	$V_{ioffst2}$	Middle-speed mode, Vin < AVCC0 - 1.2 V	0.3	0.459	0.58	mV/code
		Middle-speed mode, Vin ≥ AVCC0 - 1.2 V	0.24	-	0.56	
	$V_{ioffst3}$	High-speed mode, Vin < AVCC0 - 1.2 V	0.35	0.52	0.65	
		High-speed mode, Vin ≥ AVCC0 - 1.2 V	0.28	-	0.61	
Wait time after trimming*1	T_{turn_tm2}	Middle-speed mode	-	-	1.5	µS
	T_{turn_tm3}	High-speed mode	-	-	1	
Load current	I_{load}	-	-	-	100	µA
Load capacitance	C_L	-	-	-	20	pF

Note 1. These values are based on simulation. They are not production tested.

2.15 Flash Memory Characteristics

2.15.1 Code Flash Memory Characteristics

Table 2.64 Code flash characteristics (1)

Parameter		Symbol	Min	Typ	Max	Unit	Conditions
Reprogramming/erasure cycle*1		N_{PEC}	1000	-	-	Times	-
Data hold time	After 1000 times N_{PEC}	t_{DRP}	20*2, *3	-	-	Year	T_a = +85°C

Note 1. The reprogram/erase cycle is the number of erasures for each block. When the reprogram/erase cycle is n times (n = 1,000), erasing can be performed n times for each block. For instance, when 4-byte programming is performed 256 times for different addresses in 1-KB blocks, and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasure is not enabled (overwriting is prohibited).
Note 2. Characteristic when using the flash memory programmer and the self-programming library provided by Renesas Electronics.
Note 3. This result is obtained from reliability testing.

Table 2.65 Code flash characteristics (2)

High-speed operating mode

Conditions: VCC = AVCC0 = AVCC1 = 2.7 to 5.5 V

Parameter		Symbol	FCLK = 1 MHz			FCLK = 32 MHz			Unit
			Min	Typ	Max	Min	Typ	Max	
Programming time	8-byte	t_{P8}	-	116	998	-	54	506	µs
Erasure time	2-KB	t_{E2K}	-	9.03	287	-	5.67	222	ms
Blank check time	8-byte	t_{BC8}	-	-	56.8	-	-	16.6	µs
	2-KB	t_{BC2K}	-	-	1899	-	-	140	µs
Erase suspended time		t_{SED}	-	-	22.5	-	-	10.7	µs
Startup area switching setting time		t_{SAS}	-	21.9	585	-	12.1	447	ms
Access window time		t_{AWS}	-	21.9	585	-	12.1	447	ms
OCD/serial programmer ID setting time		t_{OSIS}	-	21.9	585	-	12.1	447	ms
Flash memory mode transition wait time 1		t_{DIS}	2	-	-	2	-	-	µs
Flash memory mode transition wait time 2		t_{MS}	5	-	-	5	-	-	µs

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.

Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.

Note: The frequency accuracy of FCLK must be ± 3.5% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.

Table 2.66 Code flash characteristics (3)

Middle-speed operating mode

Conditions: VCC = AVCC0 = AVCC1 = 1.8 to 5.5 V, Ta = -40 to +85°C

Parameter		Symbol	FCLK = 1 MHz			FCLK = 8 MHz			Unit
			Min	Typ	Max	Min	Typ	Max	
Programming time	8-byte	t_{P8}	-	157	1411	-	101	966	µs
Erasure time	2-KB	t_{E2K}	-	9.10	289	-	6.10	228	ms
Blank check time	8-byte	t_{BC8}	-	-	87.7	-	-	52.5	µs
	2-KB	t_{BC2K}	-	-	1930	-	-	414	µs
Erase suspended time		t_{SED}	-	-	32.7	-	-	21.6	µs
Startup area switching setting time		t_{SAS}	-	22.8	592	-	14.2	465	ms
Access window time		t_{AWS}	-	22.8	592	-	14.2	465	ms
OCD/serial programmer ID setting time		t_{OSIS}	-	22.8	592	-	14.2	465	ms
Flash memory mode transition wait time 1		t_{DIS}	2	-	-	2	-	-	µs
Flash memory mode transition wait time 2		t_{MS}	720	-	-	720	-	-	ns

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.

Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.

Note: The frequency accuracy of FCLK must be ± 3.5% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.

2.15.2 Data Flash Memory Characteristics

Table 2.67 Data flash characteristics (1)

Parameter		Symbol	Min	Typ	Max	Unit	Conditions
Reprogramming/erasure cycle*1		N_{DPEC}	100000	1000000	-	Times	-
Data hold time	After 10000 times of N_{DPEC}	t_{DDRP}	20*2, *3	-	-	Year	Ta = +85°C
	After 100000 times of N_{DPEC}		5*2, *3	-	-	Year	
	After 1000000 times of N_{DPEC}		-	1*2, *3	-	Year	Ta = +25°C

Note 1. The reprogram/erase cycle is the number of erasure for each block. When the reprogram/erase cycle is n times (n = 100,000), erasing can be performed n times for each block. For instance, when 1-byte programming is performed 1,000 times for different addresses in 1-byte blocks, and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasure is not enabled. (overwriting is prohibited.)
Note 2. Characteristics when using the flash memory programmer and the self-programming library provided by Renesas Electronics.
Note 3. These results are obtained from reliability testing.

Table 2.68 Data flash characteristics (2)
High-speed operating mode
Conditions: VCC = AVCC0 = AVCC1 = 2.7 to 5.5 V

Parameter		Symbol	FCLK = 4 MHz			FCLK = 32 MHz			Unit
			Min	Typ	Max	Min	Typ	Max	
Programming time	1-byte	t_{DP1}	-	52.4	463	-	42.1	387	µs
Erasure time	1-KB	t_{DE1K}	-	8.98	286	-	6.42	237	ms
Blank check time	1-byte	t_{DBC1}	-	-	24.3	-	-	16.6	µs
	1-KB	t_{DBC1K}	-	-	1872	-	-	512	µs
Suspended time during erasing		t_{DSED}	-	-	13.0	-	-	10.7	µs
Data flash STOP recovery time		t_{DSTOP}	5	-	-	5	-	-	µs

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of FCLK must be ± 3.5% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.

Table 2.69 Data flash characteristics (3)
Middle-speed operating mode
Conditions: VCC = AVCC0 = AVCC1 = 1.8 to 5.5 V, Ta = -40 to +85°C

Parameter		Symbol	FCLK = 4 MHz			FCLK = 8 MHz			Unit
			Min	Typ	Max	Min	Typ	Max	
Programming time	1-byte	t_{DP1}	-	94.7	886	-	89.3	849	µs
Erasure time	1-KB	t_{DE1K}	-	9.59	299	-	8.29	273	ms
Blank check time	1-byte	t_{DBC1}	-	-	56.2	-	-	52.5	µs
	1-KB	t_{DBC1K}	-	-	2.17	-	-	1.51	ms
Suspended time during erasing		t_{DSED}	-	-	23.0	-	-	21.7	µs
Data flash STOP recovery time		t_{DSTOP}	720	-	-	720	-	-	ns

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of FCLK must be ± 3.5% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.

2.15.3 Serial Wire Debug (SWD)

Table 2.70 SWD characteristics (1) (1 of 2)
Conditions: VCC = AVCC0 = AVCC1 = 2.4 to 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
SWCLK clock cycle time	$t_{SWCKcyc}$	80	-	-	ns	Figure 2.71
SWCLK clock high pulse width	t_{SWCKH}	35	-	-	ns	
SWCLK clock low pulse width	t_{SWCKL}	35	-	-	ns	
SWCLK clock rise time	t_{SWCKr}	-	-	5	ns	
SWCLK clock fall time	t_{SWCKf}	-	-	5	ns	

Table 2.70 SWD characteristics (1) (2 of 2)
Conditions: VCC = AVCC0 = AVCC1 = 2.4 to 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
SWDIO setup time	t_{SWDS}	16	-	-	ns	Figure 2.72
SWDIO hold time	t_{SWDH}	16	-	-	ns	
SWDIO data delay time	t_{SWDD}	2	-	70	ns	

Table 2.71 SWD characteristics (2)
Conditions: VCC = AVCC0 = AVCC1 = 1.6 to 2.4 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
SWCLK clock cycle time	$t_{SWCKcyc}$	250	-	-	ns	Figure 2.71
SWCLK clock high pulse width	t_{SWCKH}	120	-	-	ns	
SWCLK clock low pulse width	t_{SWCKL}	120	-	-	ns	
SWCLK clock rise time	t_{SWCKr}	-	-	5	ns	
SWCLK clock fall time	t_{SWCKf}	-	-	5	ns	
SWDIO setup time	t_{SWDS}	50	-	-	ns	Figure 2.72
SWDIO hold time	t_{SWDH}	50	-	-	ns	
SWDIO data delay time	t_{SWDD}	2	-	150	ns	

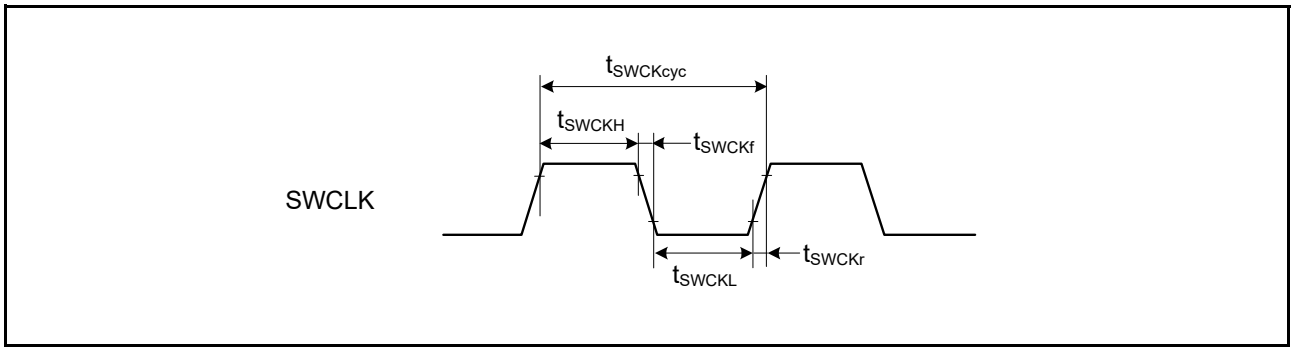


Figure 2.71 SWD SWCLK timing

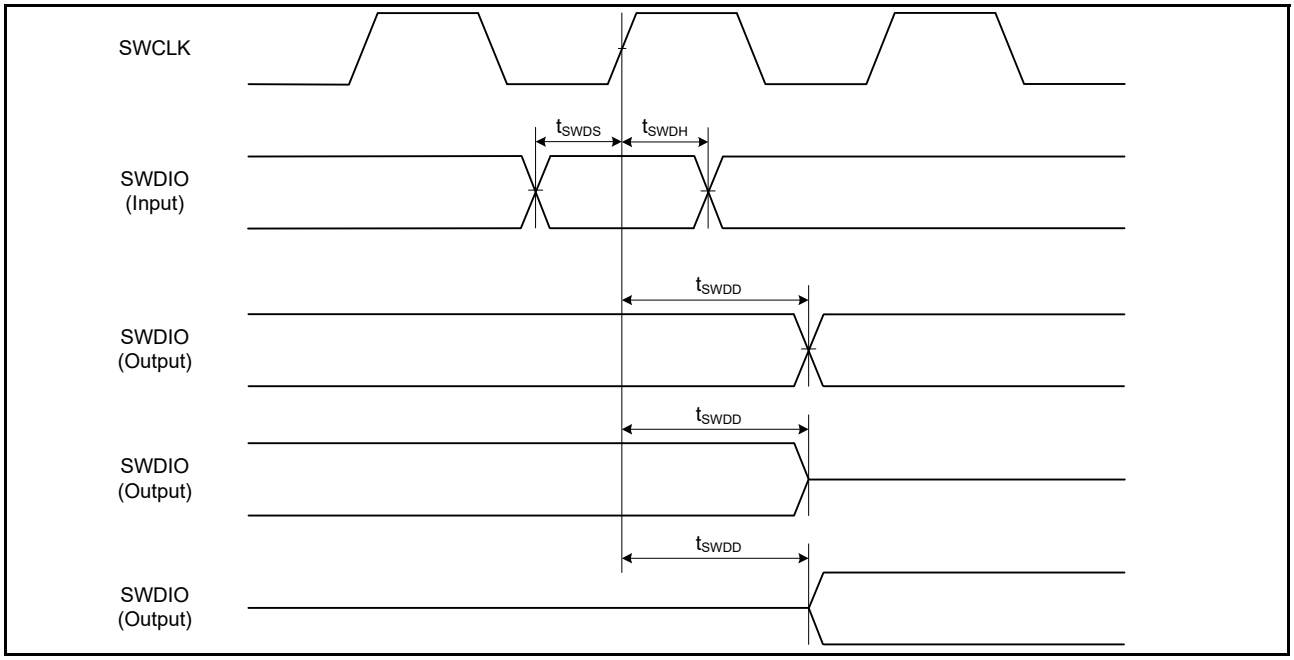


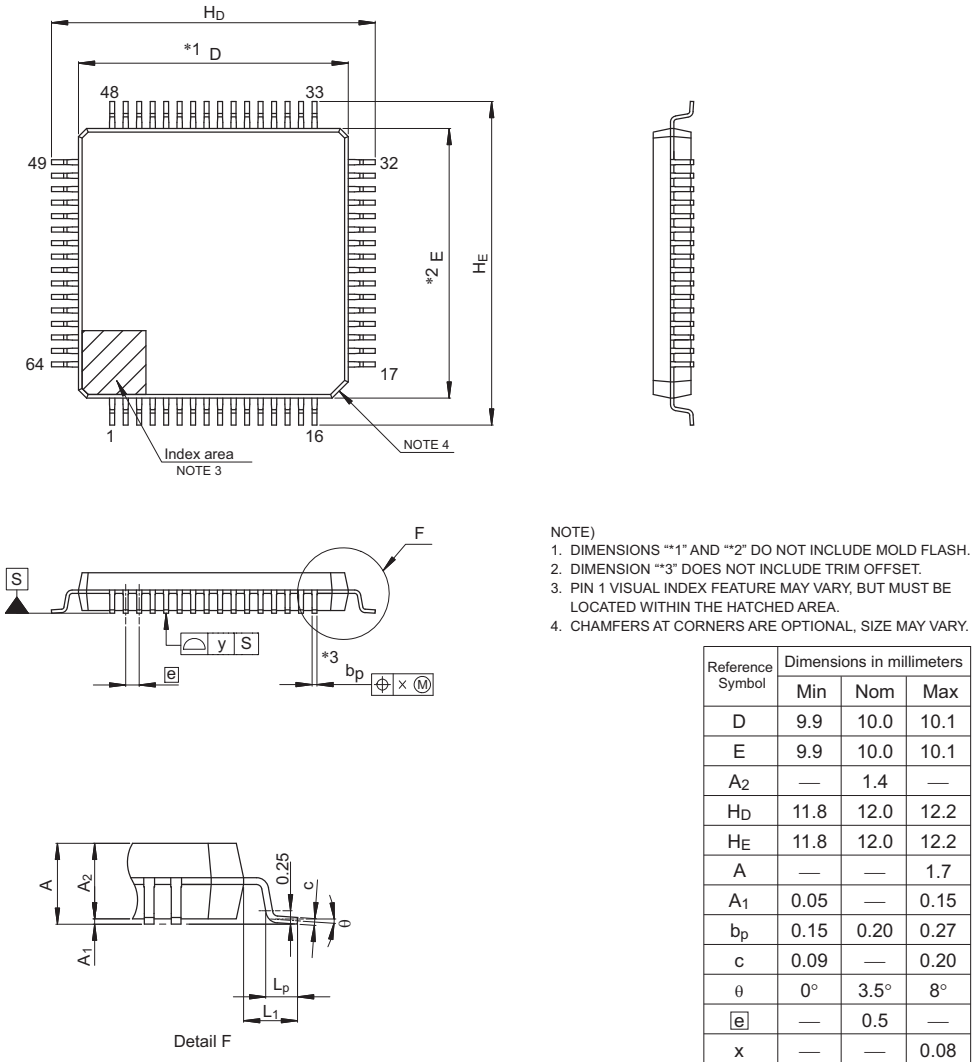
Figure 2.72 SWD input/output timing

Appendix 1.Package Dimensions

Information on the latest version of the package dimensions or mountings is displayed in “Packages” on the Renesas Electronics Corporation website.

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP64-10x10-0.50	PLQP0064KB-C	—	0.3

Unit: mm



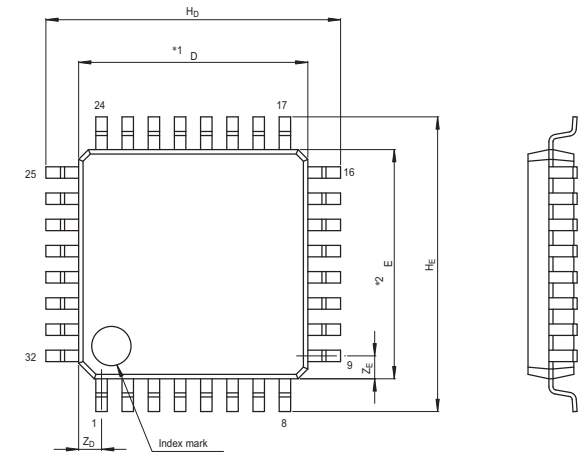
NOTE)
1. DIMENSIONS “*1” AND “*2” DO NOT INCLUDE MOLD FLASH.
2. DIMENSION “*3” DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

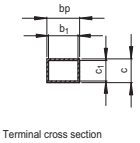
Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A_2	—	1.4	—
H_D	11.8	12.0	12.2
H_E	11.8	12.0	12.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

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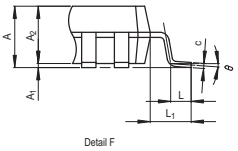
Figure 1.1 LQFP 64-pin

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP32-7x7-0.80	PLQP0032GB-A	32P6U-A	0.2g

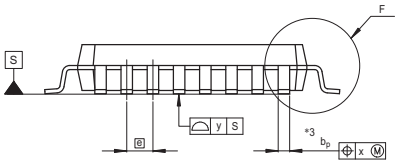




Terminal cross section



Detail F

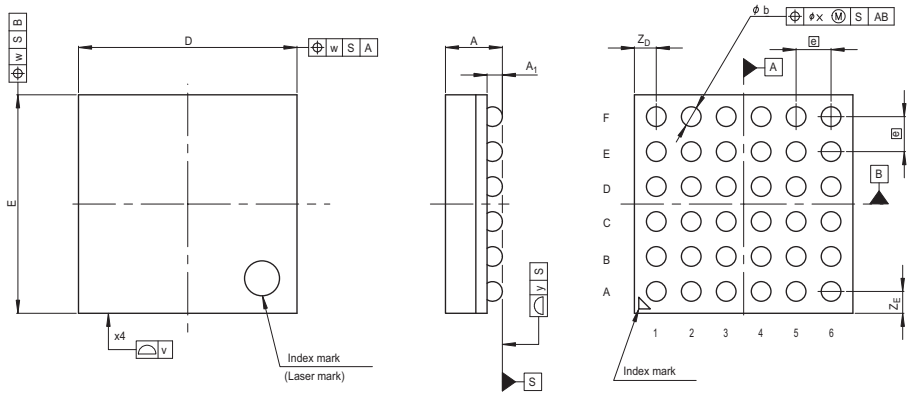


NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.9	7.0	7.1
E	6.9	7.0	7.1
A_2	—	1.4	—
H_D	8.8	9.0	9.2
H_E	8.8	9.0	9.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.32	0.37	0.42
b_1	—	0.35	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.8	—
x	—	—	0.20
y	—	—	0.10
Z_D	—	0.7	—
Z_E	—	0.7	—
L	0.3	0.5	0.7
L_1	—	1.0	—

Figure 1.2 LQFP 32-pin

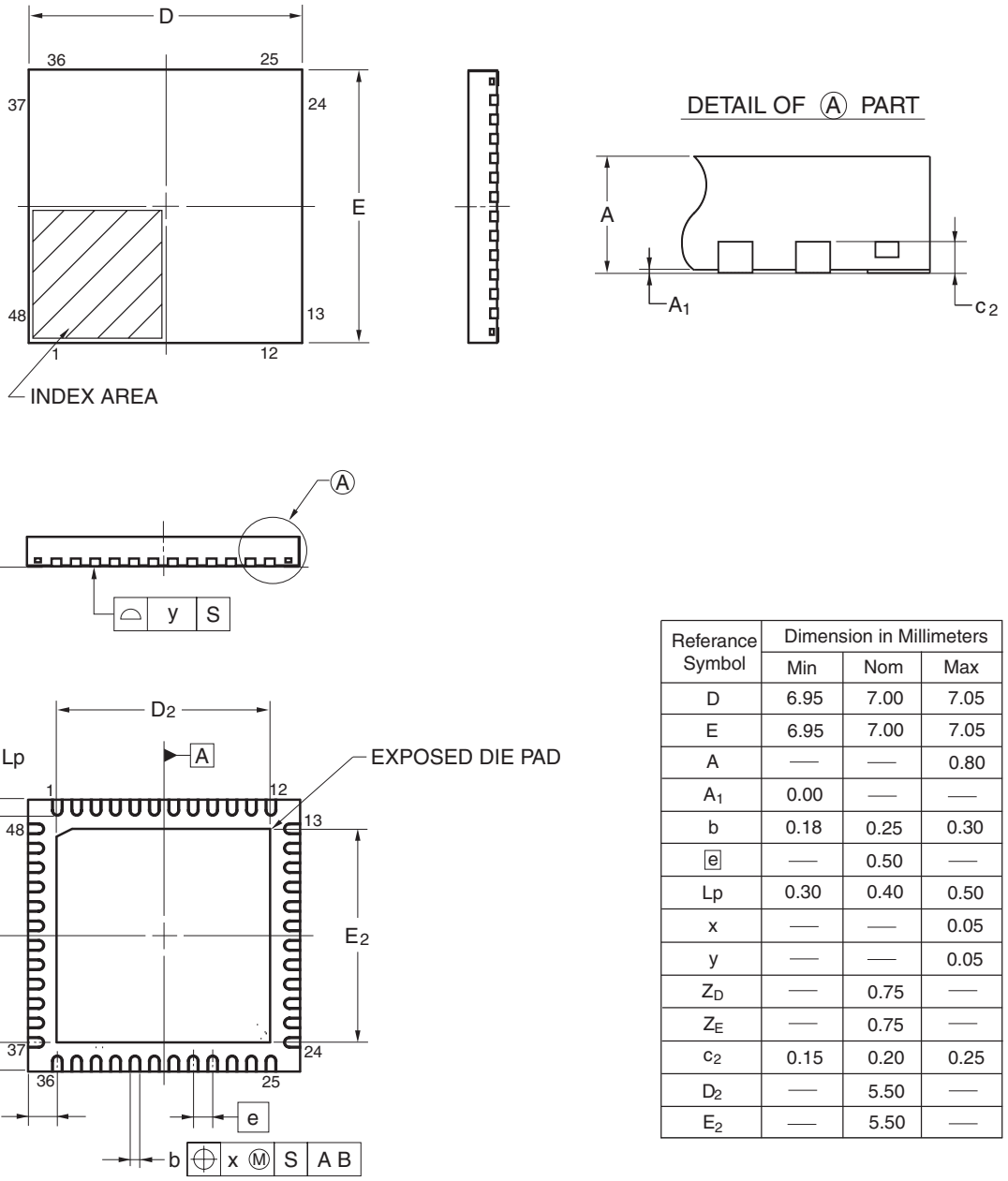
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFBGA36-5x5-0.80	PLBG0036GA-A	36FHE	0.1g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	5.0	—
E	—	5.0	—
v	—	—	0.15
w	—	—	0.20
A	—	—	1.4
A_1	0.3	0.35	0.4
e	—	0.8	—
b	0.4	0.45	0.5
x	—	—	0.08
y	—	—	0.10
Z_D	—	0.5	—
Z_E	—	0.5	—

Figure 1.3 BGA 36-pin

JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-HWQFN48-7x7-0.50	PWQN0048KB-A	48PJN-A P48K8-50-5B4-6	0.13

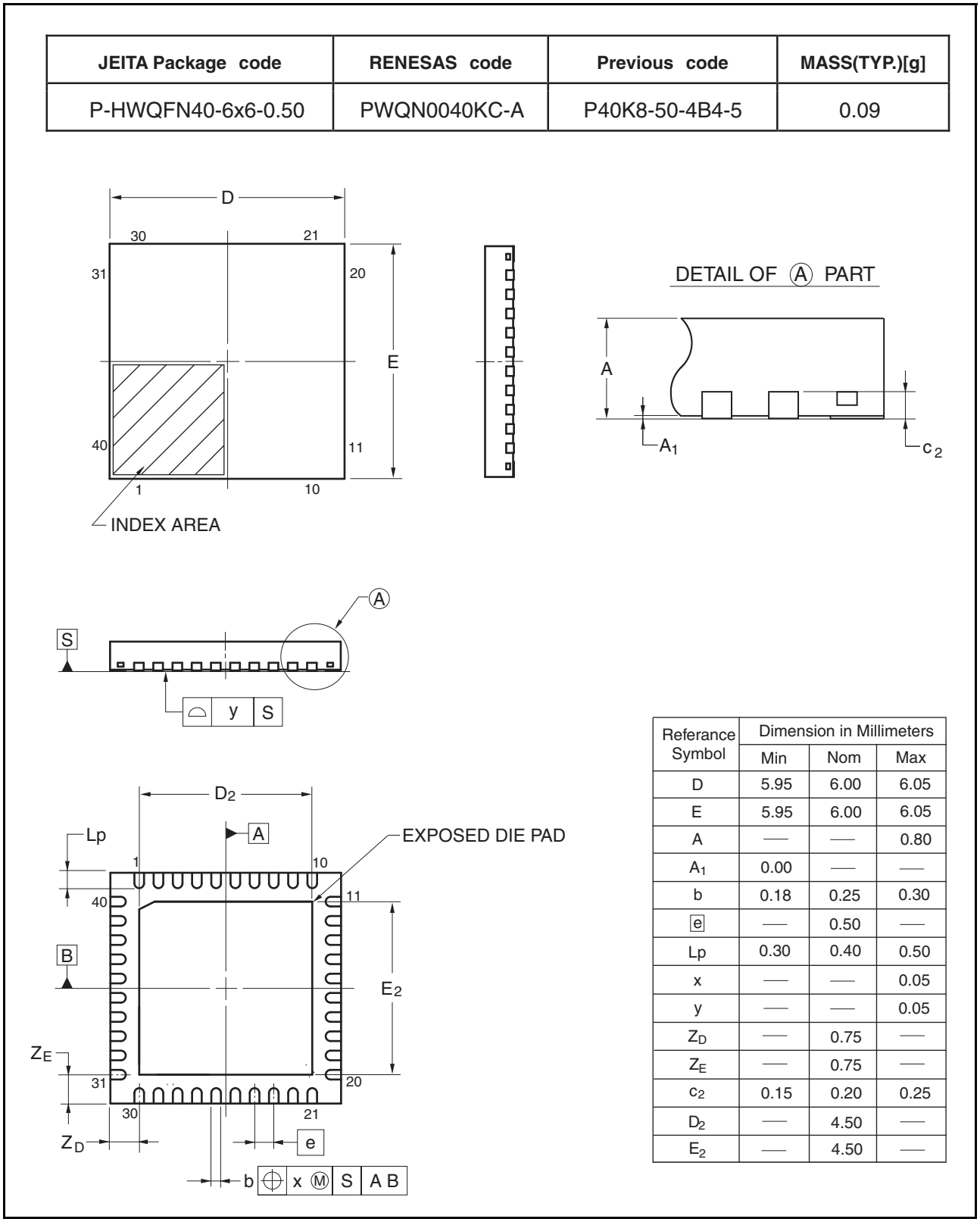


Referance Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.95	7.00	7.05
E	6.95	7.00	7.05
A	—	—	0.80
A_1	0.00	—	—
b	0.18	0.25	0.30
e	—	0.50	—
Lp	0.30	0.40	0.50
x	—	—	0.05
y	—	—	0.05
Z_D	—	0.75	—
Z_E	—	0.75	—
c_2	0.15	0.20	0.25
D_2	—	5.50	—
E_2	—	5.50	—

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Figure 1.4 QFN 48-pin

JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-HWQFN40-6x6-0.50	PWQN0040KC-A	P40K8-50-4B4-5	0.09



Referance Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	5.95	6.00	6.05
E	5.95	6.00	6.05
A	—	—	0.80
A_1	0.00	—	—
b	0.18	0.25	0.30
e	—	0.50	—
Lp	0.30	0.40	0.50
x	—	—	0.05
y	—	—	0.05
Z_D	—	0.75	—
Z_E	—	0.75	—
c_2	0.15	0.20	0.25
D_2	—	4.50	—
E_2	—	4.50	—

Figure 1.5 QFN 40-pin

Revision History	RA2A1 Group Datasheet

Rev.	Date	Summary
1.00	Oct 8, 2019	First release
1.10	Mar 16, 2020	Updated for 1.10

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RA2A1 Microcontroller Group Datasheet

Publication Date: Rev.1.10 Mar 16, 2020

Published by: Renesas Electronics Corporation

General Precautions

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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(Rev.4.0-1 November 2017)

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