RD2-4028

LVDS to DisplayPort Output

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1. Purpose and Scope

This document provides a description of, and set up instructions for, the DisplayPort™ transmitter STDP4028 reference design board [RD2-4028_400-535] targeted for LVDS to DP conversion applications.

2. Description

The STDP4028 is an integrated circuit featuring a four lane DisplayPort transmitter, quad LVDS/LVTTL receiver with I2S, and SPDIF audio inputs for digital Audio-video conversion application. This device also includes SPI interface, I2C Slave (host interface), I2C Master Interface, UART (GProbe) interface, and general-purpose IO pins. The RD2-4028 is a low cost compact four layer board that includes necessary interfaces and features to fully demonstrate the STDP4028 transmitter functionalities.

This reference design meets the following:

1. Stand-alone operation: Includes necessary firmware (either IROM or external SPI) to work independently; this means the intended functionalities are performed without depending on external controller (Host).
2. Slave configuration: Provision to configure the device by an external Host controller through the Host Interface to I2C (most likely when no SPI Flash is used).

2.1. Set Up Instructions

The picture below is a connection diagram showing the RD2-4028 board used for transferring a quad-LVDS video stream from a TV/Monitor SoC and I2S or SPDIF audio stream into a DisplayPort stream. This board uses the standard DisplayPort connector recommended in the DP 1.1a specification to connect the DisplayPort output to an external DisplayPort sink device, such as a monitor.

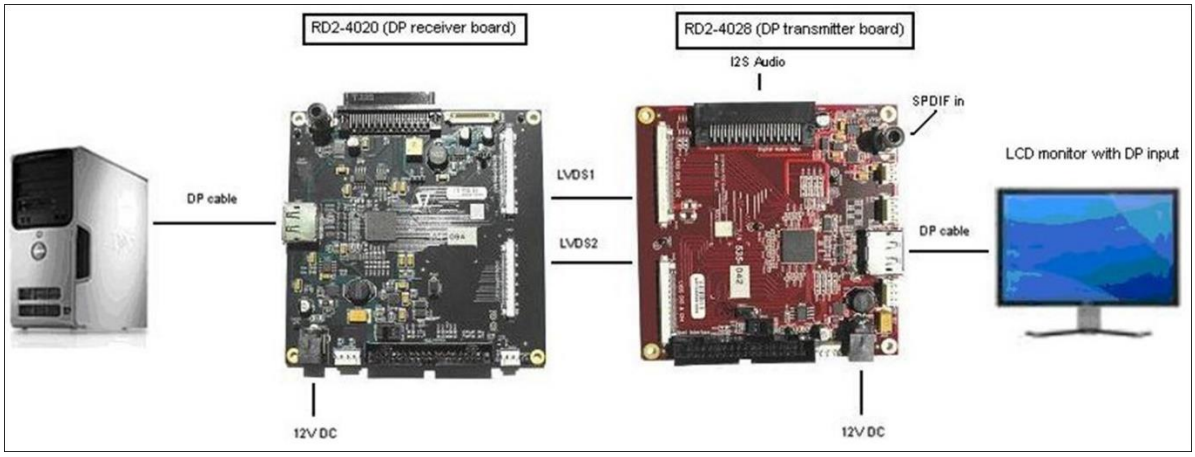


Figure 1. Connection Diagram: Quad-LVDS to DP Stream

Note: The LVDS output is also configurable as dual channel or single channel, depending on the use cases.

1. Connect the Quad LVDS input from an external TV/Monitor SoC to the RD2-4028 reference board using an LVDS cable (typically provided quad/dual channel cable, depending on order type). You can also use the RD2-4020 reference board as the source device for generating QLVDS output (shown in the connection diagram).
2. Connect the DisplayPort output of the RD2-4028 to the external sink device using a DP cable (not provided with board).
3. Connect the 12 V (4A) DC power brick supplied for powering the board. An external digital audio (I2S or SPDIF) source is recommended for testing digital audio conversion by the STDP4028 device into DisplayPort output.
4. Once the connection is established, power ON the RD2-4028 board, source, and sink devices. An image should pop up on the display and you should hear the audio within 5-6 seconds.

Note: The default configuration is quad channel LVDS video input and SPDIF audio in. For dual channel LVDS input, change the bootstrap setting Boot[5] to GND (populate R510 and remove 509). STDP4028 register setting changes are required in order to receive audio on I2S input. This can be done through I2C host configuration or through firmware changes.

The RD2-4028 supports video resolution from 640 x 480 up to 2560 x 1600 and audio up to 8 Ch.

2.1.1. I2C Host Port

Host connector (CN4010) allows configuration of STDP4028 IC from an external host (microcontroller) through conventional I2C interface. User can plug two wires into pin 5 and pin 6 of this connector to access the I2C port of the chip. STDP4028 default device ID is 0xE6/0xE7, but can be changed through bootstrap settings. Refer to the STDP4028 datasheet for further details.

2.1.2. In-System Programming (ISP)

RD2-4028 uses SPI Flash to store the firmware. In case of a new firmware upgrade, the following method can be used.

- ISP through UART connector: Allows programming the SPI Flash through UART (RS232) connector. Requires GProbe board (RS232 converter circuit) and GProbe software tool (contact Kinetic).

2.2. Diagnosis

If the image does not come up, follow the steps below for diagnosis.

Note: The diagnosis requires the Kinetic GProbe software and hardware tool. Contact Kinetic for the GProbe software and board.

1. Install the GProbe diagnostic tool on a computer and set the baud rate to 115,200.
2. Connect GProbe board (not supplied) to the serial port (or USB port if using USB version) of the computer.
3. Connect the other end of the GProbe board to connector (CN902) on the RD2-4028 board using 4-wire cable (part of the GProbe board).

Note: CHECK POLARITY while connecting the cable; Pin 1 is marked on the board. The 4-wire cable connection from CN504 to GProbe board is 1 to 1.

4. Hit the Reset button on the RD2-4028 board (RESET SW901). You will see the firmware version and date of firmware in the GProbe window. This indicates the DP receiver IC is functional. If the message does not appear, reprogram the Flash using the ISP method described in the GProbe user guide.
5. Using an oscilloscope, check the video input and output from the STDP4028.

Note: Refer to the STDP4028 datasheet for pin out descriptions.

3. Board Description

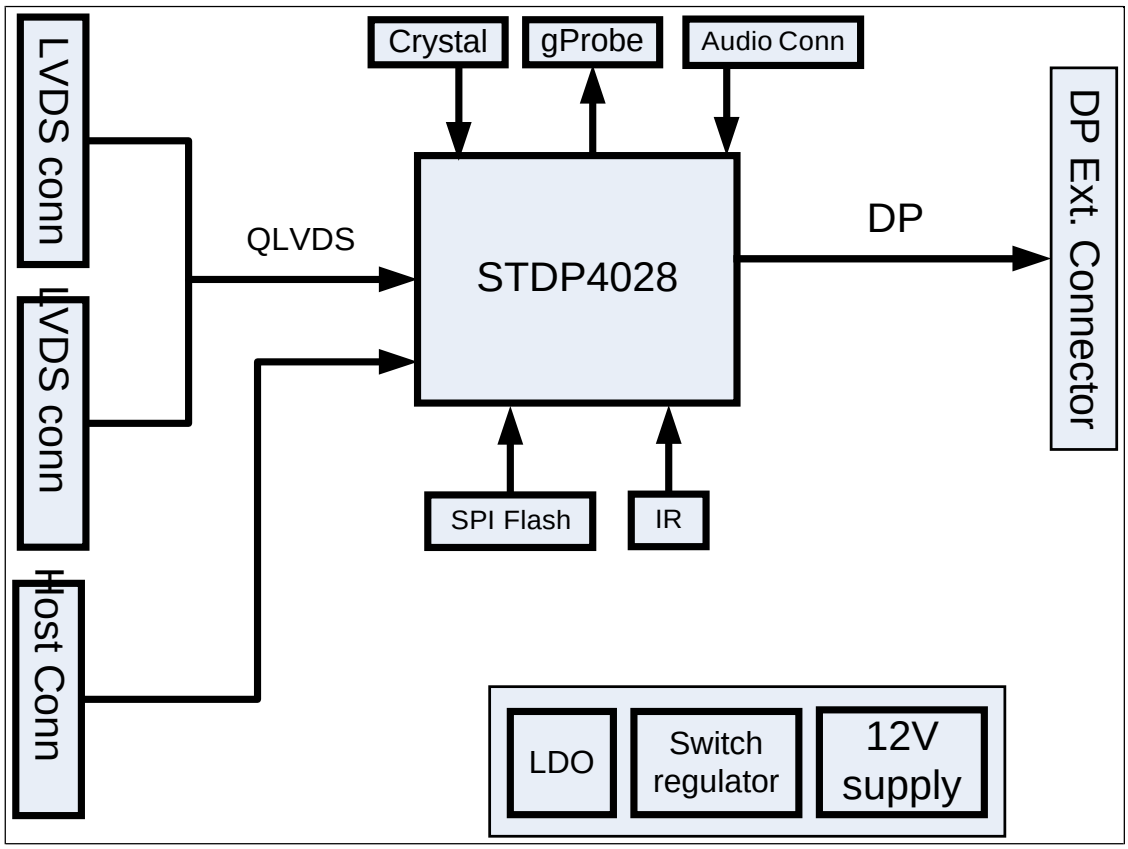


Figure 2. Block Diagram

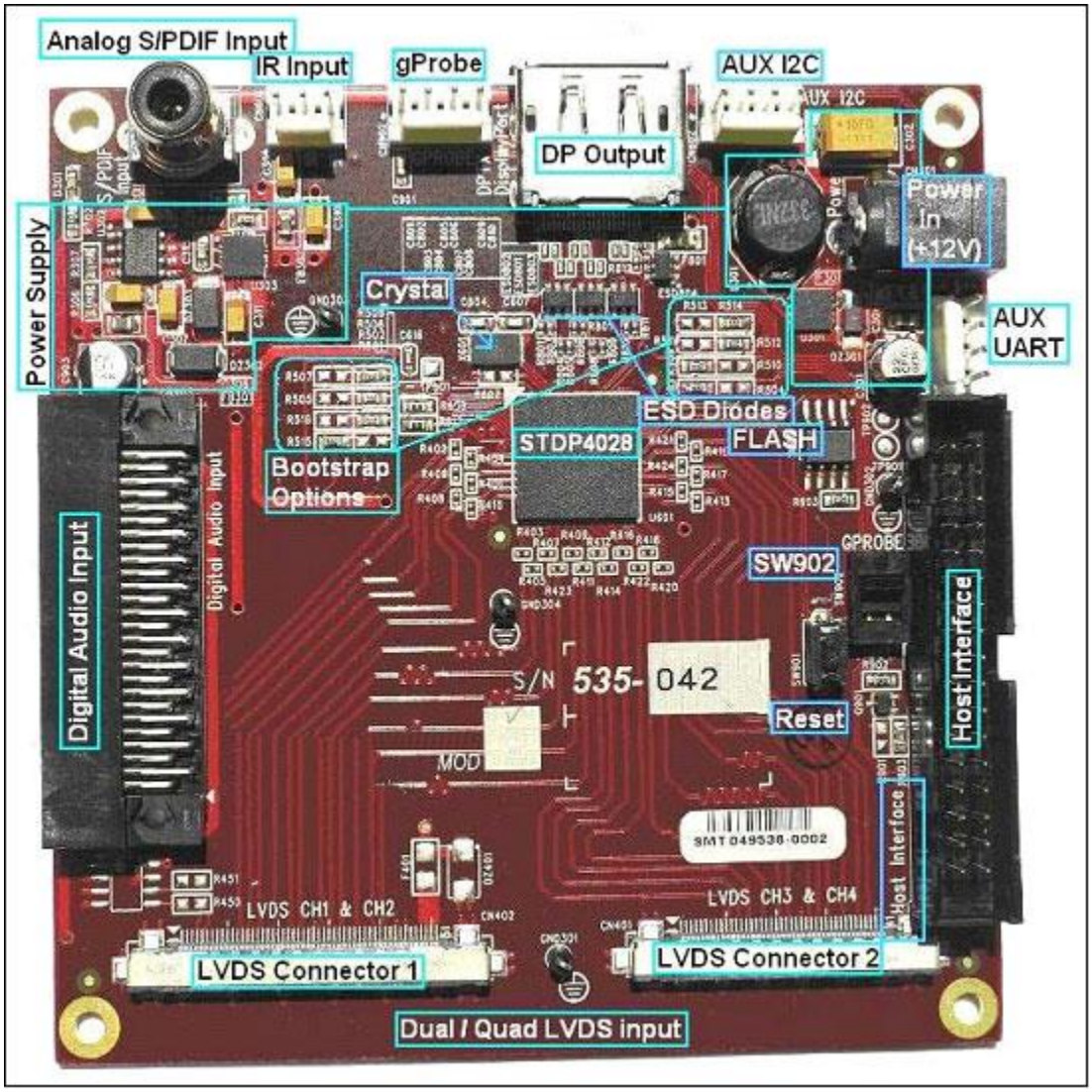


Figure 3. Board Picture

3.1. Principal Components and Functions

Below is a summary of all necessary connectors, switches, and other components. Please refer to the latest board schematics for further details.

Table 3.1-1. Principal Components and Functions

Label	Description	RefDes
Power Input (+12V)	Input 12 V, down conversion to 5 V, 3.3 V, and 1.2 V. This board uses a switch regulator for 5 V and an LDO [**low- dropout**] for 3.3 V and 1.2 V. Note the analog and digital supplies (3.3A and 3.3D or 1.2A and 1.2D) are isolated using ferrite beads.	CN301
STDP4028	The STDP4028 is capable of receiving and converting Quad/Dual/Single LVDS video and I2S (or SPDIF) audio input into a DisplayPort output. This device offers LVDS input interface configurable to map a wide range of display controller products. The Quad LVDS interface supports video signals up to 400 MHz pixel rate with flexible channel and lane swapping options.	U601
DP Output	DisplayPort output connector	CN801
Flash	The board includes an SPI Flash of 2 MB to hold the firmware. The SPI Flash can be programmed (ISP) through UART interface.	U602
Quad LVDS Input	LVDS input connectors can be used as Quad, Dual LVDS inputs. Connector1: 402 (51 pin), Connector2: 401 (41 pin)	CN401 CN402
Digital Audio Input	The I2S (8 channel) or S/PDIF (single wire, 3.3V) audio input signals from the external audio Codec card are received by CN903.	CN903
S/PDIF Input	Standard S/PDIF input connector.	CN904
Host Interface	Host Interface (I2C): This board includes a provision to access the STDP4028 device from an external host controller through the Host Interface (I2C port) connection.	CN901
GProbe	GProbe Interface (+3.3V logic): The board also includes a GProbe connector that connects to the STDP4028 UART port for communication with external PC sources for debug purposes. The Kinetic GProbe tool (software) and PC serial port interface board together create a debug environment for device debug and firmware update. The GProbe interface is also used for ISP purposes.	CN902
Reset	Reset Button, when pressed, triggers a system master reset through the internal reset circuitry. The reset button is used for system reset and debug purposes and is not required for production board design as the STDP4028 produces an internal reset during power ON.	SW901
IR Input	An IR connector for interfacing the IR receiver.	CN601
AUX_I2C	I2C over AUX/ I2C Slave	CN602
AUX_UART	UART over AUX	CN603
LED	Single LED for indicating the power on status.	D301
Crystal	An external crystal of 27 MHz. The design makes use of internal oscillator circuitry.	X601
ESD Diodes	ESD protection diodes for DisplayPort signal (main lanes, AUX and HPD line). The board implements low cost ESD diodes.	ESD801 ESD802 ESD803 ESD804
SW902	Switches UART between Host Interface & GProbe Interface (see mark on PCB).	SW902
Bootstrap Options	The bootstrap options can be configured for: IROM/SPI Flash Dual/Quad LVDS Input Refer to the datasheet for more details.	R503 R504 R509 R510

3.2. Connector Descriptions

The RD2-4028 has the following connectors. The locations of these connectors are shown in the board picture in Figure 3.

CN301 – +12V DC 4A Power Input Jack

CN902 – GProbe Interface (4x1 pin keyed header) connects to the UART port of the STDP4028. Use the Kinetic GProbe board and interface cable for connecting the board to an external PC that has GProbe software running.

Pin 1	+5V
Pin 2	GPROBE_TX
Pin 3	GPROBE_RX
Pin 4	GND

CN901 – I2C Host Interface (header 17X2) connector for connecting external host. This is used only when an external host controller accesses the DisplayPort Transmitter; not used for normal operation. In normal operation, internal MCU controls the overall functioning of the DisplayPort Transmitter (refer to the schematics for complete pin description for the Host Interface).

Pin 1	+5V
Pin 2	+5V
Pin 3 & 4	GND
Pin 5	AUX_I2C_SCL
Pin 6	AUX_I2C_SDA
Pin 7	HOST_TX
Pin 8	HOST_RX
Pin 9	RESET from Host
Pin 10	NC
Pin 11 & 12	GND
Pin 13	AUX_UART_TX
Pin 14	AUX_UART_RX
Pin 15	I2C_SCL
Pin 16	I2C_SDA
Pin 17 & 18	NC
Pin 19 & 20	GND
Pin 21 & 22	NC
Pin 23	IRQ/BOOT7
Pin 24	IR_IN
Pin 25 & 26	NC
Pin 27 & 28	GND
Pin 29	GPIO_3/BOOT6
Pin 30	GPIO_0/BOOT3
Pin 31	TP901
Pin 32	GPIO_1/BOOT2
Pin 33	TP902
Pin 34	GPIO_2/BOOT5

CN801– DisplayPort Transmitter MOLEX47272-0002 connector and pin out details.

Pin 1	ML_Lane 0(p)
Pin 2	GND
Pin 3	ML_Lane 0 (n)
Pin 4	ML_Lane 1 (p)
Pin 5	GND
Pin 6	ML_Lane 1 (n)
Pin 7	ML_Lane 2 (p)
Pin 8	GND
Pin 9	ML_Lane 2 (n)
Pin 10	ML_Lane 3 (p)
Pin 11	GND
Pin 12	ML_Lane 3 (n)
Pin 13	GND
Pin 14	GND
Pin 15	AUX_CH (p)
Pin 16	GND
Pin 17	AUX_CH (n)
Pin 18	Hot Plug Detect
Pin 19	Return (GND)
Pin 20	DP_PWR

CN401 & CN402 – LVDS input (refer to the schematics for LVDS connectors pin out description).

CN401 [LVDS Connector2]

Pin 1 through 8	NC
Pin 9	GND
Pin 10	LVDS_31N
Pin 11	LVDS_31P
Pin 12	LVDS_32N
Pin 13	LVDS_32P
Pin 14	LVDS_33N
Pin 15	LVDS_33P
Pin 16	GND
Pin 17	LVDS_CLK3N
Pin 18	LVDS_CLK3P
Pin 19	GND
Pin 20	LVDS_34N
Pin 21	LVDS_34P
Pin 22	LVDS_35N
Pin 23	LVDS_35P
Pin 24	GND
Pin 25	GND
Pin 26	LVDS_41N
Pin 27	LVDS_41P
Pin 28	LVDS_42N
Pin 29	LVDS_42P
Pin 30	LVDS_43N
Pin 31	LVDS_43P
Pin 32	GND
Pin 33	LVDS_CLK4N
Pin 34	LVDS_CLK4P
Pin 35	GND
Pin 36	LVDS_44N
Pin 37	LVDS_44P
Pin 38	LVDS_45N
Pin 39	LVDS_45P
Pin 40 & 41	GND

CN402 [LVDS Connector1]

Pin 1	GND
Pin 2 & 3	NC
Pin 4	DNP/LVDS_DDC_SDA
Pin 5	DNP/LVDS_DDC_SCL
Pin 6 through 10	NC
Pin 11	GND
Pin 12	LVDS_11N
Pin 13	LVDS_11P
Pin 14	LVDS_12N
Pin 15	LVDS_12P
Pin 16	LVDS_13N
Pin 17	LVDS_13P
Pin 18	GND
Pin 19	LVDS_CLK1N
Pin 20	LVDS_CLK1P
Pin 21	GND
Pin 22	LVDS_14N
Pin 23	LVDS_14P
Pin 24	LVDS_15N
Pin 25	LVDS_15P
Pin 26 & 27	GND
Pin 28	LVDS_21N
Pin 29	LVDS_21P
Pin 30	LVDS_22N
Pin 31	LVDS_22P
Pin 32	LVDS_23N
Pin 33	LVDS_23P
Pin 34	GND
Pin 35	LVDS_CLK2N
Pin 36	LVDS_CLK2P
Pin 37	GND
Pin 38	LVDS_24N
Pin 39	LVDS_24P
Pin 40	LVDS_25N
Pin 41	LVDS_25P
Pin 42 through 46	GND
Pin 47	NC
Pin 48	+12V
Pin 49	+12V
Pin 50	+12V
Pin 51	+12V

LVDS input configuration table

Quad LVDS input	CN402	CN401
Dual LVDS input	CN402	NC

CN904 – SPDIF Input connector.

Pin 1	GND
Pin 2	I2S_0
Pin 3	GND

CN903 – I2S Digital Audio Input (52 pin) connector.

Pin A1	NC
Pin A2 & A3	GND
Pin A4 through A6	NC
Pin A7	GND
Pin A8 & A9	NC
Pin A10	I2S_3
Pin A11	I2S_2
Pin A12	I2S_1
Pin A13	NC
Pin A14	DNP/I2S_0
Pin A15	DNP/I2S_0
Pin A16 & A17	GND
Pin A18 through A21	NC
Pin A22	I2S_BCLK
Pin A23	+5V
Pin A24	I2S_WCLK
Pin A25	+5V
Pin A26	+5V
Pin B1	GND
Pin B2 & B3	NC
Pin B4 & B5	GND
Pin B6 & B7	NC
Pin B8 & B9	GND
Pin B10 through B13	NC
Pin B14 & B15	GND
Pin B16 through B18	NC
Pin B19 & B20	GND
Pin B21	+12V
Pin B22	NC
Pin B23	+12V
Pin B24	NC
Pin B25	+12V
Pin B26	GND

CN602 – I2C Host Interface (similar to CN901 purpose with 4 pin header only)

Pin 1	+5V
Pin 2	I2C_SCL
Pin 3	I2C SDA
Pin 4	GND

CN603 – UART Interface (for UART-over-Aux testing)

Pin 1	+5V
Pin 2	Aux_UART_TX
Pin 3	Aux_UART_RX
Pin 4	GND

CN601 – IR Input

Pin 1	GND
Pin 2	+5V
Pin 3	IR_IN

3.3. Switches

Host Interface Switch: (SW902): This switch selects the use of GProbe connector or Host Interface connector.

Pin 1	HOST_TX
Pin 2	UART_TX
Pin 3	GPROBE_TX
Pin 4	HOST_RX
Pin 5	UART_RX
Pin 6	GPROBE_RX

3.4. Stuffing Options

3.4.1. Dual/quad TTL

Dual bus LVDS configuration: stuff R510, unstuff R509

Quad bus LVDS configuration: stuff R509, unstuff R510

3.4.2. IROM/SPI-Flash

OCM boot from IROM code: stuff R504, unstuff R503

OCM boot from external ROM code: stuff R503, unstuff R504