

## F2950

High Linearity SP2T Wi-Fi RF Switch 100MHz to 8GHz

The F2950 is a high power, reflective 50Ω, single-pole double-throw (SP2T) RF switch. This device covers a 100MHz to 8GHz frequency range to support a wide variety of applications including WLAN 802.11.

The F2950 uses a single positive supply voltage and is compatible with both 1.8V and 3.3V control logic.

### Competitive Advantage

The F2950 provides extremely low insertion loss across a very broad bandwidth while providing high linearity performance across its operating range.

- Optimized for Wi-Fi applications
- Wide bandwidth
- Low insertion loss
- Excellent linearity
- High power handling for large peak-to-average applications
- Fast switching
- No external matching required
- Minimal footprint

### Typical Applications

- 802.11 Wi-Fi
- Wireless Access Points, Gateways and Router Applications
- LTE and 4G Communication Systems
- 2-Way Radios
- General Purpose

### Features

- Low insertion loss: 0.58dB at 2.5GHz
- High isolation: 44dB at 2.5GHz
- Excellent linearity:
  - IIP3 +69dBm at 2.4GHz and 5.9GHz
  - IIP2 +111dBm at 2.4GHz
  - IIP2 +122dBm at 5.9GHz
- Second Harmonic: -93dBc at 5.9GHz
- Third Harmonic: -85dBc at 5.9GHz
- Typical switching speed: 170ns
- Supply voltage: +2.7V to +5.5V
- 1.8V and 3.3V compatible control logic
- -40°C to +105°C operating temperature range
- 1.5 × 1.5 mm, 6-DFN package

### Block Diagram

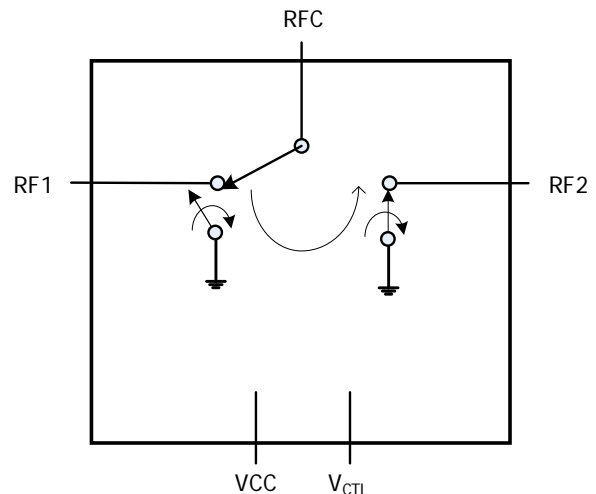


Figure 1. Block Diagram

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## 1. Pin Information

### 1.1 Pin Assignments

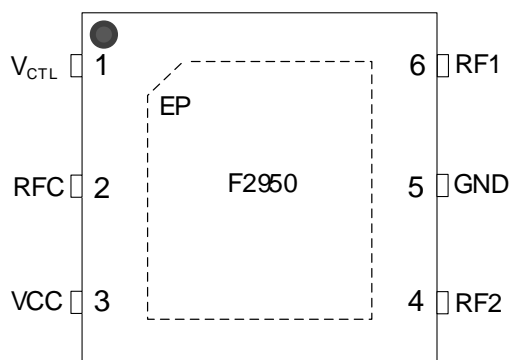


Figure 2. Pin Assignments – Top View

### 1.2 Pin Descriptions

Pin	Name	Function
1	V <sub>CTL</sub>	Logic control pin. See Table 3 for logic control states.
2	RFC	RF common port. Matched to 50Ω in the insertion loss state only. If this pin is not 0V DC, then an external coupling capacitor must be used.
3	V <sub>CC</sub>	Power supply. Bypass to GND with capacitors as close as possible to the pin.
4	RF2	RF2 port. Matched to 50Ω in the insertion loss state only. If this pin is not 0V DC, then an external coupling capacitor must be used.
5	GND	Ground. Ground this pin as close to the device as possible.
6	RF1	RF1 port. Matched to 50Ω in the insertion loss state only. If this pin is not 0V DC, then an external coupling capacitor must be used.
-	EP	Exposed pad. Internally connected to GND. Solder this exposed pad to a PCB pad that uses multiple ground vias to provide heat transfer out of the device into the PCB ground planes. These multiple ground vias are also required to achieve the specified RF performance.

## 2. Specifications

### 2.1 Absolute Maximum Ratings

Stresses beyond those listed below may cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameter		Symbol	Minimum	Maximum	Unit
V <sub>CC</sub> to GND		V <sub>CC</sub>	-0.3	+6.0	V
V <sub>CTL</sub> to GND		V <sub>LOGIC</sub>	-0.3	Lower of (V <sub>CC</sub> + 0.3, 3.9)	V
RF1, RF2, RFC to GND		V <sub>RF</sub>	-0.3	+0.3	V
Maximum Input CW Power, Z <sub>S</sub> = Z <sub>L</sub> = 50Ω, T <sub>EP</sub> = 25°C, V <sub>CC</sub> = 5.25V (any port, insertion loss state) <sup>[1]</sup>	100MHz ≤ f <sub>RF</sub> ≤ 200MHz	P <sub>ABSCW1</sub>	-	28	dBm
	200MHz < f <sub>RF</sub> ≤ 500MHz	P <sub>ABSCW2</sub>	-	29	
	500MHz < f <sub>RF</sub> ≤ 1GHz	P <sub>ABSCW3</sub>	-	30	
	1GHz < f <sub>RF</sub> ≤ 6GHz	P <sub>ABSCW4</sub>	-	31	
	f <sub>RF</sub> > 6GHz	P <sub>ABSCW5</sub>	-	30	
Maximum Peak Power, Z <sub>S</sub> = Z <sub>L</sub> = 50Ω, T <sub>EP</sub> = 25°C, V <sub>CC</sub> = 5.25V (any port, insertion loss state) <sup>[1][2]</sup>	100MHz ≤ f <sub>RF</sub> ≤ 200MHz	P <sub>ABSPK1</sub>	-	35	dBm
	200MHz < f <sub>RF</sub> ≤ 500MHz	P <sub>ABSPK2</sub>	-	36	
	500MHz < f <sub>RF</sub> ≤ 1GHz	P <sub>ABSPK3</sub>	-	37	
	1GHz < f <sub>RF</sub> ≤ 6GHz	P <sub>ABSPK4</sub>	-	38	
	f <sub>RF</sub> > 6GHz	P <sub>ABSPK5</sub>	-	37	
Maximum Junction Temperature		T <sub>JMAX</sub>	-	-	°C
Storage Temperature Range		T <sub>STOR</sub>	-65	+150	°C
Lead Temperature (soldering, 10s)		T <sub>LEAD</sub>	-	+260	°C

1. T<sub>EP</sub> is the temperature of the exposed paddle.
2. 5% duty cycle of 4.6ms period in a 50Ω environment.

### 2.2 ESD Ratings

ESD Model/Test	Symbol	Rating	Unit
Electrostatic Discharge – HBM (JEDEC/ESDA JS-001-2012)	V <sub>ESDHBM</sub>	2000 (Class C2)	V
Electrostatic Discharge – CDM (JEDEC 22-C101F)	V <sub>ESDCDM</sub>	500 (Class C2)	V

### 2.3 Recommended Operating Conditions

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Power Supply Voltage	$V_{CC}$		2.7 <sup>[1]</sup>	3.3	5.5	V
Operating Temperature Range	$T_{EP}$	Exposed paddle	-40	+25	+105	°C
RF Frequency Range	$f_{RF}$		0.1		8	GHz
RF Input Power <sup>[2]</sup>	$P_{RF\_CW}$	CW, insertion loss state	See Figure 3			dBm
	$P_{RF\_PULSE}$	5% duty cycle of 4.6ms period, insertion loss state	See Figure 3			
RFC, RF1, RF2 Port Impedance	$Z_{RF}$			50		$\Omega$

- Functional with reduced performance for  $2.3V \leq V_{CC} < 2.7V$ .
- Levels based on:  $V_{CC} = 2.7V$  to  $5.5V$ ,  $100MHz \leq f_{RF} \leq 8GHz$ ,  $Z_s = Z_L = 50\Omega$ . See Figure 3 for power handling derating vs. RF frequency.

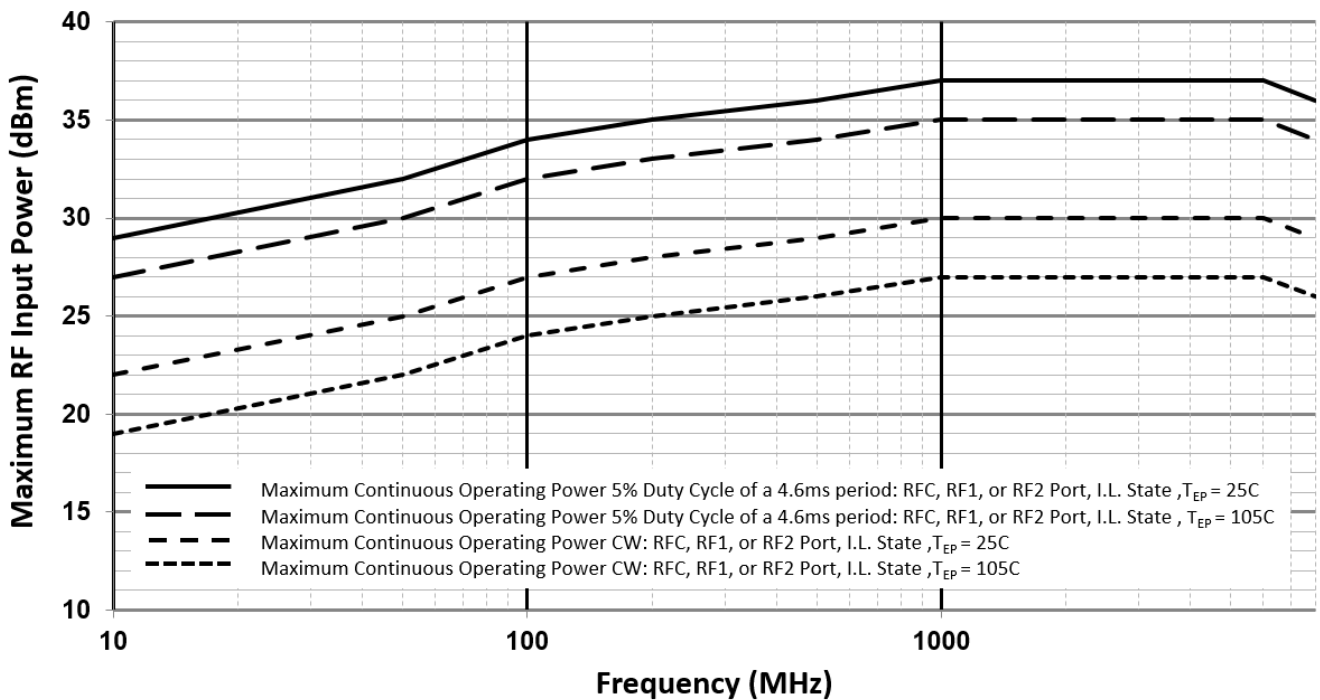


Figure 3. Maximum RF Input Operating Power vs. RF Frequency ( $Z_s = Z_L = 50\Omega$ )

### 2.4 Thermal Specifications

Parameter	Symbol	Value	Unit
Junction to Ambient Thermal Resistance	$\theta_{JA}$	200	°C/W
Junction to Case Thermal Resistance (Case is defined as the exposed paddle)	$\theta_{JC\_BOT}$	132	°C/W
Moisture Sensitivity Rating (Per J-STD-020)	-	MSL 1	-

## 2.5 Electrical Specifications

See F2950 Typical Application Circuit. Specifications apply when operated with  $V_{CC} = +3.3V$ ,  $T_{EP} = +25^{\circ}C$ ,  $P_{IN} = 0dBm$ ,  $Z_S = Z_L = 50\Omega$ , single tone and two tone signals applied at RF1 or RF2 and measured at RFC when in the ON state, PCB board trace and connector losses are de-embedded, unless otherwise noted.

**Table 1. Electrical Characteristics (1)**

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Logic Input High Threshold	$V_{IH}$	$V_{CTL}$ pin	1.1 [2]	-	Lower of ( $V_{CC}$ , 3.6)	V
Logic Input Low Threshold	$V_{IL}$	$V_{CTL}$ pin	-0.3	-	0.6	V
Logic Current	$I_{IH}, I_{IL}$	$V_{CTL}$ pin	<b>-1</b>	-	<b>+1</b>	$\mu A$
DC Current	$I_{CC}$		-	170	<b>250</b> <sup>[1]</sup>	$\mu A$
Insertion Loss (RF1 or RF2 to RFC)	IL	$f_{RF} = 100MHz$ to $900MHz$	-	0.54	0.74	dB
		$f_{RF} = 900MHz$ to $2500MHz$ [3]	-	0.58	<b>0.79</b>	
		$f_{RF} = 2500MHz$ to $3700MHz$	-	0.61	0.83	
		$f_{RF} = 3700MHz$ to $4900MHz$	-	0.64	0.88	
		$f_{RF} = 4900MHz$ to $6000MHz$	-	0.67	0.90	
		$f_{RF} = 6000MHz$ to $8000MHz$	-	0.73	-	
Isolation (RF1 or RF2 to RFC)	ISO1	$f_{RF} = 100MHz$ to $900MHz$	48	53	-	dB
		$f_{RF} = 900MHz$ to $2500MHz$	39	44	-	
		$f_{RF} = 2500MHz$ to $3700MHz$	35	40	-	
		$f_{RF} = 3700MHz$ to $4900MHz$	32	37	-	
		$f_{RF} = 4900MHz$ to $6000MHz$	-	34	-	
		$f_{RF} = 6000MHz$ to $8000MHz$	-	31	-	
Isolation (RF1 to RF2, RF2 to RF1)	ISO2	$f_{RF} = 100MHz$ to $900MHz$	50	54	-	dB
		$f_{RF} = 900MHz$ to $2500MHz$	40	44	-	
		$f_{RF} = 2500MHz$ to $3700MHz$	35	40	-	
		$f_{RF} = 3700MHz$ to $4900MHz$	32	37	-	
		$f_{RF} = 4900MHz$ to $6000MHz$	-	34	-	
		$f_{RF} = 6000MHz$ to $8000MHz$	-	30	-	
Return Loss (RFC, RF1, RF2)	RL	$f_{RF} = 100MHz$ to $900MHz$	-	25	-	dB
		$f_{RF} = 900MHz$ to $2500MHz$	-	23	-	
		$f_{RF} = 2500MHz$ to $3700MHz$	-	22	-	
		$f_{RF} = 3700MHz$ to $4900MHz$	-	21	-	
		$f_{RF} = 4900MHz$ to $6000MHz$	-	20	-	
		$f_{RF} = 6000MHz$ to $8000MHz$	-	20	-	

- Items in min/max columns in **bold italics** are guaranteed by test.
- Items in min/max columns that are not bold italics are guaranteed by design characterization.
- Minimum or maximum specification confirmed by test at 2.5GHz and by design characterization over the whole frequency range.

Table 2. Electrical Characteristics (2)

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit	
Input IP3	IIP3	$f_{RF} = 2.4\text{GHz}$ at $P_{IN} = +24\text{dBm/}$ tone 100MHz tone spacing	-	69	-	dBm	
		$f_{RF} = 5.9\text{GHz}$ at $P_{IN} = +24\text{dBm/}$ tone 100MHz tone spacing	-	69	-		
Input IP2	IIP2	$f_1 = 700\text{MHz}$ , $f_2 = 1.7\text{GHz}$ $P_{IN} = +24\text{dBm/}$ tone Measure 2.4GHz product	-	111	-	dBm	
		$f_1 = 2.4\text{GHz}$ , $f_2 = 3.5\text{GHz}$ $P_{IN} = +24\text{dBm/}$ tone Measure 5.9GHz product	-	122	-		
Second Harmonic	H2	$f_{RF} = 2.4\text{GHz}$ , $P_{IN} = +30\text{dBm}$ Measure 4.8GHz product	-	104	-	dBc	
		$f_{RF} = 5.9\text{GHz}$ , $P_{IN} = +30\text{dBm}$ Measure 11.8GHz product	-	93	-		
Third Harmonic	H3	$f_{RF} = 2.4\text{GHz}$ , $P_{IN} = +30\text{dBm}$ Measure 7.2GHz product	-	85	-	dBc	
		$f_{RF} = 5.9\text{GHz}$ , $P_{IN} = +30\text{dBm}$ Measure 17.7GHz product	-	85	-		
Input 1dB compression <sup>[3]</sup>	P1dB	$f_{RF} = 2.4\text{GHz}$	-	40	-	dBm	
		$f_{RF} = 6\text{GHz}$	-	40	-		
		$f_{RF} = 8\text{GHz}$	-	39	-		
Spurious Output <sup>[4]</sup>	Pspur1	$f_{OUT} > 5\text{MHz}$ All ports terminated, RBW = 100Hz	-	-97	-	dBm	
	Pspur2	$f_{OUT} \leq 5\text{MHz}$ All ports terminated, RBW = 100Hz	-	-125	-		
Maximum Video Feed-Through on RF Ports	VID <sub>FT</sub>	Peak transient during switching. Measured with 20ns rise time, 0V to 3.3V (3.3V to 0V) control pulse applied to V <sub>CTL</sub> .	Rise	-	10	-	mVpp
			Fall	-	21	-	
Switching Time <sup>[5]</sup>	SW <sub>TIME</sub>	50% V <sub>CTL</sub> to 90% RF	-	170	230	ns	
		50% V <sub>CTL</sub> to 10% RF	-	170	230		
		50% V <sub>CTL</sub> to 99% RF	-	190	270		
		50% V <sub>CTL</sub> to 1% RF	-	190	270		
Maximum Switching Rate	SW <sub>RATE</sub>	-	-	125	-	kHz	

1. Items in min/max columns in **bold italics** are confirmed by test.
2. Items in min/max columns that are not bold italics are confirmed by design characterization.
3. The input 1dB compression point is a linearity figure of merit. Refer to the Absolute Maximum Ratings section and Figure 3 for the maximum RF input power.
4. Spurious due to on-chip negative voltage generator. Spurious fundamental is approximately 5.7MHz.
5.  $f_{RF} = 1\text{GHz}$ . Rise and fall time of V<sub>CTL</sub> = 20ns.

### 3. Typical Operating Conditions (TOCs)

Unless otherwise noted:

- $V_{CC} = +3.3V$
- $T_{EP} = 25^{\circ}C$
- $Z_S = Z_L = 50\Omega$
- $f_{RF} = 1GHz$
- Small signal tests done at 0dBm input power
- All temperatures are referenced to the exposed paddle
- Evaluation Kit traces and connector losses are de-embedded



## 4. Typical Performance Characteristics [1]

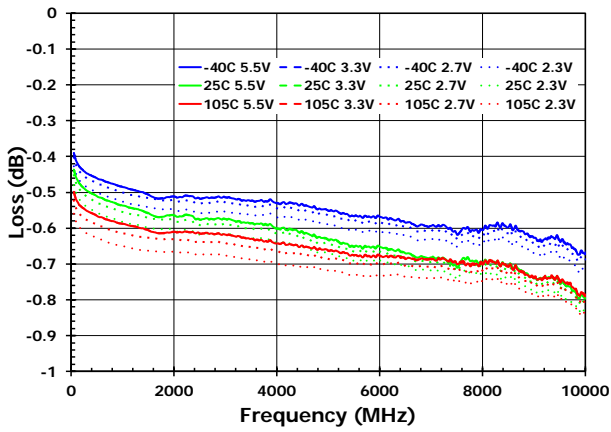


Figure 4. RF1 to RFC Insertion Loss vs. Frequency Across Temperature

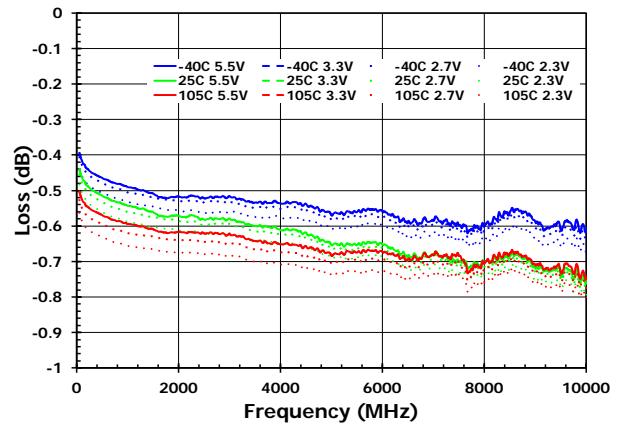


Figure 5. RF2 to RFC Insertion Loss vs. Frequency Across Temperature

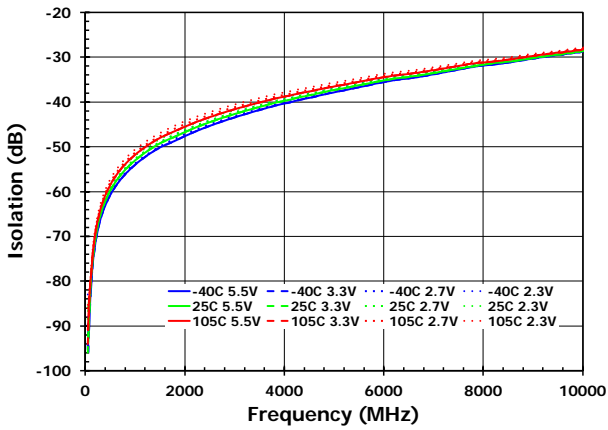


Figure 6. RF1 to RFC Isolation vs. Frequency Across Temperature

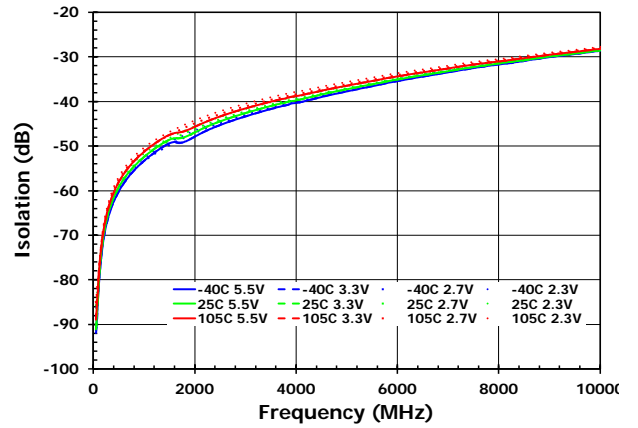


Figure 7. RF2 to RFC Isolation vs. Frequency Across Temperature

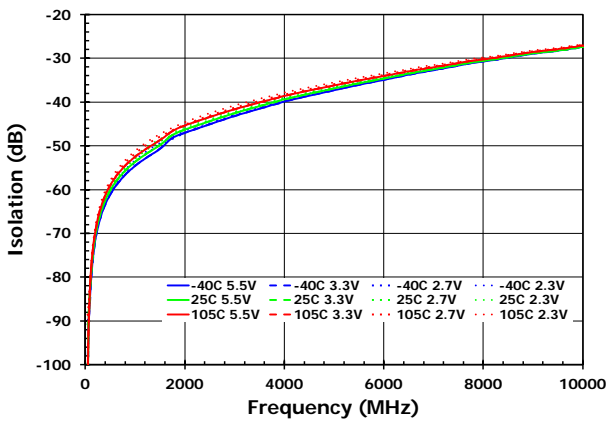


Figure 8. RF1 to RF2 Isolation vs. Frequency Across Temperature [RF1 Selected]

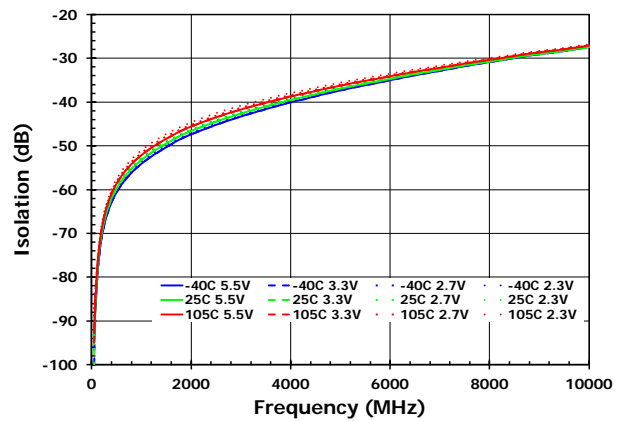


Figure 9. RF2 to RF1 Isolation vs. Frequency Across Temperature [RF2 Selected]

## 5. Typical Performance Characteristics [2]

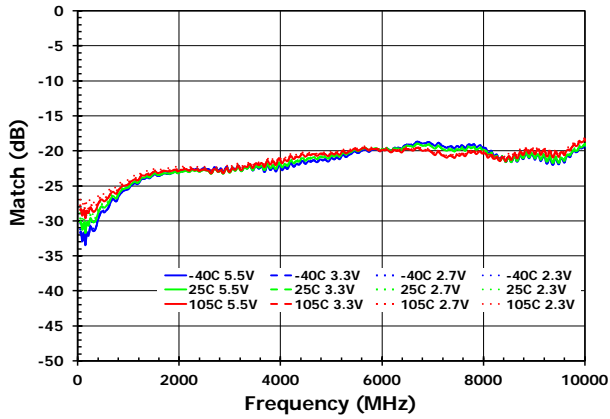


Figure 10. RF1 Return Loss vs. Frequency Across Temperature [RF1 Selected]

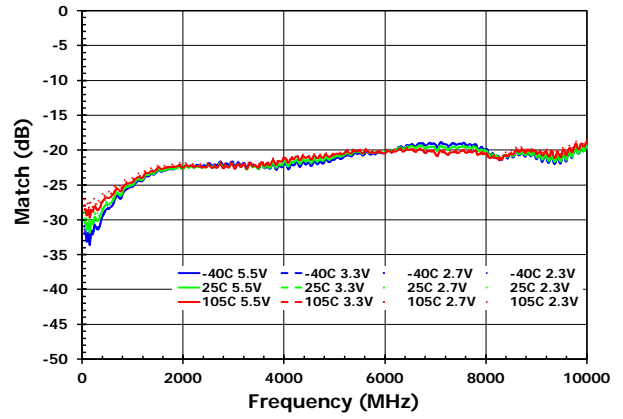


Figure 11. RF2 Return Loss vs. Frequency Across Temperature [RF2 Selected]

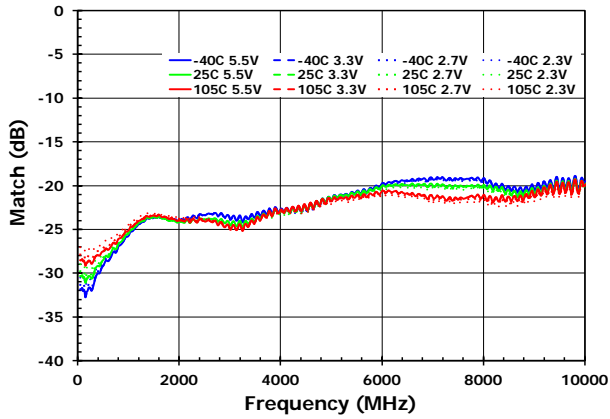


Figure 12. RFC Return Loss vs. Frequency Across Temperature [RF1 Selected]

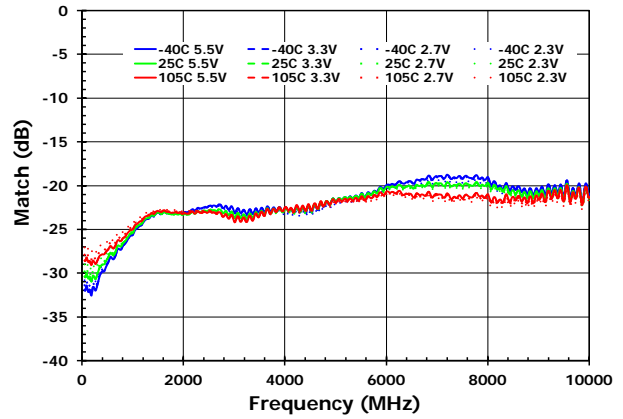


Figure 13. RFC Return Loss vs. Frequency Across Temperature [RF2 Selected]

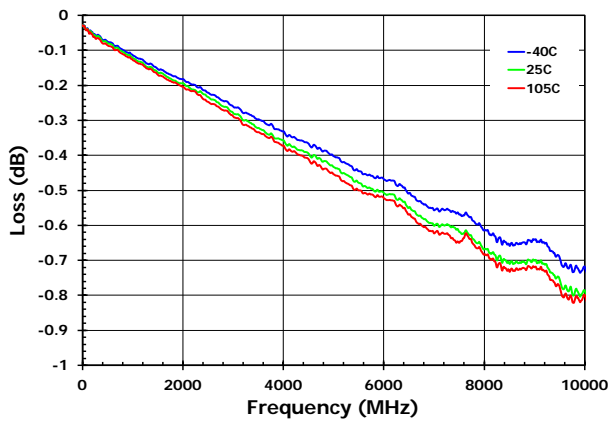


Figure 14. EVKit PCB and Connector Thru Loss vs. Frequency Across Temperature

## 6. Typical Performance Characteristics [3]

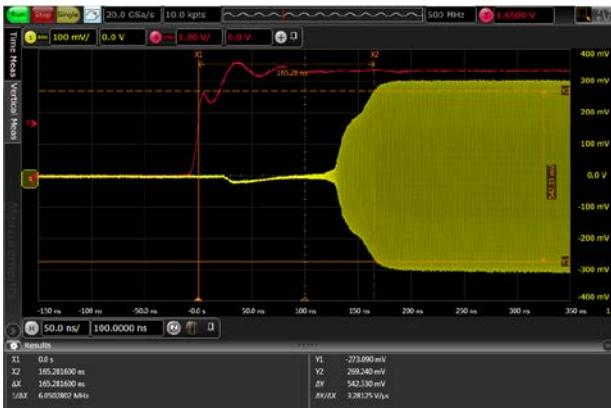


Figure 15. Switching Time Isolation to Insertion Loss State

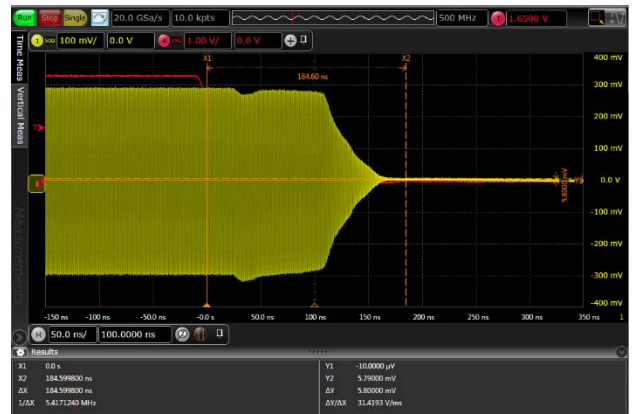


Figure 16. Switching Time Insertion Loss to Isolation State

## 7. Control Mode

Table 3. Switch Control Truth Table

V <sub>CTL</sub>	RFC to RF1	RFC to RF2
LOW	OFF	ON
HIGH	ON	OFF

## 8. Application Information

### 8.1 Default Start-up

The V<sub>CTL</sub> control pin includes no internal pull-down resistors to logic LOW or pull-up resistors to logic HIGH.

### 8.2 Power Supplies

A common V<sub>CC</sub> power supply should be used for all pins requiring DC power. All supply pins should be bypassed with external capacitors to minimize noise and fast transients. Supply noise can degrade noise figure and fast transients can trigger ESD clamps and cause them to fail. Supply voltage change or transients should have a slew rate slower than 1V / 20μs. In addition, all control pins should remain at 0V (±0.3V) while the supply voltage ramps up or while it returns to zero.

### 8.3 Control Pin Interface

If a clean control signal cannot be guaranteed due to overshoot, undershoot, ringing, etc., the following circuit at the input of the control pin is recommended.

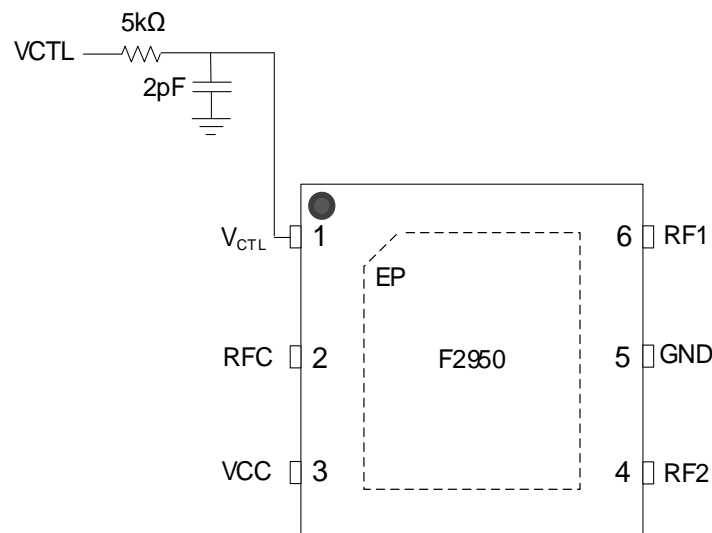


Figure 17. Control Pin Signal Integrity Improvement Circuit

## 9. Evaluation Kit

### 9.1 Evaluation Kit Picture

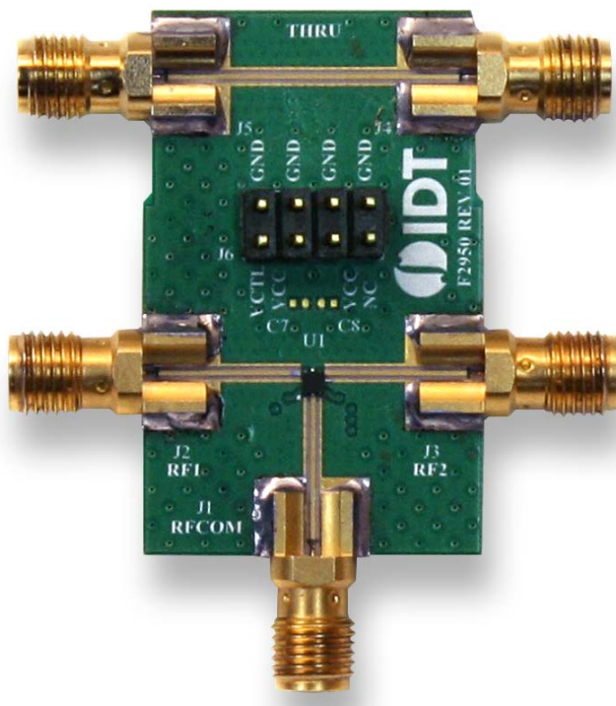


Figure 18. Top View

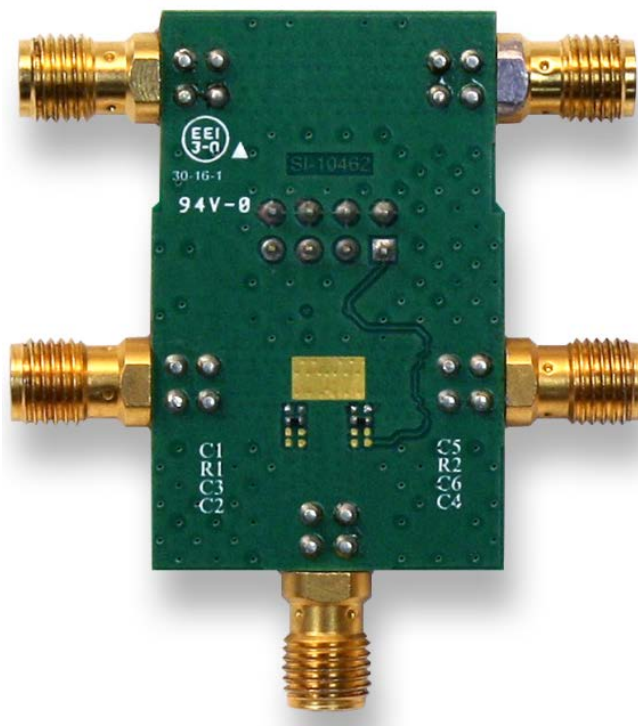


Figure 19. Bottom View

## 9.2 Evaluation Kit / Applications Circuit

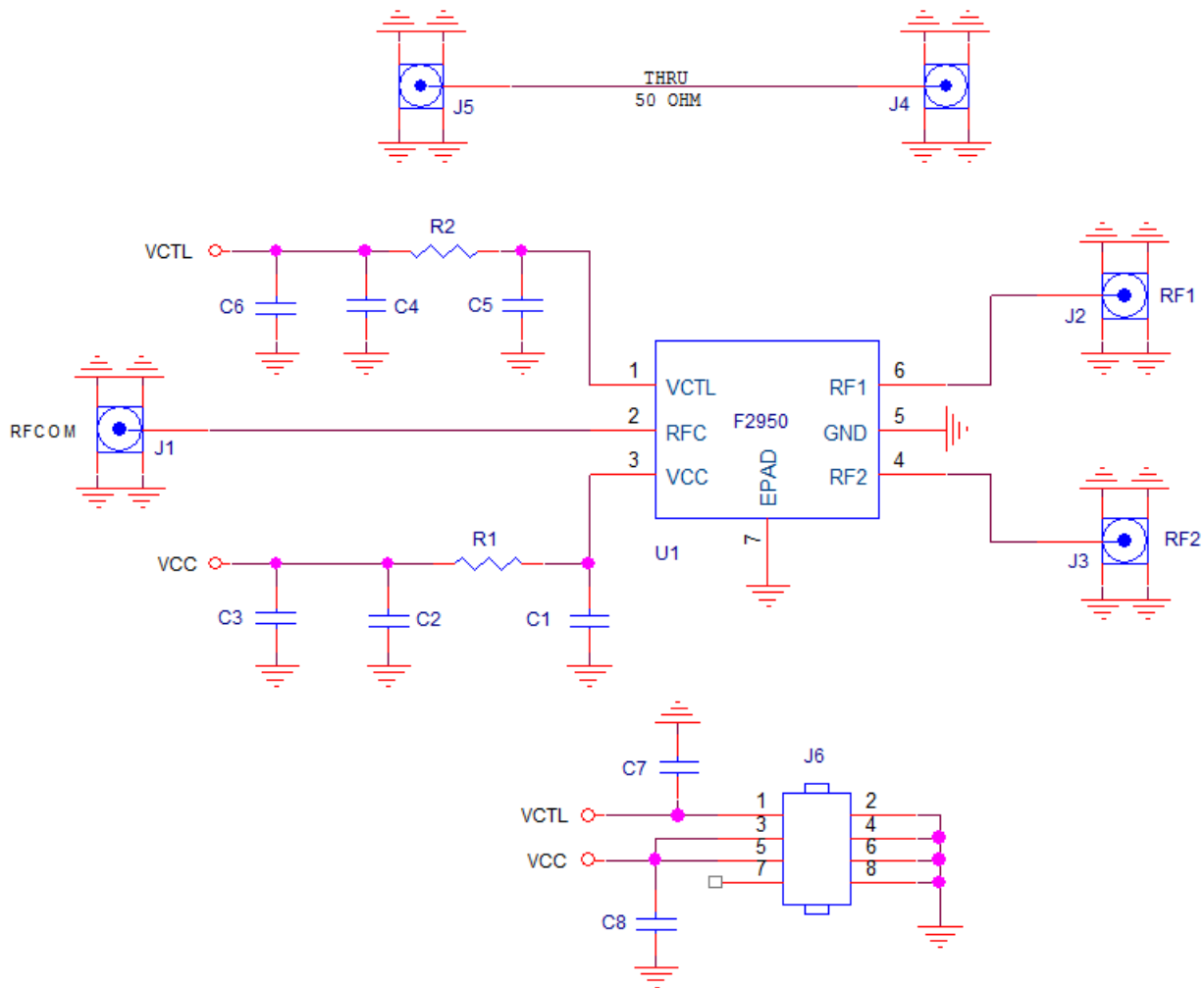


Figure 20. Electrical Schematic

Table 4. Bill of Material (BOM)

Part Reference	QTY	Description	Manufacturer Part #	Manufacturer
C1	1	0.1 $\mu$ F $\pm$ 10%, 16V, X7R, Ceramic Capacitor (0402)	GRM155R71C104K	Murata
C2 – C8	0	Not Installed (0402)	-	-
R1, R2	2	0 $\Omega$ , 1/10W, Jumper (0402)	ERJ-2GE0R00X	Panasonic
J1 – J5	5	50 $\Omega$ Edge SMA Connector	142-0761-881	Cinch Connectivity
J6	1	Conn Header Vert 4x2 Pos Gold	67997-108HLF	Amphenol FCI
U1	1	SP2T Switch 1.5mm x 1.5mm 6-pin NEG6 DFN	F2950NEGK6	Renesas
	1	Printed Circuit Board	F2950 EVKit	Renesas

## 9.3 Evaluation Kit (EVKit) Operation

### 9.3.1. External Supply Setup

1. Set up a VCC power supply in the voltage range of 2.7V to 5.5V with the power supply output disabled.
2. Connect the disabled VCC supply connection to J6 pin 3 or 5 and GND to J6 pin 2, 4, 6, or 8.

### 9.3.2. Logic Control Setup

1. With the logic control line disabled, set the logic HIGH and LOW levels to satisfy the levels stated in the electrical specifications table.
2. Connect the disabled logic control line to VCTL (pin 1 of J6) and GND to J6 pin 2, 4, 6, or 8.

### 9.3.3. Turn On Procedure

1. Set up the supplies and EVKit as noted in the External Supply Setup and Logic Control Setup sections above.
2. Enable the VCC supply.
3. Enable the logic control signal.
4. Set the VCTL logic setting to achieve the desired Table 3 configuration. Note that the VCTL control logic should not be applied without VCC being present.
5. Enable any RF signal.

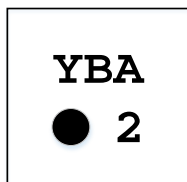
### 9.3.4. Turn Off Procedure

1. Disable any applied RF signal.
2. Set VCTL to GND.
3. Disable the VCC supply.

## 10. Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.

## 11. Marking Diagram



- Line 1: Y = last digit of the year, BA = sequential letters for traceability purposes
- Line 2: Pin 1 dot, 2 = F2950 part number code

## 12. Ordering Information

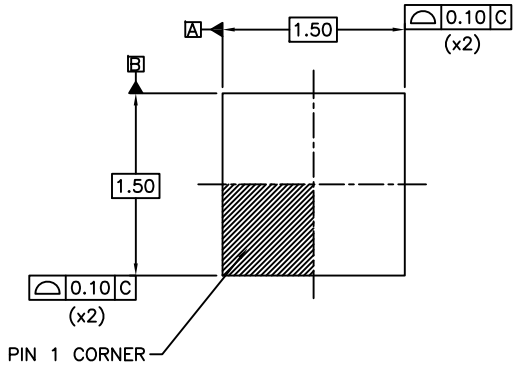
Part Number	Package Description	MSL Rating	Carrier Type	Temperature Range
F2950NEGK	1.5mm x 1.5mm x 0.55mm <a href="#">NEG6</a> DFN	MSL1	Cut Tape	-40°C to +105°C
F2950NEGK8		MSL1	Reel	
F2950EVBI	Evaluation Board			

## 13. Revision History

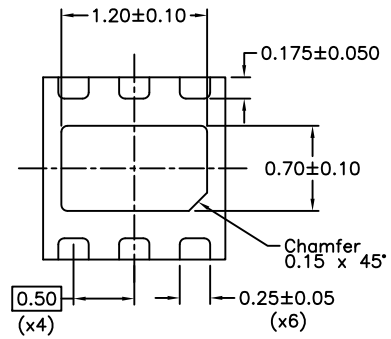
Revision	Date	Description
1.01	Mar 9, 2022	Updated the IIP2 specifications.
1.00	Aug 8, 2017	Initial release.



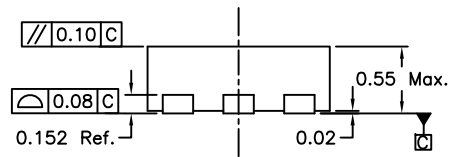
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	4/20/16	JH



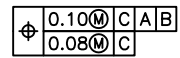
TOP VIEW



BOTTOM VIEW




SIDE VIEW



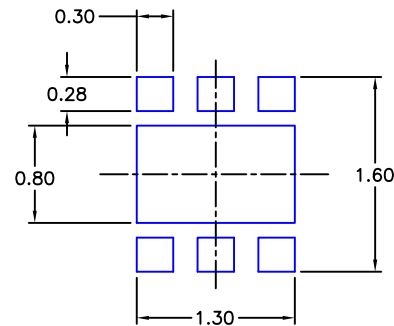
ALL FEATURES

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
2. ALL DIMENSIONS ARE IN MILLIMETERS.

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DECIMAL	ANGULAR	
X±	±1°	
XX±		
XXX±		
APPROVALS	DATE	TITLE
DRAWN <i>BAC</i>	4/20/16	NEG6 PACKAGE OUTLINE
CHECKED		1.5 x 1.5 mm BODY
		0.50 mm PITCH DFN
	SIZE	DRAWING No.
	C	PSC-4653
		REV
		00
DO NOT SCALE DRAWING		SHEET 1 OF 2


REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	4/20/16	JH



RECOMMENDED LAND PATTERN DIMENSION

NOTES:

1. ALL DIMENSIONS ARE IN MM. ANGLES IN DEGREES.
2. TOP DOWN VIEW AS VIEWED ON PCB.
3. NSMD PATTERN ASSUMED.
4. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

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XX±		TITLE NEG6 PACKAGE OUTLINE			
XXX±		1.5 x 1.5 mm BODY			
		0.50 mm PITCH DFN			
APPROVALS	DATE	SIZE	DRAWING No.	REV	
DRAWN <i>RAC</i>	4/20/16	C	PSC-4653	00	
CHECKED		DO NOT SCALE DRAWING			SHEET 2 OF 2

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