

General description

The DA7210 is a high fidelity audio codec with integrated true-ground capless headphone driver suitable for a variety of low power, digital portable audio products.

Featuring a high efficiency headphone amplifier and supporting economic single supply voltages down to 1.8 V, the ultra-low 2.5 mW power consumption extends music playback time for battery operated equipment.

Eight analogue input pins allow multiple audio sources to be internally mixed, eliminating the need for external switches. Both single-ended and fully-differential line and microphone inputs are supported with built-in variable gain amplifiers to optimise dynamic range prior to digitisation.

DA7210 provides simultaneous connection to stereo headphone, stereo line outputs, and a mono differential output. Stereo line outputs can be differential or single-ended. Both stereo outputs have volume control from -54 dB to +15 dB.

Filtering and gain control is performed digitally including 5-band EQ and a digital input AGC with programmable attack and decay parameters. A configurable signal processing engine allows various enhancements and effects on the digital audio signal like acoustic filtering, wind noise suppression and 3D sound.

The multi-slot I2S/PCM interface supports all common sample rates between 8 and 96 kHz in master or slave mode operation.

Key features

- Stereo multi-bit Delta Sigma DAC with SNR 100 dB ('A' weighted @ 48 kHz)
- Stereo multi-bit Delta Sigma ADC with SNR 96 dB ('A' weighted @ 48 kHz)
- Ultra low-power stereo headphone driver with
 - Stereo DAC to HP playback power: 2.5 mW
 - 2x58 mW output power (16 Ω)
 - 'Capless' output via GND centred signals
 - Four level charge pump with continuous tracking of audio signal (Class G)
 - Short circuit protection
- Support of 8, 11.025, 12, 16, 22.05, 24, 32, 44.1, 48 and 96 kHz sample rates
- On-chip PLL with signal shaper and audio Sample Rate Matching
- Wide range of external clocks including industry standard 256xFs, system clock 12, 13, 24, 26 or 27 MHz and low power 32 kHz mode
- Audio serial data bus supports I2S, left/right justified, DSP and TDM modes
- Stereo or mono differential microphone interface
- Programmable ultra-low noise bias supply for electret microphones
- Volume controlled stereo auxiliary inputs and outputs supporting FM Radio and fixed gain speaker amplifiers
- Multi-mode audio routing and mixers
- Pop & click suppression circuitry
- ASSP DSP filter engine for digital audio enhancements (acoustic filtering, wind noise suppression, 5-band equaliser, 3D sound, automatic gain control)
- Supports supply from single voltage (1.8/2.5 V)
- Extensive modular power control
- Package: 49 bump WL-CSP – 0.4 mm pitch

Applications

- Personal media players
- Portable consumer devices
- Music handsets
- Personal navigation devices

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Ultra-low power stereo codec**1 Terms and definitions**

| | |
|--------|---|
| ADC | Analogue to Digital Converter |
| ALC | Automatic Level Control |
| ASSP | Application Specific Standard Product |
| DAC | Digital to Analogue Converter |
| DAI | Digital Audio Interface |
| DMIC | Digital microphone |
| DSP | Digital Signal Processor or Digital Signal Processing |
| FIR | Finite Impulse Response (Filter) |
| I2C | Inter-Integrated Circuit interface |
| I2S | Inter-IC Sound |
| IIR | Infinite Impulse Response (Filter) |
| GP | General Purpose (Filter) |
| LDO | Low Dropout regulator |
| MCLK | Master Clock |
| PCM | Pulse Code Modulation |
| PGA | Programmable Gain Amplifier |
| PLL | Phase Locked Loop |
| PSRR | Power Supply Rejection Ratio |
| RDL | Redistribution Layer |
| RC | Resistance-Capacitance |
| SC | System Controller |
| SDM | Sigma Delta Modulator |
| SNR | Signal to Noise Ratio |
| SRM | Sample Rate Matching |
| TDM | Time Division Multiplexing |
| THD+N | Total Harmonic Distortion plus Noise |
| VCO | Voltage-Controlled Oscillator |
| WL-CSP | Wafer Level-Chip Scale Packaging |

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2 Block diagram

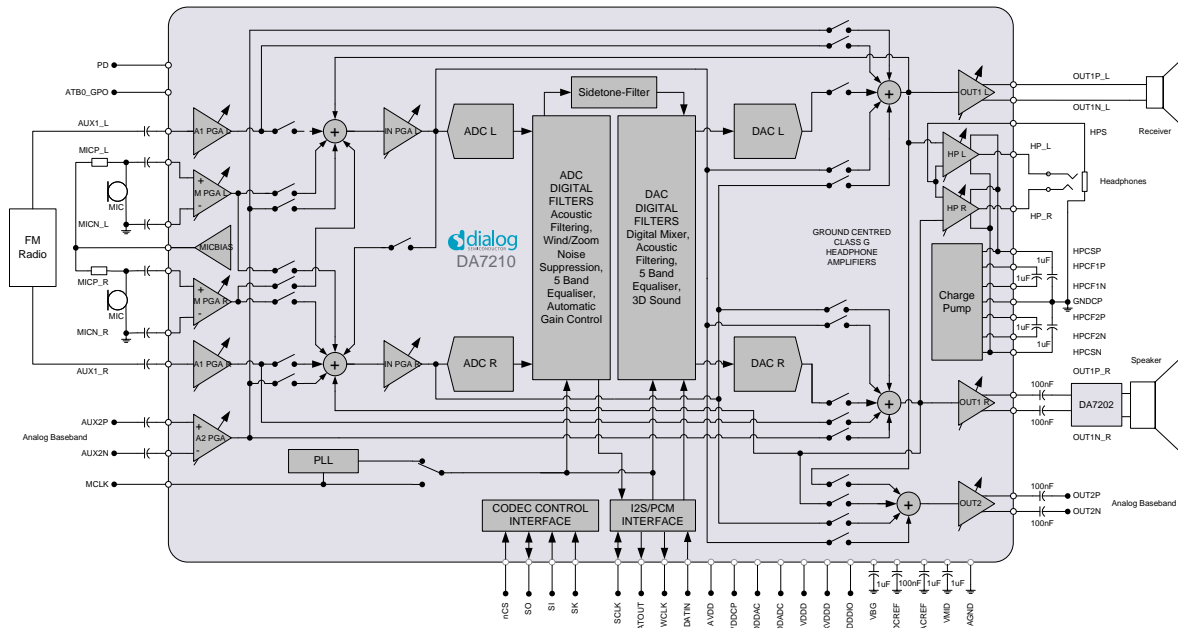


Figure 1: DA7210 block diagram

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3 Pinout



Figure 2: DA7210 pad arrangement (bottom view ball side up)

Table 1: Pin description

| Pin no. | Pin name | Type (Table 2) | Description |
|--------------------------------|----------|-------------------|--|
| Supplies and references | | | |
| 7A | AVDD | PS | Analogue supply (PLL, bias, etc) |
| 2A | VDDDAC | PS | DAC and line output supplies |
| 5B | VDDADC | PS | Mic input and ADC supplies |
| 2F | VDDCP | PS | Charge pump supply |
| 1G | XVDDD | PS | Digital supply (regulator input) |
| 2G | VDDD | PS | Digital supply (1.5 V, if on-chip regulator is active) |
| 3G | VDDDIO | PS | Digital supply for I/O |
| 3A | DACREF | AI | Decoupling capacitor for DAC |
| 4D | ADCREF | AI | Decoupling capacitor for ADC |
| 6A | VMID | AI | Decoupling capacitor for VMID |
| 5C | VBG | AI | Decoupling capacitor for VBG |
| 5E | MICBIAS | AO | Current supply for microphone (2mA max) |

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| Pin no. | Pin name | Type (Table 2) | Description |
|--------------------------------|----------|-------------------|--|
| 1A | GPO | AIO | General Purpose Output |
| 6B | AGND | VSS | Analogue GND |
| 3D | AGND1 | VSS | Analogue GND |
| 1E | GNDCP | VSS | Digital and charge pump ground, attached to paddle |
| Control | | | |
| 5F | SO | DO | 4-WIRE Data output |
| 5G | SI | DIO | 4-WIRE Data input/2-WIRE bidirectional Data |
| 6G | SK | DI | 4-WIRE/2-WIRE Clock |
| 4F | nCS | DI | 4-wire Chip select |
| 4E | PD | DI | Power down signal (power down when high) |
| 2B | HPS | AIO | Headphone Ground Sense |
| Digital Audio Interface | | | |
| 4G | CLK | DIO | Digital Audio bit clock |
| 3F | WCLK | DIO | Digital Audio left/right clock |
| 7F | DATIN | DI | Digital Audio Data input |
| 6F | DATOUT | DO | Digital Audio Data output |
| 7G | MCLK | DI | Master clock input |
| Audio inputs/outputs | | | |
| 6C | MICP_L | AI | Left channel differential microphone +ve input |
| 7B | MICN_L | AI | Left channel differential microphone –ve input |
| 7C | MICP_R | AI | Right channel differential microphone +ve input |
| 6D | MICN_R | AI | Right channel differential microphone –ve input |
| 5D | AUX1_L | AI | Left channel single-ended auxiliary input |
| 6E | AUX1_R | AI | Right channel single-ended auxiliary input |
| 7D | AUX2P | AI | 2nd channel differential auxiliary +ve input |
| 7E | AUX2N | AI | 2nd channel differential auxiliary –ve input |
| 4C | OUT1P_L | AO | Differential or single ended +ve line out left |
| 5A | OUT1N_L | AO | Differential –ve line out left |
| 4A | OUT1P_R | AO | Differential or single ended +ve line out right |
| 4B | OUT1N_R | AO | Differential –ve line out right |
| 3C | OUT2N | AO | 2nd channel differential auxiliary -ve output |
| 3B | OUT2P | AO | 2nd channel differential auxiliary +ve output |
| 1B | HP_L | AO | Left head phone amp output |
| 2C | HP_R | AO | Right head phone amp output |
| Charge pump | | | |
| 3E | HPCF1P | PS | Head phone amp charge pump floating cap1 +ve |
| 1F | HPCF1N | PS | Head phone amp charge pump floating cap1 –ve |
| 2E | HPCF2P | PS | Head phone amp charge pump floating cap2 +ve |

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| Pin no. | Pin name | Type (Table 2) | Description |
|---------|----------|-------------------|--|
| 1D | HPCF2N | PS | Head phone amp charge pump floating cap2 -ve |
| 1C | HPCSP | PS | Head phone amp charge pump storage cap +ve |
| 2D | HPCSN | PS | Head phone amp charge pump storage cap -ve |

Table 2: Pin type definition

| Pin type | Description |
|----------|-----------------------|
| AI | Analogue Input |
| AO | Analogue Output |
| AIO | Analogue Input/Output |
| DI | Digital Input |
| DO | Digital Output |
| DIO | Digital Input/Output |
| PS | Power Supply |
| VSS | Power Supply |

3.1 The 49-ball DA7210 device

On the DA7210, all supplies are accessible as external pins. The VDD pin is only required for capacitive decoupling. If the LDO is not required to supply the digital core voltage, the VDD supply should still be applied to the XVDD pin and the LDO should be disabled.

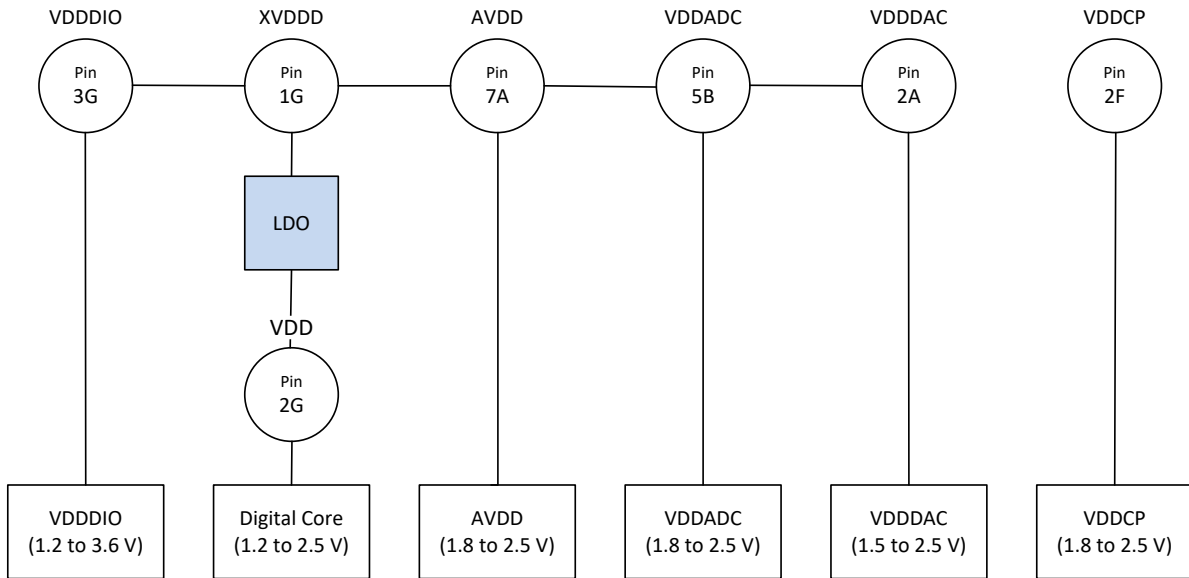


Figure 3: DA7210 power supply topology

4 Absolute maximum ratings

Table 3: Absolute maximum ratings

| Parameter | Description | Conditions (Note 1) | Min | Max | Unit |
|--|--|---------------------|------|----------|------|
| | Storage temperature | | -40 | +95 | °C |
| Ta | Operating temperature | | -40 | +85 | °C |
| AVDD, VDDDAC, VDDADC, VDDD, VDDDIO | Power Supply Input | | -0.3 | 2.75 | V |
| VDDDIO | | 3.6 V mode | -0.3 | 3.6 | V |
| | Supply voltage all input pins except power | | -0.3 | AVDD+0.3 | V |
| | Maximum power dissipation | | | 200 | mW |
| | Package thermal resistance | | | 40 | k/W |
| | ESD susceptibility | Human body model | | 2 | kV |

Note 1 Stresses beyond those listed under 'Absolute maximum ratings' may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

5 Recommended operating conditions

Table 4: Recommended operating conditions

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|----------------------------|--------------------------|--|------|-----|-----|------|
| | Operating temperature | | -40 | | +85 | °C |
| VDDD | Supply voltage digital | Min and max values can accept +/-5% tolerances | 1.2 | | 2.5 | V |
| VDDDIO | Supply voltage I/O | Min and max values can accept +/-5% tolerances | 1.2 | | 2.5 | V |
| | | 3.6 V mode | 2.65 | | 3.6 | V |
| AVDD, VDDADC, VDDDAC | Supply voltage analogue | Min and max values can accept +/-5% tolerances | 1.8 | | 2.5 | V |
| VDDCP | Supply voltage headphone | Max value can accept +/-5% tolerances | 1.8 | | 2.5 | V |

6 Electrical characteristics

Table 5: Power dissipation table

| Parameter | Description | Conditions (Note 2) | Min | Typ | Max | Unit |
|-----------|--|---|-----|------|-----|------|
| | All registers at default values | Powerdown | | 6 | | μA |
| | Digital playback to lineout | DACL/R to OUT1L/R | | 3.15 | | mW |
| | Digital playback to HP no load | DACL/R to HPL/R quiescent | | 2.54 | | mW |
| | Digital playback to HP with load | DACL/R to HPL/R 16 Ω load 0.1 mW | | 4.66 | | mW |
| | Analogue bypass to lineout | AUX1L/R to OUT1L/R | | 2.87 | | mW |
| | Analogue bypass to HP no load | AUX1L/R to HPL/R quiescent | | 2.43 | | mW |
| | Analogue bypass to HP with load | AUX1L/R to HPL/R 16 Ω load 0.1 mW | | 4.57 | | mW |
| | Microphone stereo record | MICL/R to ADCL/R | | 2.38 | | mW |
| | Mic one channel record and digital playback to lineout | MICR to ADCR and DACR to OUT2 | | 3.10 | | mW |
| | Mic stereo record and digital playback to HP no load | MICL/R to ADCL/R and DACL/R to HPL/R quiescent | | 4.35 | | mW |
| | Mic stereo record and digital playback to HP with load | MICL/R to ADCL/R and DACL/R to HPL/R 16 Ω load 0.1 mW | | 6.49 | | mW |

Note 2 SC_CLK_DIS, 0x03[7] = 1 for all measurements
VMID_BUFF_EN, 0x96[2:0] = 000 for all modes not using DAC

Ultra-low power stereo codec

Test conditions: VDD=2.5 V, Ta=25°C, fs=48 kHz, 24-bit audio data unless specified otherwise

Table 6: Electrical characteristics: Microphone bias

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|---------------------------|------------------------------|--|------------|---------------|------------|-------------------|
| V _{BIAS} | Bias Voltage | No load, AVDD = 2.5 V No load, AVDD = 1.8 V | 2.2 1.5 | Pro-grammable | 2.3 1.6 | V |
| I _{BIAS} | Maximum Current | Voltage drop < 50 mV | | 2 | | mA |
| PSRR with respect to AVDD | Power Supply Rejection Ratio | 20 Hz - 2 kHz 2 kHz - 20 kHz | 70 50 | | | dB |
| V _N | Output Noise Voltage | | | 5 | | μV _{RMS} |
| | Capacitive Load | I _{BIAS} < 100 μA, 100 μA < I _{BIAS} < 2 mA | | 100 200 | | pF |

Table 7: Electrical characteristics: Input mixing units

(MICP_L, MICN_L, AUX_L, MICP_R, MICN_R, AUX1_R, AUX2P, AUX2N)

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|---------------------------|---|---|-------------------------|----------------------|----------------------|-------------------|
| V _{MAX} | Full-scale Input Signal | single-ended differential MIC-PGA=0 dB IN-PGA=0 dB | | 0.8*AVDD 1.6*AVDD | | V _{PP} |
| R _{IN} | Input resistance | Mic, meas. single ended AUX1 AUX2 | 12 6 24 | 15 variable 30 | 18 40 36 | kΩ |
| | Frequency Response | +/- 0.5 dB | 20 | | 20k | Hz |
| | Amplitude Ripple | 20 Hz – 20 kHz | -0.5 | | 0.5 | dB |
| | Programmable Gain Note 3 | M-PGA AUX1-PGA AUX2-PGA IN-PGA | -6 -48 -6 -4.5 | | 24 21 12 18 | dB |
| | Programmable Gain Step Size | M-PGA, AUX2-PGA AUX1-PGA, IN-PGA | | 6 1.5 | | dB |
| | Absolute Gain Accuracy | 0 dB @ 1 kHz | -1.0 | | 1.0 | dB |
| | Input Gain L/R-Mismatch | 20 Hz – 20 kHz | -0.1 | | 0.1 | dB |
| | Input Gain Step Error | 20 Hz – 20 kHz | -0.1 | | 0.1 | dB |
| V _{NOISE} | Input Noise Level | Inputs connected to GND A-weighting input referred, measured @ ADC output Mic (Gain = 42 dB) AUX1 (Gain = 21 dB) AUX2 (Gain = 18 dB) | | 5 6.5 8.8 | | μV _{RMS} |
| PSRR with respect to AVDD | Power Supply Rejection Ratio | 20 Hz - 2 kHz 2 kHz - 20 kHz, single ended input | 80 70 | | | dB |

Note 3 The gain describes the ratio of input and output signal level at the related amplifier stage (independent of whether the connection is single ended or differential).

Ultra-low power stereo codec

Table 8: Electrical characteristics: Analogue to digital converter (ADC)

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|---------------------------------|---|--|----------|-------------------------|------------------|-----------------|
| V _{MAX} | Full-scale Input Signal | Corresponding digital level 0 dBFS | | 1.6* AVDD | | V _{PP} |
| SNR | Signal to Noise Ratio | A-weighting, no input selected | | 96 | | dB |
| THD+N | Total Harmonic Distortion Plus Noise | -1 dBFS | | -89 | | dB |
| | Channel separation | | | 90 | | dB |
| B _{PASS} | Pass band | | | | 0.45*fs | kHz |
| B _{STOP} | Stop band | fs ≤ 48 kHz fs = 88.2/96 kHz | 0.56*fs | | 7*fs 3.5*fs | kHz |
| | Pass band Ripple | Voice Mode Music Mode | | | +/-0.3 +/-0.1 | dB |
| | Stop band Attenuation | Voice Mode Music Mode | 70 55 | | | dB |
| | Group delay | Voice Mode Music Mode (Note 4) fs= 88.2/96 kHz | | 4.3/fs 18/fs 9/fs | 600 | µs |
| | Group delay mismatch | Between left and right channel | | | 2 | µs |
| PSRR with respect to AVDD | Power Supply Rejection Ratio | 20 Hz - 2 kHz 2 kHz - 20 kHz | 80 70 | | | dB |

Note 4 5-band-equaliser disabled.

Ultra-low power stereo codec

Table 9: Electrical characteristics: Digital to analogue converter (DAC)

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|---------------------------------|---|--|----------|----------------------------|------------------|-----------------|
| V _{MAX} | Full-scale Output Signal | Corresponding digital level 0 dBFS | | 1.6* V _{DDDAC} | | V _{PP} |
| SNR | Signal to Noise Ratio | A weighting | | 102 | | dB |
| THD+N | Total Harmonic Distortion Plus Noise | -1 dBFS | | -90 | | dB |
| THD+N | Total Harmonic Distortion Plus Noise | -1 dBFS, 32 kHz PLL mode | | -80 | | dB |
| | Channel separation | | | 90 | | dB |
| B _{PASS} | Pass band | | | | 0.45*fs | kHz |
| B _{STOP} | Stop band | fs ≤ 48 kHz fs = 88.2/96 kHz | 0.56*fs | | 7.5*fs 3.5*fs | kHz |
| | Pass band Ripple | Voice Mode Music Mode | | | ±0.15 ±0.1 | dB |
| | Stop band Attenuation | Voice Mode Music Mode | 70 55 | | | dB |
| | Group delay | Voice Mode Music Mode fs = 88.2/96 kHz | | 4.8/fs 18.5/fs 9/fs | 650 | µs |
| | Group delay variation | 20 Hz to 20 kHz | | | 1 | µs |
| | Group delay mismatch | Between left and right channel | | | 2 | µs |
| PSRR with respect to AVDD | Power Supply Rejection Ratio | 20 Hz - 2 kHz 2 kHz - 20 kHz | 70 60 | | | dB |

Ultra-low power stereo codec

Table 10: Electrical characteristics: Line out and receiver amplifier

(OUT1P_L, OUT1N_L, OUT1P_R, OUT1N_R)

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|---------------------------|--------------------------------------|--|----------|-----------------------|----------|-----------------|
| V _{MAX} | Full-scale Input Signal | No load, single-ended No load, differential | | 0.8*AVDD 1.6 *AVDD | | V _{PP} |
| | Load Impedance | single-ended output mode | 500 | 2k | 1 200 | Ω μH pF |
| | | differential output mode | 25 | 32 | 1 200 | Ω μH pF |
| | Frequency Response | +/- 0.5 dB | 20 | | 20k | Hz |
| | Amplitude Ripple | 20 Hz – 20 kHz | -0.5 | | 0.5 | dB |
| | Programmable Gain | | -54 | | 15 | dB |
| | Mute Attenuation | | | 100 | | dB |
| | Programmable Gain Step Size | | | 1.5 | | dB |
| | Absolute Gain Accuracy | 0 dB @ 1 kHz | -0.8 | | 0.8 | dB |
| | Input Gain L/R-Mismatch | 20 Hz – 20 kHz | -0.1 | | 0.1 | dB |
| | Input Gain Step Error | 20 Hz – 20 kHz | -0.1 | | 0.1 | dB |
| SNR | Signal to Noise Ratio | A weighting | | 102 | | dB |
| V _{NOISE} | Output Noise Level | 20 - 20 kHz, unweighted gain < -15 dB single-ended differential | | <5.5 <4.5 | | μV |
| THD+N | Total Harmonic Distortion Plus Noise | -1 dBFS, 44.1 kHz slave mode non A-weighting | | -90 | | |
| PSRR with respect to AVDD | Power Supply Rejection Ratio | 20 Hz - 2 kHz 2 kHz - 20 kHz single-ended output | 70 47 | | | dB |
| | | 20 Hz - 2 kHz 2 kHz - 20 kHz differential output | 90 70 | | | dB |

Ultra-low power stereo codec
Table 11: Electrical characteristics: Line out amplifier
 (OUT2P, OUT2N)

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|---------------------------|--------------------------------------|---|----------|----------|----------|-----------------|
| V _{MAX} | Full-scale Input Signal | No load | | 1.6*AVDD | | V _{PP} |
| | Load Impedance | | 25 | 32 | 1 200 | Ω μH pF |
| | Frequency Response | +/- 0.5 dB | 20 | | 20k | Hz |
| | Amplitude Ripple | 20 Hz – 20 kHz | -0.5 | | 0.5 | dB |
| | Programmable Gain | | -18 | | 6 | dB |
| | Programmable Gain Step Size | | | 6 | | dB |
| | Input Gain L/R-Mismatch | 20 Hz – 20 kHz | -0.1 | | 0.1 | dB |
| | Input Gain Step Error | 20 Hz – 20 kHz | -0.2 | | 0.2 | dB |
| SNR | Signal to Noise Ratio | A-weighting, gain = 0 dB | | 102 | | dB |
| V _{NOISE} | Output Noise Level | 20 -20 kHz, unweighed Gain < -15 dB, gain ≤ -12 dB | | <5 | | μV |
| THD+N | Total Harmonic Distortion Plus Noise | -1 dBFS , A-weighting | | -90 | | |
| PSRR with respect to AVDD | Power Supply Rejection Ratio | 20 Hz - 2 kHz 2 kHz - 20 kHz | 90 70 | | | dB |

Table 12: Electrical characteristics: Dynamic charge pump
 (HPCSP, HPCSN)

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|-----------|---------------------------------|---|-----|---|-----|------|
| VDDCSP | Positive dynamic supply voltage | VDDCP/3/4 can optionally be enabled if two flying caps are available | | VDDCP VDDCP/2 (VDDCP/3, VDDCP/4) | | |
| VDDCSN | Negative dynamic supply voltage | -VDDCP/3/4 can optionally be enabled if two flying caps are available | | -VDDCP -VDDCP/2 (-VDDCP/3, -VDDCP/4) | | |
| | Floating capacitors | | | 1.0 | | μF |
| | Storage capacitors | | | 1.0 | | μF |

Table 13: Electrical characteristics: Headphone amplifier
 (HPL, HPR)

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|---------------------------|--------------------------------------|--|------|---------------------------------------|------------|-------------------|
| V _{MAX} | Full-scale Output Signal | No load | | 1.6*VDD CP | | V _{PP} |
| | DC output offset | | | 100 | | μV |
| P _{MAX} | Output Power per channel | VDDCP = 1.8 V, THD < 0.1%, R _L =16 Ω 1 kHz | | 28 | | mW _{RMS} |
| | | VDDCP = 2.5 V, THD < 0.1%, R _L =16 Ω 1 kHz | | 58 | | mW _{RMS} |
| | Dynamic internal supply voltages | VDD/3 or VDD/4 can optionally be selected if two flying caps are available | | ±VDD ±VDD/2 (±VDD/3 (±VDD/4) | | |
| I _Q | Quiescent current per channel | from VDDCP | | 100 | | uA |
| | Load Impedance | 13 < R _L < ∞ | 13 | 16 | 400 500 | Ω μH pF |
| | Frequency Response | +/- 0.5 dB | 20 | | 20k | |
| | Amplitude Ripple | 20 Hz – 20 kHz | -0.5 | | 0.5 | dB |
| | Programmable Gain | | -54 | | 15 | dB |
| | Mute Attenuation | | | 100 | | dB |
| | Programmable Gain Step Size | | | 1.5 | | dB |
| | Absolute Gain Accuracy | 0 dB @ 1 kHz | -0.8 | | 0.8 | dB |
| | Input Gain L/R-Mismatch | 20 Hz – 20 kHz | -0.1 | | 0.1 | dB |
| | Input Gain Step Error | 20 Hz – 20 kHz | -0.1 | | 0.1 | dB |
| SNR | Signal to Noise Ratio | A weighting, gain = 0 dB | | 100 | | dB |
| V _{NOISE} | Output Noise Level | 20 to 20 kHz, unweighted, gain < -15 dB | | <4.5 | | μV _{rms} |
| THD+N | Total Harmonic Distortion Plus Noise | VDDCP = 1.8 V, -5 dBFS, R _L =16 Ω | | -80 | | dB |
| PSRR with respect to AVDD | Power Supply Rejection Ratio | 20 Hz - 2 kHz | 70 | | | dB |
| | | 2 kHz - 20 kHz | 50 | | | |
| | Output power per channel | VDDCP=2.5 V, THD<1%, R _L =16 Ω, 1 kHz | | 72 | | mW |

Table 14: Electrical characteristics: Phase locked loop (MCLK)

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|--|--------------------------|--|--------|--------|--------|------------------|
| | Input Jitter | cycle to cycle | | | 35 | ps |
| | | rms | | | 100 | ps |
| | Input Impedance | DC impedance > 10 MΩ | 300 | 1 | 2 | Ω |
| | | | 0.5 | | | pF |
| Interface mode (MCLK is 256 Fs, PLL off) | | | | | | |
| F _{in} | Input frequency | 256 Fs 128 Fs (96 kHz) | 11.289 | | 12.288 | MHz |
| Oscillator mode (MCLK from standard oscillator, PLL on) | | | | | | |
| F _{in} | Input frequency | 12.0, 13.0, 13.5, 14.4, 19.2, 19.68 MHz (x 1, 2 or 4), 32 kHz mode | 10 | 32.768 | 80 | MHz |
| | | | | | kHz | |
| | I2S tracking range (SRM) | Maximum mismatch of I2S word-clock | | | 4 | % |
| | I2S clock drift | Maximum frequency drift of I2S word clock | | | 50 | ppm/s |
| V _{IN AC} | MCLK Shaper range | For AC coupling with internal clock shaping | 300 | 500 | 1000 | mV _{PP} |

Table 15: Electrical characteristics: Digital I/O

(Ta = -40 to +85°C)

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|---------------------------|---|--------------------------|-------------------------|---------------|-------------------------|------|
| V _{IH} | CLK, WCLK, DATIN, SK, nCS, SI, PD, MCLK, Input High Voltage | | 0.7*V _{DDDI} O | | V _{DDDI} O | V |
| V _{IL} | CLK, WCLK, DATIN, SK, nCS, SI, PD, MCLK, Input Low Voltage | | -0.3 | | 0.3*V _{DDDI} O | V |
| V _{OH @} 1 mA | CLK, WCLK, DATOUT Output High Voltage | | 0.8*V _{DDDI} O | | V _{DDDI} O | V |
| V _{OH} | SO (open drain mode) Output High Voltage | | | OPEN DRAIN | 3.6 | V |
| V _{OL @} 1 mA | CLK, WCLK, DATOUT Output Low Voltage | | 0 | | 0.3 | V |
| | MCLK Input High Voltage | DC-coupled TTL signal | 0.7*V _{DDDI} O | | V _{DDDI} O | V |
| | MCLK Input Low Voltage | | -0.3 | | 0.3*V _{DDDI} O | V |

7 Timing characteristics

7.1 Digital audio interface timing - I2S/DSP (in master/slave mode)

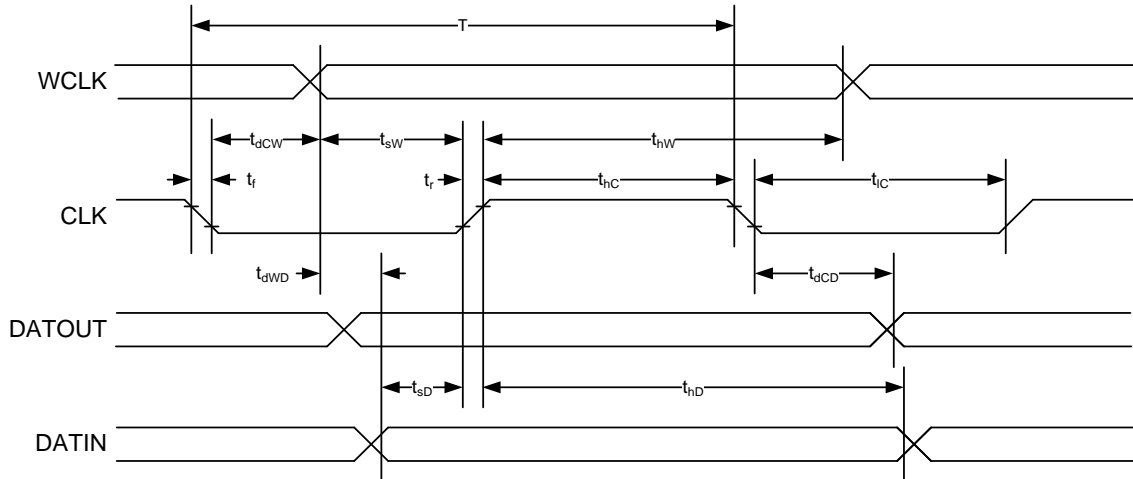
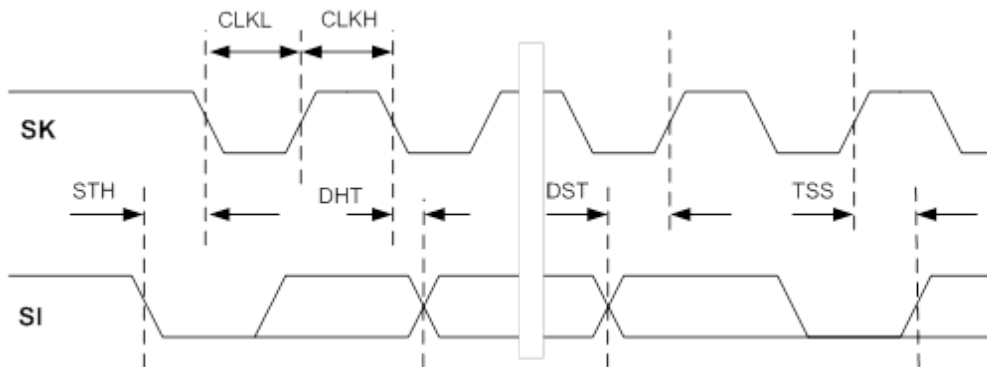


Figure 4: I2S/DSP timing diagram

Table 16: I2S/DSP timing characteristics

($T_a = -40$ to $+85^\circ\text{C}$)

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|-----------|----------------------|------------------------------|-------------------------------|-----|------|----------------|
| | Input impedance | DC impedance > 10 M Ω | 300 1.0 | | 2.5 | Ω pF |
| T | CLK period | | 75 | | | ns |
| t_r | CLK rise time | | | | 8 | ns |
| t_f | CLK fall time | | | | 8 | ns |
| t_{hC} | CLK high period | | 40% | | 60% | T |
| t_{lC} | CLK low period | | 40% | | 60% | T |
| t_{dCW} | CLK to WCLK delay | | -30% | | +30% | T |
| t_{dCD} | CLK to DATOUT delay | | -30% | | +30% | T |
| t_{hW} | WCLK high time | DSP mode | 100% | | | T |
| | | Non-DSP mode | Word length | | | T |
| t_{lW} | WCLK low time | DSP mode | 100% | | | T |
| | | Non-DSP mode | Word length | | | T |
| t_{sW} | WCLK setup time | Slave mode | 7 | | | ns |
| t_{hW} | WCLK hold time | Slave mode | 2 | | | ns |
| t_{sD} | DATIN setup time | | 7 | | | ns |
| t_{hD} | DATIN hold time | | 2 | | | ns |
| t_{dWD} | DATOUT to WCLK delay | | DATOUT is synchronised to CLK | | | |

7.2 Digital audio control timing - 2-wire control timing

Figure 5: 2-wire control timing diagram
Table 17: 2-wire control timing characteristics

(Ta = -40 to +85°C)

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|---------------------------|---------------------------------|------------|-----|-----|------|------|
| | Bus free time STOP to START | | 1.3 | | | μs |
| | Bus Line Capacitive load | | | | 100 | pF |
| Standard/Fast Mode | | | | | | |
| | SK clock frequency | | 1 | | 400 | kHz |
| | Bus free time STOP to START | | 1.3 | | | μs |
| | Start condition set-up time | | 0.6 | | | μs |
| STH | Start condition hold time | | 0.6 | | | μs |
| CLKL | SK low time | | 1.3 | | | μs |
| CLKH | SK high time | | 0.6 | | | μs |
| | 2-wire SK and SI rise/fall time | | | | 300 | ns |
| DST | SI set-up time | | 100 | | | ns |
| DHT | SI hold-time | | 0 | | | ns |
| TSS | Stop condition set-up time | | 0.6 | | | μs |
| High Speed Mode | | | | | | |
| | SK clock frequency | | 1 | | 1700 | kHz |
| | Start condition set-up time | | 160 | | | ns |
| STH | Start condition hold time | | 160 | | | ns |
| CLKL | SK low time | | 160 | | | ns |
| CLKH | SK high time | | 60 | | | ns |
| | HS-2-wire SK rise/fall time | | | | 40 | ns |
| | HS-2-wire SI rise/fall time | | | | 80 | ns |
| DST | SI set-up time | | 10 | | | ns |
| | SI hold-time | | 0 | | | ns |
| TSS | Stop condition set-up time | | 16 | | | ns |

7.3 Digital audio interface timing - 4-wire control timing

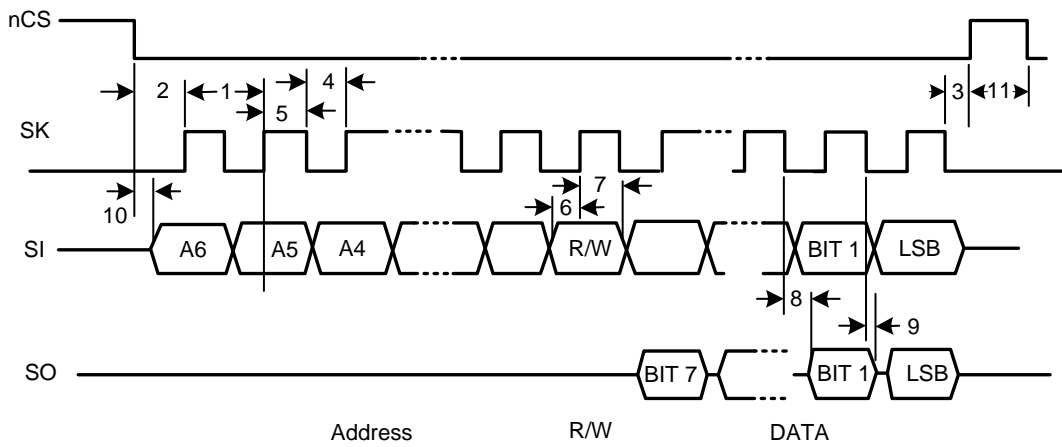


Figure 6: 4-wire control timing diagram

Timing shown is valid for active low and active high CS.

Table 18: 4-wire control timing characteristics

(Ta = -40 to +85°C)

| Parameter | Description | Label in plot | Min | Typ | Max | Unit |
|-----------|---------------------|------------------------------------|----------|-----|-----|------|
| tc | Cycle time | 1 | 70 | | | ns |
| tcSS | Enable lead time | 2, from CS active to first SK edge | 20 | | | ns |
| tscs | Enable lag time | 3, from last SK edge to CS idle | 20 | | | ns |
| tCL | Clock low time | 4 | 0.4 x tc | | | ns |
| tCH | Clock high time | 5 | 0.4 x tc | | | ns |
| tSIS | Data In setup time | 6 | 5 | | | ns |
| tSIH | Data In hold time | 7 | 5 | | | ns |
| tSOV | Data Out valid time | 8 | | | 22 | ns |
| tSOH | Data Out hold time | 9 | 6 | | | ns |
| tH | Data access time | 10 | | | 22 | ns |
| twCS | CS inactive time | 11 | 20 | | | ns |

Table 19: Start-up times after setting SC_MST_EN = 1

| Source | Output | Comment | Min | Typ | Max | Unit |
|--------------------------------|---------|---|-----|-----|-----|------|
| | VBG | VBG voltage >90% with 1 μF VBG capacitor | | 25 | | ms |
| All analogue inputs and DACL/R | HPL/R | Slave mode; 200 ms added delay required | 200 | 200 | | ms |
| All analogue inputs and DACL/R | HPL/R | 32 kHz PLL master mode; 200 ms added delay required | | 500 | | ms |
| All analogue inputs and DACL/R | OUT1L/R | Slave mode | | 250 | | ms |
| All analogue inputs | ADCL/R | Slave mode | | 200 | | ms |

Ultra-low power stereo codec

| Source | Output | Comment | Min | Typ | Max | Unit |
|---------------------|--------|------------------------|-----|-----|-----|------|
| All analogue inputs | ADCL/R | 32 kHz PLL master mode | | 600 | | ms |

8 Functional description

DA7210 is an ultra-low power audio codec with a true ground headphone, mixing capability and a programmable ASSP filter engine. It offers Hi-Fi audio quality with class-leading power consumption for portable media applications.

Featuring a high-efficiency headphone amplifier and a minimum supply voltage of 1.8 V, the ultra-low 2.5 mW power consumption extends music playback time for battery operated equipment.

The integrated PLL uses a FRACT-N PLL architecture that supports a large range of input and output frequencies. This can accept standard mobile phone/USB system clock frequencies, thus enabling audio data synchronisation when no master clock is readily available.

Eight analogue input pins allow multiple audio sources to be internally mixed, eliminating the need for external switches. Both single-ended and fully-differential line and microphone inputs are supported with built-in variable gain amplifiers to optimise dynamic range prior to digitisation. This allows a diverse variety of analogue audio sources such as baseband voice, mobile TV, Wi-Fi and FM radio to be managed.

Input and output mixers with stereo-to-mono conversion also support mono configurations such as headset/baseband line outputs.

Three output drivers are available in the output stage of the DA7210. One output driver will directly drive standard 3-wire 16 Ω headphones whilst the other two provide two adjustable, fully differential stereo lineout channels. For example the dc-coupled, dedicated pop-free drivers may be connected simultaneously to stereo headphones, stereo speakers and a mono line out without external switches.

All filtering and sidetone functions are performed digitally including 5-band EQ and a digital input AGC with programmable attack and decay parameters.

The multi-slot I2S/PCM interface supports all common sample rates between 8 and 96 kHz in master or slave modes.

8.1 Stereo codec

8.1.1 Input signal chain

The DA7210 has three flexible stereo analogue inputs that can be set up as line inputs, microphone inputs, or both. They can be configured as differential or single ended. Line inputs (AUX1_L/R and AUX2_P/N) and microphone outputs can be routed to the ADC or directly to the output mixers via a bypass path.

Ultra-low power stereo codec

8.1.2 Microphone inputs

The DA7210 includes two analogue microphone inputs, which can be used as a stereo or two mono microphones. These can either be connected in (i) fully differential mode for improved common mode noise rejection and (ii) single ended or in pseudo-differential (by connecting MICN to GND). The larger signal should be always connected to MICPL or MICPR and the smaller should be connected to MICNL or MICNR.

The microphone PGAs are enabled by the MIC_L_EN/MIC_R_EN controls (address 0x07/0x08, (Table 48 and Table 49). For maximum flexibility each microphone channel includes an individual gain setting MIC_L_VOL (address 0x7, Table 48), which have a range of -6 dB to +24 dB in 6 dB steps. A maximum gain from microphone to ADC input of +42 dB can be selected with a resolution of 1.5 dB.

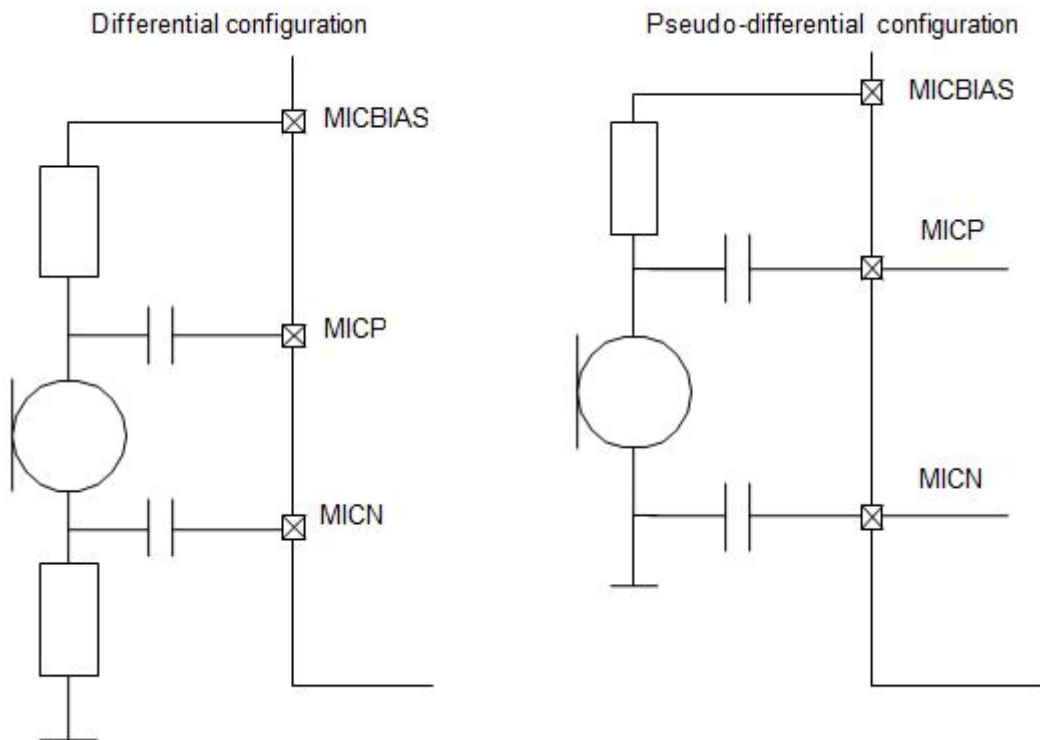


Figure 7: Typical microphone applications

Standard electret microphones can be supplied from an on chip microphone bias. This generates an ultra-low noise voltage to feed several electret microphones with up to 2 mA. Depending on the provided AVDD level, the bias voltage can be configured via MICBIAS_SEL (address 0x07, Table 48). If it is not needed then the microphone bias can be powered down using MICBIAS_EN (address 0x07, Table 48).

8.1.3 Auxiliary inputs

Standard analogue sources are supported via the stereo line inputs AUX1. Mono sound sources are intended to be connected to the differential auxiliary line input AUX2 or alternatively the right channel of AUX1.

Enabled via AUX1_L_EN (Address 0x09, Table 50), AUX1_R_EN (Address 0x0A, Table 51) and AUX2_EN (Address 0x0B, Table 52), auxiliary inputs can be summed with each other and with the microphone paths, which enables a flexible audio mixing (see Figure 15).

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A maximum gain from auxiliary to ADC input of +39/36 dB with a resolution of 1.5 dB can be selected. The gain describes the overall input signal to output signal ratio (independent whether the path is single ended or differential).

8.1.4 Stereo audio ADC

DA7210 includes a low power 24 bit high quality stereo audio ADC, which uses a continuous time delta-sigma modulator providing improved robustness against uncorrelated environmental noise. The ADC supports sampling rates from 8 kHz to 96 kHz. A master clock has to be provided at MCLK whenever the ADC or DAC are in operation.

Dependent on the intended recording path, the stereo ADC can power down one channel at a time via controls ADC_L_EN and ADC_R_EN (address 0x10, [Table 57](#)) to provide optimal power dissipation. To enable saturation free maximum signal-to-noise, the input levels of the ADC are adjusted with input PGAs.

The inputs to left and right input mixers are controlled by the bits in the INMIX_L and INMIX_R registers (addresses 0x0D and 0x0E, [Table 54](#) and [Table 55](#)). Gain settings for the left and right PGAs are controlled by INPGA_L_VOL and INPGA_R_VOL (address 0x0C, [Table 53](#)) with a range of 4.5 dB to 18 dB with 1.5 dB resolution.

For smooth volume changes the gain update can be synchronised to signal zero crossings enabled using INZX_L_EN and INZX_R_EN (address 0x24, [Table 77](#)). Disabling the left ADC saves power for mono recordings of stereo input signals by using the analogue stereo to mono conversion from the input mixer. This configuration requires setting the INPGA_L_VOL to 0 dB ('0011') and the assertion of IN_R_IN_L (address 0x0E, [Table 55](#)).

The IIR filters are enabled using ADC_HPF_EN (address 0xF, [Table 56](#), and see blocks 'ADC HP' in [Figure 16](#)). The filters (typ. <2 Hz roll-off) are configurable by control ADC_HPF_F0 (address 0x0F, [Table 56](#)) and, if enabled, will remove any DC offset from the input path. After Reset, the filters for both channels are enabled by default. Enabling the high pass filter is especially important if the ADC output is fed back into the DAC.

By default the ADC bias current is minimised, but it is possible to improve the THD+N performance of the ADC by approximately 4 dB by increasing this current. The bias current is increased by setting the ADC_T2 bit (address 0x95[3], [Table 182](#)).

Also by default the VMID buffer current is enabled for DAC operation, but this buffer is not required for analogue only paths and for ADC only operation. The VMID bias current can be disabled by setting the VMID_BUFF_EN bits (address 0x96[2:0], [Table 183](#)) and a significant power saving can be made.

Table 20: ADC digital high pass filter specifications

| Sampling frequency (kHz) | Cut-off frequency (Hz) at ADC_HPF_F0 setting | | | |
|--------------------------|--|-----|-----|------|
| | 00 | 01 | 10 | 11 |
| 48 | 2 | 4 | 8 | 16 |
| 44.1 | 1.8 | 3.7 | 7.3 | 14.7 |
| 32 | 1.3 | 2.7 | 5.3 | 10.7 |
| 24 | 1 | 2 | 4 | 8 |
| 22.05 | 0.9 | 1.8 | 3.7 | 7.3 |
| 16 | 0.7 | 1.3 | 2.7 | 5.3 |
| 12 | 0.5 | 1 | 2 | 4 |
| 11.025 | 0.4 | 0.9 | 1.8 | 3.7 |
| 8 | 0.3 | 0.7 | 1.3 | 2.7 |

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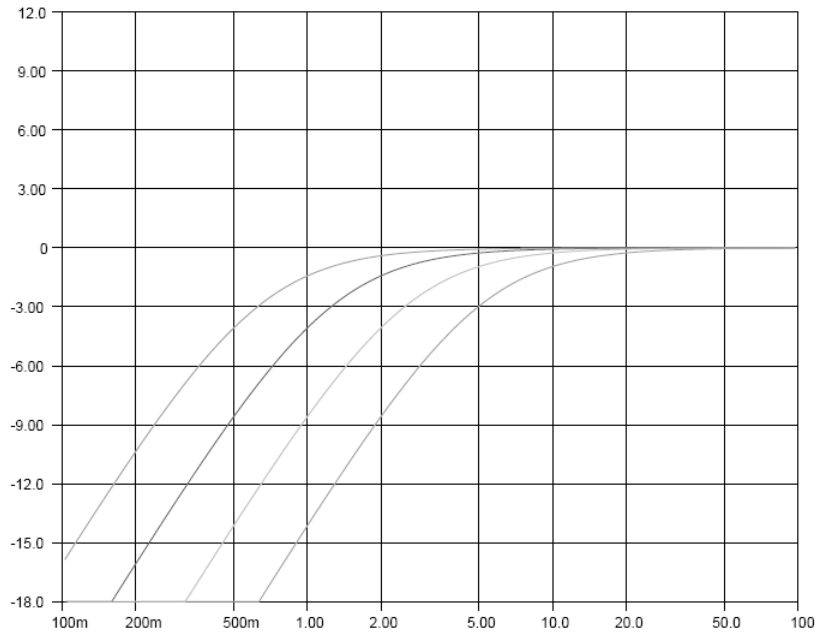


Figure 8: ADC and DAC DC blocking (cut-off frequency setting '00' to '11', 16 kHz)

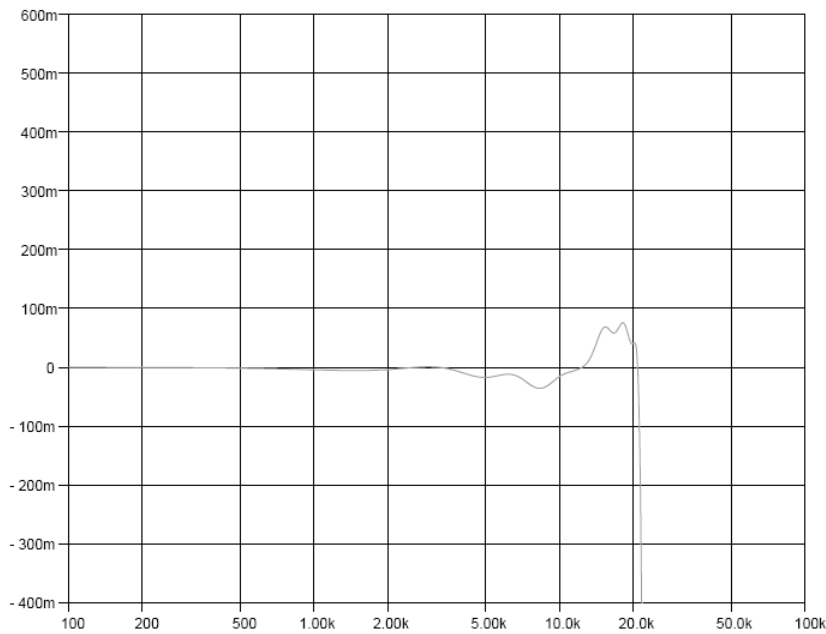


Figure 9: ADC pass band attenuation (audio mode, 48 kHz)

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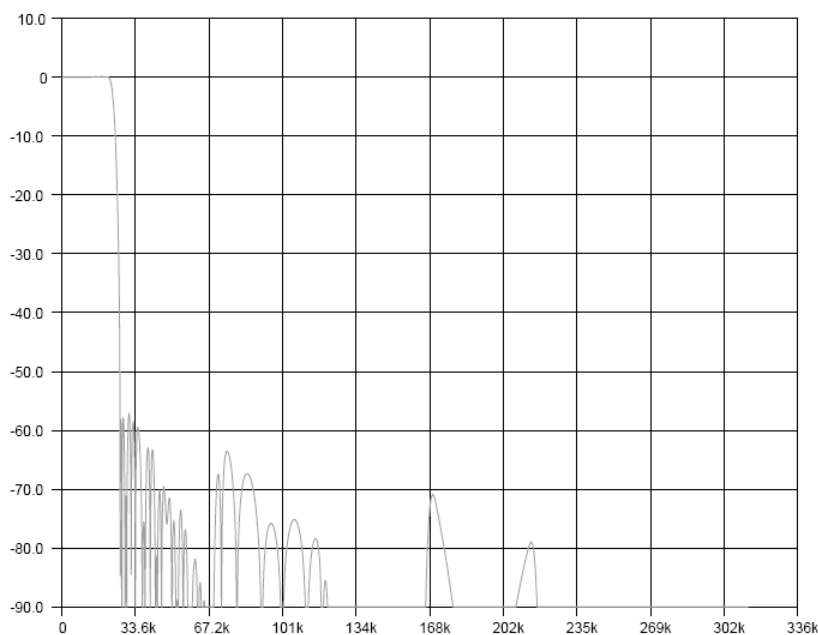


Figure 10: ADC pass band suppression (audio mode, 48 kHz)

8.1.5 Automatic level control (ALC)

For improved sound recordings of signals with a widely changing loudness the DA7210 offers an automatic recording level control (ALC).

It is enabled via ALC_EN (address 0x10, Table 57) and monitors the analogue signal before it enters the ADC and adapts the input gain to keep a constant recording volume irrespective of the analogue input signal level.

Figure 11 (below) illustrates the operation of the ALC. It shows an input signal with high level. The output level is reduced when its level is above the upper threshold, and increased when it falls below the minimum threshold.

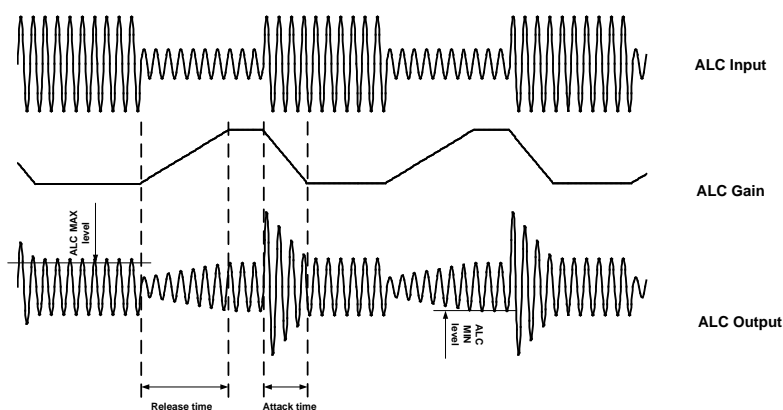


Figure 11: Operation of ALC

If this absolute value of an analogue signal is greater than ALC_MAX (address 0x83, Table 172), then the gain is ramped down at a rate determined by the ALC_ATT (address 0x86, Table 175).

If this absolute value is lower than a level set in ALC_MIN (address 0x84, Table 173), the gain is ramped up at a rate determined by ALC_REL (address 0x87, Table 176).

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ALC_MAX needs to be greater than ALC_MIN (minimum delta 1.5 dB). The target level is best achieved by setting these values close to each other. A wider delta allows for a larger input range, and that will reduce the ALC activity. The value of ALC_REL is configured in increments of 4 sample periods. The gain-ramping is performed inside the input PGA in steps of 1.5 dB. To prevent audible clicks each analogue gain step is interpolated by 8 digital volume steps of 0.25 dB inside the ADC (the rate refers to the intermediate steps inside the ADC). However, the level must be lower than ALC_MIN for a time greater than the hold time in order for this gain increase to take place.

The hold time is determined by ALC_DEL (address 0x88, [Table 177](#)) in increments of ALC_REL periods, which allows long hold periods to be programmed for a reduction of potential 'gain pumping' during dynamic signal content.

For ALC noise value, refer to [Table 21](#).

Table 21: Permitted register values for ALC_NOIS (0x85 [5:0])

| Dec | Bin | Hex | Level (dB) | Dec | Bin | Hex | Level (dB) |
|-----|--------|-----|------------|-----|--------|-----|------------|
| 60 | 111100 | 3C | -0.5 | 29 | 011101 | 1D | -47 |
| 59 | 111011 | 3B | -2 | 28 | 011100 | 1C | -48.5 |
| 58 | 111010 | 3A | -3.5 | 27 | 011011 | 1B | -50 |
| 57 | 111001 | 39 | -5 | 26 | 011010 | 1A | -51.5 |
| 56 | 111000 | 38 | -6.5 | 25 | 011001 | 19 | -53 |
| 55 | 110111 | 37 | -8 | 24 | 011000 | 18 | -54.5 |
| 54 | 110110 | 36 | -9.5 | 23 | 010111 | 17 | -56 |
| 53 | 110101 | 35 | -11 | 22 | 010110 | 16 | -57.5 |
| 52 | 110100 | 34 | -12.5 | 21 | 010101 | 15 | -59 |
| 51 | 110011 | 33 | -14 | 20 | 010100 | 14 | -60.5 |
| 50 | 110010 | 32 | -15.5 | 19 | 010011 | 13 | -62 |
| 49 | 110001 | 31 | -17 | 18 | 010010 | 12 | -63.5 |
| 48 | 110000 | 30 | -18.5 | 17 | 010001 | 11 | -65 |
| 47 | 101111 | 2F | -20 | 16 | 010000 | 10 | -66.5 |
| 46 | 101110 | 2E | -21.5 | 15 | 001111 | 0F | -68 |
| 45 | 101101 | 2D | -23 | 14 | 001110 | 0E | -69.5 |
| 44 | 101100 | 2C | -24.5 | 13 | 001101 | 0D | -71 |
| 43 | 101011 | 2B | -26 | 12 | 001100 | 0C | -72.5 |
| 42 | 101010 | 2A | -27.5 | 11 | 001011 | 0B | -74 |
| 41 | 101001 | 29 | -29 | 10 | 001010 | 0A | -75.5 |
| 40 | 101000 | 28 | -30.5 | 9 | 001001 | 09 | -77 |
| 39 | 100111 | 27 | -32 | 8 | 001000 | 08 | -78.5 |
| 38 | 100110 | 26 | -33.5 | 7 | 000111 | 07 | -80 |
| 37 | 100101 | 25 | -35 | 6 | 000110 | 06 | -81.5 |
| 36 | 100100 | 24 | -36.5 | 5 | 000101 | 05 | -83 |
| 35 | 100011 | 23 | -38 | 4 | 000100 | 04 | -84.5 |
| 34 | 100010 | 22 | -39.5 | 3 | 000011 | 03 | -86 |
| 33 | 100001 | 21 | -41 | 2 | 000010 | 02 | -86 |
| 32 | 100000 | 20 | -42.5 | 1 | 000001 | 01 | -86 |
| 31 | 011111 | 1F | -44 | 0 | 000000 | 00 | -86 |
| 30 | 011110 | 1E | -45.5 | | | | |

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Examples for ALC_ATT (address 0x86, [Table 175](#)).

(fs=44.1 kHz; sample period = 22.67 μs)

| Setting | ms per 1 dB step |
|---------------|------------------|
| 11111111 (FF) | 23.2 |
| 10111111 (BF) | 17.4 |
| 01111111 (7F) | 11.6 |
| 00111111 (3F) | 5.8 |
| 00011111 (1F) | 2.9 |
| 00001111 (0F) | 1.5 |
| 00000100 (04) | 0.5 |

Examples for ALC_REL (address 0x87, [Table 176](#)).

(fs=44.1 kHz; sample period = 22.67 μs)

| Setting | ms per 1 dB step |
|---------------|------------------|
| 11111111 (FF) | 92.9 |
| 10111111 (BF) | 69.7 |
| 01111111 (7F) | 46.4 |
| 00111111 (3F) | 23.2 |
| 00011111 (1F) | 11.6 |
| 00001111 (0F) | 5.8 |
| 00000100 (04) | 0.5 |

8.1.6 Noise gate

A noise gate feature is provided to avoid 'noise pumping' where the gain of the channel is increased to the maximum when there is no signal is present (that is only noise). If the level of the input signal drops below the threshold configured inside control ALC_NOIS (address 0x85, [Table 174](#)) the channel gain is held.

8.2 Output signal chain

8.2.1 Stereo audio DAC

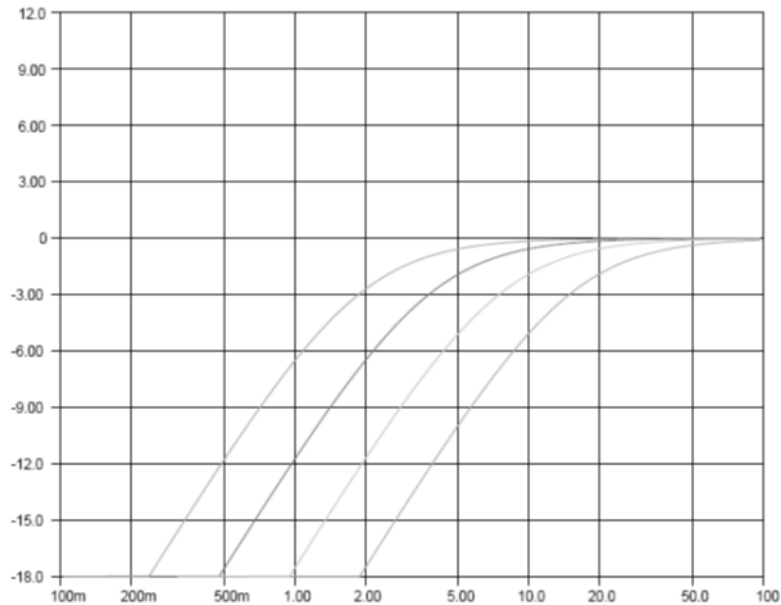
The integrated stereo DAC is suitable for high quality audio playback of MP3 files and portable multimedia files of all kinds. The DAC has individually enabled channels via controls DAC_L_EN and DAC_R_EN (address 0x17, [Table 64](#)).

The DA7210 supports the option of individually phase inverted output signals using controls DAC_L_INV (address 0x15, [Table 62](#)).and DAC_R_INV (address 0x16, [Table 63](#)).

A digital high pass filter for each DAC channel is implemented (configurable by control DAC_HPF_F0 (address 0x14, [Table 61](#)) that can be enabled via control DAC_HPF_EN (address 0x14, [Table 61](#), see blocks 'DAC HP' in [Figure 16](#)). After Reset, the high pass filters for both channels are enabled by default.

Table 22: DAC digital high pass filter specifications

| Sampling frequency (kHz) | Cut-off frequency (Hz) at DAC_HP_F0 setting | | | |
|--------------------------|---|-----|-----|------|
| | 00 | 01 | 10 | 11 |
| 48 | 2 | 4 | 8 | 16 |
| 44.1 | 1.8 | 3.7 | 7.3 | 14.7 |
| 32 | 1.3 | 2.7 | 5.3 | 10.7 |
| 24 | 1 | 2 | 4 | 8 |
| 22.05 | 0.9 | 1.8 | 3.7 | 7.3 |
| 16 | 0.7 | 1.3 | 2.7 | 5.3 |
| 12 | 0.5 | 1 | 2 | 4 |
| 11.025 | 0.4 | 0.9 | 1.8 | 3.7 |
| 8 | 0.3 | 0.7 | 1.3 | 2.7 |


Figure 12: DAC DC blocking (cut-off frequency setting '00' to '11', 48 kHz)

8.2.2 Soft mute

To improve the user's perception of audio reconfigurations, the DAC channel signals may be soft muted by asserting control `SOFT_MUTE` (address 0x18, [Table 65](#)). The soft mute function attenuates the digital input to the DAC, ramping the gain down in steps of 0.1875 dB from the nominal level to -77.25 dB, before completely muting the channel.

When `SOFT_MUTE` is released, the attenuation is set to -77.25 dB, and then ramped up to the initial gain. Both left and right channels are muted simultaneously. The ramping speed is dependent on the audio sample rate and can be configured by control `MUTE_RATE` (address 0x18, [Table 65](#)). Status bits `SOFTMUTED` and `MUTING` may be read from the system status register (address 0x02, [Table 44](#)).

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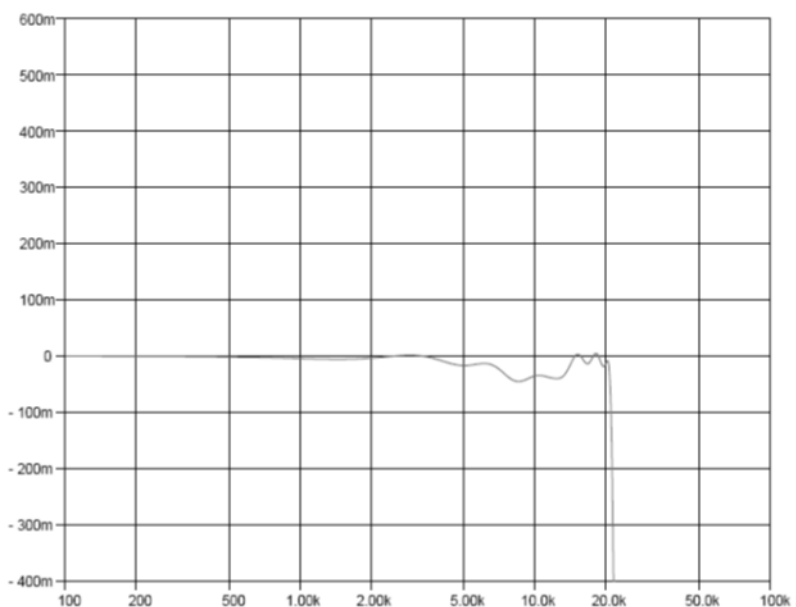


Figure 13: DAC pass band attenuation (audio mode, 48 kHz)

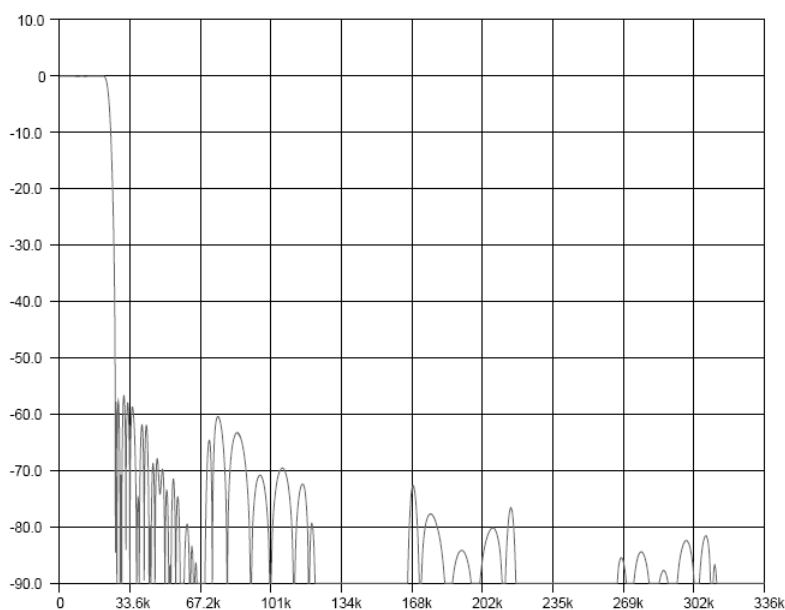


Figure 14: DAC pass band suppression (audio mode, 48 kHz)

8.2.3 Output mixer and line-out amplifier

For playback the output mixer has to be enabled via OUT1_L_EN and OUT1_R_EN (addresses 0x1C, [Table 69](#) and 0x1D, [Table 70](#)). The audio signal can be mixed from all sources and listened to via headphones/speakers and recorded simultaneously if required.

OUTMIX_L and OUTMIX_R (addresses 0x1C, [Table 69](#) and 0x1D, [Table 70](#)) are independent of the input path, thus allowing recording of a different audio signal when listening to stereo sources like FM Radio or MP3 playback. The playback sound can be mixed with background or inverted background microphone signals (side tone) to enable a basic headphone environmental noise reduction or to compensate unwanted damping of environmental sound happening with sealed headphones. Playback signals can be inverted individually for left and right channel via OUT_L_INV (address 0x1C, [Table 69](#)), OUT_R_INV (address 0x1D, [Table 70](#)) or for playback of signals from the DAC via DAC_L_INV/DAC_R_INV (address 0x15, [Table 62](#)).

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A stereo to mono conversion can either be realised by the input or the output mixer. This allows direct feeding of phone earpiece receivers, high power speaker amplifiers and other mono devices with the complete audio content. Unused channels of the stereo line out can be switched off to reduce power consumption using OUT1_L_EN (address 0x1E, [Table 71](#)) and OUT1_R_EN (address 0x1F, [Table 72](#)). The mixer allows listening to mono signals like baseband or Bluetooth voice also at both channels of stereo headphones.

Each differential channel of OUT1 can alternatively be individually configured to be single ended via OUT1_L_SE (address 0x1E, [Table 71](#)) and OUT1_R_SE (address 0x1F, [Table 72](#)). Typical earpiece receivers with an impedance $> 32 \Omega$ can be driven directly in differential mode at all outputs. This amplifier offers individual programmable volume control from +15 dB to -54 dB in 1.5 dB steps, then mute for steps below -54 dB using controls OUT1_L_VOL (address 0x1E, [Table 71](#)) and OUT1_R_VOL (address 0x1F, [Table 72](#)). For smooth volume changes, the gain update can be synchronised to zero-crossing of the signal using OUTZX_L_EN and OUTZX_R_EN (address 0x24, [Table 77](#)). If no zero-crossing is detected within 2048 sample periods, the gain change is applied unconditionally. The left and right channels are synchronised independently.

The differential AUX2 and the line output OUT2 provide a separate voice link like required to support analogue audio of baseband modules used in smart or VoIP phones. OUT2 is enabled via OUT2_EN (Address 0x20, [Table 73](#)) and is able to select via OUT2_OUTMIX_R/OUT2_OUTMIX_L either the left or right channel of the output mixer or via OUT2_IN_R/OUT2_IN_L (Address 0x20, [Table 73](#)) a signal from the input mixer. The gain is adjusted via control OUT2_VOL (Address 0x20, [Table 73](#)).

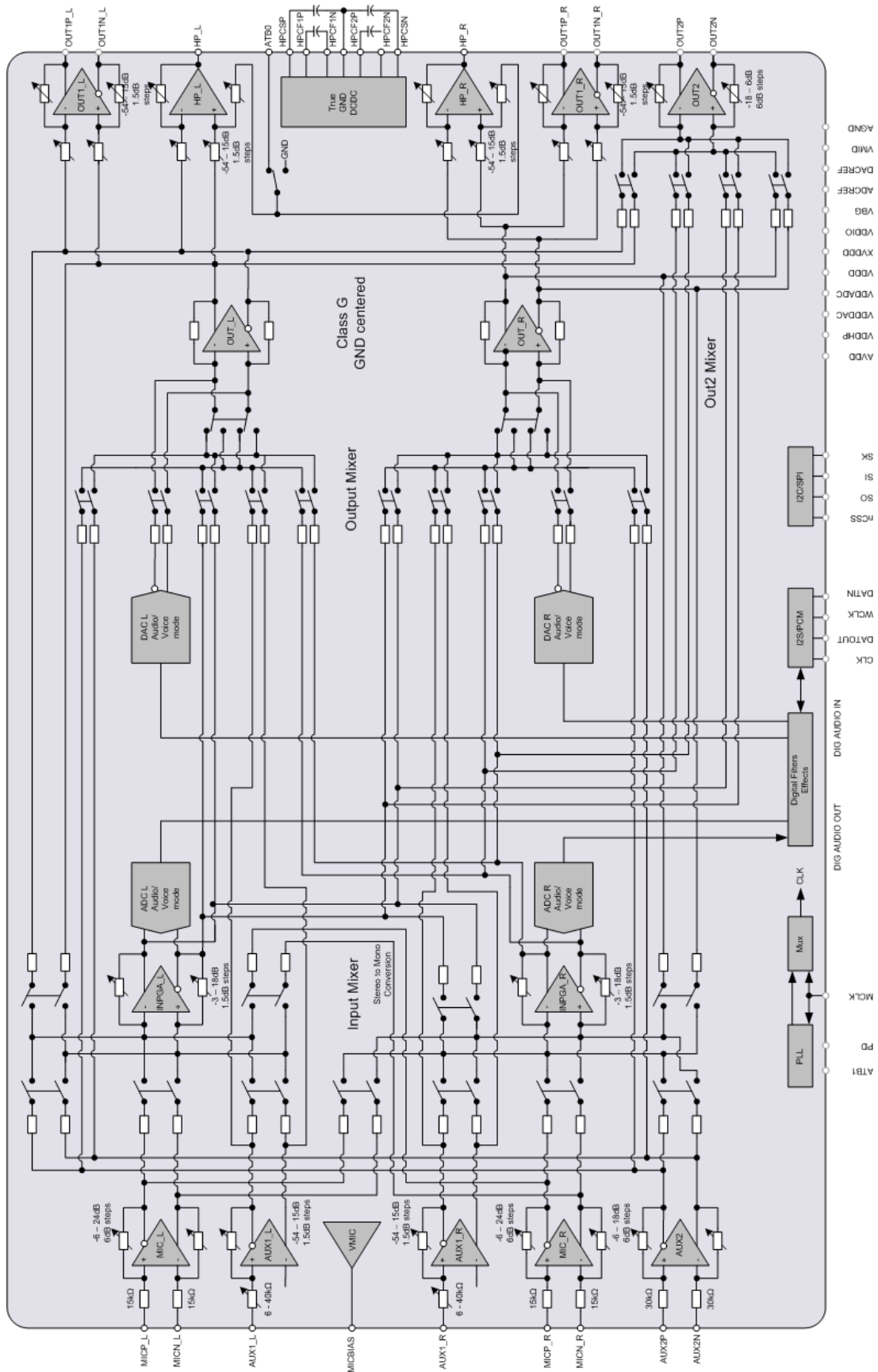


Figure 15: DA7210 audio signal paths

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8.2.4 Headphone amplifier

The headphone Class G amplifiers are enabled by controls HP_L_EN and HP_R_EN (address 0x23, [Table 76](#)) and their output can be set to high impedance mode using HP_HIGHZ_L and HP_HIGHZ_R (address 0x23, [Table 76](#)).

They offer 'true ground' technology, which allows cost and space optimisation by removing the need for large capacitors in the headphone paths. This also enhances the bass performance, which is typically reduced by conventional AC-coupling. In comparison to alternative approaches like 'phantom ground', the 'true ground' technology generates real ground-centred output signals, and provides common GND as required for Mini-USB connectors and CEA-936-A compliant interfaces.

Integrated short-circuit protection enables a 'resistors free' connection to a standard audio jack to achieve a maximum output power of up to 58 mW per channel (referenced to VDDCP). The output mixing units enable the support of single-ended mono and stereo, as well as differential headphones selected by OUT_R_INV (address 0x1D, [Table 70](#)).

Headphone load impedance is typically 16 Ω, but the paths can also be used as volume controlled lineout signals for external speaker amplifiers and audio devices. The headphone Class G amplifiers are supplied from the positive VDDCP rail via a capacitive charge pump that generates the negative rail required for 'true ground' mode. For improved power efficiency it provides dynamically adjusted supply voltage levels VDD, VDD/2, VDD/3 and VDD/4, which are automatically adjusted by DA7210 from the average left and right level of the headphone audio signals see control HP_CFG (address 0x23, [Table 76](#)).

To minimise the number of external components the charge pump provides a restricted mode enabled via HP_2CAP_MODE (address 0x23, [Table 76](#)) which removes the need for the second flying cap (at pins HPCF2P and HPCF2N), but disables the VDD/3 and VDD/4 supply voltage levels.

Unlike conventional solutions DA7210 does not require any coupling capacitors at the 'true ground' headphone amplifier input. An embedded offset compensation circuit suppresses click and pop noise during both start-up and dynamic supply-voltage adjustments.

Table 23: Headphone/OUT1 amplifier gain settings

| GAIN | CODE | | GAIN | CODE | | GAIN | CODE |
|---------|------|--|---------|------|--|--------|------|
| MUTE | 0x10 | | -31.5dB | 0x20 | | -7.5dB | 0x30 |
| -54.0dB | 0x11 | | -30.0dB | 0x21 | | -6.0dB | 0x31 |
| -52.5dB | 0x12 | | -28.5dB | 0x22 | | -4.5dB | 0x32 |
| -51.0dB | 0x13 | | -27.0dB | 0x23 | | -3.0dB | 0x33 |
| -49.5dB | 0x14 | | -25.5dB | 0x24 | | -1.5dB | 0x34 |
| -48.0dB | 0x15 | | -24.0dB | 0x25 | | 0dB | 0x35 |
| -46.5dB | 0x16 | | -22.5dB | 0x26 | | 1.5dB | 0x36 |
| -45.0dB | 0x17 | | -21.0dB | 0x27 | | 3.0dB | 0x37 |
| -43.5dB | 0x18 | | -19.5dB | 0x28 | | 4.5dB | 0x38 |
| -42.0dB | 0x19 | | -18.0dB | 0x29 | | 6.0dB | 0x39 |
| -40.5dB | 0x1A | | -16.5dB | 0x2A | | 7.5dB | 0x3A |
| -39.0dB | 0x1B | | -15.0dB | 0x2B | | 9.0dB | 0x3B |
| -37.5dB | 0x1C | | -13.5dB | 0x2C | | 10.5dB | 0x3C |
| -36.0dB | 0x1D | | -12.0dB | 0x2D | | 12.0dB | 0x3D |
| -34.5dB | 0x1E | | -10.5dB | 0x2E | | 13.5dB | 0x3E |
| -33.0dB | 0x1F | | -9.0dB | 0x2F | | 15.0dB | 0x3F |

[Table 23](#) relates to the registers shown below

- HP_L_VOL: 0x21[5:0]
- HP_R_VOL: 0x22[5:0]
- OUT1_L_VOL: 0x1e[5:0]

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- OUT1_R_VOL: 0x1f[5:0]

To enable volume balance settings the gain of the headphone buffers can be programmed independently for both channels by controls HP_L_VOL (addresses 0x21, and HP_R_VOL (addresses 0x22, [Table 75](#)) according to [Table 23](#). The gain steps are 1.5 dB from +15 dB down to -54 dB, and mute for the steps below -54 dB. Alternatively the channels' gain settings can be combined with bit STEREO_TRACK (address 0x23, [Table 76](#)) and controlled for both channels with volume register HP_R_VOL (address 0x22, [Table 75](#)).

For smooth volume changes the gain update can be synchronised to audio signal zero-crossings by enabling HPZX_L_EN and HPZX_R_EN (address 0x24, [Table 77](#)). If no zero-crossing is detected within 2048 sample periods, the gain change is applied unconditionally. The left and right channels are synchronised independently.

The headphone outputs are supported by DC offset compensation circuitry to minimise any possible pop and click artefacts during power up/down. To ensure sufficient time for the DC compensation circuitry to operate, a delay of 200 ms must be added after SC_MST_EN (address 0x03, [Table 45](#)) bit is enabled.

8.2.5 Ambient noise suppression

DA7210 supports stereo noise suppression by subtracting inverted noise signals from the AUX1 inputs at the headphone outputs. The noise signal must pass through the input PGA, be inverted and then mixed with the outputs from the DAC. The signal at the AUX1 inputs for example, can be from microphones picking up ambient noise at the user's ears.

This mode is enabled via control NOISE_SUP (address 0x01 CONTROL, [Table 43](#)) and then offers a modified headphones volume control via a combination of three gain stages:

- Headphones gain settings > 0 dB

All headphone gains settings > 0 dB will be applied to the headphone PGA, but the equivalent gain will be synchronously subtracted from the input PGA to equalise the overall net gain in the ambient noise signal path.

For sufficient range of operation, the starting values of INPGA_L_VOL and INPGA_R_VOL (address 0x0C, must be configured ≥ 10.5 dB (settings 1010 to 1111) before enabling the noise suppression mode.

- Headphones gain settings ≤ 0 dB

When DAC is selected to the headphone output any update of the gain less than or equal to 0 dB, using controls HP_L_VOL/HP_R_VOL (address 0x21, [Table 74](#) and address 0x22, [Table 75](#)), will be implemented instead using the controls DAC_L_GAIN and DAC_R_GAIN (address 0x15, [Table 62](#) and address 0x16, [Table 63](#)). If this were not the case then a large signal on AUX1 could cause clipping at the headphone output.

For the ambient noise signals from the AUX1 path all headphones gain changes ≤ 0 dB will be implemented using the settings of AUX1_L_VOL and AUX1_R_VOL (address 0x09, [Table 50](#)). To allow the full minimum headphone volume of -54 dB, these AUX1_L_VOL and AUX1_R_VOL controls need to be set to ≥ 6 dB (setting > 110101) before enabling the noise suppression mode.

NOTE – The ALC has to be disabled during noise suppression mode and it is recommended to enable zero-crossing for gain updates at the headphone amplifier and the AUX1 PGA (see the register ZEROX (address 0x24, [Table 77](#))). Headphone volume changes should enable digital gain ramping for DAC playback. The controls INPGA_L_VOL, INPGA_R_VOL, AUX1_L_VOL, AUX1_R_VOL, DAC_L_GAIN, and DAC_R_GAIN should not be written to when noise suppression is enabled.

8.2.6 Digital signal processing engine

The digital signal processing engine includes a configurable audio processor that offers flexible routing and extensive audio enhancement and effects. Linear phase FIR filters perform the interpolation and decimation for the required sigma-delta sample rates. Configurable high-pass

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filtering (optionally enabled) removes any signal DC offset (see blocks 'ADC HP' and 'DAC HP' in Figure 16) and offers 5-band equalisation during recording and sound playback.

Alternatively it can provide dedicated voice band filtering at samples rates ≤ 16 kHz (see blocks 'ADC IIR' and 'DAC IIR' in Figure 16).

An additional general purpose (GP) filter engine offers up to eight second-order biquad filter stages with configurable 16-bit coefficients, and supports flexible digital audio routing and mixing arrangements. Figure 16 shows some possible routings (a subset of the available settings) for filter blocks GP1A to GP2D with the related control registers. Typical use cases with example configurations are explained in the section 8.3.

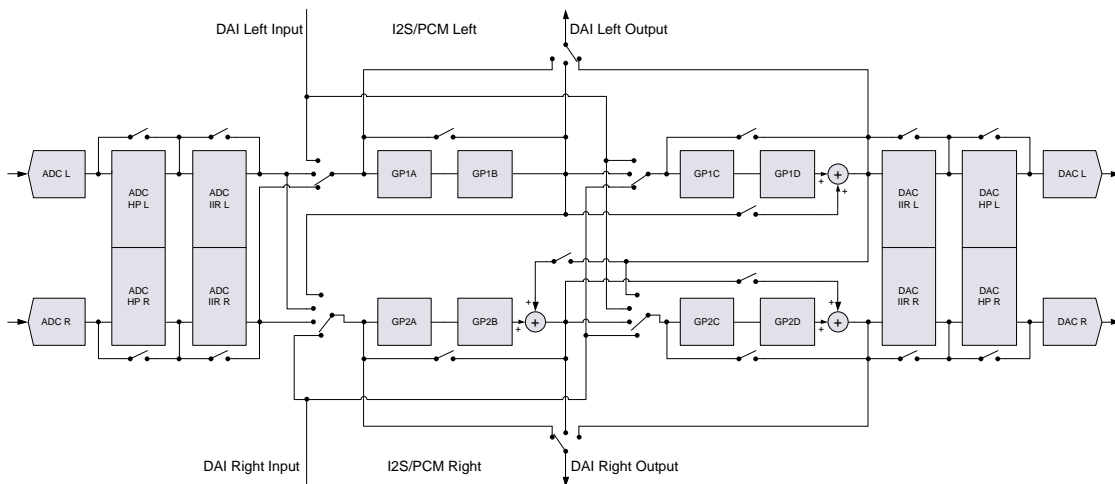


Figure 16: Digital signal processing engine (simplified block diagram)

The GP filter sections are implemented using a Direct Form 1 architecture, as shown in Figure 17.

This structure implements the transfer function:

$$H(z) = \frac{a_0 + a_1 z + a_2 z^2}{1 - b_1 z - b_2 z^2}$$

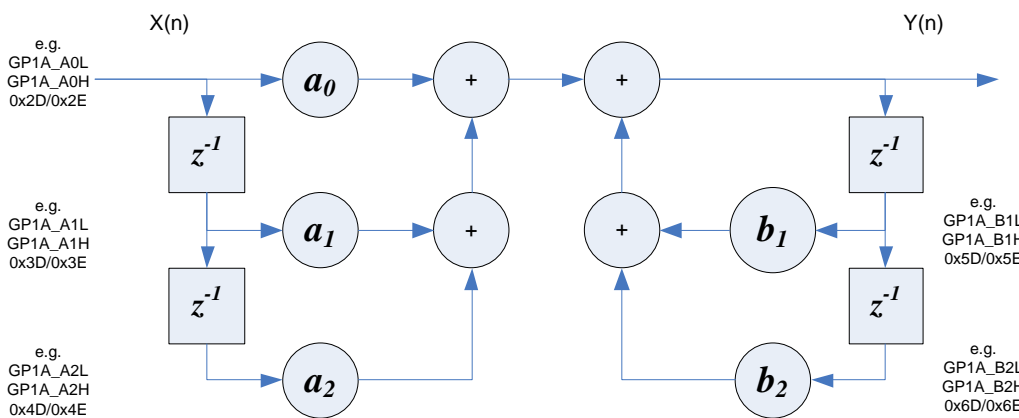


Figure 17: Direct form I implementation of a second order IIR filter

Each of the five coefficients may be configured by the user, for each filter section. The coefficients are specified as 16-bit two's-complement numbers, ranging from -2 to +2. Denominator coefficients must be negated, that is, if b1 is positive then a negative value (-b1) must be programmed, and

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conversely, if b_1 is negative then a positive value ($+b_1$) must be programmed. Coefficients must be selected carefully to specify a stable filter.

The filter sections are arranged in four groups, where the input to each filter group can be programmed to be one of up to seven possible sources:

- The two digital audio interface (DAI) output ports (left or right)
- The output from the two ADC channels (left or right)
- The output from a previously processed filter group (one of the up to three remaining groups)

If the processing function of a filter is not required the group can be disabled. In this case, the output path of the filter group is connected directly to the input source. Disabling a filter group reduces the power consumption of the filter group to a minimum.

8.3 Programming the general purpose filter

The general purpose filter is configured using two groups of registers. These are coefficient programming and path selection. The coefficients should be programmed using the registers GP1A_A0L (address 0x2D, [Table 86](#)) to GP2D_B2H (address 0x7C, [Table 165](#)). Coefficients are programmed as two 8-bit registers of signed values representing the range +2 to -2.

Example

GP1A_B1L and GP1A_B1H contain the two's complement low and high bytes of the $-b_1$ coefficient of filter illustrated in [Figure 17](#). If a coefficient value of 1.45 is required, $-b_1$ is programmed as the coefficient number multiplied by a scaling factor.

The scaling factor 214 is used to convert the floating point number into an integer value for programming. The low byte will always be an 8-bit unsigned hexadecimal value, while the high byte contains the sign bit of the two's complement word.

Scale the unsigned decimal coefficient value:

$$b_1 = 1.45 \times 214 = 23756.8 \approx 23757$$

The unsigned scaled value in binary:

$$b_1 = 0101110011001100b$$

Convert to two's complement; invert the binary value and add the MSB sign bit:

$$b_1 = 10100011001100112 = A333h$$

$$GP1A_B1L = 33h = 00110011$$

$$GP1A_B1H = A3h = 10100011, \text{ where MSB is the two's complement sign-bit}$$

Note that the denominator coefficient is explicitly negated. The value of the $-b_1$ term is positive, so a negative value must be programmed. There are eight fully programmable, second-order IIR biquad filter sections grouped in the following pairs:

- 1AB
- 1CD
- 2AB
- 2CD

The output of the first section in each group is cascaded with the second section. The filter sections are processed in a fixed order: 1A, 1B, 1C, 1D, 2A, 2B, 2C, 2D.

Each filter group can be programmed to take its input from one of seven possible sources, that is, from either an ADC or an I2S channel, or from any filter section that has been previously processed using GP_1AB_SRC and GP_2AB_SRC (address 0x7D, [Table 166](#)) and GP_1CD_SRC and GP_2CD_SRC (address 0x7E, [Table 167](#)) It is possible to cascade all eight GP filters together using these registers. Each filter block can be enabled or disabled in register DSP_CFG (address 0x7F, [Table 168](#)).

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Table 24: GP filter section enable bits

| Control | Definition |
|----------|-----------------------|
| GP1AB_EN | Enable GP section 1AB |
| GP1CD_EN | Enable GP section 1CD |
| GP2AB_EN | Enable GP section 2AB |
| GP2CD_EN | Enable GP section 2CD |

The outputs of some groups can be summed together, as controlled by register DSP_CFG (address 0x7F, [Table 168](#)).

Table 25: Band-equaliser corner frequencies

| Control | Definition |
|-----------|--|
| DSP_MIX_1 | Output of group 1AB is summed with 1CD |
| DSP_MIX_2 | Output of group 1CD is summed with 2AB |
| DSP_MIX_3 | Output of group 2AB is summed with 2CD |

When using the summing facility, the user must ensure that the source signal filter sections are activated and their output levels are such that clipping does not occur.

At 88.2 kHz and 96 kHz sample rates, the number of useable filter sections is halved. Only sections 1B, 1D, 2B and 2D are available.

8.4 Hi-Fi recording

8.4.1 5-band equaliser for recording path

To allow user-specific sound control, the recording path includes a programmable 5-band equaliser (combined in the ADC IIR blocks in [Figure 16](#)). This is enabled using control ADC_EQ_EN (address 0x13, [Table 60](#)).

A low-pass filter, three band-pass filters and a high-pass filter with turn over frequencies at approximately 50 Hz, 300 Hz, 1.2 kHz and 5 kHz (bandpass centre frequencies at 150, 500 and 2500 Hz) are controlled using the registers ADC_EQ1_VOL to ADC_EQ5_VOL (addresses: 0x11, [Table 58](#); 0x12, [Table 59](#); 0x13, [Table 60](#)). These registers boost or damp each frequency band from -10.5 dB to +12 dB in 1.5 dB steps. Saturation of the signal from boosted frequencies can be prevented by an overall damping control ADC_EQ_GAIN (address 0x13, [Table 60](#)), which provides attenuation from -18 dB to 0 dB in 6 dB steps.

Table 26: 5-band-equaliser turn-over/centre frequencies

| Sampling frequency kHz | Low pass 50 Hz | Band pass 150 Hz | Band pass 500 Hz | Band pass 2500 Hz | High pass 5000 Hz |
|------------------------|----------------|------------------|------------------|-------------------|-------------------|
| 96.0 | n.a. | n.a. | n.a. | n.a. | n.a. |
| 88.2 | n.a. | n.a. | n.a. | n.a. | n.a. |
| 48.0 | 67 | 143 | 627 | 2565 | 5100 |
| 44.1 | 62 | 131 | 576 | 2357 | 4686 |
| 32.0 | 45 | 95 | 418 | 1710 | 3400 |
| 24.0 | 67 | 144 | 659 | 2953 | 6230 |
| 22.05 | 62 | 132 | 605 | 2713 | 5724 |
| 16.0 | 45 | 96 | 439 | 1969 | 4153 |
| 12.0 | 67 | 147 | 726 | 2230 | 3050 |
| 11.025 | 62 | 135 | 667 | 2049 | 2802 |
| 8.0 | 45 | 98 | 484 | 1486 | 2033 |

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The 5-band equaliser cannot be used at 88.2 kHz and 96 kHz sampling rates, and is automatically disabled if the ADC is configured to Voice Mode using control ADC_HP_F0 (address 0x0F, Table 56). The frequency responses of the 5-band equaliser are illustrated in Figure 18 to Figure 22.

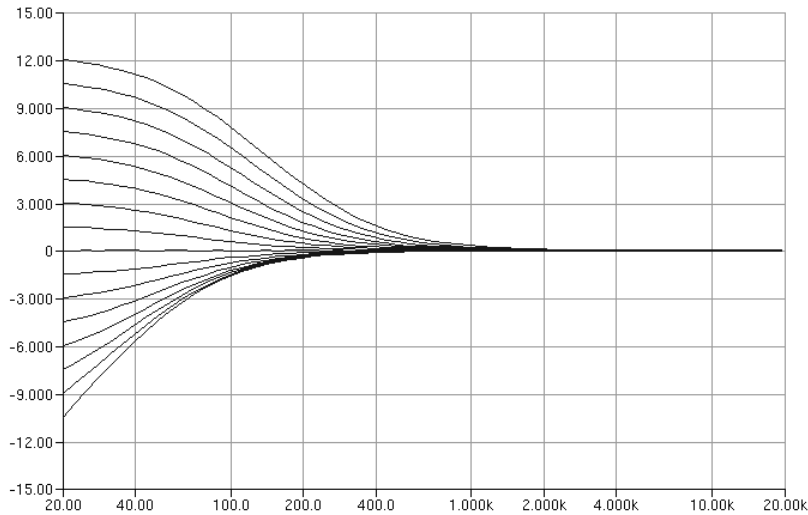


Figure 18: Band 5 (LP 50 Hz) frequency response at FS = 48 kHz

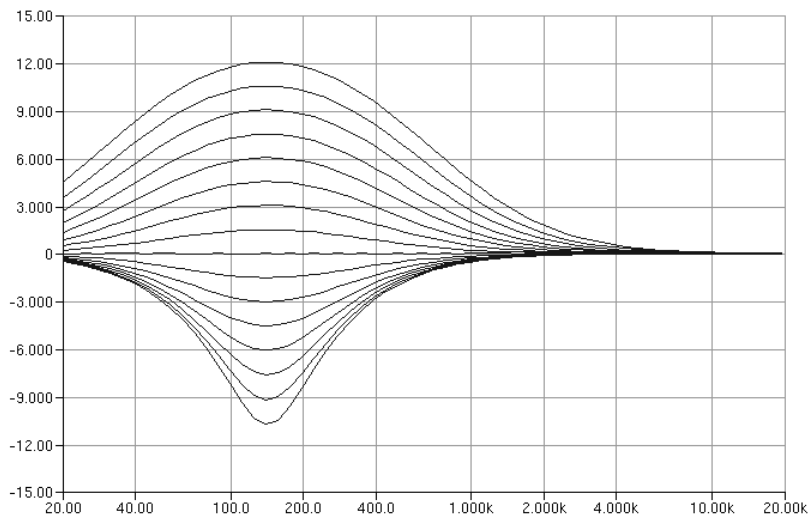


Figure 19: Band 5 (BP 150 Hz) frequency response at FS = 48 kHz

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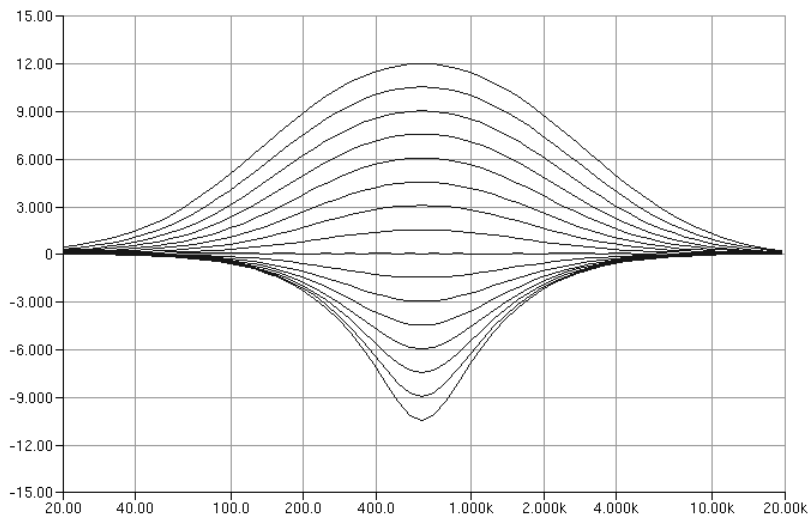


Figure 20: Band 5 (BP 500 Hz) frequency response at FS = 48 kHz

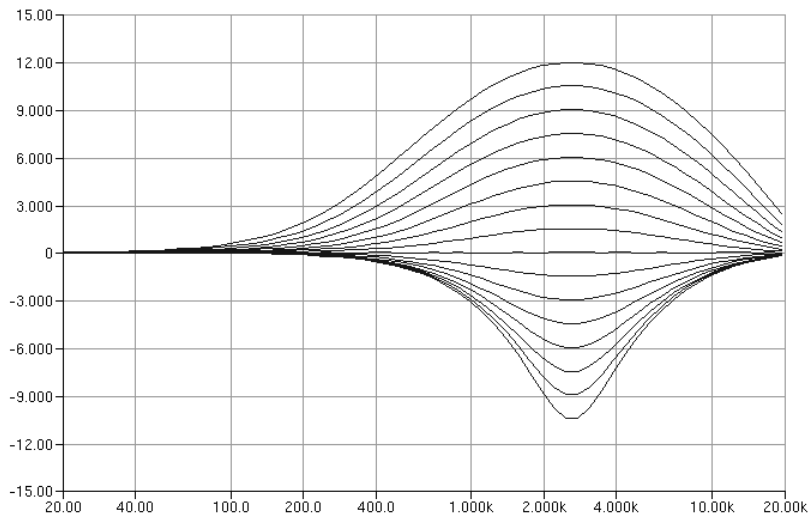


Figure 21: Band 5 (BP 2500 Hz) frequency response at FS = 48 kHz

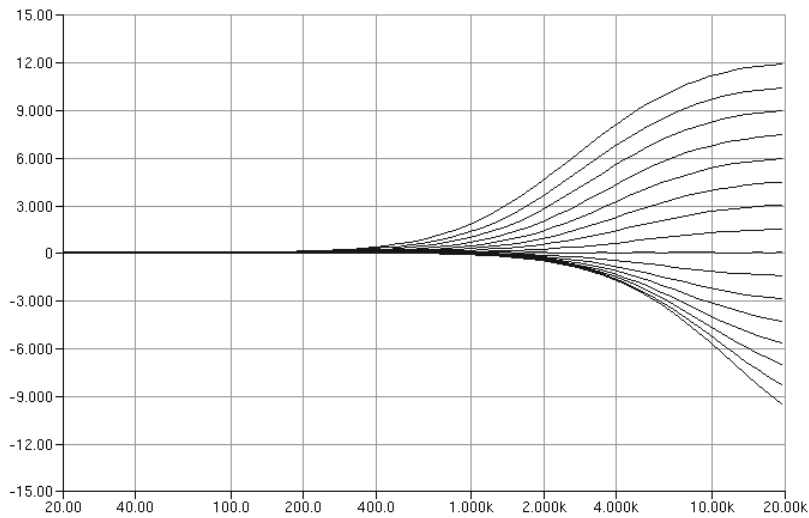


Figure 22: Band 5 (HP 5000 Hz) frequency response at FS = 48 kHz

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8.4.2 Digital audio processing for the record path

When Record only is selected, the DAC and playback filter units can be powered down. The general purpose filter engine can offer 8th order stereo filters to correct the acoustic frequency response of the connected microphone (Figure 23).

If less filtering is required, filter stages can be bypassed using the filter enable controls described in Table 24.

For mono playback, this can also be achieved by switching off a complete channel (blocks not required are highlighted in the following figures in light grey).

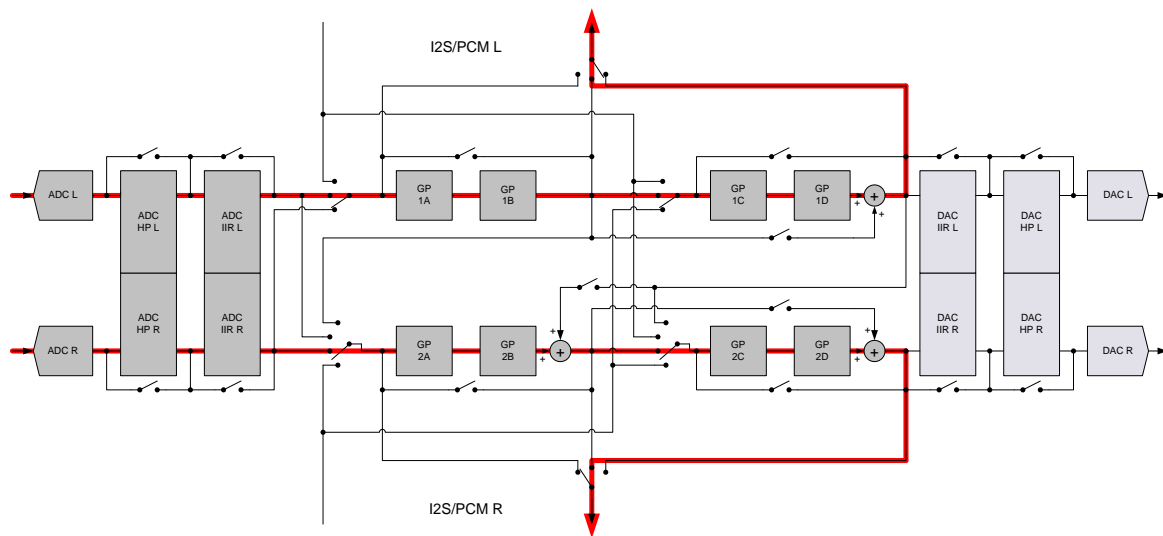


Figure 23: Record only

If it is intended to listen to the recording as it is being made, or to listen to another sound at the same time as the recording, the general purpose filter engine offers a split mode for parallel record and playback equalisation. This mode supports applications that perform active noise cancellation.

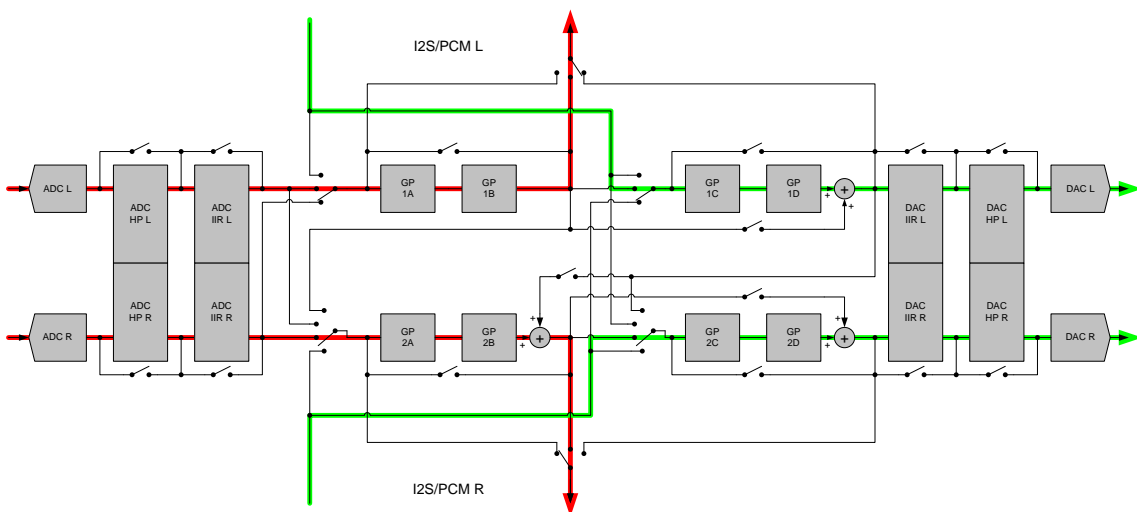


Figure 24: Record with sound monitor

8.5 Hi-Fi playback

8.5.1 5-band equaliser for playback path

To allow user-specific sound settings, the digital playback path includes a programmable 5-band equaliser, which is enabled using control DAC_EQ_EN (address 0x1B, Table 68).

A low-pass filter, three band pass filters and a high-pass filter, with corner frequencies at approximately 100 Hz, 300 Hz, 1 kHz, 3 kHz and 3 kHz (for FS = 44.1 kHz) are controlled by the registers DAC_EQ1_VOL to DAC_EQ5_VOL (addresses: 0x19, Table 66; 0x1A, Table 67; 0x1B, Table 68). These registers boost or damp each frequency band from -10.5 dB to +12 dB in 1.5 dB steps. Saturation of the signal from boosted frequencies can be prevented by an overall damping control ADC_EQ_GAIN (address 0x1B, Table 68).

The 5-band equaliser cannot be used at a 96 kHz sampling rate and is automatically disabled if the ADC is configured to Voice Mode using control DAC_VOICE_EN (address 0x14, Table 61). Details of corner frequencies are shown in Table 26. Frequency responses are illustrated in Figure 18 to Figure 22.

8.5.2 Digital audio processing for playback path

In addition to the user selectable sound settings offered by the 5-band equaliser, the playback path offers up to 8th order configurable audio filtering, for example, to correct the frequency response of connected receivers, speakers or headphones.

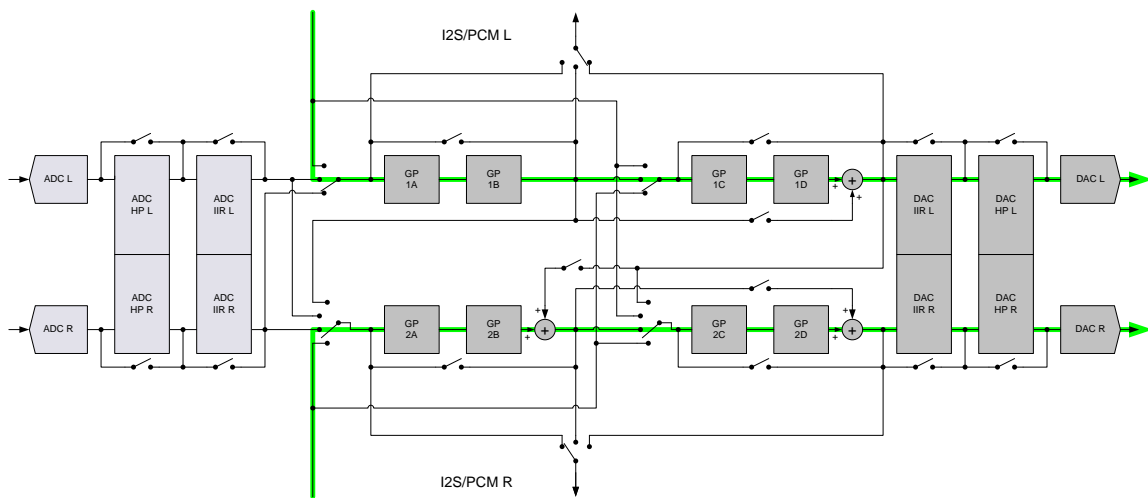


Figure 25: Stereo playback (for example, freefield headphone equalisation)

For applications with stereo speakers the digital signal processing offers stereo widening with 3D audio effects.

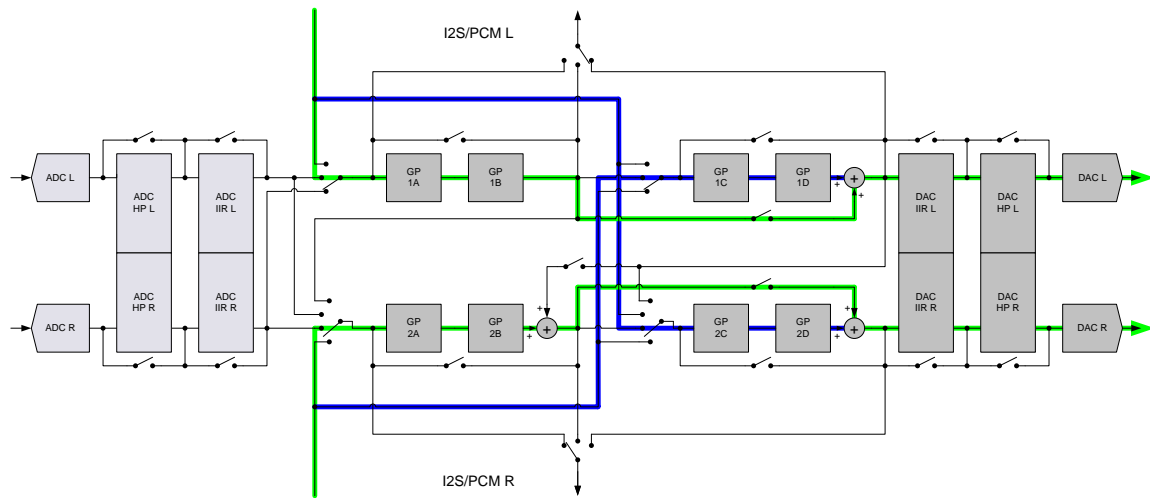


Figure 26: Sound spatialiser for stereo speaker

8.6 Telephone/Bluetooth voice recording/playback at low sample rates

DA7210 offers a dedicated Voice Mode with configurable voice in-band and enhanced out-of-band suppression for sample rates up to 16 kHz.

8.6.1 Voice filtering for recording at low sample rates

When the sampling frequency is 8, 11.025, 12 or 16 kHz, a voice mode can be enabled via ADC_VOICE_EN (address 0xF, [Table 56](#)) where the low frequency roll off is configured using control ADC_VOICE_F0 (address 0xF, [Table 56](#)).

Note 5 Voice filter setting takes precedence over the 5-band equaliser. If the voice filter is enabled for the ADC path, the 5 band equaliser for recording is disabled.

Table 27: Voice mode recording high-pass filter specifications

| Cut-off frequency [Hz] at ADC_VOICE_F0 setting | | | | | | | | |
|--|------|------|-----|-----|-----|-----|-----|-----|
| Fs [kHz] | 000 | 001 | 010 | 011 | 100 | 101 | 110 | 111 |
| 8.0 | 2.5 | 25 | 50 | 100 | 150 | 200 | 300 | 400 |
| 11.025 | 3.4 | 34.5 | 69 | 138 | 207 | 276 | 413 | 551 |
| 12.0 | 3.75 | 37.5 | 75 | 150 | 225 | 300 | 450 | 600 |
| 16.0 | 5 | 50 | 100 | 200 | 300 | 400 | 600 | 800 |

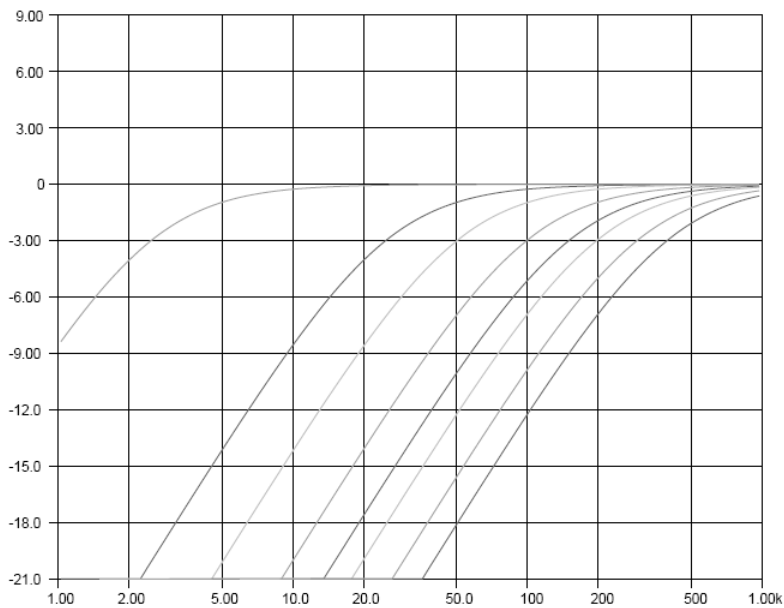


Figure 27: Voice mode recording high-pass filter (cut-off frequency setting '000' to '111', 8 kHz)

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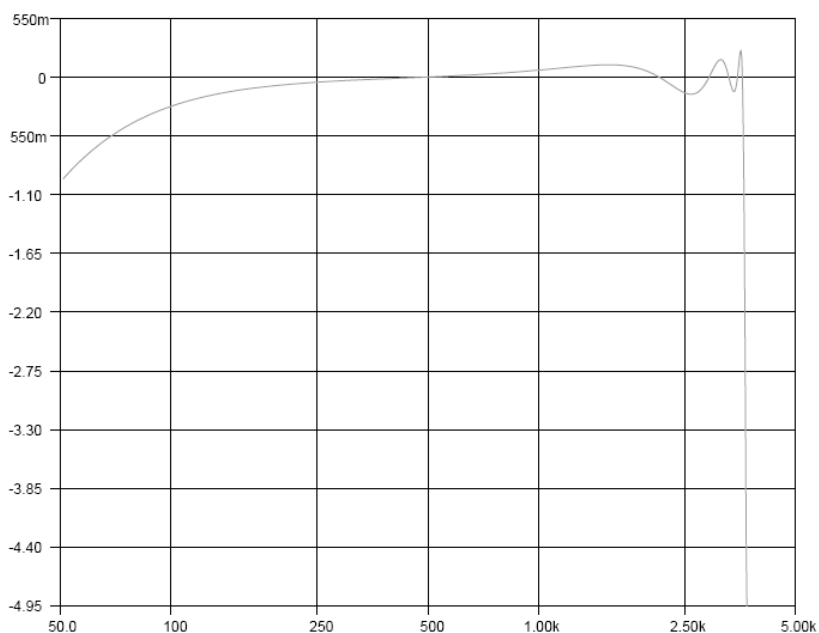


Figure 28: Voice mode recording frequency response (setting '001', 8 kHz)

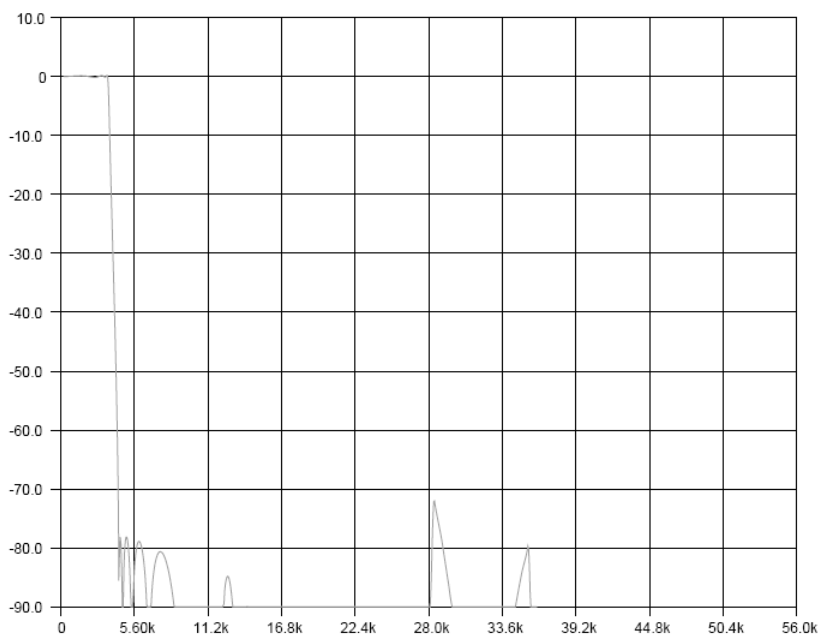


Figure 29: Voice mode recording stop band suppression (8 kHz)

8.6.2 Voice filtering for playback at low sample rates

For playback the voice mode is enabled via DAC_VOICE_EN (Address 0x14, Table 61) where the low frequency roll off is configured via control DAC_VOICE_F0 (Address 0x14, Table 61).

Note 6 Voice filter setting takes precedence over the 5 band-equaliser. If the voice filter is enabled for the DAC signal the 5-band-equalizer for playback is automatically disabled.

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Table 28: Voice mode playback high-pass filter specifications

| Cut-off frequency [Hz] at DAC VOICE_F0 setting | | | | | | | | |
|--|------|------|-----|-----|-----|-----|-----|-----|
| Fs [kHz] | 000 | 001 | 010 | 011 | 100 | 101 | 110 | 111 |
| 8.0 | 2.5 | 25 | 50 | 100 | 150 | 200 | 300 | 400 |
| 11.025 | 3.4 | 34.5 | 69 | 138 | 207 | 276 | 413 | 551 |
| 12.0 | 3.75 | 37.5 | 75 | 150 | 225 | 300 | 450 | 600 |
| 16.0 | 5 | 50 | 100 | 200 | 300 | 400 | 600 | 800 |

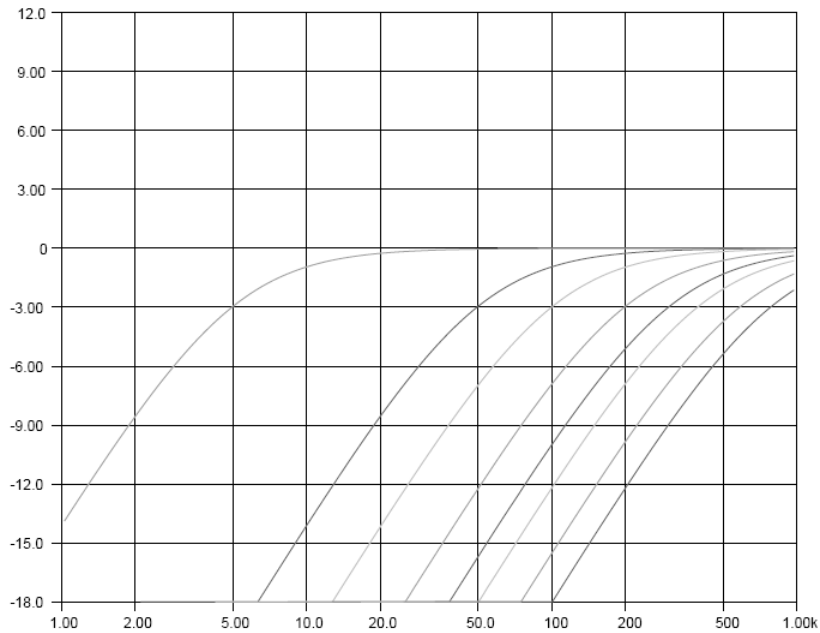


Figure 30: Voice mode playback high-pass filter (cut-off frequency setting '000' to '111', 16 kHz)

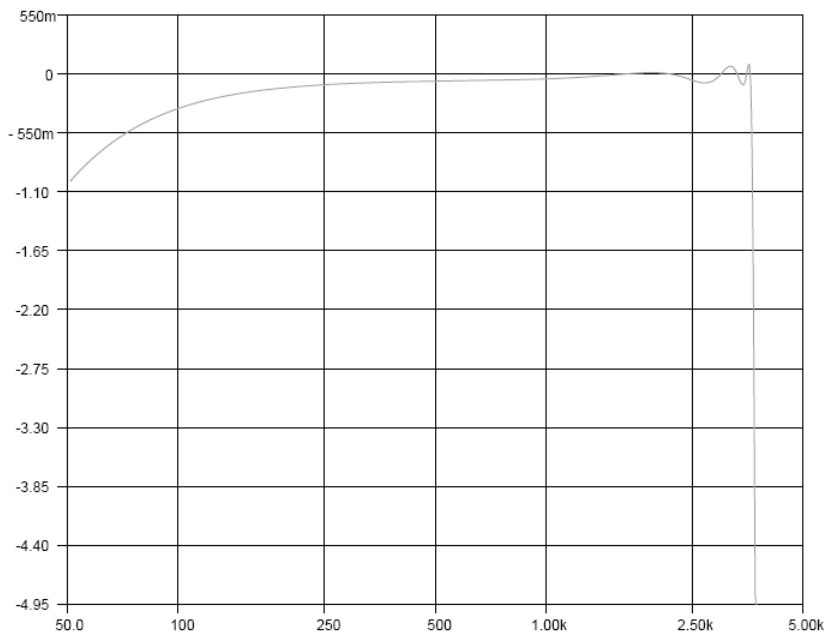


Figure 31: Voice mode playback frequency response (setting '001', 8 kHz)

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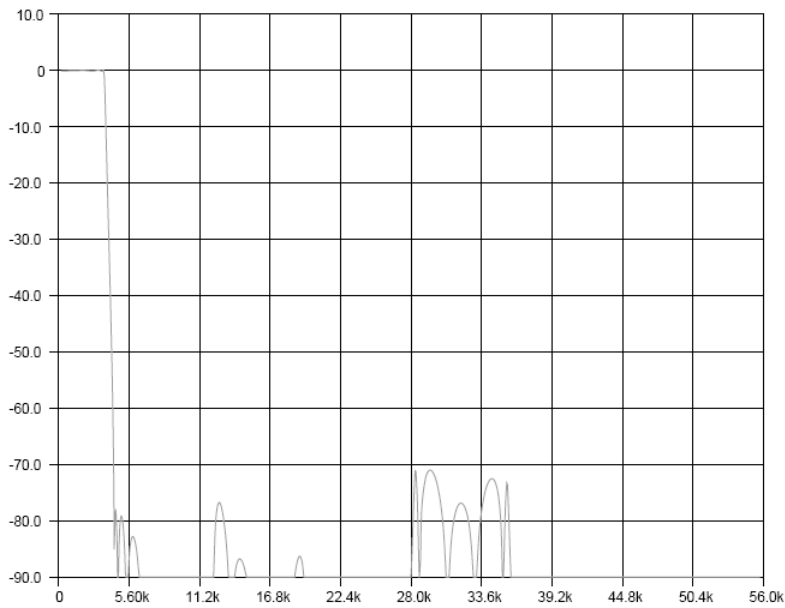


Figure 32: Voice mode playback stop band suppression (8 kHz)

8.6.3 Digital audio processing for phone applications

The general purpose filter engine offers a parallel 4th order acoustic equalisation of microphone and receiver/speaker, and filtering of the sidetone signal to suppress oscillations from any acoustic feedback loop. This allows corrections to the frequency response of acoustic transducers and their mechanical environment that is required for GSM/3GPP type approval of mobile phone applications.

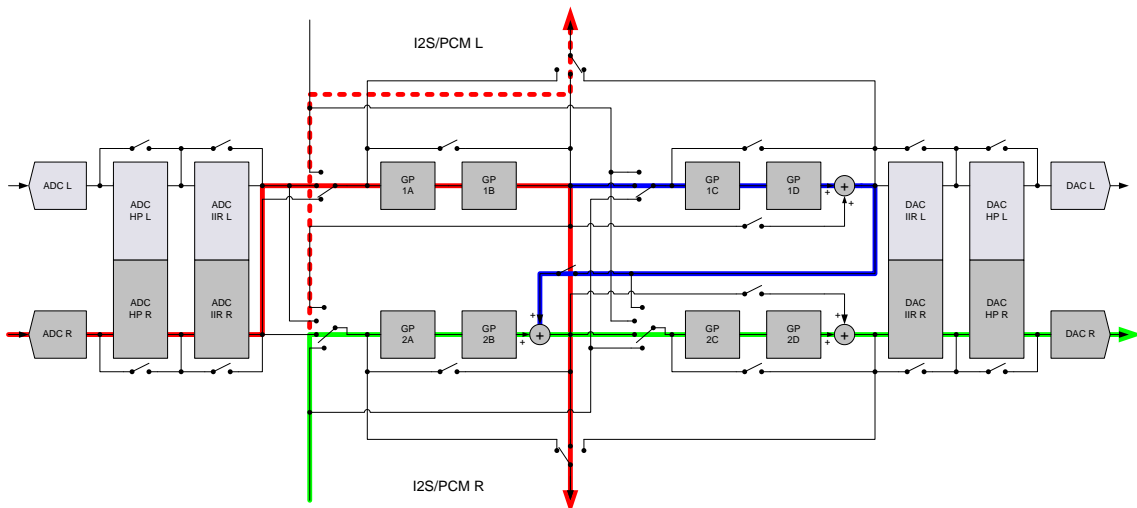


Figure 33: Transmit (red), receive (green) and sidetone (blue) sound filtering for phone applications

9 INTERFACES

9.1 Digital audio interface (DAI)

Audio data is transferred to and from DA7210 via a serial 2-wire or serial 4-wire digital audio interface. This is enabled with bit DAI_EN (address 0x28, [Table 81](#)). It is compatible with the Phillips I2S bus specification in normal, left justified, and right justified modes, and operates in both master and slave modes. In addition to I2S, the codec supports the DSP/PCM format of Bluetooth and mobile phone voice links, and offers a multi device TDM mode. The four bus lines are the clock (CLK), the serial data-in line (DATAIN), the serial data-out line (DATAOUT), and the word select line (WCLK).

For voice stream monitoring within dual processor architectures, DA7210 includes loop back modes that allow merging of the mono (left) RX and TX data into the PCM/I2S TX data stream configured via control DAI_OUT_R_SRC (address 0x25, [Table 78](#)).

Serial data and control signals are clocked onto the bus at the falling edge of the CLK clock signal. This guarantees that they are stable at the rising edge of CLK. The serial data is sampled into DA7210 on the rising edge of the CLK clock signal.

The interface is enabled via DAI_EN (address 0x28, [Table 81](#)) and can operate as either the bus master or as a slave (see control DAI_MODE (address 0x26, [Table 79](#)). In master mode, DA7210 generates the WCLK and CLK signals, whereas in the default slave mode these are inputs to the device. If the output from the ADC is not required, the serial data output from this pin can be disabled using control DAI_OE (address 0x28, [Table 81](#)).

The device may also be used in a system where several devices are connected to the master, using Time Division Multiplexing (TDM). The serial input and output data for each device is valid at a certain offset from the start of the frame. The serial data output from the device is tri-stated until the data from the device is valid, thus allowing several devices to have their serial data out pins connected together.

9.1.1 Operation modes DAI interface

Serial data is transferred as two's complement with the MSB first. The protocol format is selected via control DAI_FORMAT (address 0x28, [Table 81](#)). DA7210 is configured to operate with data word lengths of 16, 20, 24, or 32 bits using control DAI_WORD (address 0x26, [Table 79](#)).

In master mode the device can be configured via DAI_FRAME (address 0x26, [Table 79](#)) to generate either twice the selected word-length bit clocks per frame, or 256, 128, or 64 bit clocks per frame. In slave modes, the device may be clocked by any number of bit clocks per frame provided that there are sufficient clocks to transfer all the data bits, which are defined by the word length configuration register.

In loop mode, the RX right data overrides available TX left data using control DAI_SRC_SEL (address 0x25, [Table 78](#)).

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9.1.2 Right justified mode

In right-justified mode the LSB of the left channel is valid on the rising edge of the bit clock preceding the falling edge of word clock. The LSB of the right channel is valid on the rising edge of the bit clock preceding the rising edge of the word clock.

WCLK = 1; left channel data
 WCLK = 0; right channel data

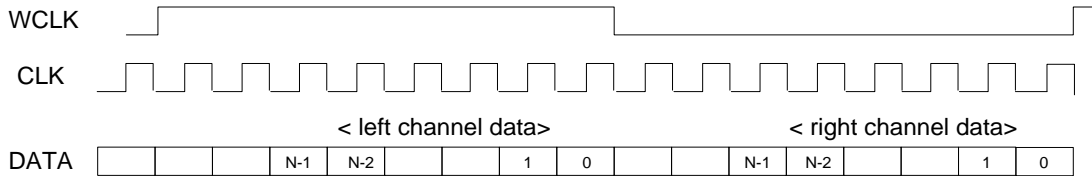


Figure 34: Right justified format

9.1.3 Left justified mode

In left-justified mode the MSB of the right channel is valid on the rising edge of the bit clock following the falling edge of the word clock.

The MSB of the left channel is valid on the rising edge of the bit clock following the rising edge of the word clock.

WCLK = 1; left channel data
 WCLK = 0; right channel data

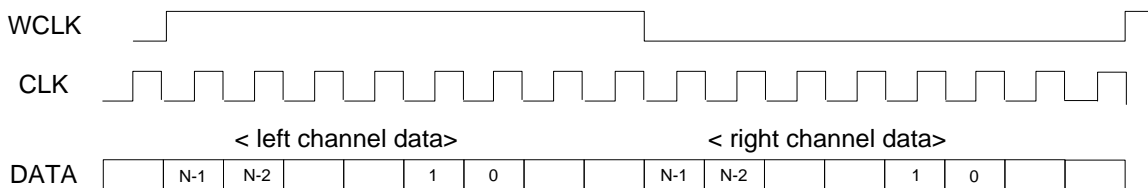


Figure 35: Left justified format

9.1.4 I2S mode

In I2S mode, the MSB of the left channel is valid on the second rising edge of the bit clock after the falling edge of the word clock.

Similarly the MSB of the right channel is valid on the second rising edge of the bit clock after the rising edge of the word clock.

WCLK = 1; right channel data
 WCLK = 0; left channel data

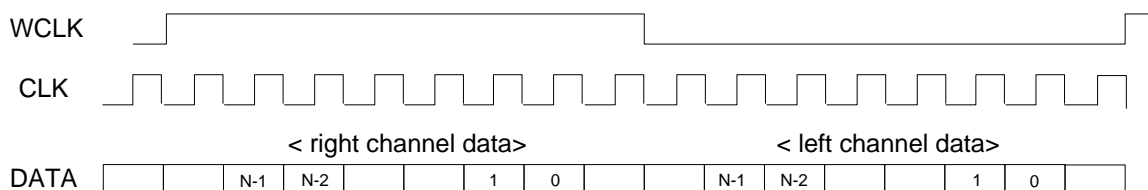
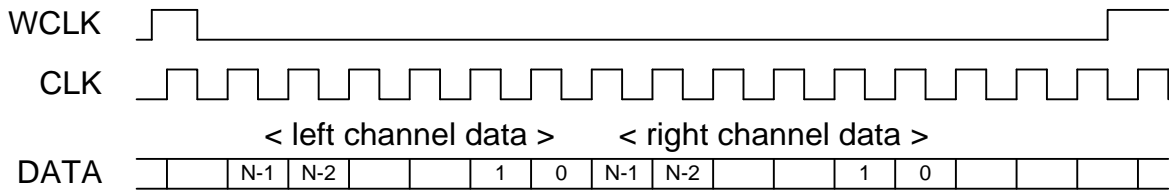


Figure 36: I2S format

9.1.5 DSP mode

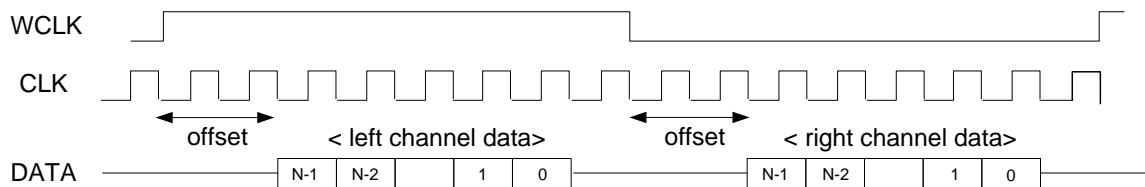
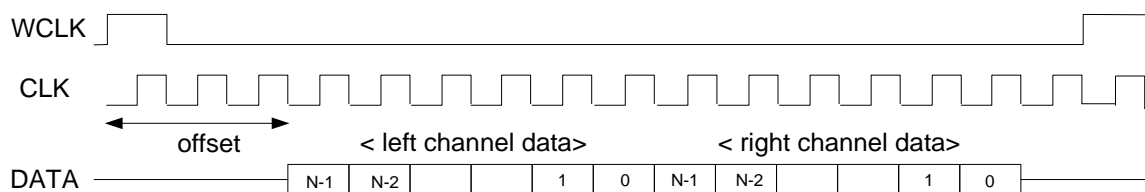
In DSP mode, the rising edge of the word clock starts the data transfer, first with the left channel data, and followed immediately by the right channel data. Each data bit is valid on the falling edge of the bit clock.


Figure 37: DSP format
9.1.6 TDM mode

TDM modes are implemented by defining the data to be valid a certain number of bit clock periods after the start of the frame. This is configured using the offset value `DAI_TDM_OFFSETS` (address 0x27, [Table 80](#)). It is recommended that TDM is used in either the Left Justified or DSP mode.

In the Left Justified TDM mode, the left channel data is valid `DAI_TDM_OFFSETS` clock cycles after the rising edge of the word clock, and the right channel data is valid after the same `DAI_TDM_OFFSETS` number of clock cycles after the falling edge of the word clock.

In the DSP TDM mode, the left channel data is valid `DAI_TDM_OFFSETS` clock cycles after the rising edge of the word clock pulse, and the right channel data is valid immediately after the left channel data. The number of bits of the data is determined by the word length setting in the configuration registers. The serial data output pin will be tri-stated when the output is not valid.


Figure 38: TDM left justified format

Figure 39: TDM DSP format

TDM mode is enabled via `DAI_TDM` (address 0x28 [Table 81](#)) and may be configured to operate in mono only using the control `DAI_TDM_MONO` (address 0x26 [Table 79](#)). In this case, only one channel data is received from the bus and placed on the bus. Other devices may place data on the bus immediately after the left channel data.

9.1.7 Clocking schemes

The internal system clock of the DA7210 runs at either 12.288 MHz or 11.2896 MHz. Which of these two system clock speeds is used depends on the audio sample rate as shown in [Table 29](#). However, the external MCLK input choice has a number of options that depend on the sample rate, the `MCLK_RANGE` setting, whether the device is operating in Master or Slave Mode, and whether the PLL has been enabled.

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For all DA7210 operations, the device must be started with an external MCLK input to allow register settings to be made. The DA7210 will not start up correctly unless this external clock is available. The initial frequency of the MCLK input during register set up is unimportant as long as it is within the 10 to 80 MHz range, but the frequency must be valid for DAC, ADC and filter operation.

Note: In PLL-enabled modes, register writes are clocked into the register map by the control interface clock (SK) until the PLL clock is locked and available.

Table 29: Internal system clock frequency

| Sample rate (kHz) | System clock rate FSYS (MHz) | ADC/DAC clock rate FSDM (MHz) |
|-------------------|------------------------------|-------------------------------|
| 8 | 12.288 | 3.072 |
| 16 | 12.288 | 3.072 |
| 32 | 12.288 | 3.072 |
| 48 | 12.288 | 3.072 |
| 96 | 12.288 | 3.072 |
| 11.025 | 11.2896 | 2.8224 |
| 25.05 | 11.2896 | 2.8224 |
| 44.1 | 11.2896 | 2.8224 |
| 88.2 | 11.2896 | 2.8224 |

Table 30: Block enable and system standby bits

| I/O | Block enable register bit | SC_MST_EN = 1 required to enable I/O block bit? | Start-up register bit for setting I/O to standby |
|---------------|---------------------------|---|--|
| MIC_L | 0x07[7] | Yes | 0x05[0] |
| MIC_R | 0x08[7] | Yes | 0x05[1] |
| AUX1_L | 0x09[7] | Yes | 0x05[3] |
| AUX1_R | 0x0A[7] | Yes | 0x05[2] |
| AUX2 | 0x0B[3] | Yes | 0x05[4] |
| ADC_L | 0x10[3] | Yes | 0x05[5] |
| ADC_R | 0x10[7] | Yes | 0x05[6] |
| OUT1_L | 0x1E[7] | Yes | 0x04[0] |
| OUT1_R | 0x1F[7] | Yes | 0x04[1] |
| OUT2 | 0x20[7] | Yes | 0x04[2] |
| HP_L | 0x23[7] | Yes | 0x04[3] |
| HP_R | 0x23[3] | Yes | 0x04[4] |
| DAC_L | 0x17[7] | Yes | 0x04[5] |
| DAC_R | 0x17[3] | Yes | 0x04[6] |
| INMIX_L mixer | 0x0D[7] | No | n/a |
| INMIX_R mixer | 0x0E[7] | No | n/a |
| OUT_L mixer | 0x1C[7] | No | n/a |
| OUT_R mixer | 0x1D[7] | No | n/a |

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Table 30 summarises the registers bits that must be enabled before SC_MST_EN is enabled if that block operation is required. Each block can be set in and out of standby after SC_MST_EN = 1.

9.1.8 Master mode

In Master mode (controlled by DAI_MODE - address 0x26, **Table 79**) DA7210 can generate all supported audio sampling rates directly from a provided MCLK signal at either 12.288 MHz or 11.2896 MHz. In this case the PLL is not required and it should be bypassed and disabled with PLL_EN (address 0x2C, **Table 85**).

DA7210 can also generate all internal clocks without offset, as well as the sample rate, the CLK signal, and the WCLK signal from an MCLK signal in the range of 10 MHz to 80 MHz. This is done using the embedded fractional-N PLL (see controls MCLK_RANGE and PLL_DIV_L to PLL_DIV_H).

Table 31: ADC and DAC clock frequencies

| Sample rate [kHz] | Voice mode (Note 7) | ADC decimation | DAC SDM oversample | SDM rate Fs | FSDM frequency [kHz] |
|-------------------|---------------------|----------------|--------------------|-------------|----------------------|
| 8 | | 96 | 32 | 384 | 3072 |
| 8 | Y | 96 | 16 | 384 | 3072 |
| 11.025 | Y | 64 | 32 | 256 | 2822.4 |
| 12 | Y | 64 | 32 | 256 | 3072 |
| 16 | | 48 | 16 | 192 | 3072 |
| 16 | Y | 48 | 8 | 192 | 3072 |
| 22.05 | | 32 | 16 | 128 | 2822.4 |
| 24 | | 32 | 16 | 128 | 3072 |
| 32 | | 24 | 8 | 96 | 3072 |
| 44.1 | | 16 | 8 | 64 | 2822.4 |
| 48 | | 16 | 8 | 64 | 3072 |
| 96 Note 8 | | 8 | 4 | 32 | 2822.4 |

Note 7 Voice filter has stopband attenuation of >75 dB. The IIR engine implements voice filtering, or 5-band equalisation. For rates other than 44.1 kHz, the 5-band equalisation turnover frequencies scale with the sampling rate.

Note 8 No TDM on digital audio interface

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Table 32: Master mode PLL-DIV look up table

| Input MCLK [MHz] | PLL_DIV_H | PLL_DIV_H | PLL_DIV_H | Audio frequency [kHz] |
|------------------|-----------|-----------|-----------|-----------------------|
| 12.0 | 0xE8 | 0x6C | 0x2 | 44.1 (Note 9) |
| 12.0 | 0xF3 | 0x12 | 0x7 | 48.0 (Note 10) |
| 13.0 | 0xDF | 0x28 | 0xC | 44.1 (Note 9) |
| 13.0 | 0xE8 | 0xFD | 0x5 | 48.0 (Note 10) |
| 13.5 | 0xDB | 0x0A | 0xD | 44.1 (Note 9) |
| 13.5 | 0xE4 | 0x82 | 0x3 | 48.0 (Note 10) |
| 14.4 | 0xD4 | 0x5A | 0x2 | 44.1 (Note 9) |
| 14.4 | 0xDD | 0x3A | 0x0 | 48.0 (Note 10) |
| 19.2 | 0xBB | 0x43 | 0x9 | 44.1 (Note 9) |
| 19.2 | 0xC1 | 0xEB | 0x8 | 48.0 (Note 10) |
| 19.68 | 0xB9 | 0x6D | 0xA | 44.1 (Note 9) |
| 19.68 | 0xBF | 0xEC | 0x0 | 48.0 (Note 10) |
| 19.8 | 0xB8 | 0xFB | 0xB | 44.1 (Note 9) |
| 19.8 | 0xBF | 0x70 | 0x0 | 48.0 (Note 10) |

Note 9 Including harmonics such as 11.025, 22.05 and 88.2 kHz sample rates.

Note 10 Including audio frequencies such as 8.0, 12.0, 16.0, 32.0, 24.0, 36.0, 48.0, 96.0 kHz sample rates.

Table 33: SRM mode PLL-DIV look up table

| Input MCLK [MHz] | PLL_DIV_H | PLL_DIV_M | PLL_DIV_L |
|------------------|-----------|-----------|-----------|
| 0.032768 | 0xD4 | 0x99 | 0x0 |
| 12.0 | 0xED | 0xBF | 0x5 |
| 13.0 | 0xE4 | 0x13 | 0x0 |
| 13.5 | 0xDF | 0xC6 | 0x8 |
| 14.4 | 0xD8 | 0xCA | 0x1 |
| 19.2 | 0xBE | 0x97 | 0x9 |
| 19.68 | 0xBC | 0xAC | 0xD |
| 19.8 | 0xBC | 0x35 | 0xE |

9.1.9 Programming master and 32 kHz mode – PLL enabled

If DA7210 is to be used in Master Mode with the PLL, a clock signal must first be applied to the MCLK pin. The frequency of this clock must either be 32.768 kHz (32 kHz Mode), or within the range 10 to 80 MHz.

MCLK_RANGE (address 0x2B[5:4]) must be set to the appropriate frequency range at the MCLK pin.

The Sample Rate Matching (SRM) only needs to be enabled if 32 kHz Mode is being used. SRM is enabled by asserting MCLK_SRM_EN (address 0x26[7]).

For the PLL to assume initial lock, it is necessary to set the PLL division ratio bits in registers 0x29, 0x2A, 0x2B. The settings for PLL Master Mode differ from those of PLL 32 kHz Mode. For 32 kHz mode, MCLK_RANGE (address 0x2C[5:4]) = 00. For all other PLL Master Mode operations, MCLK_RANGE (address 0x2C[5:4]) = 01, 10 or 11. These settings will allow the PLL lock cycle to start in the correct frequency range. It is not necessary to assert MCLK_DET_ENA in PLL Master Mode as the CLK and WCLK outputs are produced by the DA7210 itself.

It is also necessary to assert vco_rst, 0x90[0] to ensure successful PLL lock. To access this bit is necessary to first enter the following register settings 0x8A = 8Bh and 0x8B =B4h.

As with non-PLL slave mode, to set the required sample rate, the correct clock division ratio must be set within register 0x2C[3:0], (see [Table 36](#)).

Table 34: PLL master mode register setting recommendations

| | | | | |
|---------------------|---|---------------|---|---|
| 0x2C PLL | 4 | MCLK_SHAPE_EN | 0 | Enable MCLK shaper for low level non TTL signals - optional |
| | 5 | MCLK_DET_EN | 0 | Enable automatic detection of sample rate |
| | 6 | MCLK_SRM_EN | 0 | Enable DAI sample rate tracking, sample rate defined by FS |
| | 7 | PLL_EN | 1 | 0: Disable and bypass PLL 1: Enable PLL |

Dialog Semiconductor recommend that good quality external clocks are used to supply the DAI, but if the only available MCLK source is of poor quality, it can be improved by using the optional bit MCLK_SHAPE_EN.

[Figure 40](#) shows a basic start-up up configuration sequence for PLL master mode.

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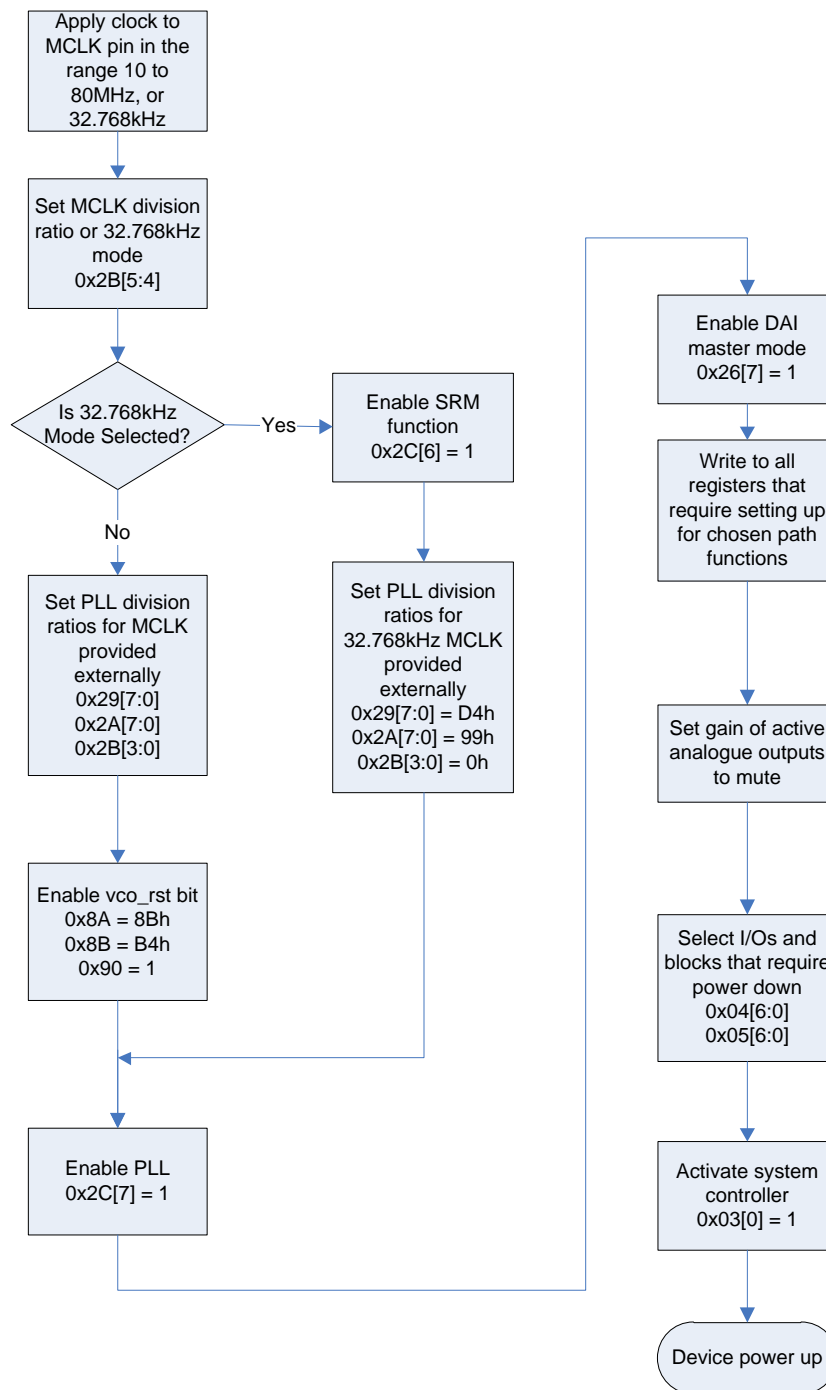


Figure 40: PLL master mode start up sequence

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9.2 Slave mode

Slave mode is selected by setting DAI_MODE (address 0x26, [Table 79](#)) = 0. The CLK and WCLK signals are supplied by the application.

9.2.1 Conditions:

(i) Sample Rate Matching (SRM) Disabled

SRM is not needed if the audio sample rate is known and the CLK and WCLK signals are derived from the same master clock as the MCLK input. In this case CLK and WCLK are synchronised with MCLK, so the SRM function should be disabled and the PLL_DIV registers programmed as shown in [Table 13](#). Alternatively, lowest power dissipation can be achieved if the MCLK frequency can be set to 256×Fs (12.288 MHz or 11.2896 MHz) and the PLL switched off.

(ii) Sample Rate Matching (SRM) Enabled

SRM is needed if the sample rate on the audio interface is unknown, or the CLK and WCLK signals are derived from a different clock domain to the MCLK input.

SRM (MCLK_SRM_EN = 1 address 0x2C, [Table 85](#)) keeps the internal clocks synchronised with WCLK.

If the sample rate is known, the value of FS should be set accordingly. If the sample rate is not known, it can be derived from WCLK and automatically programmed by asserting MCLK_DET_EN (address 0x2C, [Table 85](#)).

The Sample Rate Matching (SRM) functions by pulling the PLL frequency away from the nominal value specified by the PLL control registers (addresses 0x29 to 0x2B, [Table 84](#)). In this mode the register settings shown in [Table 34](#) should be used. Enabling the SRM offers maximum flexibility for clocking schemes as it removes the need to have common clock domains for the application processor and audio codec processor.

9.2.2 Programming slave mode – PLL not enabled

In either Slave or Master mode, and when the PLL is not enabled, an exact multiple of (256 * Fs) must be input to the MCLK pin (see [Table 35](#)).

In order to set the correct clock division ratio within the DA7210 for a particular sample rate, it is necessary to set the correct sample rate setting in the FS register (address 0x2C [3:0], [Table 85](#)). The possible sample rates and MCLK frequencies are shown in [Table 35](#).

Table 35: MCLK frequencies in non-PLL slave mode

| Sample rate (kHz) | MCLK (MHz) | | | |
|-------------------|-----------------|-----------------|-----------------|-----------------|
| | MCLK_RANGE = 00 | MCLK_RANGE = 01 | MCLK_RANGE = 10 | MCLK_RANGE = 11 |
| 8 | n/a | 12.288 | 24.576 | 49.152 |
| 16 | n/a | 12.288 | 24.576 | 49.152 |
| 32 | n/a | 12.288 | 24.576 | 49.152 |
| 48 | n/a | 12.288 | 24.576 | 49.152 |
| 96 | n/a | 12.288 | 24.576 | 49.152 |
| 11.025 | n/a | 11.2896 | 22.5792 | 45.1584 |
| 25.05 | n/a | 11.2896 | 22.5792 | 45.1584 |
| 44.1 | n/a | 11.2896 | 22.5792 | 45.1584 |
| 88.2 | n/a | 11.2896 | 22.5792 | 45.1584 |

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Table 36: Non-PLL slave mode and PLL master mode sample rate settings

| 0x2C[3:0] | Sample rate |
|-----------|-------------|
| 0000 | Not used |
| 0001 | 8 kHz |
| 0010 | 11.025 kHz |
| 0011 | 12 kHz |
| 0100 | Not used |
| 0101 | 16 kHz |
| 0110 | 22.05 kHz |
| 0111 | 24 kHz |
| 1000 | Not used |
| 1001 | 32 kHz |
| 1010 | 44.1 kHz |
| 1011 | 48 kHz |
| 1100 | Not used |
| 1101 | Not used |
| 1110 | 88.1 kHz |
| 1111 | 96 kHz |

If only analogue paths are required then it is possible to use MCLK = 32.768 kHz for the register setup. For all other 32.768 kHz modes, the PLL must be enabled for any operation that requires ADC, DAC or digital filtering.

Figure 41: Non-PLL mode start-up sequence shows a basic start-up up configuration sequence for non-PLL slave mode.

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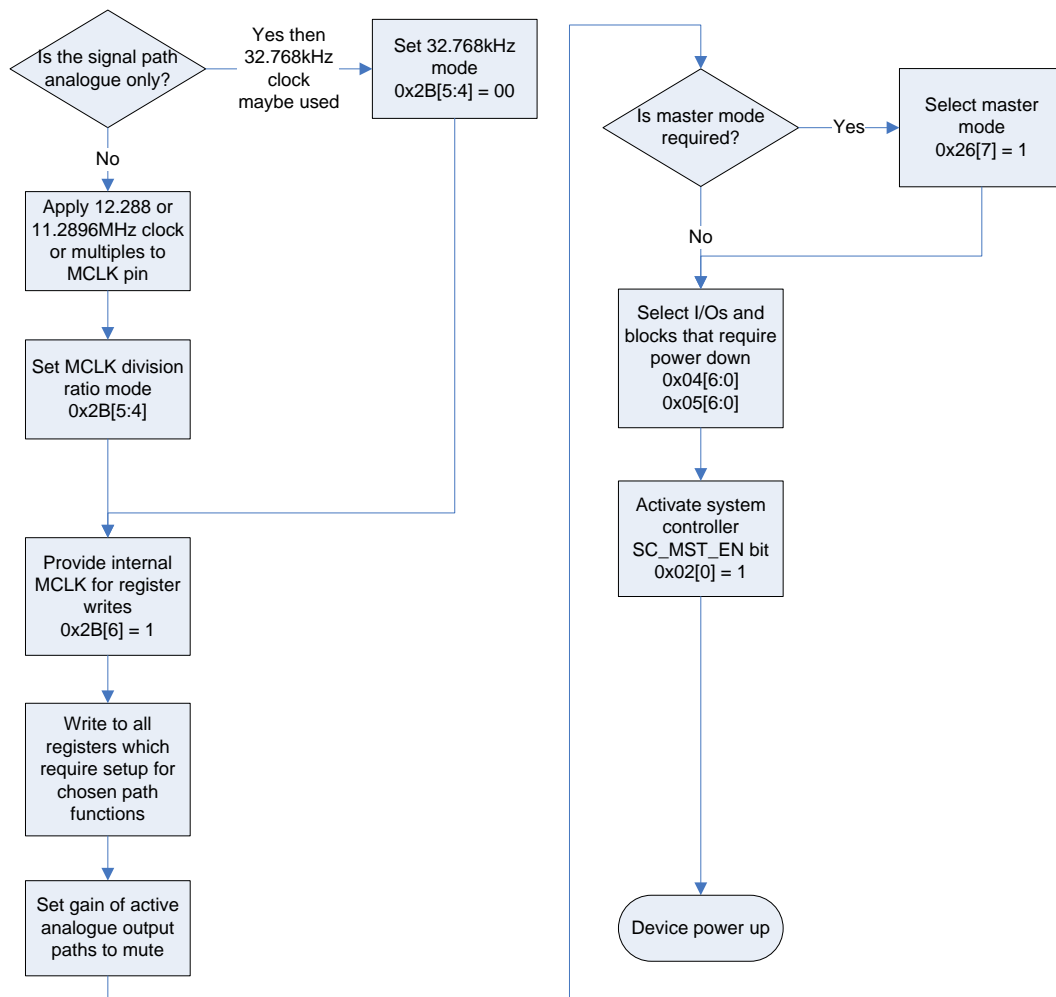


Figure 41: Non-PLL mode start-up sequence

9.2.3 Programming slave mode – PLL enabled

If PLL mode is enabled and the MCLK_DET_EN (0x2C[5]) bit is set, the value read from this register will be the automatically detected sample rate from the PLL track circuitry. Register 0x2C[3:0] can be set to 0000 in this case. Sample rate changes will be updated on the positive edge of DAI clock.

It is also recommended that the Sample Rate Matching (SRM) tracking function is enabled (register 0x2C[6]) when the PLL is used in slave mode. This means that any changes in the sample rate can be tracked automatically without any input from the controlling processor. Failure to enable SRM can result in intermittent audible clicking on the DAC outputs.

In order to allow the PLL to assume initial lock, it is necessary to set the PLL division ratio bits and the MCLK_RANGE in registers 0x29, 0x2A, 0x2B and 0x2C. These functions cause the PLL lock cycle to start in the correct frequency range. The division ratio settings for SRM mode differ from those of master mode (see section 9.1.8).

It is also necessary to set the vco_rst bit, 0x90[0] = 1 to ensure a successful PLL lock. To access this bit, it is necessary to first enter the following register settings: 0x8A = 8Bh and 0x8B = B4h.

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Table 37: SRM mode PLL division ratio settings

| MCLK (MHz) | PLL_DIV_H 0x29[7:0] | PLL_DIV_M 0x2A[7:0] | PLL_DIV_L 0x2B[3:0] |
|------------|------------------------|------------------------|------------------------|
| 0.032768 | 0xD4 | 0x99 | 0x0 |
| 12.0 | 0xED | 0xBF | 0x5 |
| 13.0 | 0xE4 | 0x13 | 0x0 |
| 13.5 | 0xDF | 0xC6 | 0x8 |
| 14.4 | 0xD8 | 0xCA | 0x1 |
| 19.2 | 0xBE | 0x79 | 0x7 |
| 19.68 | 0xBC | 0xAC | 0xD |
| 19.8 | 0xBC | 0x35 | 0xE |

Table 36 contains the division ratios for a selection of common oscillator frequencies that can be used for generating the internal 256 * Fs master clock from the PLL. If an uncommon frequency is used, the division ratio values can be calculated.

The feedback divide ratio PLL_DIV is a 20-bit two's complement value in the range -0.5 to +0.5, which can be calculated using

$$PLL_DIV = \frac{\left(\frac{8 * FSYS}{FMCLK}\right) - 9}{16}$$

For example, if FMCLK = 13.7 MHz and FSYS = 12.288 MHz then PLL_DIV = -0.114033, which equals 0xE2CEC as a 20-bit two's-complement number. This value is written to the three PLL_DIV registers:

- PLL_DIV_H (0x29) = E2h
- PLL_DIV_M (0x2A) = CEh
- PLL_DIV_L (0x2B[3:0]) = Ch

Note 11 A PLL division ratio calculation tool is available on request.

Dialog Semiconductor recommend that good quality external clocks are used to supply the DAI, but if the only available MCLK source is of poor quality. It can be improved by using the optional bit MCLK_SHAPE_EN.

Table 38: Slave mode PLL-enabled register setting recommendations

| | | | | |
|---------------------|---|---------------|---|---|
| 0x2C PLL | 4 | MCLK_SHAPE_EN | 0 | Enable MCLK shaper for low level non TTL signals - optional |
| | 5 | MCLK_DET_EN | 1 | Enable automatic detection of sample rate |
| | 6 | MCLK_SRM_EN | 1 | Enable DAI sample rate tracking, sample rate defined by FS |
| | 7 | PLL_EN | 1 | 0: Disable and bypass PLL 1: Enable PLL |

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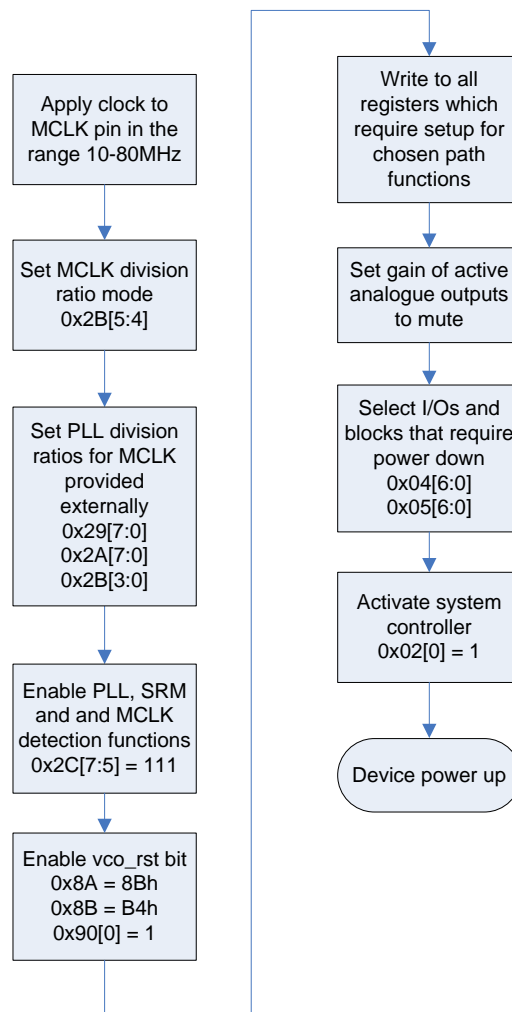


Figure 42: PLL Slave mode start-up sequence

9.2.4 32 kHz master or slave mode

With the 32 kHz mode enabled, the DA7210 is able to accept a standard watch-crystal frequency (32.768 kHz) input on MCLK. It does this by enabling an on-chip reference oscillator and using the SRM system to track the MCLK input. The 32 kHz mode is enabled by setting MCLK_RANGE (address 0x2B, Table 84), and since the SRM is required, the PLL_DIV settings in Table 32 should be used.

The 32 kHz mode works with the DA7210 in Master (Note 12) or Slave modes, but it is not possible to use the automatic detection of audio sample rate.

Note 12 In 32 kHz Master Mode the sample rates 11.025, 22.05, 44.1 and 88.2 kHz will have a maximum offset of 0.14%.

9.2.5 Phase locked loop (PLL)

A PLL is integrated into the codec. This uses standard oscillator master clock signals to generate the target audio sample rates and all internal clock signals. If no $256 * F_s$ master clock signal is provided, the PLL can be enabled with control PLL_EN (address 0x2C, Table 85). The PLL supports a wide range of common oscillator frequencies between 10 and 20 MHz (see Table 32)

The PLL can also be fed from the 2nd or 4th harmonics of these frequencies via an input clock divider (configured using control MCLK_RANGE (address 0x2B, Table 84). The master clock input can be either a standard TTL signal. It can also be any kind of saw tooth, square or sine wave if the embedded signal shaper is enabled via control MCLK_SHAPE_EN (address 0x2C, Table 85). If the host provides the $256 * F_S$ master clock, the PLL can be disabled to reduce dissipation power.

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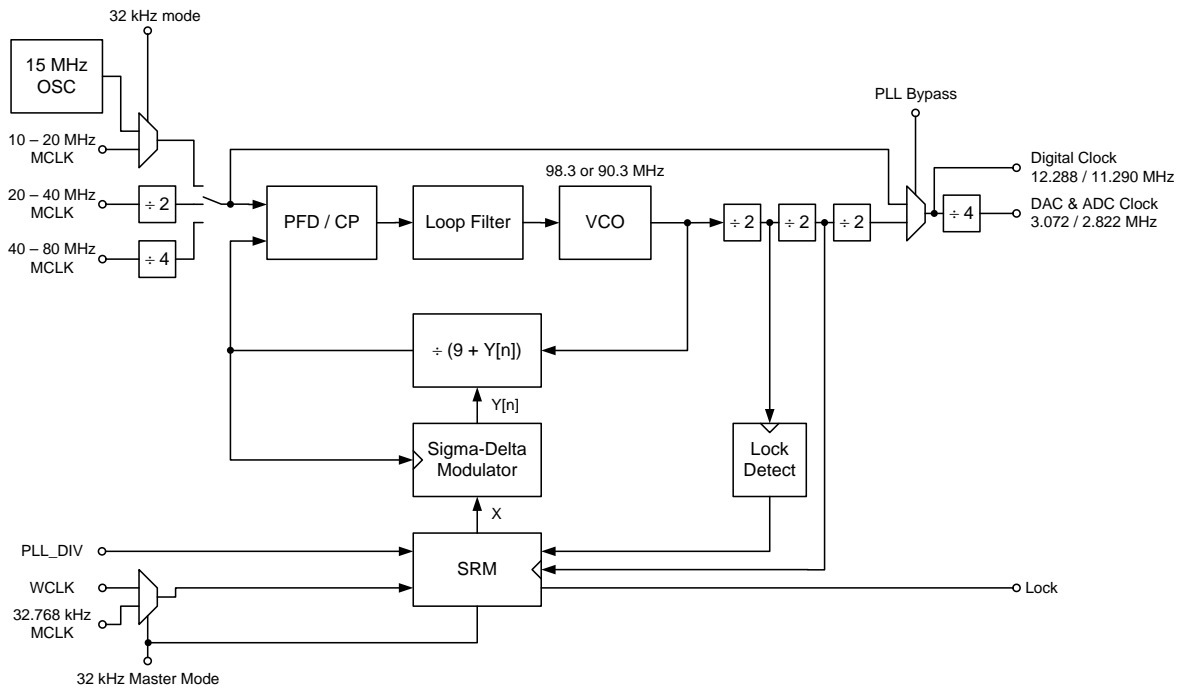


Figure 43: PLL block diagram

9.2.6 Control interface

The DA7210 is selectable to be either a 2-wire or a 4-wire connection (I2C or SPI compliant). The default for the serial interface is will be default in 2-wire mode, but can be configured to be in 4-wire mode after a passive to active transition (default: falling edge) is detected three times on the nCS pin following the power-on-reset, or after the powerdown pin was released. In 2-wire applications the nCS pin should be tied permanently to the passive state through a resistor. Data is shifted into or out from DA7210 under control of the host processor that also provides the serial clock.

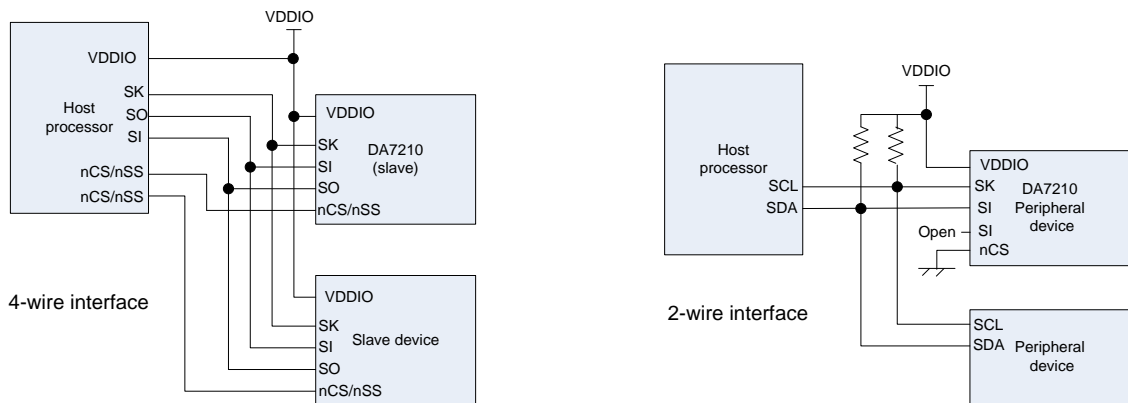


Figure 44: Schematic of a 4-wire and a 2-wire control bus

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9.2.7 4-wire communication

In 4-wire mode the DA7210 register map is split into two pages with each page containing up to 128 registers. The register at address zero on each page is used as a page control register (address 0x00, [Table 42](#), and address 0x80, [Table 169](#)). The default active page after reset includes all registers that are required to control audio on DA7210. Writing to the page control register changes the active page for all subsequent read/write operations. After modifying the active page it is recommended to read back the page control register to ensure that future data exchange is accessing the intended registers.

The 4-wire interface features a half-duplex operation (data can be transmitted and received with in a single 16 bit frame) at enhanced clock speed (up to 14 MHz). It operates at the provided host clock frequencies.

A transmission begins when initiated by the host. Reading and writing is accomplished by the use of an 8-bit command, which is send by the host prior to the exchanged 8 bit data. The byte from the host begins shifting in on the SI pin under the control of the serial clock SK provided from the host. The first 7 bits specify the register address (0 to 127, decimal) which will be written or read by the host. The register address is automatically decoded after receiving the 7th address bit. The command word ends with an R/W bit, which specifies together with the control bit 0x7D (Address, 0x82, [Table 171](#)) the direction of the following data exchange. During register writing the host continues sending out data during the following 8 SK clocks. For reading the host stops transmitting and the 8-bit register is clocked out of DA7210 during the consecutive 8 SK clocks of the frame. Address and data are transmitted with MSB first.

The polarity (active state) of nCS is defined by control bit 0x24 (Address 0x24,) nCS resets the interface when inactive and it has to be released between successive cycles.

The SO output from DA7210 is normally in high-impedance state and active only during the second half of read cycles to allow other 4-wire compatible peripherals to share the same read-back line. A pull-up or pull-down resistor may be needed at the SO line if a floating logic signal can cause unintended current consumption inside other circuits.

Table 39: 4 wire interface

| Configurations | | | |
|---------------------|------------------|-----------------------------------|-------------------------------------|
| CPOL clock polarity | CPHA clock phase | Output data is updated at SK edge | Input data is registered at SK edge |
| 0 (idle low) | 0 | falling | rising |
| 0 (idle low) | 1 | rising | falling |
| 1 (idle high) | 0 | rising | falling |
| 1 (idle high) | 1 | falling | rising |

The DA7210 4-wire interface offers two further configuration bits. Clock polarity (CPOL) and clock phase (CPHA) define when the interface will latch the serial data bits.

NOISE_SUP (Address 0x82, [Table 171](#)) determines whether SK idles high (CPOL = 1) or low (CPOL = 0). CPHA (Address 0x82, [Table 171](#)) determines on which SK edge data is shifted in and out. With CPOL = 0 and CPHA = 0 setting DA7210 latches data on the SK rising edge. If the CPHA is set to 1 the data is latched on the SK falling edge. NOISE_SUP and CPHA states allow four different combinations of clock polarity and phase; each setting is incompatible with the other three. The host and DA7210 must be set to the same CPOL and CPHA states to communicate with each other.

The DA7210 4-wire interface has a fixed configuration according to [Table 40](#).

Table 40: 4 wire clock configurations

| Parameter | |
|---------------|--|
| Signal lines | nCS Chip select |
| | SI Serial input data Master out Slave in |
| | SO Serial output data Master in Slave out |
| | SK Transmission clock |
| Interface | Push-pull with tristate |
| Data rate | Effective read/write data Up to 7 Mbps |
| Transmission | Half-duplex MSB first |
| | 16 bit cycles 7-bit address, 1-bit read/write, 8-bit data |
| Configuration | CPOL clock polarity (default 0 = clock idles low) |
| | CPHA clock phase (default 1 = register data at falling edge) |
| | RW-POL R/W bit level for reading (default 1 = high level for reading) |
| | nCS- POL active level of nCS (default 0 = active low) |

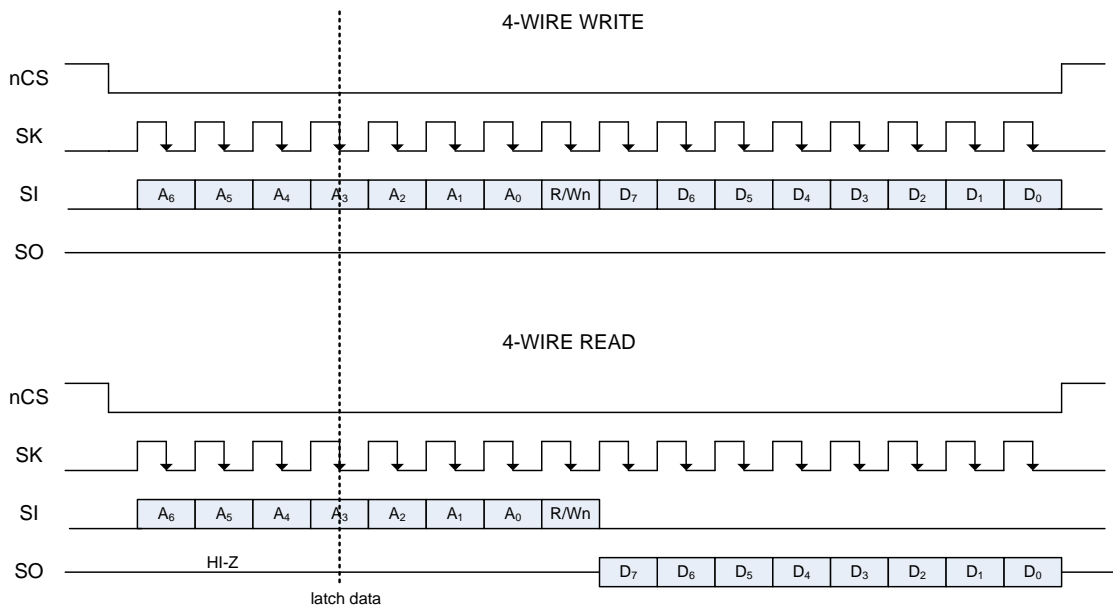


Figure 45: 4-wire host write and read timing (nCS_POL = '0', CPOL = '0', CPHA = '1')

Note 13 Accessing a register at high clock rates directly after writing it does not guarantee a correct value. It is recommended to keep a delay of one frame until re-accessing a register that has just been written (for example by writing/reading another register address in between).

9.2.8 2-wire communication

The 2-wire interface supports 7-bit address protocol. DA7210 responds to the device address 001 1010.

SK provides the 2-wire clock and SI carries all the control bidirectional 2-wire data. The 2-wire interface is open-drain, supporting multiple devices on a single line. The attached devices only drive the bus lines low by connecting them to ground.

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The bus lines are pulled high by pull-up resistors (2 KΩ to 20 KΩ range). As a result, two devices cannot conflict if they drive the bus simultaneously. In standard/fast mode the highest frequency of the bus is 400 kHz.

The exact frequency can be determined by the application and does not have any relation to the DA7210 internal clock signals. DA7210 will follow the host clock speed within the described limitations, and does not initiate any clock arbitration or slow down.

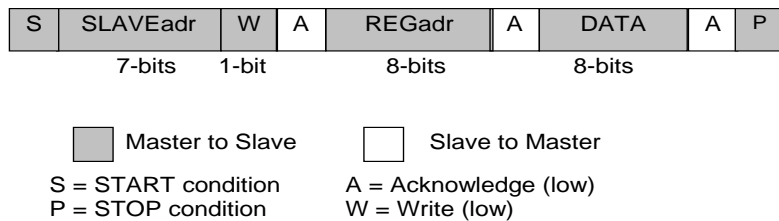
In high speed mode, the maximum frequency of the bus is 1.7 MHz. This mode is supported if the SK line is driven with a push-pull stage from the host and if the host enables an external 3 mA pull-up at the SI pin to decrease the rise time of the data. In this mode the SI line on DA7210 is able to sink up to 12 mA. In all other respects the high speed mode behaves as the standard/fast mode.

Communication on the 2-wire bus always takes place between two devices, one acting as the master and the other as the slave, but DA7210 will only operate as a slave. The 2-wire interface has direct (linear) access to the whole DA7210 register space (except 0x00 and 0x80). This is achieved by using the MSB of the 2-wire 8 bit register address as a selector of the register page.

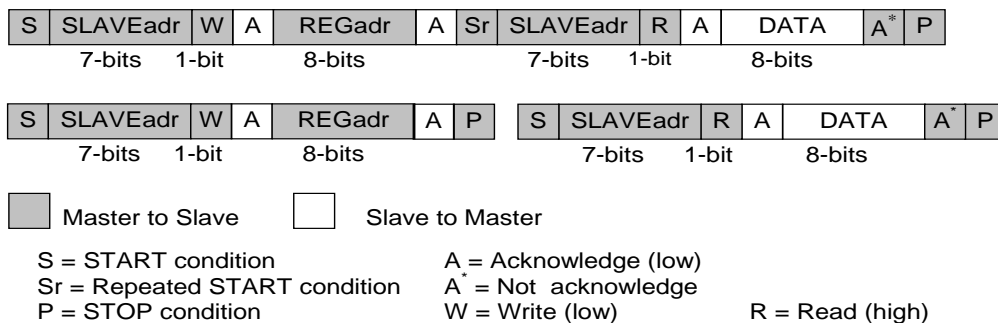
9.2.9 Details of the 2-wire control bus protocol

Data is transmitted access the 2-wire bus in groups of eight bits. To send a bit, the SI line is driven towards the intended state while the SK is LOW (a low on SI indicates a zero bit). Once the SI has settled, the SK line is brought HIGH and then LOW. This pulse on SK clocks the SI bit into the receiver's shift register.

A two byte serial protocol is used containing one byte for address and one byte data. Data and address transfer is MSB transmitted first for both read and write operations. All transmission begins with the START condition from the master during the bus is in IDLE state (the bus is free). It is initiated by a high to low transition on the SI line while the SK is in the high state (a STOP condition is indicated by a low to high transition on the SI line while the SK is in the high state).


Figure 46: 2-wire byte write (SI/DATA line)

When the host reads data from a register it first has to write access DA7210 with the target register address. It then read accesses DA7210 with a Repeated START or alternatively a second START condition. After receiving the data the host sends no acknowledge and terminates the transmission with a STOP condition.


Figure 47: Examples of 2-wire byte read (SI/DATA line)

Consecutive (page) read out mode is initiated from the master by sending an Acknowledge instead of Not acknowledge after receipt of the data word. The 2-wire control block then increments the address

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pointer to the next 2-wire address and sends the data to the master. This enables an unlimited read of data bytes until the master sends a NACK ('Not Acknowledge') directly after the receipt of data, followed by a subsequent STOP condition.

If a non-existent 2-wire address is read out then the DA7210 will return code zero.

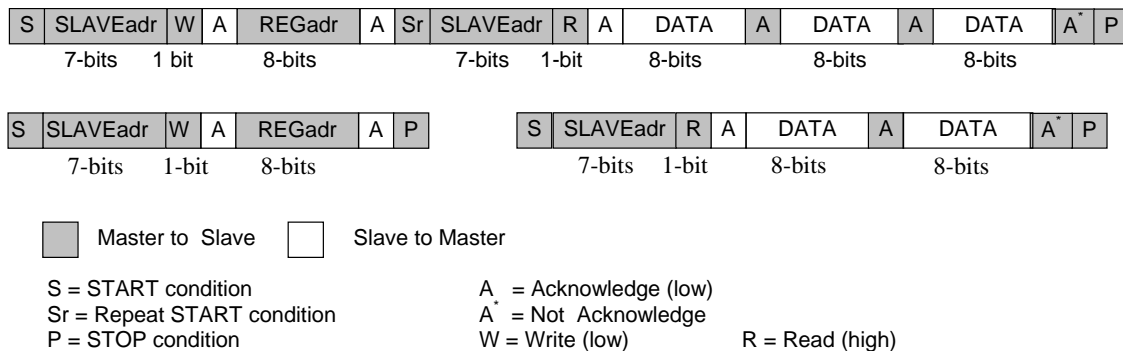


Figure 48: Examples of 2-wire page read (SI/DATA line)

Note 14 The slave address after the Repeated START condition must be the same as the previous slave address.

Consecutive (page) write mode is supported if the Master sends several data bytes following a slave register address. The 2-wire control block then increments the address pointer to the next 2-wire address, stores the received data and sends an Acknowledge until the master sends the STOP condition.

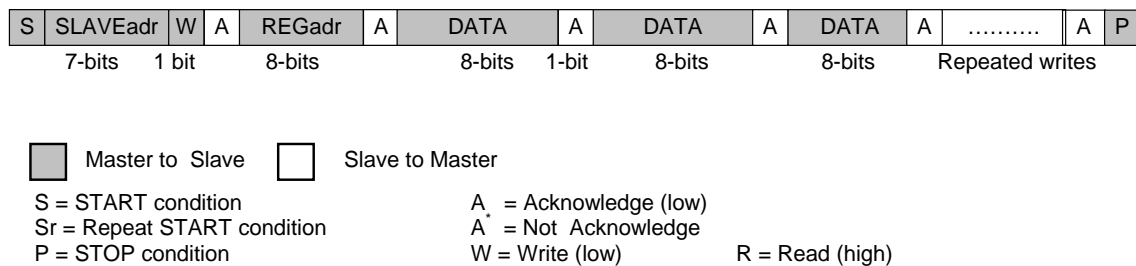


Figure 49: 2-wire page write (SI/DATA line)

Using the control WRITE_MODE (address 0x01, [Table 43](#)) the device can be configured to accept an alternate write mode where the host transmits alternate addresses and write data. This allows the host to perform several write operations to non-consecutive registers. Data will be stored at the previously received register address:

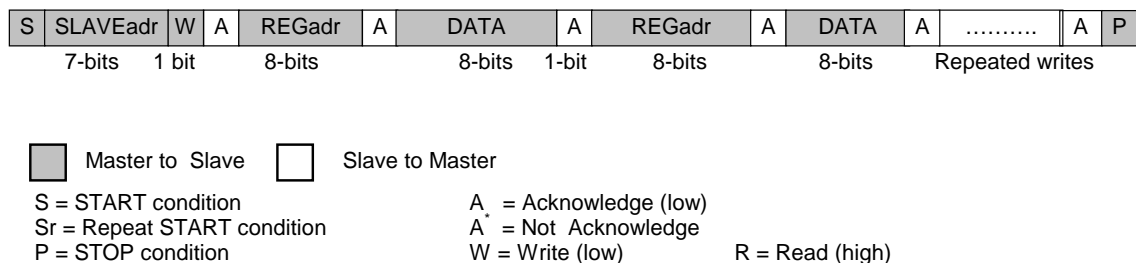


Figure 50: 2-wire repeated write (SI/DATA line)

If a new START or STOP condition occurs within a message, the bus will return to IDLE-mode.

10 Register definitions

WARNING: Any writes to RESERVED registers or bits can result in unexpected operation. This section gives an overview of all user accessible registers in the Register map table.

Detailed descriptions are given in Register description tables, which are grouped per functional block.

10.1 Register map

Table 41: Register map

| Address | Function | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Default |
|---------|-------------|-------------------|--------------------|------------------|----------------|------------------|--------------------|-----------------|------------|------------|
| 0 | PAGE0 | REG_PAGE | | | | | | | | 0b00000000 |
| 1 | CONTROL | WRITE_MODE | | | | NOISE_SUP | BIAS_EN | V_IO | | 0b00010000 |
| 2 | STATUS | | | | | MUTING | SOFTMUTED | I2S_LOCK | PLL_LOCK | 0b00000000 |
| 3 | STARTUP1 | SC_CLK_DIS | | | SC_OVERRIDE | | | | SC_MST_EN | 0b00000000 |
| 4 | STARTUP2 | | | | | STARTUP2[6:0] | | | | 0b00000000 |
| 5 | STARTUP3 | | | | | STARTUP3[6:0] | | | | 0b00000000 |
| 7 | MIC_L | MIC_L_EN | MICBIAS_EN | MICBIAS_SEL[1:0] | | MIC_L_MUTE | MIC_L_VOL[2:0] | | | 0b00000000 |
| 8 | MIC_R | MIC_R_EN | | | | MIC_R_MUTE | MIC_R_VOL[2:0] | | | 0b00000000 |
| 9 | AUX1_L | AUX1_L_EN | | AUX1_L_VOL[5:0] | | | | | | 0b00010000 |
| 0a | AUX1_R | AUX1_R_EN | | AUX1_R_VOL[5:0] | | | | | | 0b00010000 |
| 0b | AUX2 | | | | | AUX2_EN | AUX2_MUTE | AUX2_VOL[1:0] | | 0b00000000 |
| 0c | IN_GAIN | | INPGA_R_VOL[3:0] | | | INPGA_L_VOL[3:0] | | | | 0b00000000 |
| 0d | INMIX_L | IN_L_EN | | | IN_L_OUTMIX_L | IN_L_A2 | IN_L_A1_L | IN_L_MIC_R | IN_L_MIC_L | 0b00000000 |
| 0e | INMIX_R | IN_R_EN | | IN_R_IN_L | IN_R_OUTMIX_R | IN_R_A2 | IN_R_A1_R | IN_L_MIC_L | IN_L_MIC_R | 0b00000000 |
| 0f | ADC_HPF | ADC_VOICE_EN | ADC_VOICE_F0[2:0] | | | ADC_HPF_EN | ADC_HPF_F0[1:0] | | | 0b00001000 |
| 10 | ADC | ADC_R_EN | ADC_R_MUTE | | | ADC_L_EN | ADC_L_MUTE | | ALC_EN | 0b00000000 |
| 11 | ADC_EQ1_2 | ADC_EQ2_VOL[7:4] | | | | ADC_EQ1_VOL[3:0] | | | | 0b00000000 |
| 12 | ADC_EQ3_4 | ADC_EQ4_VOL[7:4] | | | | ADC_EQ3_VOL[3:0] | | | | 0b00000000 |
| 13 | ADC_EQ5 | ADC_EQ_EN | | ADC_EQ_GAIN[1:0] | | ADC_EQ5_VOL[3:0] | | | | 0b00000000 |
| 14 | DAC_HPF | DAC_VOICE_EN | DAC_VOICE_F0[2:0] | | | DAC_HPF_EN | DAC_MUTE | DAC_HPF_F0[1:0] | | 0b00001000 |
| 15 | DAC_L | DAC_L_INV | DAC_L_GAIN[6:0] | | | | | | | 0b00010000 |
| 16 | DAC_R | DAC_R_INV | DAC_R_GAIN[6:0] | | | | | | | 0b00010000 |
| 17 | DAC_SEL | DAC_R_EN | DAC_R_SRC[2:0] | | | DAC_L_EN | DAC_L_SRC[2:0] | | | 0b01010100 |
| 18 | SOFT_MUTE | SOFT_MUTE | RAMP_EN | | | | MUTE_RATE[2:0] | | | 0b01000000 |
| 19 | DAC_EQ1_2 | DAC_EQ2_VOL[7:4] | | | | DAC_EQ1_VOL[3:0] | | | | 0b00000000 |
| 1a | DAC_EQ3_4 | DAC_EQ4_VOL[7:4] | | | | DAC_EQ3_VOL[3:0] | | | | 0b00000000 |
| 1b | DAC_EQ5 | DAC_EQ_EN | | DAC_EQ_GAIN | | DAC_EQ5_VOL[3:0] | | | | 0b00000000 |
| 1c | OUTMIX_L | OUT_L_EN | OUT_L_INV | | OUT_L_DAC_L | OUT_L_IN_R | OUT_L_IN_L | OUT_L_A2 | OUT_L_A1_L | 0b00000000 |
| 1d | OUTMIX_R | OUT_R_EN | OUT_R_INV | | OUT_R_DAC_R | OUT_R_IN_R | OUT_R_IN_L | OUT_R_A2 | OUT_R_A1_R | 0b00000000 |
| 1e | OUT1_L | OUT1_L_EN | OUT1_L_SE | OUT1_L_VOL[5:0] | | | | | | 0b00110101 |
| 1f | OUT1_R | OUT1_R_EN | OUT1_R_SE | OUT1_R_VOL[5:0] | | | | | | 0b00110101 |
| 20 | OUT2 | OUT2_EN | OUT2_SEL[3:0] | | | OUT2_VOL[2:0] | | | | 0b00000011 |
| 21 | HP_L_VOL | | HP_L_VOL[5:0] | | | | | | 0b00010000 | |
| 22 | HP_R_VOL | | HP_R_VOL[5:0] | | | | | | 0b00010000 | |
| 23 | HP_CFG | HP_R_EN | HP_MODE | STEREO_TRACK | HP_HIGHZ_R | HP_L_EN | HP_2CAP_MODE | | HP_HIGHZ_L | 0b00000010 |
| 24 | ZEROX | HPZX_R_EN | HPZX_L_EN | OUTZX_R_EN | OUTZX_L_EN | INZX_R_EN | INZX_L_EN | A1ZX_R_EN | A1ZX_L_EN | 0b00000000 |
| 25 | DAI_SRC_SEL | DAI_IN_R_MIX | DAI_OUT_R_SRC[2:0] | | | DAI_IN_L_MIX | DAI_OUT_L_SRC[2:0] | | | 0b01110110 |
| 26 | DAI_CFG1 | DAI_MODE | | DAI_TDM_MONO | DAI_FRAME[1:0] | | DAI_WORD[1:0] | | 0b00000000 | |
| 27 | DAI_CFG2 | DAI_TDM_OFFS[7:0] | | | | | | | 0b00000000 | |
| 28 | DAI_CFG3 | DAI_EN | | | | DAI_OE | DAI_TDM | DAI_FORMAT[1:0] | | 0b00001000 |
| 29 | PLL_DIV1 | PLL_DIV_H[7:0] | | | | | | | | 0b00000000 |
| 2a | PLL_DIV2 | PLL_DIV_M[7:0] | | | | | | | | 0b00000000 |
| 2b | PLL_DIV3 | | PLL_BYP | MCLK_RANGE[1:0] | | | PLL_DIV_L[3:0] | | | 0b00010000 |
| 2c | PLL | PLL_EN | MCLK_SRM_EN | MCLK_DET_EN | MCLK_SHAPE_EN | FS[3:0] | | | | 0b00001010 |
| 2d | GP1A_A0L | GP1A_A0L[7:0] | | | | | | | | 0b00000000 |
| 2e | GP1A_A0H | GP1A_A0H[7:0] | | | | | | | | 0b01000000 |
| 2f | GP1B_A0L | GP1B_A0L[7:0] | | | | | | | | 0b00000000 |

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|----|----------|---------------|------------|
| 30 | GP1B_A0H | GP1B_A0H[7:0] | 0b01000000 |
| 31 | GP2A_A0L | GP2A_A0L[7:0] | 0b00000000 |
| 32 | GP2A_A0H | GP2A_A0H[7:0] | 0b01000000 |
| 33 | GP2B_A0L | GP2B_A0L[7:0] | 0b00000000 |
| 34 | GP2B_A0H | GP2B_A0H[7:0] | 0b01000000 |
| 35 | GP1C_A0L | GP1C_A0L[7:0] | 0b00000000 |
| 36 | GP1C_A0H | GP1C_A0H[7:0] | 0b01000000 |
| 37 | GP1D_A0L | GP1D_A0L[7:0] | 0b00000000 |
| 38 | GP1D_A0H | GP1D_A0H[7:0] | 0b01000000 |
| 39 | GP2C_A0L | GP2C_A0L[7:0] | 0b00000000 |
| 3a | GP2C_A0H | GP2C_A0H[7:0] | 0b01000000 |
| 3b | GP2D_A0L | GP2D_A0L[7:0] | 0b00000000 |
| 3c | GP2D_A0H | GP2D_A0H[7:0] | 0b01000000 |
| 3d | GP1A_A1L | GP1A_A1L[7:0] | 0b00000000 |
| 3e | GP1A_A1H | GP1A_A1H[7:0] | 0b00000000 |
| 3f | GP1B_A1L | GP1B_A1L[7:0] | 0b00000000 |
| 40 | GP1B_A1H | GP1B_A1H[7:0] | 0b00000000 |
| 41 | GP2A_A1L | GP2A_A1L[7:0] | 0b00000000 |
| 42 | GP2A_A1H | GP2A_A1H[7:0] | 0b00000000 |
| 43 | GP2B_A1L | GP2B_A1L[7:0] | 0b00000000 |
| 44 | GP2B_A1H | GP2B_A1H[7:0] | 0b00000000 |
| 45 | GP1C_A1L | GP1C_A1L[7:0] | 0b00000000 |
| 46 | GP1C_A1H | GP1C_A1H[7:0] | 0b00000000 |
| 47 | GP1D_A1L | GP1D_A1L[7:0] | 0b00000000 |
| 48 | GP1D_A1H | GP1D_A1H[7:0] | 0b00000000 |
| 49 | GP2C_A1L | GP2C_A1L[7:0] | 0b00000000 |
| 4a | GP2C_A1H | GP2C_A1H[7:0] | 0b00000000 |
| 4b | GP2D_A1L | GP2D_A1L[7:0] | 0b00000000 |
| 4c | GP2D_A1H | GP2D_A1H[7:0] | 0b00000000 |
| 4d | GP1A_A2L | GP1A_A2L[7:0] | 0b00000000 |
| 4e | GP1A_A2H | GP1A_A2H[7:0] | 0b00000000 |
| 4f | GP1B_A2L | GP1B_A2L[7:0] | 0b00000000 |
| 50 | GP1B_A2H | GP1B_A2H[7:0] | 0b00000000 |
| 51 | GP2A_A2L | GP2A_A2L[7:0] | 0b00000000 |
| 52 | GP2A_A2H | GP2A_A2H[7:0] | 0b00000000 |
| 53 | GP2B_A2L | GP2B_A2L[7:0] | 0b00000000 |
| 54 | GP2B_A2H | GP2B_A2H[7:0] | 0b00000000 |
| 55 | GP1C_A2L | GP1C_A2L[7:0] | 0b00000000 |
| 56 | GP1C_A2H | GP1C_A2H[7:0] | 0b00000000 |
| 57 | GP1D_A2L | GP1D_A2L[7:0] | 0b00000000 |
| 58 | GP1D_A2H | GP1D_A2H[7:0] | 0b00000000 |
| 59 | GP2C_A2L | GP2C_A2L[7:0] | 0b00000000 |
| 5a | GP2C_A2H | GP2C_A2H[7:0] | 0b00000000 |
| 5b | GP2D_A2L | GP2D_A2L[7:0] | 0b00000000 |
| 5c | GP2D_A2H | GP2D_A2H[7:0] | 0b00000000 |
| 5d | GP1A_B1L | GP1A_B1L[7:0] | 0b00000000 |
| 5e | GP1A_B1H | GP1A_B1H[7:0] | 0b00000000 |
| 5f | GP1B_B1L | GP1B_B1L[7:0] | 0b00000000 |
| 60 | GP1B_B1H | GP1B_B1H[7:0] | 0b00000000 |
| 61 | GP2A_B1L | GP2A_B1L[7:0] | 0b00000000 |
| 62 | GP2A_B1H | GP2A_B1H[7:0] | 0b00000000 |
| 63 | GP2B_B1L | GP2B_B1L[7:0] | 0b00000000 |

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|----|---------------|-------------------|--|-----------------|-----------|--------------------|------------|------------|------------|
| 64 | GP2B_B1H | GP2B_B1H[7:0] | | | | 0b00000000 | | | |
| 65 | GP1C_B1L | GP1C_B1L[7:0] | | | | 0b00000000 | | | |
| 66 | GP1C_B1H | GP1C_B1H[7:0] | | | | 0b00000000 | | | |
| 67 | GP1D_B1L | GP1D_B1L[7:0] | | | | 0b00000000 | | | |
| 68 | GP1D_B1H | GP1D_B1H[7:0] | | | | 0b00000000 | | | |
| 69 | GP2C_B1L | GP2C_B1L[7:0] | | | | 0b00000000 | | | |
| 6a | GP2C_B1H | GP2C_B1H[7:0] | | | | 0b00000000 | | | |
| 6b | GP2D_B1L | GP2D_B1L[7:0] | | | | 0b00000000 | | | |
| 6c | GP2D_B1H | GP2D_B1H[7:0] | | | | 0b00000000 | | | |
| 6d | GP1A_B2L | GP1A_B2L[7:0] | | | | 0b00000000 | | | |
| 6e | GP1A_B2H | GP1A_B2H[7:0] | | | | 0b00000000 | | | |
| 6f | GP1B_B2L | GP1B_B2L[7:0] | | | | 0b00000000 | | | |
| 70 | GP1B_B2H | GP1B_B2H[7:0] | | | | 0b00000000 | | | |
| 71 | GP2A_B2L | GP2A_B2L[7:0] | | | | 0b00000000 | | | |
| 72 | GP2A_B2H | GP2A_B2H[7:0] | | | | 0b00000000 | | | |
| 73 | GP2B_B2L | GP2B_B2L[7:0] | | | | 0b00000000 | | | |
| 74 | GP2B_B2H | GP2B_B2H[7:0] | | | | 0b00000000 | | | |
| 75 | GP1C_B2L | GP1C_B2L[7:0] | | | | 0b00000000 | | | |
| 76 | GP1C_B2H | GP1C_B2H[7:0] | | | | 0b00000000 | | | |
| 77 | GP1D_B2L | GP1D_B2L[7:0] | | | | 0b00000000 | | | |
| 78 | GP1D_B2H | GP1D_B2H[7:0] | | | | 0b00000000 | | | |
| 79 | GP2C_B2L | GP2C_B2L[7:0] | | | | 0b00000000 | | | |
| 7a | GP2C_B2H | GP2C_B2H[7:0] | | | | 0b00000000 | | | |
| 7b | GP2D_B2L | GP2D_B2L[7:0] | | | | 0b00000000 | | | |
| 7c | GP2D_B2H | GP2D_B2H[7:0] | | | | 0b00000000 | | | |
| 7d | GPF_SRC1 | GP_2AB_SRC[2:0] | | GP_1AB_SRC[2:0] | | 0b01100100 | | | |
| 7e | GPF_SRC2 | GP_2CD_SRC[2:0] | | GP_1CD_SRC[2:0] | | 0b01110101 | | | |
| 7f | DSP_CFG | DSP_MIX[2:0] | | GP_2CD_EN | GP_1CD_EN | GP_2AB_EN | GP_1AB_EN | 0b00000000 | |
| 80 | PAGE1 | REG_PAGE | | | | | 0b00000000 | | |
| 81 | CHIP_ID | MRC[3:0] | | | MMRC[3:0] | | | 0b00010001 | |
| 82 | INTERFACE | IF_BASE_ADDR[2:0] | | | | | | 0b00101100 | |
| 83 | ALC_MAX | ALC_MERGE | | ALC_MAX[5:0] | | | | 0b01000000 | |
| 84 | ALC_MIN | | | | | ALC_MIN[5:0] | | | 0b00000000 |
| 85 | ALC_NOIS | | | | | ALC_NOIS[5:0] | | | 0b00000000 |
| 86 | ALC_ATT | | | | | ALC_ATT[7:0] | | | 0b00000000 |
| 87 | ALC_REL | | | | | ALC_REL[7:0] | | | 0b00000000 |
| 88 | ALC_DEL | | | | | ALC_DEL[7:0] | | | 0b00000000 |
| 8A | A_HID_UNLOCK | | | | | A_HID_UNLOCK[7:0] | | | 0b00000000 |
| 8B | A_TEST_UNLOCK | | | | | A_TEST_UNLOCK[7:0] | | | 0b00000000 |
| 8F | A_PLL0 | | | | | SIGDEL_DISABLE | | | 0b00000000 |
| 90 | A_PLL1 | | | | | VCORST_EN | | | 0b00000000 |
| 95 | A_ADC0 | | | ADC_T2 | | VMID_BUFF_EN | | | 0b00000000 |
| 96 | A_DAC0 | | | | | | | | 0b00000000 |
| A2 | A_CPHP6 | | | | | CP_RISE_TIME | | | 0b10000000 |
| A7 | A_CP_MODE | | | | | A_CP_MODE[7:0] | | | 0b01111110 |

10.2 Control and status registers
Table 42: PAGE0 0x00

| Bit | Mode | Symbol | Description | Reset |
|-----|------|-----------|---|---------|
| 7 | RW | REG_PAGE0 | 4-wire mode register page selection 0: Selects Register R1 to R127 1: Selects Register R129 to R255 | 0 |
| 6:0 | R | Reserved | Reserved | 0000000 |

Table 43: CONTROL 0x01

| Bit | Mode | Symbol | Description | Reset |
|-----|------|--------------|--|-------|
| 7 | R/W | WRITE_MODE | 2-wire multiple write mode 0 = page Write Mode 1 = repeated Write Mode | 0 |
| 6:4 | R | Reserved | Reserved | 001 |
| 3 | R/W | NOISE_SUP | Enable noise suppression mode (see section 8.2.5) | 0 |
| 2 | R/W | BIAS_EN | Bias current to the entire chip 0 = bias off (device power down) 1 = supply bias current (device in operation) | 0 |
| 1 | R | VDDDIO_RANGE | VDDDIO voltage 0 = VDDIO > 2.65 V 1 = VDDIO <= 2.65 V Must be set to 1 | 0 |
| 0 | R | REG_EN | Digital Regulator enable 0 = disable 1 = enable | 0 |

Table 44: STATUS 0x02

| Bit | Mode | Symbol | Description | Reset |
|-----|------|-----------|--|-------|
| 7:4 | R | Reserved | Reserved | 0000 |
| 3 | R | MUTING | 0 = unmute 1 = mute | 0 |
| 2 | R | SOFTMUTED | 0 = normal mute 1 = softmute (ref. SOFTMUTE section) | 0 |
| 1 | R | I2S_LOCK | Digital audio interface (DAI) lock status 0 = not locked 1 = locked to frame rate lock | 0 |
| 0 | R | PLL_LOCK | PLL status 0 = PLL not locked 1 = PLL locked | 0 |

Table 45: STARTUP 1 0x03

| Bit | Mode | Symbol | Description | Reset |
|-----|------|-------------|--|-------|
| 7 | W | SC_CLK_DIS | System Controller Clock Disable 0 = clock enabled 1 = clock disabled (provides power saving) | 0 |
| 6:5 | R | Reserved | Reserved | 00 |
| 4 | R/W | SC_OVERRIDE | Test enable that forces everything to be enabled instantly on the next clock cycle | 0 |
| 3:1 | R | Reserved | Reserved | 00 |
| 0 | R/W | SC_MST_EN | System Controller Master Enable. All subsystems should be enabled first before enabling this bit. 0 = everything off 1 = device active | 0 |

Table 46: STARTUP 2 0x04

| Bit | Mode | Symbol | Description | Reset |
|-----|------|----------|--|---------|
| 7 | R | Reserved | Reserved | 0 |
| 6:0 | R/W | STARTUP2 | Output standby control. 0 = normal 1 = standby [6] – DAC R standby [5] – DAC L standby [4] – HP R standby [3] – HP L standby [2] – OUT2 standby [1] – OUT1R standby [0] – OUT1L standby | 0000000 |

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Table 47: STARTUP 3 0x05

| Bit | Mode | Symbol | Description | Reset |
|-----|------|----------|--|---------|
| 7 | R | Reserved | Reserved | 0 |
| 6:0 | R/W | STARTUP3 | Input standby control. 0 = normal 1 = standby [6] – ADC R standby [5] – ADC L standby [4] – AUX2 [3] – AUX1_R input standby [2] – AUX1_L input standby [1] – MIC_R input standby [0] – MIC_L input standby Note: Standby is to reduce the power consumption and not necessarily to mute the block. | 0000000 |

10.3 Codec registers
Table 48: MIC_L 0x07

| Bit | Mode | Symbol | Description | Reset |
|-----|------|-------------|--|-------|
| 7 | R/W | MIC_L_EN | Enable left MIC amplifier 0 = disable 1 = enable (must be set before SC_MST_EN) | 0 |
| 6 | R/W | MICBIAS_EN | Enable MICBIAS supply 0 = disable 1 = enable | 0 |
| 5:4 | R/W | MICBIAS_SEL | MIC bias voltage selection 00 = 1.5 V 01 = 1.6 V 10 = 2.2 V 11 = 2.3 V | 00 |
| 3 | R/W | MIC_L_MUTE | Mute left MIC amplifier 0 = unmute 1 = mute | 0 |
| 2:0 | R/W | MIC_L_VOL | Gain of left MIC amplifier 000 = -6 dB 011 = +12 dB 001 = 0 dB 100 = +18 dB 010 = +6 dB 101/110/111 = +24 dB | 000 |

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Table 49: MIC_R 0x08

| Bit | Mode | Symbol | Description | Reset |
|-----|------|------------|--|-------|
| 7 | R/W | MIC_R_EN | Enable right MIC amplifier 0 = disable 1 = enable (must be set before SC_MST_EN) | 0 |
| 6:4 | R | Reserved | Reserved | 000 |
| 3 | R/W | MIC_R_MUTE | Mute right MIC amplifier 0 = unmute 1 = mute | 0 |
| 2:0 | R/W | MIC_R_VOL | Gain of right MIC amplifier Setting option is the same as L-channel (0x07[2:0]) | 000 |

Table 50: AUX1_L 0x09

| Bit | Mode | Symbol | Description | Reset |
|-----|------|------------|---|--------|
| 7 | R/W | AUX1_L_EN | Enable left AUX1 amplifier 0 = disable 1 = enable (must be set before SC_MST_EN) | 0 |
| 6 | R | Reserved | Reserved | 0 |
| 5:0 | R/W | AUX1_L_VOL | Gain of left AUX1 amplifier 000000 to 010000 (default) = mute 010001 = -54 dB 010010 = -52.5 dB 010011 = -51 dB ... continuing in 1.5 dB steps through 110101 = 0 dB, to ... 111111 = +15 dB | 010000 |

Table 51: AUX1_R 0x0A

| Bit | Mode | Symbol | Description | Reset |
|-----|------|------------|--|--------|
| 7 | R/W | AUX1_R_EN | Enable right AUX1 amplifier 0 = disable 1 = enable (must be set before SC_MST_EN) | 0 |
| 6 | R | Reserved | Reserved | 0 |
| 5:0 | R/W | AUX1_R_VOL | Gain of right AUX1 amplifier 000000 to 010000 (default) = mute 010001 = -54 dB 010010 = -52.5 dB 010011 = -51 dB ... continuing in 1.5 dB steps through 110101 = 0 dB, to ... 111111 = +15 dB | 010000 |

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Table 52: AUX2 0x0B

| Bit | Mode | Symbol | Description | Reset |
|-----|------|-----------|--|-------|
| 7:4 | R | Reserved | Reserved | 0000 |
| 3 | R/W | AUX2_EN | Enable AUX2 amplifier 0: disable 1: enable | 0 |
| 2 | R/W | AUX2_MUTE | Mute AUX2 amplifier 0: un-mute 1: mute | 0 |
| 1:0 | R/W | AUX2_VOL | Gain of AUX2 amplifier 00: -6dB 01: 0dB 10: +6dB 11: +12dB | 00 |

Table 53: IN_GAIN 0x0C

| Bit | Mode | Symbol | Description | Reset |
|-----|------|-------------|---|-------|
| 7:4 | R/W | INPGA_R_VOL | Gain of right input PGA 0000 = -4.5 dB 0001 = -3 dB 0010 = -1.5 dB 0011 = 0 dB 0100 = +1.5 dB 0101 = + 3 dB 0110 = +4.5 dB 0111 = + 6 dB 1000 = + 7.5 dB 1001 = + 9 dB 1010 = +10.5 dB 1011 = +12 dB 1100 = +13.5 dB 1101 = +15 dB 1110 = +16.5 dB 1111 = +18 dB <i>While ALC is active, the gain is controlled by ALC and this register setting is not effective.</i> | 0000 |
| 3:0 | R/W | INPGA_L_VOL | Gain of left input PGA 0000 = -4.5 dB 0001 = -3 dB 0010 = -1.5 dB 0011 = 0 dB 0100 = +1.5 dB 0101 = + 3 dB 0110 = +4.5 dB 0111 = + 6 dB 1000 = + 7.5 dB 1001 = + 9 dB 1010 = +10.5 dB 1011 = +12 dB 1100 = +13.5 dB 1101 = +15 dB 1110 = +16.5 dB 1111 = +18 dB <i>While ALC is active, the gain is controlled by ALC and this register setting is not effective.</i> | 0000 |

Table 54: INMIX_L 0x0D

| Bit | Mode | Symbol | Description | Reset |
|-----|------|---------------|---|-------|
| 7 | R/W | IN_L_EN | Enable left input PGA 0 = disable 1 = enable (must be set before SC_MST_EN) | 0 |
| 6:5 | R | Reserved | Reserved | 00 |
| 4 | R/W | IN_L_OUTMIX_L | 1 = Add OUTMIX_L into input mixer L | 0 |
| 3 | R/W | IN_L_A2 | 1 = Add AUX2 into input mixer L | 0 |
| 2 | R/W | IN_L_A1_L | 1 = Add AUX1_L into input mixer L | 0 |
| 1 | R/W | IN_L_MIC_R | 1 = Add MIC_R into input mixer L | 0 |
| 0 | R/W | IN_L_MIC_L | 1 = Add MIC_L into input mixer L | 0 |

Table 55: INMIX_R 0x0E

| Bit | Mode | Symbol | Description | Reset |
|-----|------|---------------|--|-------|
| 7 | R/W | IN_R_EN | Enable right input PGA 0 = disable 1 = enable (must be set before SC_MST_EN) | 0 |
| 6 | R | Reserved | Reserved | 0 |
| 5 | R/W | IN_R_IN_L | 1 = Add INPGA_L (stereo to mono) | 0 |
| 4 | R/W | IN_R_OUTMIX_R | 1 = Add OUTMIX_R into input mixer R | 0 |
| 3 | R | IN_R_A2 | 1 = Add AUX2 into input mixer R | 0 |
| 2 | R/W | IN_R_A1_R | 1 = Add AUX1_R into input mixer R | 0 |
| 1 | R/W | IN_R_MIC_L | 1 = Add MIC_L into input mixer R | 0 |
| 0 | R/W | IN_R_MIC_R | 1 = Add MIC_R into input mixer R | 0 |

Table 56: ADC_HPFC 0x0F

| Bit | Mode | Symbol | Description | Reset |
|-----|------|--------------|--|-------|
| 7 | R/W | ADC_VOICE_EN | ADC Voice Filter 0 = disable 1 = enable | 0 |
| 6:4 | R/W | ADC_VOICE_F0 | ADC Voice (8 kHz) High pass 3 dB cut-off at: 000 = 2.5 Hz 001 = 25 Hz 010 = 50 Hz 011 = 100 Hz 100 = 150 Hz 101 = 200 Hz 110 = 300 Hz 111 = 400 Hz | 000 |
| 3 | R/W | ADC_HPFC_EN | ADC High Pass Filter 0 = disable 1 = enable | 1 |
| 2 | R | Reserved | Reserved | 0 |
| 1:0 | R/W | ADC_HPFC_F0 | ADC High Pass Filter f0 is at 00 = $F_s/8192 \times \pi$ 01 = $F_s/4096 \times \pi$ 10 = $F_s/2048 \times \pi$ 11 = $F_s/1024 \times \pi$ | 00 |

Table 57: ADC 0x10

| Bit | Mode | Symbol | Description | Reset |
|-----|------|------------|--|-------|
| 7 | R/W | ADC_R_EN | Enable right ADC channel 0 = disable 1 = enable (must be set before SC_MST_EN) | 0 |
| 6 | R/W | ADC_R_MUTE | Mute right ADC channel 0 = unmute 1 = mute | 0 |
| 5:4 | R | Reserved | Reserved | 00 |
| 3 | R/W | ADC_L_EN | Enable left ADC channel 0 = disable 1 = enable (must be set before SC_MST_EN) | 0 |
| 2 | R/W | ADC_L_MUTE | Mute left ADC channel 0 = unmute 1 = mute | 0 |
| 1 | R | Reserved | Reserved | 0 |
| 0 | RW | ALC_EN | ALC enable 0 = disable 1 = enable | 0 |

Table 58: ADC_EQ1_2 0x11

| Bit | Mode | Symbol | Description | Reset |
|-----|------|-------------|---|-------|
| 7:4 | R/W | ADC_EQ2_VOL | Gain of ADC 5-Band EQ band 2: 0000 = +12 dB 0001 = +10.5 dB 0010 = +9 dB 0011 = +7.5 dB 0100 = +6 dB 0101 = +4.5 dB 0110 = +3 dB 0111 = +1.5 dB 1000 = 0 dB 1001 = - 1.5 dB 1010 = - 3 dB 1011 = - 4.5 dB 1100 = - 6 dB 1101 = - 7.5 dB 1110 = - 9 dB 1111 = -10.5 dB | 0000 |
| 3:0 | R/W | ADC_EQ1_VOL | Gain of ADC 5-Band EQ band 1: 0000 = +12 dB 0001 = +10.5 dB 0010 = +9 dB 0011 = +7.5 dB 0100 = +6 dB 0101 = +4.5 dB 0110 = +3 dB 0111 = +1.5 dB 1000 = 0 dB 1001 = - 1.5 dB 1010 = - 3 dB 1011 = - 4.5 dB 1100 = - 6 dB 1101 = - 7.5 dB 1110 = - 9 dB 1111 = -10.5 dB | 0000 |

Table 59: ADC_EQ3_4 0x12

| Bit | Mode | Symbol | Description | Reset |
|-----|------|-------------|---|-------|
| 7:4 | R/W | ADC_EQ4_VOL | Gain of ADC 5-Band EQ band 4: 0000 = +12 dB 0001 = +10.5 dB 0010 = +9 dB 0011 = +7.5 dB 0100 = +6 dB 0101 = +4.5 dB 0110 = +3 dB 0111 = +1.5 dB 1000 = 0 dB 1001 = - 1.5 dB 1010 = - 3 dB 1011 = - 4.5 dB 1100 = - 6 dB 1101 = - 7.5 dB 1110 = - 9 dB 1111 = -10.5 dB | 0000 |
| 3:0 | R/W | ADC_EQ3_VOL | Gain of ADC 5-Band EQ band 3: 0000 = +12 dB 0001 = +10.5 dB 0010 = +9 dB 0011 = +7.5 dB 0100 = +6 dB 0101 = +4.5 dB 0110 = +3 dB 0111 = +1.5 dB 1000 = 0 dB 1001 = - 1.5 dB 1010 = - 3 dB 1011 = - 4.5 dB 1100 = - 6 dB 1101 = - 7.5 dB 1110 = - 9 dB 1111 = -10.5 dB | 0000 |

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Table 60: ADC_EQ5 0x13

| Bit | Mode | Symbol | Description | Reset |
|-----|------|-------------|---|-------|
| 7 | R/W | ADC_EQ_EN | Enable ADC 5-Band EQ 0 = disable 1 = enable | 7 |
| 6 | R | Reserved | Reserved | 6 |
| 5:4 | R/W | ADC_EQ_GAIN | Gain of ADC 5-BandEQ: 00 = 0 dB 01 = -6 dB 10 = -12 dB 11 = -18 dB | 5:4 |
| 3:0 | R/W | ADC_EQ5_VOL | Gain of ADC 5-Band EQ band 5: 0000 = +12 dB 0001 = +10.5 dB 0010 = +9 dB 0011 = +7.5 dB 0100 = +6 dB 0101 = +4.5 dB 0110 = +3 dB 0111 = +1.5 dB 1000 = 0 dB 1001 = - 1.5 dB 1010 = - 3 dB 1011 = - 4.5 dB 1100 = - 6 dB 1101 = - 7.5 dB 1110 = - 9 dB 1111 = -10.5 dB | 3:0 |

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Table 61: DAC_HPFC 0x14

| Bit | Mode | Symbol | Description | Reset |
|-----|------|--------------|---|-------|
| 7 | R/W | DAC_VOICE_EN | DAC Voice Filter 0 = disable 1 = enable | 0 |
| 6:4 | R/W | DAC_VOICE_F0 | DAC Voice (8 kHz) High pass 3 dB cut-off at: 000 = 2.5 Hz 001 = 25 Hz 010 = 50 Hz 011 = 100 Hz 100 = 150 Hz 101 = 200 Hz 110 = 300 Hz 111 = 400 Hz For 11.025/12.0 and 16 kHz see Table 28 . | 000 |
| 3 | R/W | DAC_HPFC_EN | DAC High Pass Filter 0 = disable 1 = enable | 1 |
| 2 | R/W | DAC_MUTE | Mute DAC (both channels) | 0 |
| 1:0 | R/W | DAC_HPFC_F0 | DAC High Pass Filter f0 is at 00 = $F_s/8192 \times \pi$ 01 = $F_s/4096 \times \pi$ 10 = $F_s/2048 \times \pi$ 11 = $F_s/1024 \times \pi$ | 00 |

Table 62: DAC_L 0x15

| Bit | Mode | Symbol | Description | Reset |
|-----|------|------------|--|---------|
| 7 | R/W | DAC_L_INV | left DAC channel inversion 0 = normal 1 = Inverted | 0 |
| 6:0 | R/W | DAC_L_GAIN | DAC left channel digital volume control 0000000 = 12 dB 0000001 = 11.25 dB ... continuing in 0.75 dB steps through 0010000 = 0 dB 0010001 = -0.75 dB ...to 1110111 = -77.25 dB 1111xxx = mute | 0010000 |

Table 63: DAC_R 0x16

| Bit | Mode | Symbol | Description | Reset |
|-----|------|------------|---|---------|
| 7 | R/W | DAC_R_INV | 0 = normal 1 = Invert right DAC channel | 0 |
| 6:0 | R/W | DAC_R_GAIN | DAC right channel digital volume control 0000000 = 12 db 0000001 = 11.25 dB ... continuing in 0.75 dB steps through 0010000 = 0 dB 0010001 = -0.75 dB ...to 1110111 = -77.25 dB 1111xxx = mute | 0010000 |

Table 64: DAC_SEL 0x17

| Bit | Mode | Symbol | Description | Reset |
|-----|------|-----------|---|-------|
| 7 | R/W | DAC_R_EN | Enable right DAC channel 0 = disable 1 = enable (must be set before SC_MST_EN) | 0 |
| 6:4 | R/W | DAC_R_SRC | DAC_R input source selection: 000 = 1AB 001 = 2AB 010 = 1CD 011 = 2CD 100 = DAI_L 101 = DAI_R 110 = ADC_L 111 = ADC_R | 101 |
| 3 | R/W | DAC_L_EN | Enable left DAC channel 0 = disable 1 = enable (must be set before SC_MST_EN) | 0 |
| 2:0 | R/W | DAC_L_SRC | DAC_L input source selection: 000 = 1AB 001 = 2AB 010 = 1CD 011 = 2CD 100 = DAI_L 101 = DAI_R 110 = ADC_L 111 = ADC_R | 100 |

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Table 65: SOFTMUTE 0x18

| Bit | Mode | Symbol | Description | Reset |
|-----|------|-----------|---|-------|
| 7 | R/W | SOFT_MUTE | Softmute trigger 0 = disabled 1 = start SOFTMUTE | 0 |
| 6 | R/W | RAMP_EN | Digital gain ramping 0 = disabled (immediate) 1 = enabled (ramping) | 1 |
| 5:3 | R | Reserved | Reserved | 000 |
| 2:0 | R/W | MUTE_RATE | 000 = 1 sample/0.1875 dB 001 = 2 samples/0.1875 dB 010 = 4 samples/0.1875 dB 011 = 8 samples/0.1875 dB 100 = 16 samples/0.1875 dB 101 = 32 samples/0.1875 dB 110 = 64 samples/0.1875 dB 111 = not used | 000 |

Table 66: DAC_EQ1_2 0x19

| Bit | Mode | Symbol | Description | Reset |
|-----|------|-------------|---|-------|
| 7:4 | R/W | DAC_EQ2_VOL | Gain of DAC 5-Band EQ band 2: 0000 = +12 dB 0001 = +10.5 dB 0010 = +9 dB 0011 = +7.5 dB 0100 = +6 dB 0101 = +4.5 dB 0110 = +3 dB 0111 = +1.5 dB 1000 = 0 dB 1001 = - 1.5 dB 1010 = - 3 dB 1011 = - 4.5 dB 1100 = - 6 dB 1101 = - 7.5 dB 1110 = - 9 dB 1111 = -10.5 dB | 0000 |
| 3:0 | R/W | DAC_EQ1_VOL | Gain of DAC 5-Band EQ band 1: 0000 = +12 dB 0001 = +10.5 dB 0010 = +9 dB 0011 = +7.5 dB 0100 = +6 dB 0101 = +4.5 dB 0110 = +3 dB 0111 = +1.5 dB 1000 = 0 dB 1001 = - 1.5 dB 1010 = - 3 dB 1011 = - 4.5 dB 1100 = - 6 dB 1101 = - 7.5 dB 1110 = - 9 dB 1111 = -10.5 dB | 0000 |

Table 67: DAC_EQ3_4 0x1A

| Bit | Mode | Symbol | Description | Reset |
|-----|------|-------------|---|-------|
| 7:4 | R/W | DAC_EQ4_VOL | Gain of DAC 5-Band EQ band 4: 0000 = +12 dB 0001 = +10.5 dB 0010 = +9 dB 0011 = +7.5 dB 0100 = +6 dB 0101 = +4.5 dB 0110 = +3 dB 0111 = +1.5 dB 1000 = 0 dB 1001 = - 1.5 dB 1010 = - 3 dB 1011 = - 4.5 dB 1100 = - 6 dB 1101 = - 7.5 dB 1110 = - 9 dB 1111 = -10.5 dB | 0000 |
| 3:0 | R/W | DAC_EQ3_VOL | Gain of DAC 5-Band EQ band 3: 0000 = +12 dB 0001 = +10.5 dB 0010 = +9 dB 0011 = +7.5 dB 0100 = +6 dB 0101 = +4.5 dB 0110 = +3 dB 0111 = +1.5 dB 1000 = 0 dB 1001 = - 1.5 dB 1010 = - 3 dB 1011 = - 4.5 dB 1100 = - 6 dB 1101 = - 7.5 dB 1110 = - 9 dB 1111 = -10.5 dB | 0000 |

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Table 68: DAC_EQ5 0x1B

| Bit | Mode | Symbol | Description | Reset |
|-----|------|-------------|---|-------|
| 7 | R/W | DAC_EQ_EN | Enable DAC 5-Band EQ 0 = disable 1 = enable | 0 |
| 6:4 | R | Reserved | Reserved | 000 |
| 3:0 | R/W | DAC_EQ5_VOL | Gain of DAC 5-Band EQ band 5: 0000 = +12 dB 0001 = +10.5 dB 0010 = +9 dB 0011 = +7.5 dB 0100 = +6 dB 0101 = +4.5 dB 0110 = +3 dB 0111 = +1.5 dB 1000 = 0 dB 1001 = - 1.5 dB 1010 = - 3 dB 1011 = - 4.5 dB 1100 = - 6 dB 1101 = - 7.5 dB 1110 = - 9 dB 1111 = -10.5 dB | 0000 |

Table 69: OUTMIX_L 0x1C

| Bit | Mode | Symbol | Description | Reset |
|-----|------|-------------|---|-------|
| 7 | R/W | OUT_L_EN | Enable left output PGA 0 = disable 1 = enable (must be set before SC_MST_EN) | 0 |
| 6 | R/W | OUT_L_INV | OUTMIX left channel inversion 0 = normal 1 = Invert (not active for signal routed from DAC_L) | 0 |
| 5 | R | Reserved | Reserved | 0 |
| 4 | R/W | OUT_L_DAC_L | 1 = Add DAC_L | 0 |
| 3 | R/W | OUT_L_IN_R | 1 = Add IN_R | 0 |
| 2 | R/W | OUT_L_IN_L | 1 = Add IN_L | 0 |
| 1 | R/W | OUT_L_A2 | 1 = Add AUX2 | 0 |
| 0 | R/W | OUT_L_A1_L | 1 = Add AUX1_L | 0 |

Table 70: OUTMIX_R 0x1D

| Bit | Mode | Symbol | Description | Reset |
|-----|------|-------------|--|-------|
| 7 | R/W | OUT_R_EN | Enable right output PGA 0 = disable 1 = enable (must be set before SC_MST_EN) | 0 |
| 6 | R/W | OUT_R_INV | OUTMIX right channel inversion 0 = normal 1 = invert (not active for signal routed from DAC_L) | 0 |
| 5 | R | Reserved | Reserved | 0 |
| 4 | R/W | OUT_R_DAC_R | 1 = Add DAC_R | 0 |
| 3 | R/W | OUT_R_IN_R | 1 = Add IN_R | 0 |
| 2 | R/W | OUT_R_IN_L | 1 = Add IN_L | 0 |
| 1 | R/W | OUT_R_A2 | 1 = Add AUX2 | 0 |
| 0 | R/W | OUT_R_A1_R | 1 = Add AUX1_R | 0 |

Table 71: OUT1_L 0x1E

| Bit | Mode | Symbol | Description | Reset |
|-----|------|------------|---|--------|
| 7 | R/W | OUT1_L_EN | Enable left OUT1 amplifier 0 = disable 1 = enable (must be set before SC_MST_EN) | 0 |
| 6 | R/W | OUT1_L_SE | OUT1 L single-ended mode selection 0 = differential mode 1 = single-ended mode | 0 |
| 5:0 | R/W | OUT1_L_VOL | OUT1 left channel volume control 000000 – 001111 = Reserved 010000 = mute 010001 = -54 dB 010010 = -52.5 dB ... continuing in 1.5 dB steps through 110101 = 0 dB (default) to... 111111 = 15 dB | 110101 |

Table 72: OUT1_R 0x1F

| Bit | Mode | Symbol | Description | Reset |
|-----|------|------------|--|--------|
| 7 | R/W | OUT1_R_EN | Enable right OUT1 amplifier 0 = disable 1 = enable (must be set before SC_MST_EN) | 0 |
| 6 | R/W | OUT1_R_SE | OUT1 R single-ended mode selection 0 = differential mode 1 = single-ended mode | 0 |
| 5:0 | R/W | OUT1_R_VOL | OUT1 right channel volume control 000000 – 001111 = Reserved 010000 = mute 010001 = -54 dB 010010 = -52.5 dB ... continuing in 1.5 dB steps through 110101 = 0 dB (default) to... 111111 = 15 dB | 110101 |

Table 73: OUT2 0x20

| Bit | Mode | Symbol | Description | Reset |
|-----|------|---------------|--|-------|
| 7 | R/W | 1OUT2_EN | Enable OUT2 amplifier 0: disable 1: enable | 0 |
| 6 | R/W | OUT2_OUTMIX_L | 1: Add OUTMIX_L | 0 |
| 5 | R/W | OUT2_OUTMIX_R | 1: Add OUTMIX_R | 0 |
| 4 | R/W | OUT2_IN_L | 1: Add INPGA_L | 0 |
| 3 | R/W | OUT2_IN_R | 1: Add INPGA_R | 0 |
| 2:0 | R/W | OUT2_VOL | OUT2 gain control 000/001/010 : reserved 011: - 18dB | 000 |

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Table 74: HP_L_VOL 0x21

| Bit | Mode | Symbol | Description | Reset |
|-----|------|----------|--|--------|
| 7:6 | R | Reserved | Reserved | 00 |
| 5:0 | R/W | HP_L_VOL | Head phone left channel volume control 000000 – 001111 = Reserved 010000 = mute (default) 010001 = -54 dB 010010 = -52.5 dB ... continuing in 1.5 dB steps through 110101 = 0 dB to... 111111 = 15 dB If you wish the right channel volume to be the same as left channel, please refer to Table 76 (0x23 HP_CFG[5] STEREO_TRACK) | 010000 |

Table 75: HP_R_VOL 0x22

| Bit | Mode | Symbol | Description | Reset |
|-----|------|----------|---|--------|
| 7:6 | R | Reserved | Reserved | 00 |
| 5:0 | R/W | HP_R_VOL | Head phone right channel volume control 000000 – 001111 = Reserved 010000 = mute (default) 010001 = -54 dB 010010 = -52.5 dB ... continuing in 1.5 dB steps through 110101 = 0 dB to... 111111 = 15 dB If you wish the right channel volume to be the same as left channel, please refer to Table 76 (0x23 HP_CFG[5] STEREO_TRACK) | 010000 |

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Table 76: HP_CFG 0x23

| Bit | Mode | Symbol | Description | Reset |
|-----|------|--------------|--|-------|
| 7 | R/W | HP_R_EN | Enable right headphone amplifier 0 = disable 1 = enable (must be set before SC_MST_EN) | 0 |
| 6 | R/W | Reserved | Reserved | 0 |
| 5 | R/W | STEREO_TRACK | 1 = HP_R volume also controls HP_L | 0 |
| 4 | R/W | HP_HIGHZ_R | Set right head phone out to high impedance | 0 |
| 3 | R/W | HP_L_EN | Enable left headphone amplifier 0 = disable 1 = enable (must be set before SC_MST_EN) | 0 |
| 2 | R/W | Reserved | Reserved | 0 |
| 1 | R/W | HP_2CAP_MODE | Set charge pump to 2 capacitor mode | 1 |
| 0 | R/W | HP_HIGHZ_L | Set left head phone out to high impedance | 0 |

Table 77: ZEROX 0x24

| Bit | Mode | Symbol | Description | Reset |
|-----|------|-------------|--|-------|
| 7 | R/W | HPZX_R_EN | Enable zero crossing for right HP gain update | 0 |
| 6 | R/W | HPZX_L_EN | Enable zero crossing for left HP gain update | 0 |
| 5 | R/W | OUTZX_R_EN | Enable zero crossing for right OUT1 gain update | 0 |
| 4 | R/W | OUTZX_L_EN | Enable zero crossing for left OUT1 gain update | 0 |
| 3 | R/W | INZX_R_EN | Enable zero crossing for right input PGA gain update | 0 |
| 2 | R/W | INZX_L_EN | Enable zero crossing for left input PGA gain update | 0 |
| 1 | R/W | AUX1ZX_R_EN | Enable zero crossing for right AUX1 amp gain update | 0 |
| 0 | R/W | AUX1ZX_L_EN | Enable zero crossing for left AUX1 amp gain update | 0 |

Table 78: DAI_SRC_SEL 0x25

| Bit | Mode | Symbol | Description | Reset |
|-----|------|---------------|--|-------|
| 7 | R/W | DAI_IN_R_MIX | 1 = DAI receive right channel is mixed from L+R data | 0 |
| 6:4 | R/W | DAI_OUT_R_SRC | DAI_R transmit source selection: 000 = 1AB 001 = 2AB 010 = 1CD 011 = 2CD 100 = DAI_L (cross loop back) 101 = DAI_R (loop back) 110 = ADC_L 111 = ADC_R | 111 |
| 3 | R/W | DAI_IN_L_MIX | 1 = DAI receive left channel is mixed from L+R data | 0 |
| 2:0 | R/W | DAI_OUT_L_SRC | DAI_L transmit source selection: 000 = 1AB 001 = 2AB 010 = 1CD 011 = 2CD 100 = DAI_L (cross loop back) 101 = DAI_R (loop back) 110 = ADC_L 111 = ADC_R | 110 |

Table 79: DAI_CFG1 0x26

| Bit | Mode | Symbol | Description | Reset |
|-----|------|--------------|---|-------|
| 7 | R/W | DAI_MODE | 0 = DA7210 is clock slave 1 = DA7210 is clock master | 0 |
| 6:5 | R | Reserved | Reserved | 00 |
| 4 | R/W | DAI_TDM_MONO | 0 = TDM mode is stereo 1 = TDM transmits/receives left channel left DAI channel only | 0 |
| 3:2 | R/W | DAI_FRAME | Data transmission frame length: 00 = 2 x DAI_WORD 01 = 64 bitclocks 10 = 128 bitclocks 11 = 256 bitclocks | 00 |
| 1:0 | R/W | DAI_WORD | Data word length: 00 = 16 bits 01 = 20 bits 10 = 24 bits 11 = 32 bits | 00 |

Table 80: DAI_CFG2 0x27

| Bit | Mode | Symbol | Description | Reset |
|-----|------|--------------|---|----------|
| 7:0 | R/W | DAI_TDM_OFFS | TDM data for device is valid at this offset from beginning of frame. The offset is measured in the number clock cycles. | 00000000 |

Table 81: DAI_CFG3 0x28

| Bit | Mode | Symbol | Description | Reset |
|-----|------|------------|---|-------|
| 7 | R/W | DAI_EN | Enable digital audio interface 0 = disable 1 = enable | 7 |
| 6:4 | R | Reserved | Reserved | 6:4 |
| 3 | R/W | DAI_OE | DATOUT enable: 0 = disable (tristate when ADC is disabled) 1 = enabled | 3 |
| 2 | R/W | DAI_TDM | Tristate DATOUT mode enable 0 = disable (normal) 1 = enable (TDM mode) | 2 |
| 1:0 | R/W | DAI_FORMAT | Digital Audio Interface format selection 00 = I2S mode 01 = Left Justified mode 10 = right justified mode 11 = DSP mode | 1:0 |

Table 82: PLL_DIV1 0x29

| Bit | Mode | Symbol | Description | Reset |
|-----|------|-----------|---|----------|
| 7:0 | R/W | PLL_DIV_H | Feedback divider ratio bit [19:12]. Refer to Table 32 and Table 33 for suggested settings. | 00000000 |

Table 83: PLL_DIV2 0x2A

| Bit | Mode | Symbol | Description | Reset |
|-----|------|-----------|--|----------|
| 7:0 | R/W | PLL_DIV_M | Feedback divider ratio bit [11:4]. Refer to Table 32 and Table 33 for suggested settings. | 00000000 |

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Table 84: PLL_DIV3 0x2B

| Bit | Mode | Symbol | Description | Reset |
|-----|------|------------|---|-------|
| 7 | R | Reserved | Reserved | 0 |
| 6 | R/W | PLL_BYP | Bypass PLL 0 = disable (do not disable unless PLL is operational) 1 = enable (PLL bypassed) | 0 |
| 5:4 | R/W | MCLK_RANGE | MCLK frequency range: 00 = 32.768 kHz 01 = 10-20 MHz 10 = 20-40 MHz 11 = 40-80 MHz | 01 |
| 3:0 | R/W | PLL_DIV_L | Feedback divider ratio bit [3:0]. Refer to Table 32 and Table 33 for suggested settings. | 0000 |

Table 85: PLL 0x2C

| Bit | Mode | Symbol | Description | Reset |
|-----|------|---------------|--|-------|
| 7 | R/W | PLL_EN | PLL enable 0 = disable and bypass PLL 1 = enable PLL | 0 |
| 6 | R/W | MCLK_SRM_EN | Sample rate tracking 0 = disabled 1 = enabled | 0 |
| 5 | R/W | MCLK_DET_EN | automatic detection of sample rate 0 = disabled 1 = enabled | 0 |
| 4 | R/W | MCLK_SHAPE_EN | Enable MCLK shaper for low level non TTL signals 0 = disabled 1 = enabled | 0 |
| 3:0 | R/W | FS | In MCLK_DET mode, the value read from this register will be the automatically detected sample rate from the PLL track circuitry. This will be updated on the positive edge of the DAI clock. 0000 = reserved 0001 = 8 kHz 0010 = 11.025 kHz 0011 = 12 kHz 0100 = reserved 0101 = 16 kHz 0110 = 22.05 kHz 0111 = 24 kHz 1000 = reserved 1001 = 32 kHz 1010 = 44.1 kHz 1011 = 48 kHz 1100 = reserved 1101 = reserved 1110 = 88.2 kHz 1111 = 96 kHz | 1010 |

10.4 GP filter engine

Table 86: GP1A A0L 0x2D

| Bit | Mode | Symbol | Description | Reset |
|-----|------|----------|-------------------------------|----------|
| 7:0 | W | GP1A A0L | A0L bit 7:0 of A0 coefficient | 00000000 |

Table 87: GP1A A0H 0x2E

| Bit | Mode | Symbol | Description | Reset |
|-----|------|----------|--------------------------------|----------|
| 7:0 | W | GP1A A0H | A0H bit 15:8 of A0 coefficient | 01000000 |

Table 88: GP1B A0L 0x2F

| Bit | Mode | Symbol | Description | Reset |
|-----|------|----------|-------------------------------|----------|
| 7:0 | W | GP1B_A0L | A0L bit 7:0 of A0 coefficient | 00000000 |

Table 89: GP1B A0H 0x30

| Bit | Mode | Symbol | Description | Reset |
|-----|------|----------|--------------------------------|----------|
| 7:0 | W | GP1B_A0H | A0H bit 15:8 of A0 coefficient | 01000000 |

Table 90: GP2A A0L 0x31

| Bit | Mode | Symbol | Description | Reset |
|-----|------|----------|-------------------------------|----------|
| 7:0 | W | GP2A_A0L | A0L bit 7:0 of A0 coefficient | 00000000 |

Table 91: GP2A A0H 0x32

| Bit | Mode | Symbol | Description | Reset |
|-----|------|----------|--------------------------------|----------|
| 7:0 | W | GP2A_A0H | A0H bit 15:8 of A0 coefficient | 01000000 |

Table 92: GP2B_A0L 0x33

| Bit | Mode | Symbol | Description | Reset |
|-----|------|----------|-------------------------------|----------|
| 7:0 | W | GP2B_A0L | A0L bit 7:0 of A0 coefficient | 00000000 |

Table 93: GP2B_A0H 0x34

| Bit | Mode | Symbol | Description | Reset |
|-----|------|----------|--------------------------------|----------|
| 7:0 | W | GP2B_A0H | A0H bit 15:8 of A0 coefficient | 01000000 |

Table 94: GP1C_A0L 0x35

| Bit | Mode | Symbol | Description | Reset |
|-----|------|----------|-------------------------------|----------|
| 7:0 | W | GP1C_A0L | A0L bit 7:0 of A0 coefficient | 00000000 |

Table 95: GP1C_A0H 0x36

| Bit | Mode | Symbol | Description | Reset |
|-----|------|----------|--------------------------------|----------|
| 7:0 | W | GP1C_A0H | A0H bit 15:8 of A0 coefficient | 01000000 |

Table 96: GP1D_A0L 0x37

| Bit | Mode | Symbol | Description | Reset |
|-----|------|----------|-------------------------------|----------|
| 7:0 | W | GP1D_A0L | A0L bit 7:0 of A0 coefficient | 00000000 |

Table 97: GP1D_A0H 0x38

| Bit | Mode | Symbol | Description | Reset |
|-----|------|----------|--------------------------------|----------|
| 7:0 | W | GP1D_A0H | A0H bit 15:8 of A0 coefficient | 01000000 |

Table 98: GP2C_A0L 0x39

| Bit | Mode | Symbol | Description | Reset |
|-----|------|----------|-------------------------------|----------|
| 7:0 | W | GP2C_A0L | A0L bit 7:0 of A0 coefficient | 00000000 |

Table 99: GP2C_A0H 0x3A

| Bit | Mode | Symbol | Description | Reset |
|-----|------|----------|--------------------------------|----------|
| 7:0 | W | GP2C_A0H | A0H bit 15:8 of A0 coefficient | 01000000 |

Table 100: GP2D_A0L 0x3B

| Bit | Mode | Symbol | Description | Reset |
|-----|------|----------|-------------------------------|----------|
| 7:0 | W | GP2D_A0L | A0L bit 7:0 of A0 coefficient | 00000000 |

Table 101: GP2D_A0H 0x3C

| Bit | Mode | Symbol | Description | Reset |
|-----|------|----------|--------------------------------|----------|
| 7:0 | W | GP2D_A0H | A0H bit 15:8 of A0 coefficient | 01000000 |

Table 102: GP1A_A1L 0x3D

| Bit | Mode | Symbol | Description | Reset |
|-----|------|----------|-------------------------------|----------|
| 7:0 | W | GP1A_A1L | A1L bit 7:0 of A1 coefficient | 00000000 |

Table 103: GP1A_A1H 0x3E

| Bit | Mode | Symbol | Description | Reset |
|-----|------|----------|--------------------------------|----------|
| 7:0 | W | GP1A_A1H | A1H bit 15:8 of A1 coefficient | 00000000 |

Table 104: GP1B_A1L 0x3F

| Bit | Mode | Symbol | Description | Reset |
|-----|------|----------|-------------------------------|----------|
| 7:0 | W | GP1B_A1L | A1L bit 7:0 of A1 coefficient | 00000000 |

Table 105: GP1B_A1H 0x40

| Bit | Mode | Symbol | Description | Reset |
|-----|------|----------|--------------------------------|----------|
| 7:0 | W | GP1B_A1H | A1H bit 15:8 of A1 coefficient | 00000000 |

Table 106: GP2A_A1L 0x41

| Bit | Mode | Symbol | Description | Reset |
|-----|------|----------|-------------------------------|----------|
| 7:0 | W | GP2A_A1L | A1L bit 7:0 of A1 coefficient | 00000000 |

Table 107: GP2A_A1H 0x42

| Bit | Mode | Symbol | Description | Reset |
|-----|------|----------|--------------------------------|----------|
| 7:0 | W | GP2A_A1H | A1H bit 15:8 of A1 coefficient | 00000000 |

Table 108: GP2B_A1L 0x43

| Bit | Mode | Symbol | Description | Reset |
|-----|------|----------|-------------------------------|----------|
| 7:0 | W | GP2B_A1L | A1L bit 7:0 of A1 coefficient | 00000000 |

Table 109: GP2B_A1H 0x44

| Bit | Mode | Symbol | Description | Reset |
|-----|------|----------|--------------------------------|----------|
| 7:0 | W | GP2B_A1H | A1H bit 15:8 of A1 coefficient | 00000000 |

Table 110: GP1C_A1L 0x45

| Bit | Mode | Symbol | Description | Reset |
|-----|------|----------|-------------------------------|----------|
| 7:0 | W | GP1C_A1L | A1L bit 7:0 of A1 coefficient | 00000000 |

Table 111: GP1C_A1H 0x46

| Bit | Mode | Symbol | Description | Reset |
|-----|------|----------|--------------------------------|----------|
| 7:0 | W | GP1C_A1H | A1H bit 15:8 of A1 coefficient | 00000000 |

Table 112: GP1D_A1L 0x47

| Bit | Mode | Symbol | Description | Reset |
|-----|------|----------|-------------------------------|----------|
| 7:0 | W | GP1D_A1L | A1L bit 7:0 of A1 coefficient | 00000000 |

Table 113: GP1D_A1H 0x48

| Bit | Mode | Symbol | Description | Reset |
|-----|------|----------|--------------------------------|----------|
| 7:0 | W | GP1D_A1H | A1H bit 15:8 of A1 coefficient | 00000000 |

Table 114: GP2C_A1L 0x49

| Bit | Mode | Symbol | Description | Reset |
|-----|------|----------|-------------------------------|----------|
| 7:0 | W | GP2C_A1L | A1L bit 7:0 of A1 coefficient | 00000000 |

Table 115: GP2C_A1H 0x4A

| Bit | Mode | Symbol | Description | Reset |
|-----|------|----------|--------------------------------|----------|
| 7:0 | W | GP2C_A1H | A1H bit 15:8 of A1 coefficient | 00000000 |

Table 116: GP2D_A1L 0x4B

| Bit | Mode | Symbol | Description | Reset |
|-----|------|----------|-------------------------------|----------|
| 7:0 | W | GP2D_A1L | A1L bit 7:0 of A1 coefficient | 00000000 |

Table 117: GP2D_A1H 0x4C

| Bit | Mode | Symbol | Description | Reset |
|-----|------|----------|--------------------------------|----------|
| 7:0 | W | GP2D_A1H | A1H bit 15:8 of A1 coefficient | 00000000 |

Table 118: GP1A_A2L 0x4D

| Bit | Mode | Symbol | Description | Reset |
|-----|------|----------|-------------------------------|----------|
| 7:0 | W | GP1A_A2L | A2L bit 7:0 of A2 coefficient | 00000000 |

Table 119: GP1A_A2H 0x4E

| Bit | Mode | Symbol | Description | Reset |
|-----|------|----------|--------------------------------|----------|
| 7:0 | W | GP1A_A2H | A2H bit 15:8 of A2 coefficient | 00000000 |

Table 120: GP1B_A2L 0x4F

| Bit | Mode | Symbol | Description | Reset |
|-----|------|----------|-------------------------------|----------|
| 7:0 | W | GP1B_A2L | A2L bit 7:0 of A2 coefficient | 00000000 |

Table 121: GP1B_A2H 0x50

| Bit | Mode | Symbol | Description | Reset |
|-----|------|----------|--------------------------------|----------|
| 7:0 | W | GP1B_A2H | A2H bit 15:8 of A2 coefficient | 00000000 |

Table 122: GP2A_A2L 0x51

| Bit | Mode | Symbol | Description | Reset |
|-----|------|----------|-------------------------------|----------|
| 7:0 | W | GP2A_A2L | A2L bit 7:0 of A2 coefficient | 00000000 |

Table 123: GP2A_A2H 0x52

| Bit | Mode | Symbol | Description | Reset |
|-----|------|----------|--------------------------------|----------|
| 7:0 | W | GP2A_A2H | A2H bit 15:8 of A2 coefficient | 00000000 |

Table 124: GP2B_A2L 0x53

| Bit | Mode | Symbol | Description | Reset |
|-----|------|----------|-------------------------------|----------|
| 7:0 | W | GP2B_A2L | A2L bit 7:0 of A2 coefficient | 00000000 |

Table 125: GP2B_A2H 0x54

| Bit | Mode | Symbol | Description | Reset |
|-----|------|----------|--------------------------------|----------|
| 7:0 | W | GP2B_A2H | A2H bit 15:8 of A2 coefficient | 00000000 |

Table 126: GP1C_A2L 0x55

| Bit | Mode | Symbol | Description | Reset |
|-----|------|----------|-------------------------------|----------|
| 7:0 | W | GP1C_A2L | A2L bit 7:0 of A2 coefficient | 00000000 |

Table 127: GP1C_A2H 0x56

| Bit | Mode | Symbol | Description | Reset |
|-----|------|----------|--------------------------------|----------|
| 7:0 | W | GP1C_A2H | A2H bit 15:8 of A2 coefficient | 00000000 |

Table 128: GP1D_A2L 0x57

| Bit | Mode | Symbol | Description | Reset |
|-----|------|----------|-------------------------------|----------|
| 7:0 | W | GP1D_A2L | A2L bit 7:0 of A2 coefficient | 00000000 |

Table 129: GP1D_A2H 0x58

| Bit | Mode | Symbol | Description | Reset |
|-----|------|----------|--------------------------------|----------|
| 7:0 | W | GP1D_A2H | A2H bit 15:8 of A2 coefficient | 00000000 |

Table 130: GP2C_A2L 0x59

| Bit | Mode | Symbol | Description | Reset |
|-----|------|----------|-------------------------------|----------|
| 7:0 | W | GP2C_A2L | A2L bit 7:0 of A2 coefficient | 00000000 |

Table 131: GP2C_A2H 0x5A

| Bit | Mode | Symbol | Description | Reset |
|-----|------|----------|--------------------------------|----------|
| 7:0 | W | GP2C_A2H | A2H bit 15:8 of A2 coefficient | 00000000 |

Table 132: GP2D_A2L 0x5B

| Bit | Mode | Symbol | Description | Reset |
|-----|------|----------|-------------------------------|----------|
| 7:0 | W | GP2D_A2L | A2L bit 7:0 of A2 coefficient | 00000000 |

Table 133: GP2D_A2H 0x5C

| Bit | Mode | Symbol | Description | Reset |
|-----|------|----------|--------------------------------|----------|
| 7:0 | W | GP2D_A2H | A2H bit 15:8 of A2 coefficient | 00000000 |

Table 134: GP1A_B1L 0x5D

| Bit | Mode | Symbol | Description | Reset |
|-----|------|----------|-------------------------------|----------|
| 7:0 | W | GP1A_B1L | B1L bit 7:0 of B1 coefficient | 00000000 |

Table 135: GP1A_B1H 0x5E

| Bit | Mode | Symbol | Description | Reset |
|-----|------|----------|--------------------------------|----------|
| 7:0 | W | GP1A_B1H | B1H bit 15:8 of B1 coefficient | 00000000 |

Table 136: GP1B_B1L 0x5F

| Bit | Mode | Symbol | Description | Reset |
|-----|------|----------|-------------------------------|----------|
| 7:0 | W | GP1B_B1L | B1L bit 7:0 of B1 coefficient | 00000000 |

Table 137: GP1B_B1H 0x60

| Bit | Mode | Symbol | Description | Reset |
|-----|------|----------|--------------------------------|----------|
| 7:0 | W | GP1B_B1H | B1H bit 15:8 of B1 coefficient | 00000000 |

Table 138: GP2A_B1L 0x61

| Bit | Mode | Symbol | Description | Reset |
|-----|------|----------|-------------------------------|----------|
| 7:0 | W | GP2A_B1L | B1L bit 7:0 of B1 coefficient | 00000000 |

Table 139: GP2A_B1H 0x62

| Bit | Mode | Symbol | Description | Reset |
|-----|------|----------|--------------------------------|----------|
| 7:0 | W | GP2A_B1H | B1H bit 15:8 of B1 coefficient | 00000000 |

Table 140: GP2B_B1L 0x63

| Bit | Mode | Symbol | Description | Reset |
|-----|------|----------|-------------------------------|----------|
| 7:0 | W | GP2B_B1L | B1L bit 7:0 of B1 coefficient | 00000000 |

Table 141: GP2B_B1H 0x64

| Bit | Mode | Symbol | Description | Reset |
|-----|------|----------|--------------------------------|----------|
| 7:0 | W | GP2B_B1H | B1H bit 15:8 of B1 coefficient | 00000000 |

Table 142: GP1C_B1L 0x65

| Bit | Mode | Symbol | Description | Reset |
|-----|------|----------|-------------------------------|----------|
| 7:0 | W | GP1C_B1L | B1L bit 7:0 of B1 coefficient | 00000000 |

Table 143: GP1C_B1H 0x66

| Bit | Mode | Symbol | Description | Reset |
|-----|------|----------|--------------------------------|----------|
| 7:0 | W | GP1C_B1H | B1H bit 15:8 of B1 coefficient | 00000000 |

Table 144: GP1D_B1L 0x67

| Bit | Mode | Symbol | Description | Reset |
|-----|------|----------|-------------------------------|----------|
| 7:0 | W | GP1D_B1L | B1L bit 7:0 of B1 coefficient | 00000000 |

Table 145: GP1D_B1H 0x68

| Bit | Mode | Symbol | Description | Reset |
|-----|------|----------|--------------------------------|----------|
| 7:0 | W | GP1D_B1H | B1H bit 15:8 of B1 coefficient | 00000000 |

Table 146: GP2C_B1L 0x69

| Bit | Mode | Symbol | Description | Reset |
|-----|------|----------|-------------------------------|----------|
| 7:0 | W | GP2C_B1L | B1L bit 7:0 of B1 coefficient | 00000000 |

Table 147: GP2C_B1H 0x6A

| Bit | Mode | Symbol | Description | Reset |
|-----|------|----------|--------------------------------|----------|
| 7:0 | W | GP2C_B1H | B1H bit 15:8 of B1 coefficient | 00000000 |

Table 148: GP2D_B1L 0x6B

| Bit | Mode | Symbol | Description | Reset |
|-----|------|----------|-------------------------------|----------|
| 7:0 | W | GP2D_B1L | B1L bit 7:0 of B1 coefficient | 00000000 |

Table 149: GP2D_B1H 0x6C

| Bit | Mode | Symbol | Description | Reset |
|-----|------|----------|--------------------------------|----------|
| 7:0 | W | GP2D_B1H | B1H bit 15:8 of B1 coefficient | 00000000 |

Table 150: GP1A_B2L 0x6D

| Bit | Mode | Symbol | Description | Reset |
|-----|------|----------|-------------------------------|----------|
| 7:0 | W | GP1A_B2L | B2L bit 7:0 of B2 coefficient | 00000000 |

Table 151: GP1A_B2H 0x6E

| Bit | Mode | Symbol | Description | Reset |
|-----|------|----------|--------------------------------|----------|
| 7:0 | W | GP1A_B2H | B2H bit 15:8 of B2 coefficient | 00000000 |

Table 152: GP1B_B2L 0x6F

| Bit | Mode | Symbol | Description | Reset |
|-----|------|----------|-------------------------------|----------|
| 7:0 | W | GP1B_B2L | B2L bit 7:0 of B2 coefficient | 00000000 |

Table 153: GP1B_B2H 0x70

| Bit | Mode | Symbol | Description | Reset |
|-----|------|----------|--------------------------------|----------|
| 7:0 | W | GP1B_B2H | B2H bit 15:8 of B2 coefficient | 00000000 |

Table 154: GP2A_B2L 0x71

| Bit | Mode | Symbol | Description | Reset |
|-----|------|----------|-------------------------------|----------|
| 7:0 | W | GP2A_B2L | B2L bit 7:0 of B2 coefficient | 00000000 |

Table 155: GP2A_B2H 0x72

| Bit | Mode | Symbol | Description | Reset |
|-----|------|----------|--------------------------------|----------|
| 7:0 | W | GP2A_B2H | B2H bit 15:8 of B2 coefficient | 00000000 |

Table 156: GP2B_B2L 0x73

| Bit | Mode | Symbol | Description | Reset |
|-----|------|----------|-------------------------------|----------|
| 7:0 | W | GP2B_B2L | B2L bit 7:0 of B2 coefficient | 00000000 |

Table 157: GP2B_B2H 0x74

| Bit | Mode | Symbol | Description | Reset |
|-----|------|----------|--------------------------------|----------|
| 7:0 | W | GP2B_B2H | B2H bit 15:8 of B2 coefficient | 00000000 |

Table 158: GP1C_B2L 0x75

| Bit | Mode | Symbol | Description | Reset |
|-----|------|----------|-------------------------------|----------|
| 7:0 | W | GP1C_B2L | B2L bit 7:0 of B2 coefficient | 00000000 |

Table 159: GP1C_B2H 0x76

| Bit | Mode | Symbol | Description | Reset |
|-----|------|----------|--------------------------------|----------|
| 7:0 | W | GP1C_B2H | B2H bit 15:8 of B2 coefficient | 00000000 |

Table 160: GP1D_B2L 0x77

| Bit | Mode | Symbol | Description | Reset |
|-----|------|----------|-------------------------------|----------|
| 7:0 | W | GP1D_B2L | B2L bit 7:0 of B2 coefficient | 00000000 |

Table 161: GP1D_B2H 0x78

| Bit | Mode | Symbol | Description | Reset |
|-----|------|----------|--------------------------------|----------|
| 7:0 | W | GP1D_B2H | B2H bit 15:8 of B2 coefficient | 00000000 |

Table 162: GP2C_B2L 0x79

| Bit | Mode | Symbol | Description | Reset |
|-----|------|----------|-------------------------------|----------|
| 7:0 | W | GP2C_B2L | B2L bit 7:0 of B2 coefficient | 00000000 |

Table 163: GP2C_B2H 0x7A

| Bit | Mode | Symbol | Description | Reset |
|-----|------|----------|--------------------------------|----------|
| 7:0 | W | GP2C_B2H | B2H bit 15:8 of B2 coefficient | 00000000 |

Table 164: GP2D_B2L 0x7B

| Bit | Mode | Symbol | Description | Reset |
|-----|------|----------|-------------------------------|----------|
| 7:0 | W | GP2D_B2L | B2L bit 7:0 of B2 coefficient | 00000000 |

Table 165: GP2D_B2H 0x7C

| Bit | Mode | Symbol | Description | Reset |
|-----|------|----------|--------------------------------|----------|
| 7:0 | W | GP2D_B2H | B2H bit 15:8 of B2 coefficient | 00000000 |

Table 166: GPF_SRC1 0x7D

| Bit | Mode | Symbol | Description | Reset |
|-----|------|----------|-------------|-------|
| 7 | R | Reserved | Reserved | 0 |

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| Bit | Mode | Symbol | Description | Reset |
|-----|------|------------|---|-------|
| 6:4 | R/W | GP_2AB_SRC | GP Filter 2AB source selection: 000 = 1AB 001 = reserved 010 = 1CD 011 = reserved 100 = DAI_L 101 = DAI_R 110 = ADC_L 111 = ADC_R | 110 |
| 3 | R | Reserved | Reserved | 0 |
| 2:0 | R/W | GP_1AB_SRC | GP Filter 1AB source selection: 000 = reserved 001 = reserved 010 = reserved 011 = reserved 100 = DAI_L 101 = DAI_R 110 = ADC_L 111 = ADC_R | 100 |

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Table 167: GPF_SRC2 0x7E

| Bit | Mode | Symbol | Description | Reset |
|-----|------|------------|--|-------|
| 7 | R | Reserved | Reserved | 0 |
| 6:4 | R/W | GP_2CD_SRC | GP Filter 2CD source selection: 000 = 1AB 001 = 2AB 010 = 1CD 011 = reserved 100 = DAI_L 101 = DAI_R 110 = ADC_L 111 = ADC_R | 111 |
| 3 | R | Reserved | Reserved | 0 |
| 2:0 | R/W | GP_1CD_SRC | GP Filter 1CD source selection: 000 = 1AB 001 = reserved 010 = reserved 011 = reserved 100 = DAI_L 101 = DAI_R 110 = ADC_L 111 = ADC_R | 101 |

Table 168: DSP_CFG 0x7F

| Bit | Mode | Symbol | Description | Reset |
|-----|------|-----------|--|-------|
| 7 | R | Reserved | Reserved | 0 |
| 6 | R/W | DSP_MIX_3 | 1 = Output of section 2AB is mixed with 2CD | 0 |
| 5 | R/W | DSP_MIX_2 | 1 = Output of section 1CD is mixed with 2AB | 0 |
| 4 | R/W | DSP_MIX_1 | 1 = Output of section 1AB is mixed with 1CD | 0 |
| 3 | R/W | GP2CD_EN | Enable GP section 2CD 0 = disable 1 = enable | 0 |
| 2 | R/W | GP1CD_EN | Enable GP section 1CD 0 = disable 1 = enable | 0 |
| 1 | R/W | GP2AB_EN | Enable GP section 2AB 0 = disable 1 = enable | 0 |
| 0 | R/W | GP1AB_EN | Enable GP section 1AB 0 = disable 1 = enable | 0 |

Table 169: PAGE1 0x80

| Bit | Mode | Symbol | Description | Reset |
|-----|------|-----------|---|---------|
| 7 | RW | REG_PAGE1 | 4-wire mode register page selection 0: Selects Register R1 to R127 1: Selects Register R129 to R255 | 0 |
| 6:0 | R | Reserved | Reserved | 0000000 |

Table 170: CHIP_ID 0x81

| Bit | Mode | Symbol | Description | Reset |
|-----|------|--------|---|-------|
| 7:4 | R | MRC | Read back of mask revision code (MRC) – code 0 for AA release | 0001 |
| 3:0 | R | MMRC | Read back of metal mask release code (MMRC) – starts with a code 0 | 0001 |

Table 171: INTERFACE 0x82

| Bit | Mode | Symbol | Description | Reset |
|-----|------|--------------|---|-------|
| 7:5 | R | IF_BASE_ADDR | 3 MSB of 2-wire control interface base address XXX1010 + R/W 00110100 = 0x34 (write address) 00110101 = 0x35 (read address) | 001 |
| 4 | R | nCS_POL | 4-wire chip select polarity 0: nCS is low active 1: nCS is high active | 0 |
| 3 | R | RW_POL | 4-wire: Read/Write bit polarity 0: Host indicates reading access via R/W bit = '0' 1: Host indicates reading access via R/W bit = '1' | 1 |
| 2 | R | CPHA | 4-wire IF data is latched at 0: Rising edge of SK 1: Falling edge of SK | 1 |
| 1 | R | CPOL | 4-wire IF clock polarity 0: SK is low during idle 1: SK is high during idle | 0 |
| 0 | R | Reserved | Reserved | 0 |

10.5 ALC level controls
Table 172: ALC_MAX 0x83

| Bit | Mode | Symbol | Description | Reset |
|-----|------|-----------|--|--------|
| 7 | R | Reserved | Reserved | 0 |
| 6 | R/W | ALC_MERGE | ALC joined stereo mode 0 = disabled (channels updates independently) 1 = enabled (channels update synchronously) | 1 |
| 5:0 | R/W | ALC_MAX | ALC max control level (refer to Table 21) maximum value of ALC_MAX = 0x3C = -0.5 dB | 000000 |

Table 173: ALC_MIN 0x84

| Bit | Mode | Symbol | Description | Reset |
|-----|------|----------|--|--------|
| 7:6 | R | Reserved | Reserved | 00 |
| 5:0 | R/W | ALC_MIN | ALC min control level: (refer to Table 21) maximum value of ALC_MIN = 0x3B = -2 dB | 000000 |

Table 174: ALC_NOIS 0x85

| Bit | Mode | Symbol | Description | Reset |
|-----|------|----------|--|--------|
| 7:6 | R | Reserved | Reserved | 00 |
| 5:0 | R/W | ALC_NOIS | ALC noise gate level: (refer to Table 21) Note that the minimum value of ALC_NOIS is 86 dB | 000000 |

Table 175: ALC_ATT 0x86

| Bit | Mode | Symbol | Description | Reset |
|-----|------|---------|--|----------|
| 7:0 | R/W | ALC_ATT | ALC attack rate: Number of sample periods between two gain steps of 0.25 dB 00000000 = 0.25 dB/sample period | 00000000 |

Table 176: ALC_REL 0x87

| Bit | Mode | Symbol | Description | Reset |
|-----|------|---------|--|----------|
| 7:0 | R/W | ALC_REL | ALC release rate: Number of periods between two gain steps of 0.25 dB in increments of 4 sample periods 00000000 = 0.0625 dB/sample period | 00000000 |

Table 177: ALC_DEL 0x88

| Bit | Mode | Symbol | Description | Reset |
|-----|------|---------|---|----------|
| 7:0 | R/W | ALC_DEL | ALC release delay: Time delay before ALC release starts in increments of ALC_REL periods | 00000000 |

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Table 178: A_HID_UNLOCK 0x8A

| Bit | Mode | Symbol | Description | Reset |
|-----|------|--------------|---|----------|
| 7:0 | W | A_HID_UNLOCK | Register unlock: Set to 0x8B (10001011) to use the registers below | 00000000 |

Table 179: A_TST_UNLOCK 0x8B

| Bit | Mode | Symbol | Description | Reset |
|-----|------|--------------|---|----------|
| 7:0 | W | A_TST_UNLOCK | Register unlock: Set to 0xB4 (10110100) to use the registers below | 00000000 |

Table 180: A_PLL0 0x8F

Unlocking registers 0x8A and 0x8B is required to access this register

| Bit | Mode | Symbol | Description | Reset |
|-----|------|----------------|--|----------|
| 7:1 | W | Reserved | Reserved | 00000000 |
| 0 | W | SIGDEL_DISABLE | Disable sigma delta modulator in the analogue PLL. If = 1, reduces current when using internal oscillator. Must be enabled when using PLL | 0 |

Table 181: A_PLL1 0x90

Unlocking registers 0x8A and 0x8B is required to access this register

| Bit | Mode | Symbol | Description | Reset |
|-----|------|-----------|---|----------|
| 7:1 | W | Reserved | Reserved | 00000000 |
| 0 | W | VCORST_EN | Separate power-down signal for the VCO reset controller 0 = disabled 1 = enabled for all PLL operations | 1 |

Table 182: A_ADC0 0x95

Unlocking registers 0x8A and 0x8B is required to access this register

| Bit | Mode | Symbol | Description | Reset |
|-----|------|----------|--|-------|
| 7:4 | W | Reserved | Reserved | 0000 |
| 3 | W | ADC_T2 | ADC bias current increase: 0 = default current 1 = increased current; improved THD performance | 0 |
| 2:0 | W | Reserved | Reserved | 000 |

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Table 183: A_DAC0 0x96

Unlocking registers 0x8A and 0x8B is required to access this register

| Bit | Mode | Symbol | Description | Reset |
|-----|------|--------------|---|-------|
| 7:3 | W | Reserved | Reserved | 00000 |
| 2:0 | W | VMID_BUFF_EN | VMID buffer disable during ADC and analogue only modes to save power 000 = VMID buffer disabled 111 = VMID buffer enabled | 111 |

Table 184: A_CPHP6 0xA2

Unlocking registers 0x8A and 0x8B is required to access this register

| Bit | Mode | Symbol | Description | Reset |
|-----|------|--------------|---|----------|
| 7:0 | W | CP_RISE_TIME | Set 0x80 (10000000) for maximum output power. Set 0x84 (10000100) for reduced inrush current | 10000000 |

Table 185: A_CP_MODE 0xA7

Unlocking registers 0x8A and 0x8B is required to access this register

| Bit | Mode | Symbol | Description | Reset |
|-----|------|-----------|--|----------|
| 7:0 | W | A_CP_MODE | Headphone charge pump enable: Set 0x7C (01111110) | 01111110 |

11 Package information

11.1 Package outlines

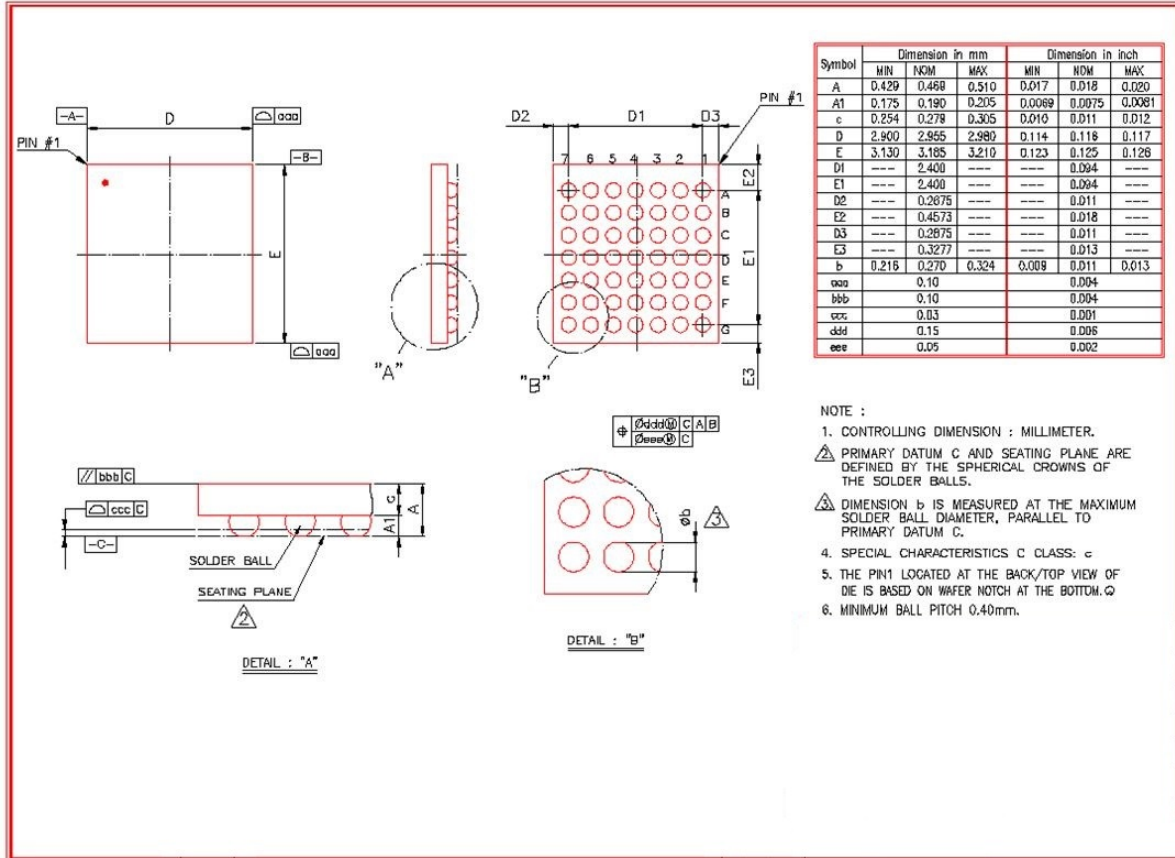


Figure 51: 49 bump WL-CSP 0.4mm pitch package outline drawing

11.2 Soldering information

Refer to the JEDEC standard J-STD-020 for relevant soldering information. This document can be downloaded from <http://www.jedec.org>.

12 Ordering information

The ordering number consists of the part number followed by a suffix indicating the packing method. For details and availability, please contact Dialog Semiconductor's local sales representative.

Table 186: Ordering information

| Part number | Package | Size (mm) | Shipment form | Pack quantity |
|--------------|------------------------------|-----------|--|---------------|
| DA7210-00UC2 | 49-bump CSP Pb-free/green | | Tape and Reel | 2,000 pcs. |
| DA7210-00UC6 | 49-bump CSP Pb-free/green | | Waffle Pack (engineering samples only - not for mass production) | 900 pcs. |

13 Applications information

13.1 Supporting information

The bass response of the analogue inputs and outputs is determined by the output coupling capacitor and associated resistive load. If smaller footprint, low value capacitors are preferred, then the low frequency cut-off will be increased.

To maintain maximum audio bandwidth, larger capacitors are recommended, taking into account the relationship

$$\text{Low frequency cut-off} = \frac{1}{2\pi RC}$$

The analogue outputs can support between 32 Ω (16 Ω for headphone outputs) and line level loads (e.g. >=10 kΩ), so the range of capacitor values is wider, and care is required when making the selection.

13.2 Minimum component recommendations

To ensure datasheet performance is maintained it is recommended that the following minimum component criteria are met. Figure 49 shows recommended components and input/output configurations.

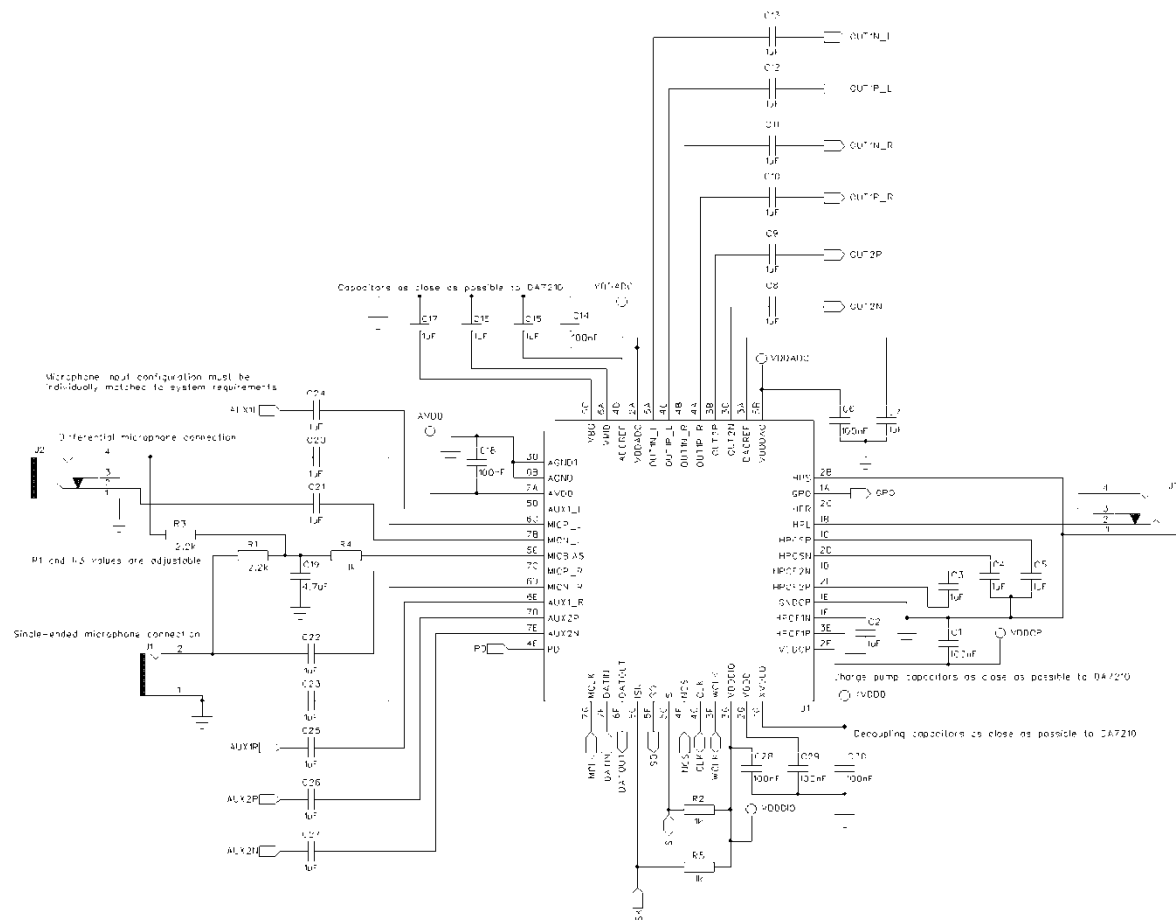


Figure 49: DA7210 49-pin CSP component recommendations

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- It is recommended that ceramic capacitors are used where possible for low ESR.
- It is recommended that C0G or X7R dielectric is used where possible to minimise distortion.
- The voltage rating of any capacitor used should be much greater than the maximum peak signal amplitude expected. It has been shown that capacitors with a large voltage rating introduce less distortion into the signal paths.
- For example the voltage rating of the 1 μF capacitors in the output paths should be chosen as 16 V.
- All capacitors $\geq 10 \mu\text{F}$ should use minimum dielectric specification X5R where possible.
- All 100 nF power supply decoupling capacitors should be placed as close as possible to associated pins. Reference: C1, C6, C14, C18, C28-30.
- All 1 μF voltage reference capacitors should be placed as close as possible to associated pins. Reference: C7, C15-17.
- The headphone output amplifier is driven by a PWM based charge pump. To maintain efficiency the 1 μF charge pump capacitors should be placed as close as possible to associated pins. Reference: C2-C5.
- The control interface data I/O pin, SI, is open drain and therefore requires an external pull-up. If the control interface data output of the system processor does not support an internal pull-up, then an external resistor R2 is required.

13.3 General component suggestions

The following components and input/output configurations are suggested below.

- Headphone output and microphone input connectors shown in Figure 49 are of the 3.5 mm RCA/phono type, but any other suitable connector is acceptable.
- J1 is configured as a mono microphone input. The ground reference connection MICN_R, pin 6D, is internally referenced to a voltage $0.45 \cdot \text{AVDD}$ and therefore must be connected to AGND (or ground plane if connected to AGND) through C23. Similarly MICP_R, pin 7C, should be connected to the signal input via C22.
- MICBIAS, pin 5E, can supply up to 2 mA of current for biasing electret microphones. The MICBIAS pin must be separated from the mic input by $\approx 200 \Omega$ resistor.
- A capacitive load of 100 nF is also required for output stability and doubles as a decoupling capacitor.
- If two microphones are supplied by this pin, then separate RC circuits are implemented for each microphone to provide isolation between inputs, as shown in Figure 49.
- J2 is configured as a differential microphone input. The positive signal input is connected to MICP_L, pin 6C, the inputs pins are internally referenced to voltage $0.45 \cdot \text{AVDD}$ and therefore must be connected through C20. Similarly, the negative signal input is connected to MICN_L, pin 7B, through C21. To maintain balance the value of R4 should match that of R3.
- When the line outputs are used to drive a differential load of 32Ω , coupling caps are not required
- If the analogue outputs, excluding the headphone outputs, are used with line level loads (e.g. $\approx 10 \text{ k}\Omega$) and minimum bass response of the outputs is not deemed important, it could be acceptable to reduce the coupling capacitors for OUT1L/R analogue output pins to less than 1 μF . An absolute minimum value of 100 nF is recommended. Reference: C8-13.
- It is unlikely that the bass response of the microphone used will be much lower than 100 Hz. The microphone inputs have an impedance $\approx 15 \text{ k}\Omega$, it could therefore be acceptable to use coupling capacitors less than 1 μF without significantly affecting the input signal bandwidth. An absolute minimum value of 100 nF is recommended.
- The input impedance of the analogue inputs is $\approx 30 \text{ k}\Omega$. If minimum bass response of the analogue inputs is not deemed important, the input coupling capacitors for MICL/R and AUX1L/R can be reduced to less than 1 μF . An absolute minimum value of 100 nF is recommended. Reference: C21-27.

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Revision history

| Revision | Date | Description |
|----------------------------|----------------|--|
| DA7210x-1DS01-080902 | September 2008 | Initial release |
| DA7210x-1DS02-080905 | September 2008 | Minor edits to parametrics |
| DA7210-IDS03-081126 | November 2008 | Based on Target spec of DS13 |
| DA7210-IDS03_1-081126 | November 2008 | Removed draft water mark |
| DA7210-IDS03_2-081127 | November 2008 | Pg 80 Updated package outline diagram |
| DA7210-IDS03_3-081203 | December 2008 | Updated Sales part number Added draft watermark |
| DA7210-IDS03_4-090105 | January 2009 | Updated the Sales part number to DA7210 Updated Figure 43 |
| DA7210-IDS03_5-090311 | March 2009 | Updated the pin out for OUT2P & OUT2N, pg5,6 Updated the recommended external components, pg 81 |
| DA7210-IDS03_6-090311 | March 2009 | Updated the PLL look up table pg 44 |
| DA7210-IDS-Rev1_4_6-090622 | April 2009 | Update OUT2 pad numbers Extend gain range of AUX_1 amplifier to -48 – 21dB Update several digital filter response figures Replace SC_CONT against 3 START_UP control registers (controls to be defined), add two DAC digital gain control registers, add control for 605HALC_MERGE mode, add control 606HRAMP_EN and move register SOFTMUTE, move ALC controls in to page 1 and main CONTROL register Update analogue routing for output mixers, headphones amplifiers and feedback loop Add noise suppression mode with control 607HNOISE_SUP for headphones volume control Change 4-wire mode detection from 1st to 3rd passive to active transition on nCS Add GP_SRC1/2 registers and update block diagram and routing figures for GP-filter engine Add electrical parameters for digital audio interface Add 32kHz MCLK mode Update register overview Updated SNR figures and add output noise figures to HP, OUT1/2 amplifiers Update ALC description Update errata for BA Remove mute control from AUX1 amplifier Change DAI_TDM_CHAN into DAI_TDM_MONO control Added package and pin info for CSP variant Removed HP invert functionality Removed OTP functionality in register 83 so it has only fixed values |
| DA7210-IDS-Rev1_5-090722 | July 2009 | Changes to based on DS Rev 1.5 Updated register map |

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| Revision | Date | Description |
|---------------------------|----------------|--|
| DA7210-IDS-Rev1_51-090817 | August 2009 | Changes to PLL range in register 0x2B Pg 8 PD descriptions Updated ordering information |
| DA7210-IDS-Rev1_52-090820 | August 2009 | Updated PLL block diagram Updated PLL-DIV look up table settings Removed DAC EQ |
| DA7210-IDS-Rev1_53-090828 | August 2009 | Pg 1,10,19 Updated power number to 2.5 mW Pg 5,7 updated QFN/CSP packaing drawing Pg 2 updated block diagram Pg 6,7 updated pin descriptions Pg 13 updated THD+N for OUT2 Pg 14 updated THD+N for HP Pg 26 updated Figure 11 Pg 35 updated para 1 Pg 52 updated register map and descriptions from GPO |
| DA7210-IDS-Rev1_54-090828 | August 2009 | Pg 9 Updated power dissipation number Updated descriptions from GPO and HPS Figure 11 updated P54 updated label and pin descriptions P 8 Updated ATB1_HPS for HPS and updated pin description |
| DA7210-IDS-Rev1_55-090828 | August 2009 | P 79 Changes made to 0x7D GPF_SRC1 description P 79 Changes made to 0x7E GPF_SRC2 |
| DA7210-IDS2a-090914 | September 2009 | Data Sheet Status Definition added P89 Draft Watermark removed |
| DA7210-IDS2b-221009 | October 2009 | Pg 1, 83, 85 remove references to QFN version, updated Ext Cpmt diagram Pg 43 rewrote clocking scheme sections, added 32Khz description Page 67 ; "WORD" length. (by the way, 10; 24bits Pg 46 updated figure 36 Pg 7 changed VDDD min to 1.2V Pg 8,9 updated ADC power and SNR/THD |
| DA7210-IDS2b-221009 | October 2009 | Pg 43 updated footnotes Pg 53-83 updated register descriptions |
| DA7210-IDS2c-181209 | December 2009 | Pg 20 Updated ALC gain step size Pg 61-83 Updated/reformatted register descriptions Pg 22 Add Softmute section Pg 55 Updated 2-wire Communication section Pg 41-53 Added programming sections for Slave and master modes Pg 93 added ALC registers Pg 83 Updated Applications information section |
| DA7210-IDS2d-240210 | February 2010 | pg 82 Updated the ordering code pg 9,10, 12 Absolute Gain Accuracy; Replace 0dBmo with 0dB pg 9,10 Removed the line "In band Spurious noise" in parametric tables Updated the STARTUP3 register |

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| Revision | Date | Description |
|-----------------------------|----------------|--|
| DA7210-IDS2e-100423 | April 2010 | <p>Updated the numbering for footnotes</p> <p>pg 84 Updated the ordering information</p> <p>pg 57 Updated the STARTUP3 register</p> <p>pg 79 Renamed register 0xA7 to A_CP_MODE</p> <p>pg 25 All of the headphone section was re-written especially noise suppression</p> <p>Pg 57: added note about reserved reg/bits</p> <p>Pg 58 added note to register 0x5</p> <p>Pg 65 0x1A : corrected to MSB first</p> <p>Pg 66 0x1D, updated the description for bit 4.</p> <p>Pg 68 0x24 : Updated label of bit 1:0 in reg AUX1ZX_R_EN</p> <p>Pg 75 Updated the external components diagram</p> <p>Pg 10-12: Updated the DAC/OUT1/2 THD+N to -90dB and added 32kHz mode</p> <p>Pg 55,56 Updated the Quick Register Reference Table</p> <p>Pg 18, 74 Added A_BGAP 0xB7 register and general description in general section.</p> <p>PG 7 Updated the Abs Maximum Ratings</p> <p>Pg 8-17 Replace N and u with n & μ</p> <p>Pg 17 Added Table for Added Start Timings</p> <p>Pg6 Renamed GPO to General Purpose Output</p> <p>Pg 6 renamed HPGND_SENSE to Headphone ground sense</p> <p>Pg6 deleted reference to PLL</p> <p>Pg9 Power Supply Rejection Ratio minimum rating updated</p> <p>Pg10 deleted In band spurious</p> <p>Pg11 Updated Power Supply Rejection Ratio minimum rating</p> <p>Pg11 Deleted Total Harmonic Distortion Plus Noise row</p> <p>Pg12 Deleted Total Harmonic Distortion Plus Noise row</p> <p>P12 Updated Quiescent current per channel Typ</p> <p>Pg44 Updated vco_rst to VCO_RST</p> <p>Pg44 Updated 0x8B = B to 0x8B =B4H</p> <p>DAC SNR numbers updated</p> |
| DA7210-IDS2f-100615-1.doc15 | June 2010 | Changed Input Frequency(Min) to 11.289 pg 13, Table Phase Lock Loop |
| DA7210-IDS3a-151015 | September 2015 | <p>Update to latest template</p> <p>Deleted 10 year guarantee note under 'Recommended operating conditions' table</p> <p>Update of block diagram to reference DA7202 device</p> <p>Formatting corrections</p> <p>Update to ordering information to include 'engineering samples only - not for mass production' for waffle pack option.</p> |
| 3.1 | 01-Feb-2019 | Removed security status |
| 3.2 | 23-Dec-2021 | Updated logo, disclaimer, copyright. |

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Status definitions

| Revision | Datasheet status | Product status | Definition |
|----------|------------------|----------------|---|
| 1.<n> | Target | Development | This datasheet contains the design specifications for product development. Specifications may be changed in any manner without notice. |
| 2.<n> | Preliminary | Qualification | This datasheet contains the specifications and preliminary characterisation data for products in pre-production. Specifications may be changed at any time without notice in order to improve the design. |
| 3.<n> | Final | Production | This datasheet contains the final specifications for products in volume production. The specifications may be changed at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via Customer Product Notifications. |
| 4.<n> | Obsolete | Archived | This datasheet contains the specifications for discontinued products. The information is provided for reference only. |

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