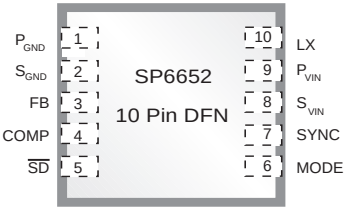
SP6652

1A, High Efficiency, Fixed 1.4 MHz Current Mode PWM Buck Regulator

FEATURES

- 1A Output Current
- 1.4MHz Constant Frequency Operation
- 97% Efficiency Possible
- 0.5µA (Max.) Shutdown Current
- Adjustable Output Voltage
- No External FETs or Schottky Diode Required
- Uses Small Value Inductors and Ceramic Output Capacitors
- Low Dropout Operation: 100% Duty Cycle
- Soft Start and Thermal Shutdown Protection
- Easy Frequency Synchonization
- Lead Free, RoHS Compliant package: I Small (3mm X 3mm) 10 Pin DFN or MSOP



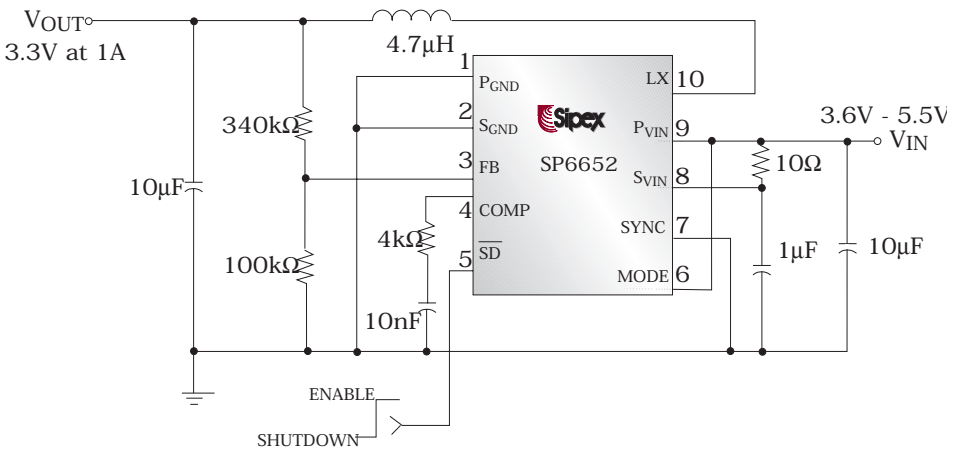
APPLICATIONS

- Mobile Phones
- PDAs
- DSCs
- MP3 Players
- USB Devices
- Point of Use Power

DESCRIPTION

The SP6652 is a high efficiency, synchronous buck regulator ideal for portable applications using one Li-Ion cell, with up to 1A of output current. The 1.4MHz switching frequency and PWM control loop are optimized for a small value inductor and ceramic output capacitor, for space constrained portable designs. In addition, the input voltage range of 2.7V to 5.5V; excellent transient response, output accuracy, and ability to transition into 100% duty cycle operation -- further extending useful battery life -- make the SP6652 a superior choice for a wide range of portable power applications. A logic level shutdown control, external clock synchronization, and forced-PWM or automatic control inputs are provided. Other features include soft-start, over current protection and 140ºC over-temperature shutdown.

TYPICAL APPLICATION CIRCUIT



ABSOLUTE MAXIMUM RATINGS

PV_{IN},S_{VIN} .....-0.3V to 6.0V
P_{GND} to S_{GND} .....-0.3V to 0.3V
LX to P_{GND} ..... - 0.3V to P_{VIN}+0.3V
Storage Temperature.....-65 °C to 150 °C
Operating Temperature..... -40°C to +85°C

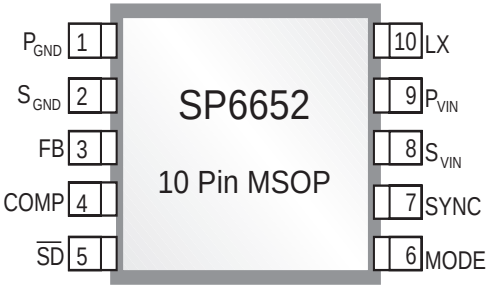
These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

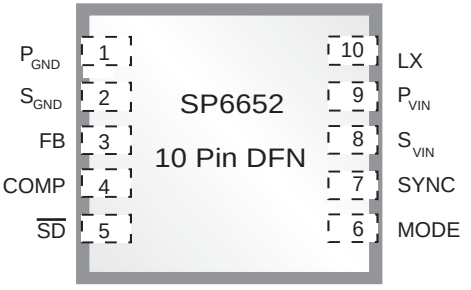
ELECTRICAL CHARACTERISTICS

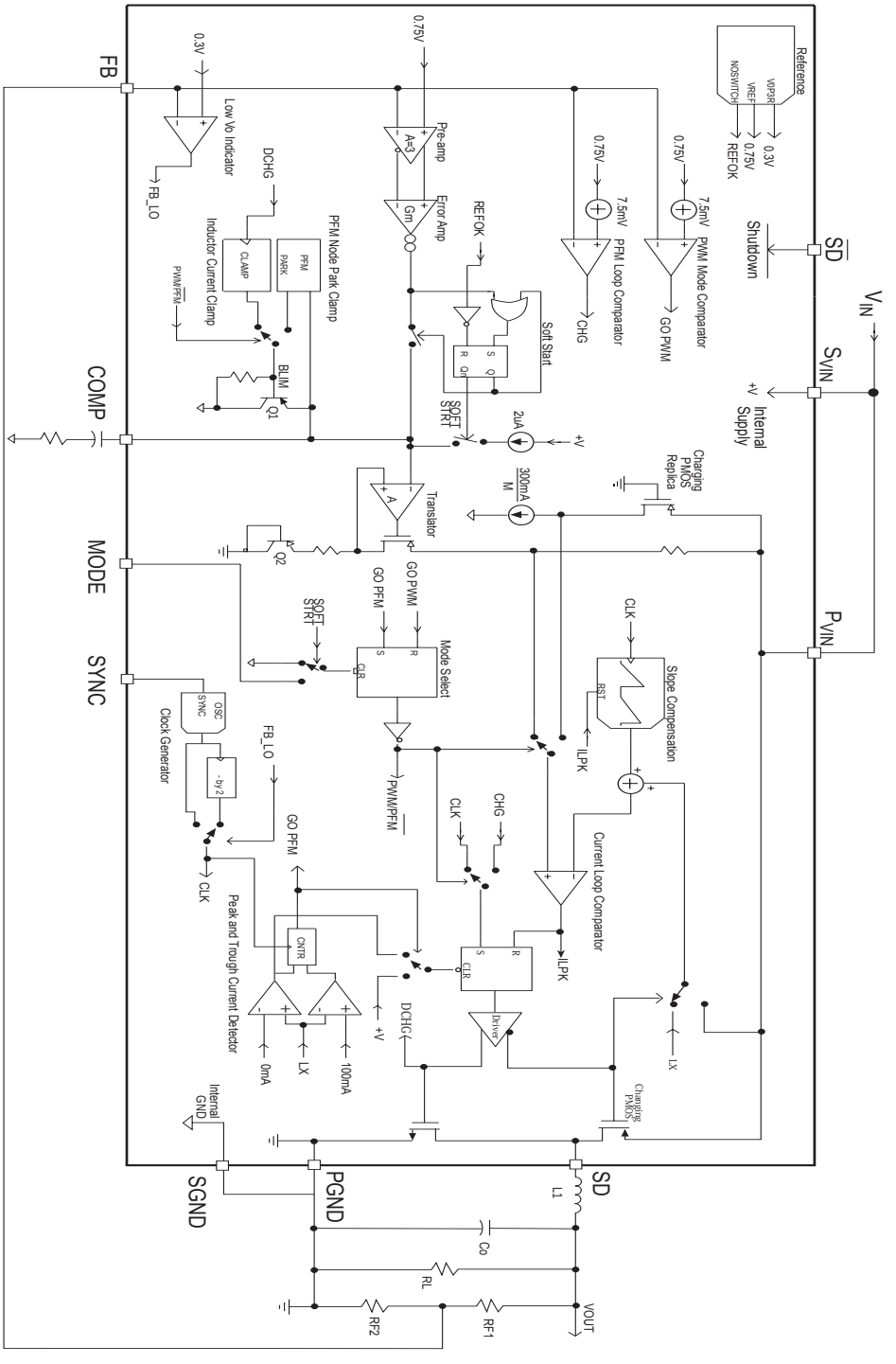
V_{IN} = UV_{IN} = V_{SDN} = 3.6V, I_O = 0mA, T_{AMB} = -40°C to +85°C, typical values at 27°C unless otherwise noted.
The ♦ denotes the specifications which apply over the full temperature range, unless otherwise specified.

PARAMETER	MIN	TYP	MAX	UNITS		CONDITIONS
Input Operating Voltage	2.85		5.5	V	♦	Result of I_Q measurement at V_{IN} = P_{VIN} = 5.5V
FB Set Voltage	0.784	0.8	0.816	V	♦	
FB Set Current	-1	0.01	1	µA	♦	V_{FB} = 0.8V
Overall FB Accuracy	-4		4	%	♦	FB = COMP
Switching Frequency	1.2	1.4	1.6	MHz		Mode = $\overline{SD}$ = V_{IN}
Minimum On-Time-Duration		180	230	ns		V_{FB} = 1.0V, V_{COMP} = 0.2V
SYNC Tracking Frequency	1.0		2.0	MHz	♦	Mode = $\overline{SD}$ = V_{IN}, V_{FB} =1.0V
SYNC Input Current	-1	0.01	1	µA	♦	
SYNC Logic Threshold Low		0.3	0.6	V	♦	High to Low Transition
SYNC Logic Threshold High	1.7			V	♦	Low to High Transition
PMOS Switch Resistance		0.4	0.6	Ω	♦	I_{PMOS} = 200mA
NMOS Switch Resistance		0.4	0.6	Ω	♦	I_{NMOS} = 200mA
Inductor Current Limit	1.3	1.5	1.7	A	♦	V_{FB} = 0.4V, Mode = $\overline{SD}$ = V_{IN}
LX Leakage Current	-3	0.1	3	µA	♦	$\overline{SD}$ = ZeroV
V_{IN} Quiecent Current		1	5	mA		V_{IN} = 3.6V, Mode = $\overline{SD}$ = V_{IN}
		3	10	mA		V_{IN} = 5.5V, Mode = $\overline{SD}$ = V_{IN}
UVLO Undervoltage Lockout Threshold, V_{IN} falling	2.55	2.7	2.85	V	♦	$\overline{SD}$ = V_{IN}
UVLO hysteresis		6		%		
Soft Start Current	1	2	4	µA	♦	$\overline{SD}$ = V_{IN}, V_{COMP} = 1V
$\overline{SD}$ MODE Input Current	-1	0.01	1	µA	♦	
$\overline{SD}$ MODE Input Threshold Voltage	0.6	0.9		V	♦	High to Low Transition
		1.25	1.8	V	♦	Low to High Transition
Slope Compensation		700		mA/µS		
Rising Over-Temperature Trip Point		140		°C		
Over-Temperature Hysteresis		14		°C		
Error Amplifier Transconductance		1		mA/V		

Pin Number	PIN NAME	DESCRIPTION
1	PGND	Power Ground Pin. Synchronous rectifier current returns through this pin.
2	SGND	Internal Ground Pin. Control circuitry returns current to this pin.
3	FB	External feedback network input connection. Connect a resistor from FB to ground and from FB to VOUT to control the output voltage. Regulation point at FB = 0.8V Typical.
4	COMP	Compensation pin for error loop. Connect an R and C in series to ground to control open loop pole and zero.
5	SD	Shutdown control input. Tie pin to VIN for normal operation, tie to ground for shutdown. TTL input threshold.
6	MODE	Connect this pin to VIN.
7	SYNC	An external clock signal can be connected to this pin to synchronize the switching frequency.
8	SVIN	Internal supply voltage. Control circuitry is powered from from this pin. Use an RC filter close to the pin to cut down supply noise.
9	PVIN	Supply voltage for the output driver stage. Inductor charging current passes through this pin.
10	LX	Inductor switching node. Inductor tied between this pin and the output capacitor to create regulated output voltage.







Current Mode Control and Slope Compensation

The SP6652 is designed to use low value ceramic capacitors and low value inductors to reduce the converter's volume and cost in portable devices. Current mode PWM control was, therefore, chosen for the ease of compensation when using ceramic output capacitors and better transient line rejection, which is important in battery powered applications. Current mode control spreads the two poles of the output power train filter far apart so that the modulator gain crosses over at -20dB/decade instead of the usual -40dB/decade. The external compensation network is, simply, a series RC circuit connected between ground and the output of the internal transconductance error amplifier.

It is well known that an unconditional instability exists for any fixed frequency current-mode converter operating above 50% duty cycle. A simple, constant-slope compensation is chosen to achieve stability under these conditions. The most common high duty cycle application is a Li-Ion battery powered regulator with a 3.3V output (D ≥ 90%). Since the current loop is critically damped when the compensation slope (denoted MC_V) equals the negative discharge slope (denoted $M2_V$), the amount of slope compensation chosen is, therefore:

$$M2 = dI_L/dT_{OFF} = -V_{OUT}/L = -3.3V/4.7\mu H = -702mA/\mu s$$

$$M2_V = M2 \bullet R_{PMOS}$$

$MC_V = -M2_V = 702mA/\mu s \bullet 0.2\Omega = 140mV/\mu s$, for $R_{PMOS} = 0.20\Omega$

The inductor current is sensed as a voltage across the PMOS charging switch and the NMOS synchronous rectifier (see BLOCK DIAGRAM). During inductor current charge, $V(PV_{IN})$-V(LX) represents the charging current ramp times the resistance of the PMOS charging switch. To keep the effective current slope compensation constant (remembering current is being compensated, not voltage) the voltage slope must be proportional to R_{PMOS}. To account for this, the slope compensation voltage is internally generated with a bias current that is also proportional to R_{PMOS}.

Over Current Protection

In steady state closed loop operation the voltage at the COMP pin controls the duty cycle. Due to the current mode control and the slope compensation, this voltage will be:

$$V(COMP) \bullet \{I_{LPK} \bullet R_{PMOS} + MC_V \bullet T_{ON} + V_{BE}(Q1)\}$$

The COMP node will be clamped when its voltage tries to exceed $V(BLIM) + V_{BE}(Q1)$. The $V_{BE}(Q1)$ term is cancelled by $V_{BE}(Q2)$ at the output of the translator. The correct value of clamp voltage is, therefore:

$$V(BLIM) = I_{L(MAX)} \bullet R_{PMOS} + MCV \bullet T_{ON}$$

The $I_{L(MAX)}$ term is generated with a bias current that is proportional to R_{PMOS}, to keep the value of current limit approximately constant over process and temperature variations, while the $MC_V \bullet T_{ON}$ is generated by a peak-holding circuit that senses the amplitude of the slope compensation ramp at the end of T_{ON}.

There is minimum on-time (T_{ON}) generated even if the COMP node is at zeroV, since the peak current comparator is reset at the end of a charge cycle and is held low during a blanking time after the start of the next charge cycle. This is necessary to swamp the transients in the inductor current ramp around switching times. The minimum T_{ON} (100ns, nominally) is not sufficient for the COMP node to keep control of the current

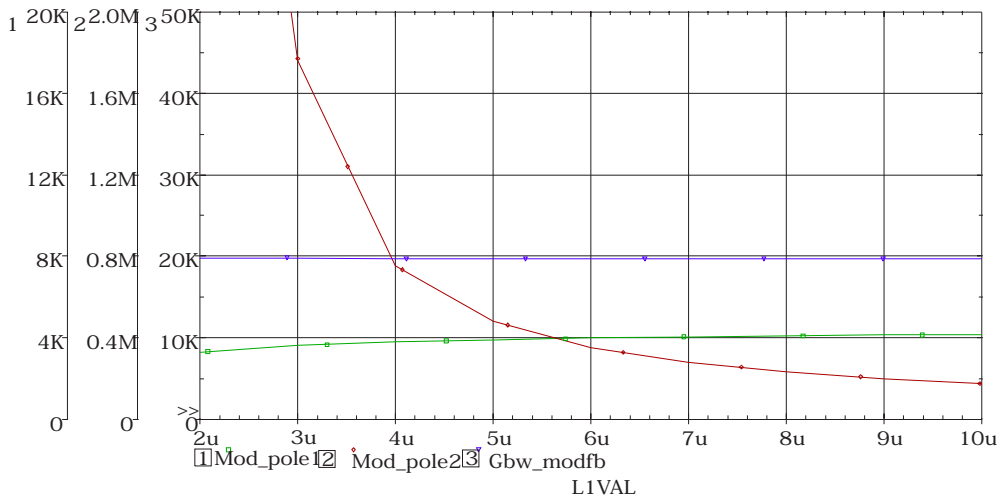
when the output voltage is low. The inductor current tends to rise until the energy loss from the discharge resistances are equal to the energy gained during the charge phase. For this reason, the clock frequency is cut in half when the feedback pin is below 0.3V, effectively reducing the minimum duty cycle in half. Above $V_{(FB)}$ = 0.3V the clock frequency is normal (see Typical Operating Characteristics: Inductor Current vs. V_{OUT})

Voltage Loop and Compensation in PWM Mode

The voltage loop section of the circuit consists of the error amplifier and the translator circuits (see functional diagram). The input of the voltage loop is the 0.8V reference voltage minus the divided down output voltage at the feedback pin. The output of the error amplifier is translated from a ground referred signal (the COMP node) to a power input voltage referred signal. The output of the voltage loop is fed to the positive terminal of the Current Loop comparator, and represents the peak inductor current necessary to close the loop.

The total power supply loop is compensated with a series RC network connected from the COMP pin to ground. Compensation is simple due to current-mode control. The modulator has two dominant poles: one at a low frequency, and one above the crossover frequency of the loop, as seen in the graph below, Linearized Modulator Frequency Response vs. Inductor Value.

The low frequency pole for L1= 5µH is 4kHz, the second pole is 500kHz, and the gain-bandwidth is 20kHz. The total loop crossover frequency is chosen to be 200kHz, which is 1/6th of the clock frequency. This sets the second modulator pole at 2.5 times the crossover frequency. Therefore the gain of the error amplifier can be 200kHz/20kHz = 10 at the first modulator pole of 4kHz. The error amp transconductance is 1mA/V, so this sets the R_Z resistor value in the compensation network at 10/1mA/V = 10kΩ. The zero frequency is placed at the first pole to provide at total system response of -20dB/decade (the zero from the error amp cancels the first modulator pole, leaving the



Conditions: V_{IN}=5V, V_{OUT}=3.3V, f_{CLK}=1.4MHz, C_{OUT}=10µF, and MC_V=132mV/µs. The inductor is varied from 2µH to 10µH

Linearized Modulator Frequency Response vs. Inductor

1 pole rolloff from the error amp pole). The compensation capacitor becomes:

$$C_C = \frac{1}{(2\pi \bullet Rz \bullet pole1)} = \frac{1}{(6.28 \bullet 10k\Omega \bullet 4kHz)}$$

$$= 4nF$$

Soft Start

Soft-start is accomplished by disconnecting the error amp and inserting a constant 2µA current to charge the compensation capacitor.

When power is first applied and the reference establishes, the clamp circuit at the COMP node sets its voltage at one VBE, which is the bottom of the inductor current range. The soft-start current continues to charge up the COMP node, slowly raising the inductor current level. The inductor current will increase at approximately:

$(I_{REFSS} / C_C) \bullet R_{PMOS}$

where:

I_{REFSS} = Soft start constant current
= 2µA nominally

C_C = Compensation capacitor

R_{PMOS} = Charging PMOS resistance

For typical circuit values of C_C=6.8nF and R_Z=8kΩ, the soft start period is TBD ms.

The inductor current will eventually rise above the required load current and the output voltage will charge up. During soft-start the error amp is disconnected and acts as a comparator. When V(FB) rises above the reference, the error amp switches to logic high and ends soft-start, at which point the error amp output is connected to the capacitated COMP node.

The switching frequency will be reduced to half the normal frequency as long as V(FB) is below 0.3V, as previously discussed in the Over Current Protection section.

100% Duty Cycle in Dropout

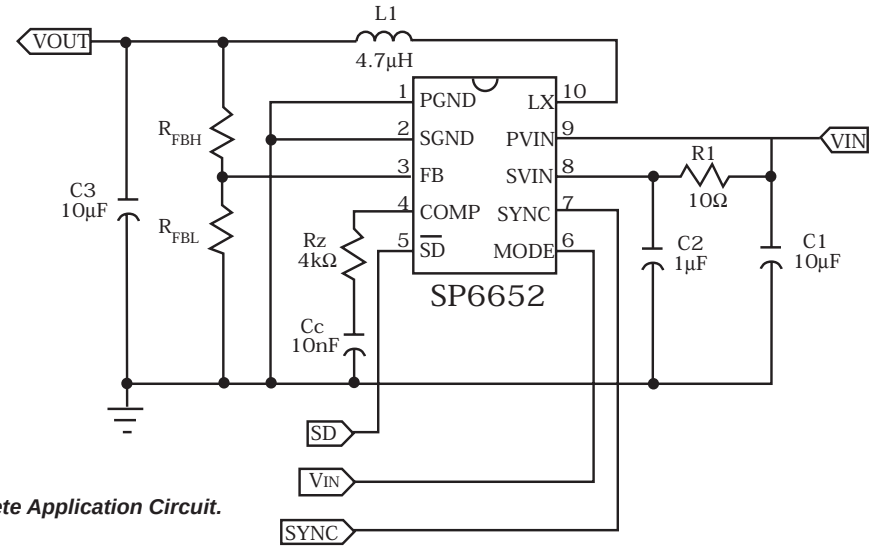
To extend the battery life in portable applications, the PWM control logic is set up such that if the output SR latch has not been reset by the Current Loop comparator at the end of a clock cycle, the charge signal continues to stay high into the beginning of the next cycle. This will happen naturally when the converter starts to go into dropout. The slope compensation ramp is reset every cycle.

External Clock Synchronization

The SP6652 has an internal 1.4MHz clock that can be defeated by connecting an external clock pulse on the SYNC. The capture range for clock synchronization is 1.0 to 2.0MHz. When a clock pulse is present on the SYNC pin, the internal oscillator bias current is scaled back, handing control of the clock pulses to the faster external clock. The pulse width of the clock is approximately 50 ns, whether internally generated or externally applied.

Thermal Shutdown

The internal die temperature is monitored by a comparator that issues a “TOO HOT” signal when the junction temperature reaches 140˚C, nominally. This signal that inhibits all internal circuits until the temperature has decreased to approximately 135˚C, at which point a normal soft start sequence is initiated.



Complete Application Circuit.

COMPONENT SELECTION

The SP6652 PWM buck regulator circuit requires 3 capacitors: 10µF for the PVIN input, 1µF input bypass for the SVIN and 10µF for the output are typically recommended. For the input capacitor, a value even larger than 10µF will help reduce input voltage ripple for applications sensitive to ripple on the battery voltage. See the Typical Performance Characteristics section for waveforms on input and output ripple with 10µF capacitors. All the capacitors should be surface mount ceramic for low lead inductance necessary at the 1.4MHz switching frequency of the SP6652 and to obtain low ESR. This also helps improve bypassing on the input pin and ripple on the output. Ceramic capacitors with X5R or X7R temperature grade are recommended for most applications. A selection of recommended capacitors is included in Table 1. The 1µF SVIN input capacitor should have a series resistor of about 10Ω value connected from the input to the SVIN pin to form an RC low pass filter to remove high frequency spikes present on the input switching pin PVIN. This will keep the SP6652 internal reference and other sensitive circuits noise free and ensure better output regulation. The GND returns for the PVIN capacitor and the output capacitor should be connected directly to the PGND pin, which should connect to the thermal pad ground located under the SP6652. The GND return for the 1µF SVIN capacitor should be connected to the SGND pin, which should be connected separately to the PGND pin to avoid adding PGND noise to the SP6652 SGND pin. See the Typical SP6652 Circuit Layout for details on the recommended layout.

Output Voltage Selection

To set the output voltage for the SP6652, a pair of resistors, RF and RI are used as a voltage divider between the output voltage at the output capacitor and the FB pin and GND, as shown in the typical application circuit. The recommended value for the RI resistor is 100KΩ to 200KΩ to keep the quiescent current low, but not have the impedance too high at the FB pin for good regulation.

Manufacturers/ Website	Part Number	Capacitance/ Voltage	Capacitor Size/Type/Thickness	ESR at 100KHz
TDK/www.tdk.com	C1005X5R0J105M	1uF/6.3V	0402/X5R/0.5mm	0.03
TDK/www.tdk.com	C1608X5R0J475K	4.7uF/6.3V	0603/X5R/0.9mm	0.02
TDK/www.tdk.com	C2012X5R0J106M	10uF/6.3V	0805/X5R/1.35mm	0.02
Murata/www.murata.com	GRM155R60J105KE19B	1uF/6.3V	0402/X5R/0.55mm	0.03
Murata/www.murata.com	GRM188R60J475KE19	4.7uF/6.3V	0603/X5R/0.9mm	0.02
Murata/www.murata.com	GRM21BR60J106KE19L	10uF/6.3V	0805/X5R/1.35mm	0.02

Table 1. Capacitor Selection Note: Component highlighted in bold is used on the SP6652EB Evaluation Board.

The range of typical inductor values and sizes are shown here in Table 2.

Manufacturers/ Website	Part Number	Inductance/ Isat Rating	Inductor Length/Width/Thickness	DCR Max ohms
Coilcraft/ www.coilcraft	MSS5131-332MX	3.3uH/1.6A	5.1x5.1x3.1mm	0.032
Coilcraft/ www.coilcraft	MSS5131-332MX	4.7uH/1.4A	5.1x5.1x3.1mm	0.045
Sumida/ www.sumida.com	CDRH3D28-3R3	3.3uH/2.0A	4.0x4.0x3.0mm	0.058
Sumida/ www.sumida.com	CDRH3D28-4R7	4.7uH/1.65A	4.0x4.0x3.0mm	0.071
Wurth Elektronik/ www.we-online.de	WE-TPC #744042003	3.3uH/1.8A	4.8/4.8/1.8mm	0.065
Wurth Elektronik/ www.we-online.de	WE-TPC #744042004	4.7uH/1.65A	4.8/4.8/1.8mm	0.082

Table 2. Inductor Selection Note: Component highlighted in bold is used on the SP6652EB Evaluation Board.

The output voltage can be set using the formula:
$V_{OUT} = V_{FB}*(1 + R_F/R_I)$

Where V_{FB} = 0.8V typically, and for no-load T_{ON} is kept within 200nsec Minimum:
$T_{ON(MIN)} = V_{OUT}/(V_{IN} *Freq)$.

Compensation Component Selection

For simplicity in compensation with ceramic output capacitors, the SP6652 uses current mode PWM control, so all that is needed for stability is a series R_Z and C_C at the COMP pin to compensate the error amplifier. To see the actual SP6652 response with frequency, in figure 3 we have taken a bode plot of gain and frequency response of the SP6652 circuit with 3.3Vout. Looking first at the SP6652 Modulator Gain at low frequency you see a constant gain of about 26dB and the first pole or -3dB point at about 4 kHz, where the slope of the gain curve becomes about -20dB/decade. At high frequency on the SP6652 Modulator Gain curve one can see the modulator curve slope increase downward for a high frequency pole at about 150KHz, which is widely separated in frequency from the low frequency 4kHz pole, so that the SP6652 can be compensated by a zero at the low frequency pole where the gain slope is only -20dB/decade. The gain for the error amplifier is the cross-

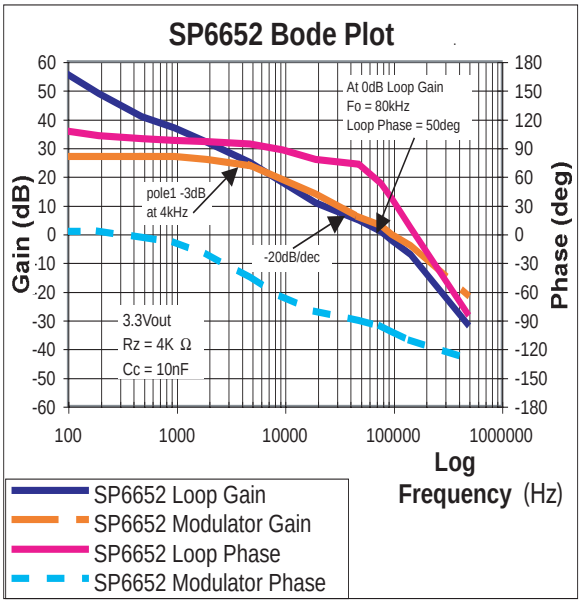


Figure 3. SP6652 Gain and Frequency Response 3.3V output voltage

over frequency f_{zero} = 80kHz (from the Bode plot) divided by the loop gain bandwidth, given as 20kHz, which is used in the following equation:

Error Amp Gain
= f_{zero} / (loop gain bandwidth)
= 80kHz / 20kHz
= 4

The error amp transconductance is about 1mS, so this sets the R_Z resistor to be:

R_Z = 4/1mS = 4KΩ

We will use R_Z = 4KΩ for the 3.3V output compensation.

The zero for loop compensation is placed at the first modulator pole of 4 kHz to provide a loop response of -20/dB/decade at the crossover frequency. The compensation capacitor Cc can be calculated from the crossover frequency pole1 and the R_Z value:

$C_C = 1/(2\pi \bullet R_Z \bullet pole1) = 1/(2\pi \bullet 4K \bullet 4kHz)$
= 10nF

From the Typical Performance Characteristics load step curves, the 2.5V output and 3.3V output are stable with R_Z = 4KΩ and C_C = 10nF. For 1.8V to 0.85V output, the values R_Z = 2KΩ and C_C = 10nF are recommended.

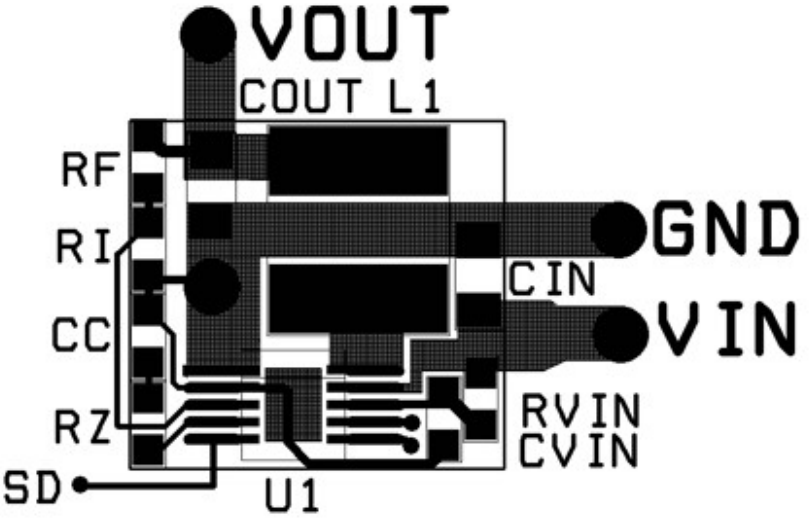


Figure 4. Typical SP6652 circuit layout.

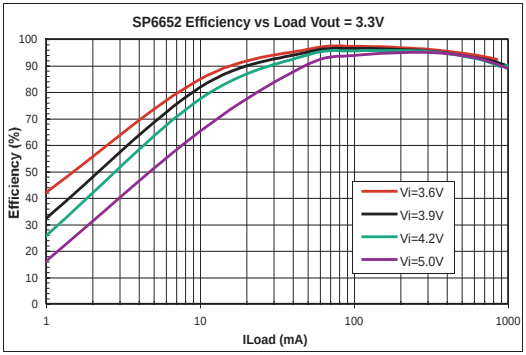


Figure 5. Efficiency vs. Load, Vout= 3.3V

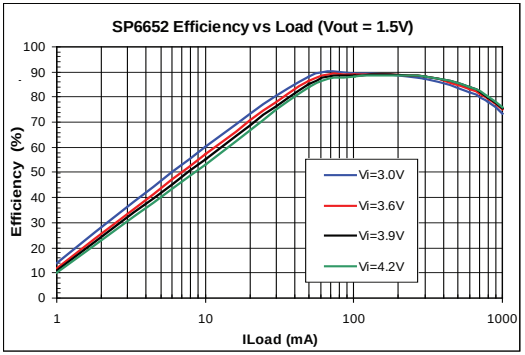


Figure 6. Efficiency vs. Load, Vout= 1.5V

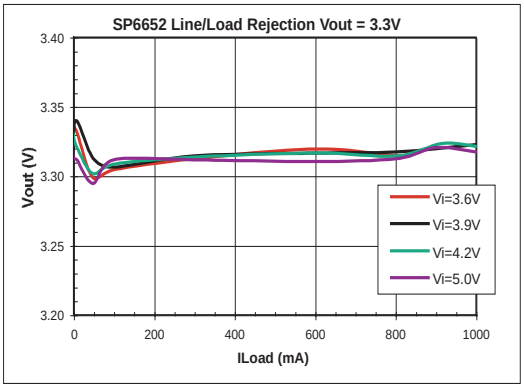


Figure 7: Line/Load Rejection , Vout = 3.3V

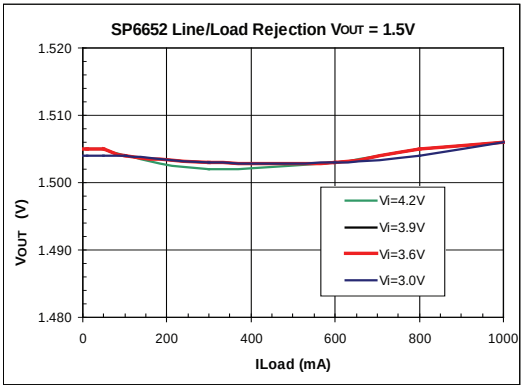


Figure 8: Line/Load Rejection , Vout = 1.5V

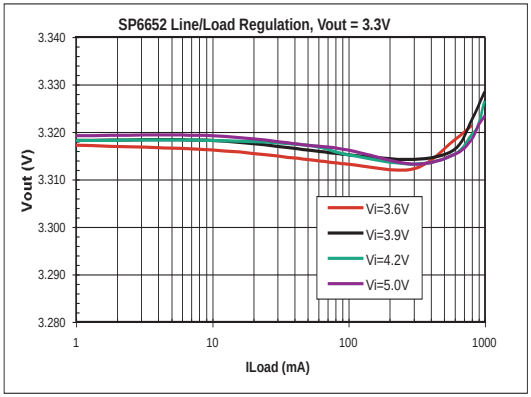


Figure 9: Line/Load Regulation , Log Scale, Vout = 3.3V

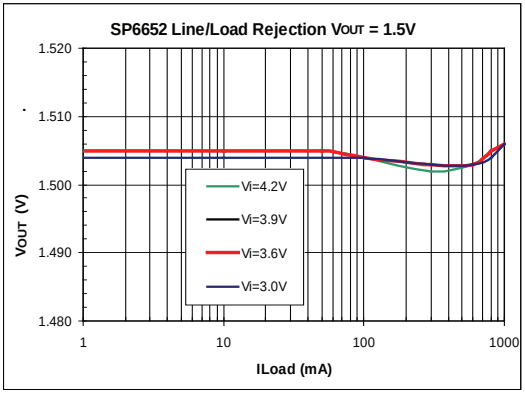


Figure 10: Line/Load Regulation , Log Scale, Vout = 1.5V

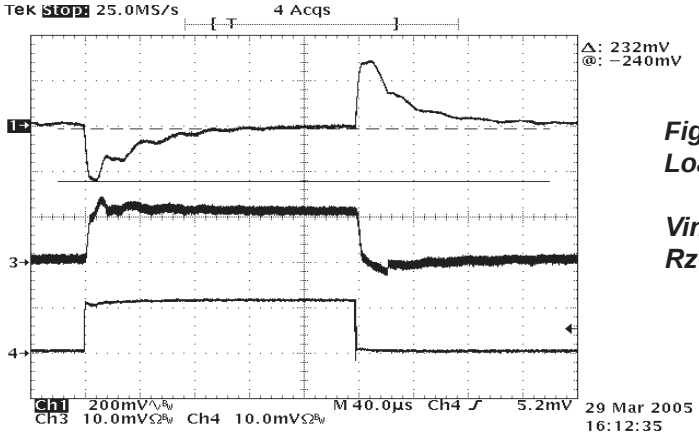


Figure 11. 0mA to 600mA Load Step Data

Vin=4.2V, Vo=3.3V
Rz=4kΩ, Cz=10nF, L1=4.7uH

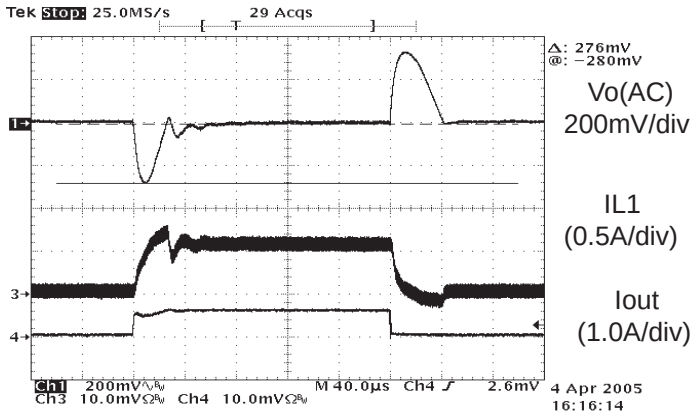


Figure 12. 0mA to 600mA Load Step Data

Vin=4.2V, Vo=1.5V
Rz=2kΩ, Cz=10nF,
L1=4.7uH

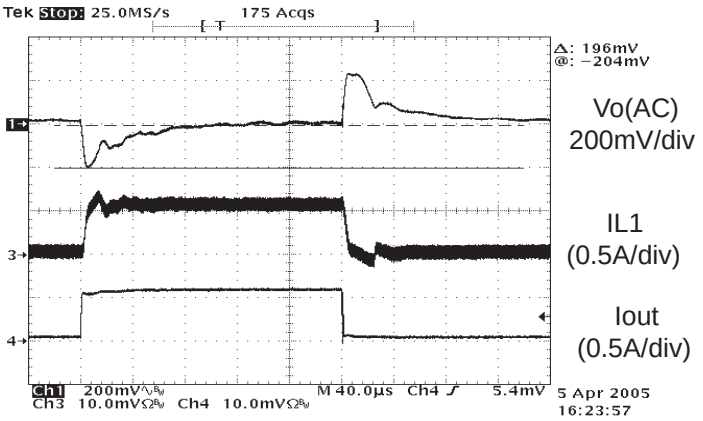


Figure 13. 0mA to 600mA Load Step Data

Vin=4.2V, Vo=2.5V
Rz=4kΩ, Cz=10nF,
L1=4.7uH

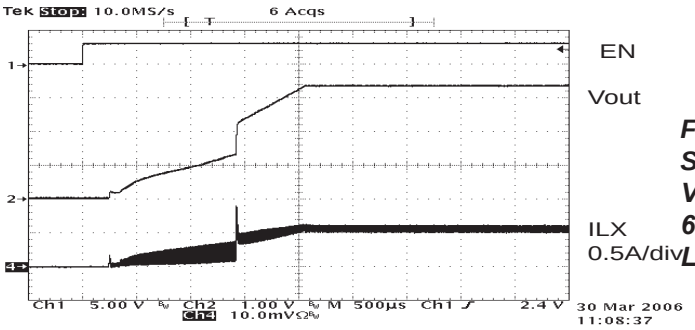


Figure 14. SP6652 600mA Start-up from Enable Vin=4.2V, Vo=3.3V, Iout = 600mA, Rz=4kΩ, Cz=10nF, L1=4.7uH

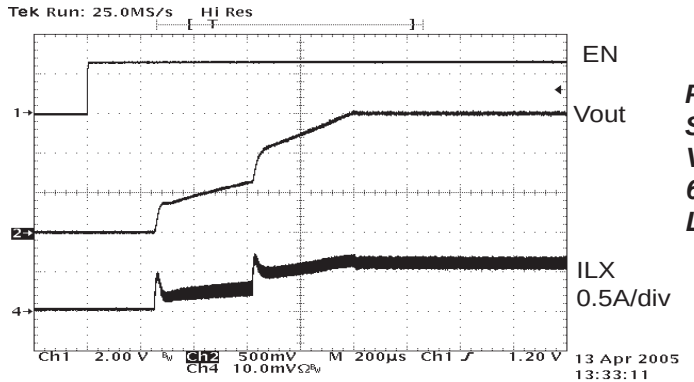


Figure 15. SP6652 600mA Start-up from Enable Vin=4.2V, Vo=1.5V, Iout = 600mA, Rz=2kΩ, Cz=10nF, L1=4.7uH

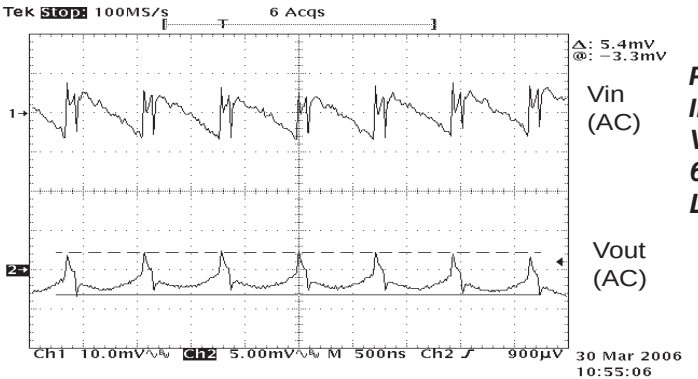


Figure 16. SP6652 600mA Input/Output Ripple Vin=4.2V, Vo=3.3V, Iout = 600mA, Rz=4kΩ, Cz=10nF, L1=4.7uH

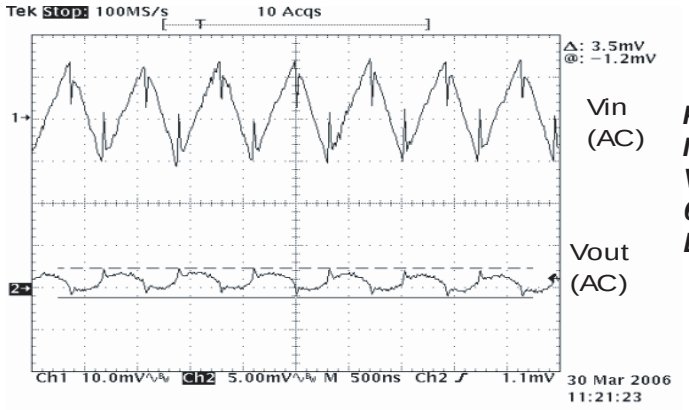
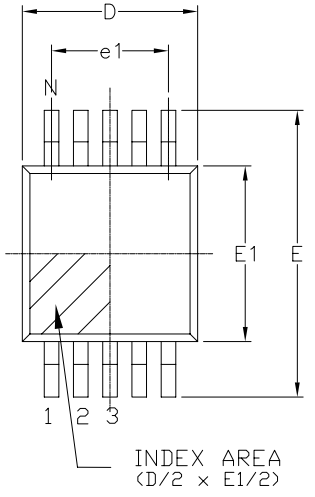
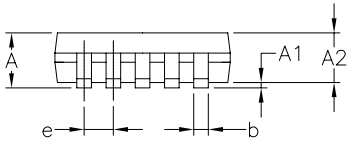


Figure 17. SP6652 600mA Input/Output Ripple Vin=4.2V, Vo=1.5V, Iout = 600mA, Rz=2kΩ, Cz=10nF, L1=4.7uH

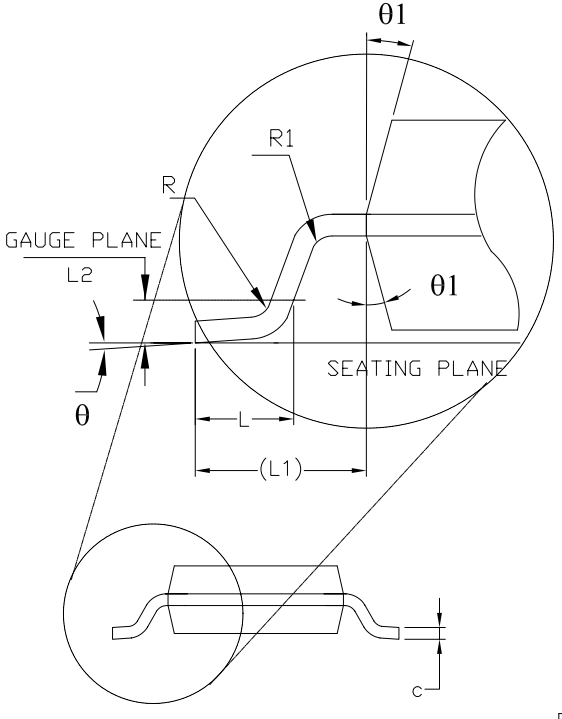
REVISION HISTORY			
REV.	DISCRIPTION	DATE	APP'D
A	DRAWING ORIGINATION	08/09/05	JL
B	DRAWING FORMAT MODIFICATION	07/19/06	JL

Top View





Side View

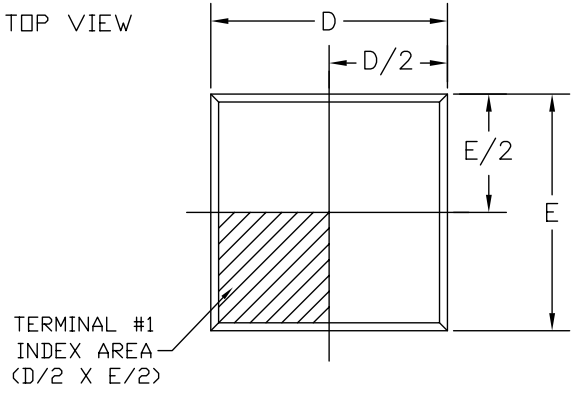


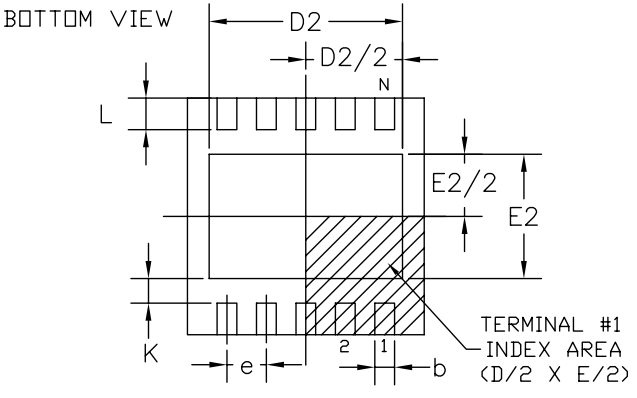
Front View

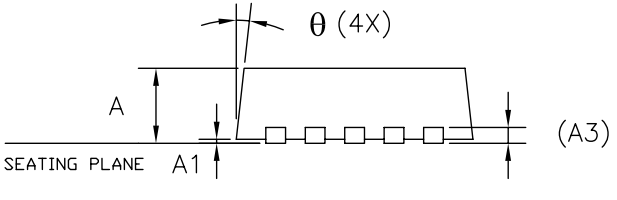
10 Pin MSOP JEDEC MO-187 Variation BA						
SYMBOLS	DIMENSIONS IN MM (Control Unit)			DIMENSIONS IN INCH (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	—	—	1.10	—	—	0.043
A1	0.00	—	0.15	0.000	—	0.006
A2	0.75	0.85	0.95	0.030	0.033	0.037
b	0.17	—	0.33	0.007	—	0.013
c	0.08	—	0.23	0.003	—	0.009
E	4.90 BSC			0.193 BSC		
E1	3.00 BSC			0.118 BSC		
e	0.50 BSC			0.020 BSC		
e1	2.00 BSC			0.079 BSC		
L	0.40	0.60	0.80	0.016	0.024	0.031
L1	0.95 REF			0.037 REF		
L2	0.25 BSC			0.010 BSC		
R	0.07	—	—	0.003	—	—
R1	0.07	—	—	0.003	—	—
θ	0°	—	8°	0°	—	8°
θ1	5°	—	15°	5°	—	15°
D	3.00 BSC			0.118 BSC		
N	10			10		

Solved by Sipex		SIPEX CORPORATION	
		10 PIN MSOP PACKAGE OUTLINE	
Packaging Approval:		Drawing No:	10-PIN MSOP
By: JL	Date: 07/19/06	Revision: B	Sheet: 1 OF 1

REVISION HISTORY			
REV.	DISCRIPTION	DATE	APP'D
A	DRAWING ORIGINATION	08/09/05	JL
B	MODIFY DRAWING FORMAT	07/10/06	JL







SIDE VIEW

10LD 3x3 DFN JEDEC MO-229 Variation VEED-5						
SYMBOLS	DIMENSIONS IN MM (Control Unit)			DIMENSIONS IN INCH (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.90	1.00	0.032	0.036	0.039
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.20 REF			0.008 REF		
b	0.18	0.25	0.30	0.007	0.010	0.012
D	3.00 BSC			0.118 BSC		
D2	2.20	—	2.70	0.087	—	0.106
E	3.00 BSC			0.118 BSC		
E2	1.40	—	1.75	0.056	—	0.069
e	0.50 BSC			0.020 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
K	0.20	—	—	0.008	—	—
θ	0°	—	14°	0°	—	14°
N	10			10		
ND	5			5		

Solved by Sipex	SIPEX CORPORATION		
	10 PIN 3x3 DFN PACKAGE OUTLINE		
Packaging Approval:	Drawing No: 10-PIN 3x3 DFN		
By: JL / Date: 07/10/06	Revision: B	Sheet: 1 OF 1	

Ordering Information

Part Number	MSL Level	RoHS	Min Temp	Max Temp	Package	Pack Type	Quantity
SP6652ER-L	L1 @ 260ºC	Yes	-40	85	DFN10	Canister	Any
SP6652ER-L/TR	L1 @ 260ºC	Yes	0	70	DFN10	Tape & Reel	3000
SP6652EU-L/TR	L1 @ 260ºC	Yes	0	70	MSOP10	Tape & Reel	2500
SP6652EU-L	L1 @ 260ºC	Yes	0	70	MSOP10	TUBE	50
SP6652ER	L1 @ 240ºC	No	-40	85	DFN10	Canister	Any
SP6652ER/TR	L1 @ 240ºC	No	-40	85	DFN10	Tape & Reel	3000
SP6652EU	L1 @ 240ºC	No	0	70	MSOP10	TUBE	50
SP6652EU-ES	L1 @ 240ºC	No	0	70	MSOP10	TUBE	50
SP6652EU/TR	L1 @ 240ºC	No	0	70	MSOP10	Tape & Reel	2500

Evaluation Boards

SP6652EB	Not Applicable to Board	No	0	70	Board	Not Available in Bulk	
SP6652LEDEB	Not Applicable to Board	No	0	70	Board	Not Available in Bulk	

Note: The SP6652EB is for regular SP6652 users, the SP652LEDEB is for LED driver users.

For latest information on ordering status, go to the Sipex Web Landing Page for this product
http://www.sipex.com/productDetails.aspx?part=SP6652&keyword=sp6652

For further assistance:

Email: Sipexsupport@sipex.com
WWW Support page: http://www.sipex.com/content.aspx?p=support
Sipex Application Notes: http://www.sipex.com/applicationNotes.aspx

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