

700V High and Low Side Driver

Features

- Drives IGBT/MOSFET power devices
- Gate drive supplies up to 20V per channel
- Undervoltage lockout for V_{CC} for V_{BS}
- 3.3V, 5V, 15V input logic compatible
- Tolerant to negative transient voltage
- Designed for use with bootstrap power supplies
- Matched propagation delays for all channels
- -40°C to 125°C operating range
- RoHS compliant
- Lead-Free

Description

The IR7106S is a high voltage, high speed, power MOSFET and IGBT gate driver with independent high-side and low-side output channels. This IC is designed to be used with low-cost bootstrap power supplies. Proprietary HVIC and latch immune CMOS technologies have been implemented in a rugged monolithic structure. The floating logic input is compatible with standard CMOS or LSTTL outputs (down to 3.3V logic). The output drivers feature a high-pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify the HVIC's use in high frequency applications. The floating channel can be used to drive N-channel power MOSFETs or IGBTs in the high-side configuration, which operates up to 700V.

Product Summary

V_{OFFSET}	$\leq 700V$
V_{OUT}	10V – 20V
I_{O+} & I_{O-} (typ.)	200mA / 350mA
t_{ON} & t_{OFF} (typ.)	220ns & 200ns

Package Options

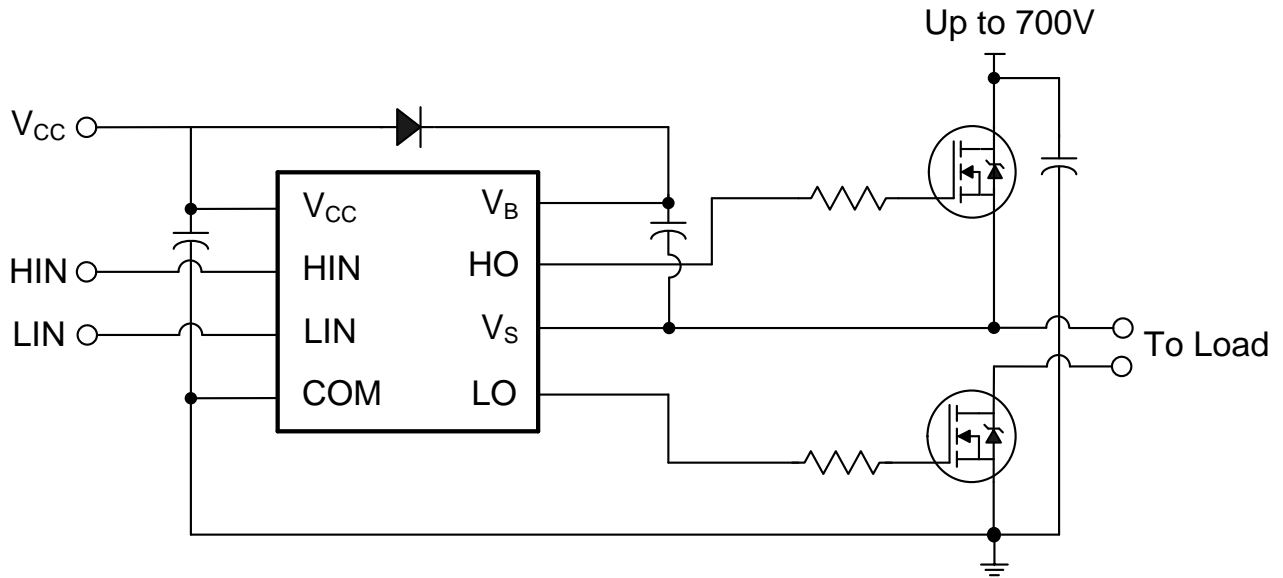


Typical Applications

- Appliance motor drives
- Servo drives
- Micro inverter drives
- General purpose three phase inverters

Base Part Number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IR7106SPBF	SO8N	Tube	95	IR7106SPBF
IR7106SPBF	SO8N	Tape and Reel	2500	IR7106STRPBF

Typical Connection Diagram



(Refer to Lead Assignments for correct pin configuration). This diagram shows electrical connections only. Please refer our Application Notes & DesignTips for proper circuit board layout.

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM unless otherwise stated in the table. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units
V _{CC}	Low side supply voltage	-0.3	25 [†]	V
V _{IN}	Logic input voltage	COM - 0.3	V _{CC} + 0.3	
V _B	High-side floating well supply voltage	-0.3	725	
V _S	High-side floating well supply return voltage	V _B - 25	V _B + 0.3	
V _{HO}	Floating gate drive output voltage	V _S - 0.3	V _B + 0.3	
V _{LO}	Low-side output voltage	COM - 0.3	V _{CC} + 0.3	
COM	Power ground	V _{CC} - 25	V _{CC} + 0.3	
dV _S /dt	Allowable V _S offset supply transient relative to V _{SS}	—	50	V/ns
P _D	Package power dissipation @ T _A ≤ +25°C	—	0.625	W
R _{thJA}	Thermal resistance, junction to ambient	—	200	°C/W
T _J	Junction temperature	—	150	°C
T _S	Storage temperature	-55	150	
T _L	Lead temperature (soldering, 10 seconds)	—	300	

† All supplies are tested at 25V.

Recommended Operating Conditions

For proper operation, the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to COM unless otherwise stated in the table. The offset rating is tested with supplies of (V_{CC} - COM) = (V_B - V_S) = 15V.

Symbol	Definition	Min	Max	Units
V _{CC}	Low-side supply voltage	10	20	V
V _{IN}	HIN, LIN, & EN input voltage	0	V _{CC}	
V _B	High-side floating well supply voltage	V _S +10	V _S +20	
V _S	High-side floating well supply offset voltage [†]	COM-5 [†]	700	
V _{HO}	Floating gate drive output voltage	V _S	V _B	
V _{LO}	Low-side output voltage	COM	V _{CC}	
COM	Power ground	-5	5	
T _A	Ambient temperature	-40	125	°C

† Logic operation for V_S of -5 V to 700V. Logic state held for V_S of -5 V to -V_{BS}. Please refer to Design Tip DT97-3 for more details.

Static Electrical Characteristics

$(V_{CC} - COM) = (V_B - V_S) = 15V$. $T_A = 25^\circ C$ unless otherwise specified. The V_{IN} and I_{IN} parameters are referenced to COM. The V_O and I_O parameters are referenced to respective V_S and COM and are applicable to the respective output leads HO or LO. The V_{CCUV} parameters are referenced to COM. The V_{BSUV} parameters are referenced to V_S .

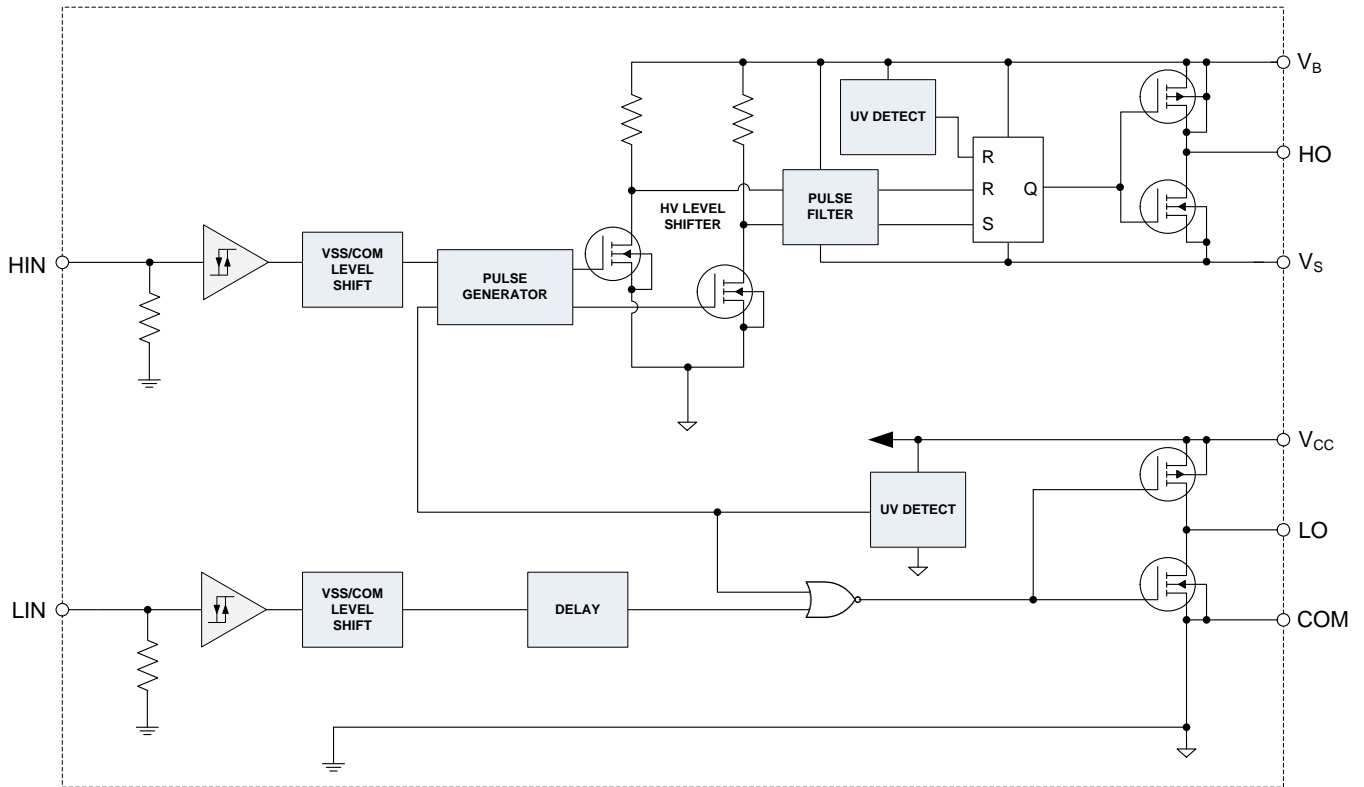
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{BSUV+}	V_{BS} supply undervoltage positive going threshold	8	8.9	9.8	V	
V_{BSUV-}	V_{BS} supply undervoltage negative going threshold	7.4	8.2	9		
V_{BSUVHY}	V_{BS} supply undervoltage hysteresis	0.3	0.7	—		
V_{CCUV+}	V_{CC} supply undervoltage positive going threshold	8	8.9	9.8		
V_{CCUV-}	V_{CC} supply undervoltage negative going threshold	7.4	8.2	9		
V_{CCUVHY}	V_{CC} supply undervoltage hysteresis	0.3	0.7	—		
I_{LK}	High-side floating well offset supply leakage	—	—	50	μA	$V_B = V_S = 700V$
I_{QBS}	Quiescent V_{BS} supply current	—	75	130		$V_{IN} = 0V$ or $5V$
I_{QCC}	Quiescent V_{CC} supply current	—	120	180		
V_{OH}	High level output voltage drop, $V_{BIAS} - V_O$	—	0.80	1.4	V	$I_O = 20mA$
V_{OL}	Low level output voltage drop, V_O	—	0.30	0.6		
I_{O+}	Output high short circuit pulsed current	120	200	—	mA	$V_O = 0V$, $PW \leq 10\mu s$
I_{O-}	Output low short circuit pulsed current	250	350	—		$V_O = 15V$, $PW \leq 10\mu s$,
V_{IH}	Logic "1" input voltage	2.9	3	—	V	$V_{CC} = 10V$ to $20V$
V_{IL}	Logic "0" input voltage	—	—	0.8		
I_{IN+}	Input bias current (HO = High)	—	5	20	μA	$V_{IN} = 5V$
I_{IN-}	Input bias current (HO = Low)	—	—	2		$V_{IN} = 0V$

Dynamic Electrical Characteristics

$V_{CC} = V_B = 15V$, $V_S = COM$, $T_A = 25^\circ C$, and $C_L = 1000pF$ unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{ON}	Turn-on propagation delay	—	220	300	ns	$V_S = 0V$
t_{OFF}	Turn-off propagation delay	—	200	280		$V_S = 0V$ or $700V$
t_R	Turn-on rise time	—	150	220		$V_S = 0V$
t_F	Turn-off fall time	—	50	80		
MT	Delay matching time (t_{ON} , t_{OFF})	—	0	50		

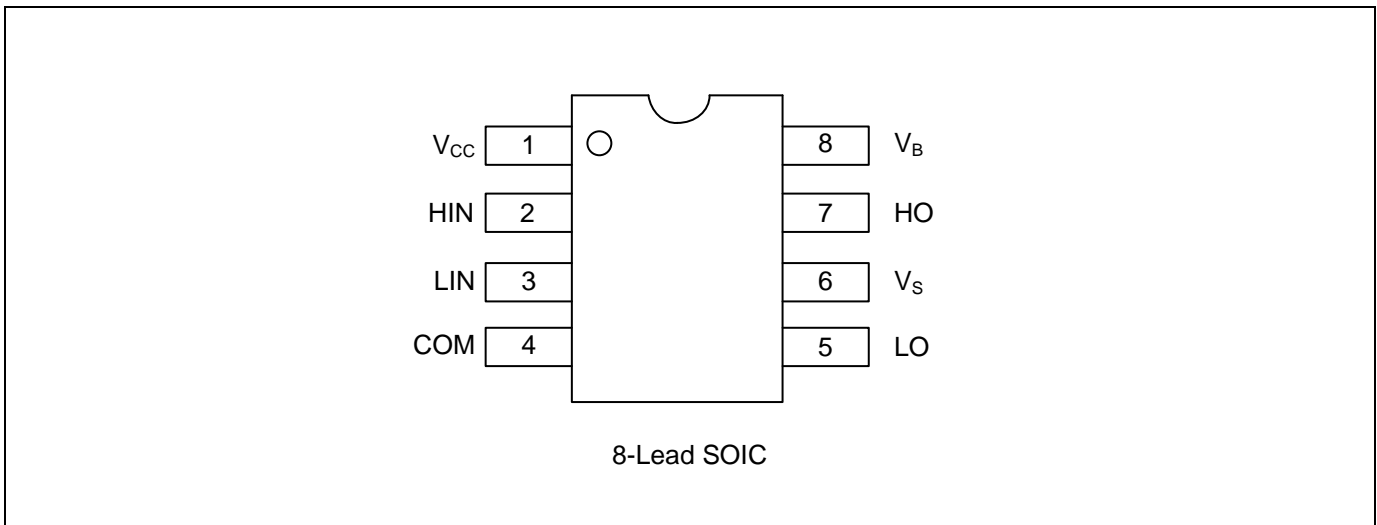
Functional Block Diagram



Lead Definitions

Symbol	Description
VCC	Low-side and logic supply voltage
VB	High-side gate drive floating supply
VS	High voltage floating supply return
HIN	Logic inputs for high-side gate driver output
LIN	Logic inputs for low-side gate driver output
HO	High-side driver output
LO	Low-side driver output
COM	Low-side gate drive return

Lead Assignments



Application Information and Additional Details

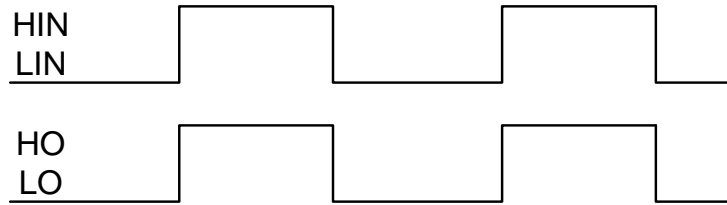


Figure 1. Input/Output Timing Diagrams

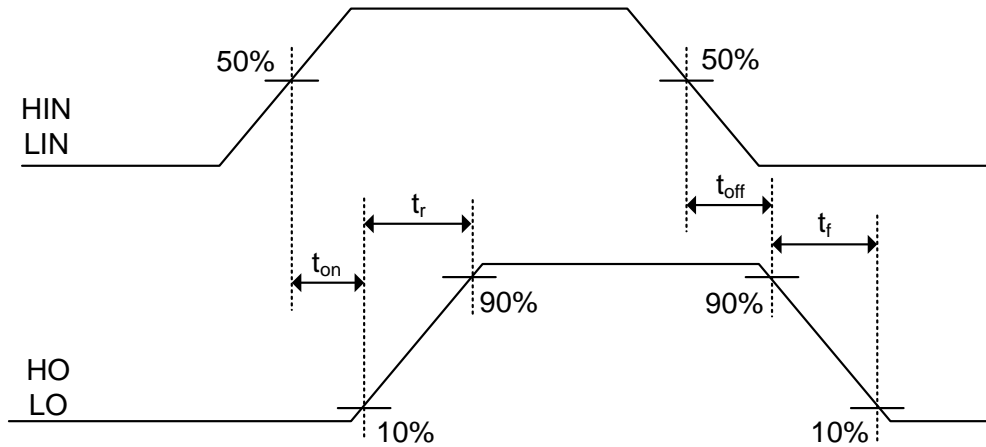


Figure 2. Switching Time Waveform Definitions

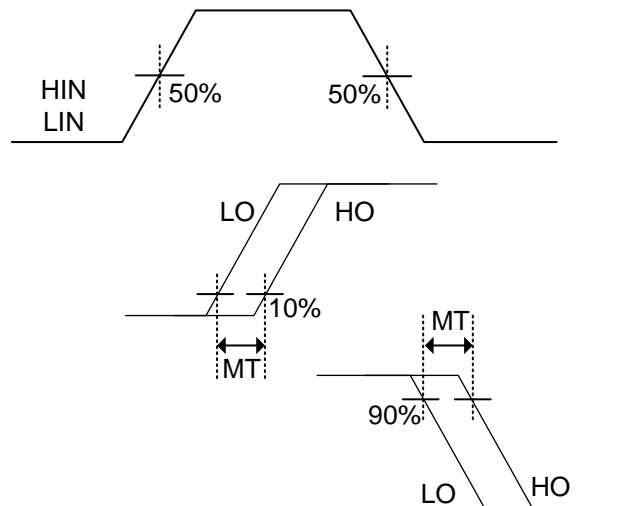
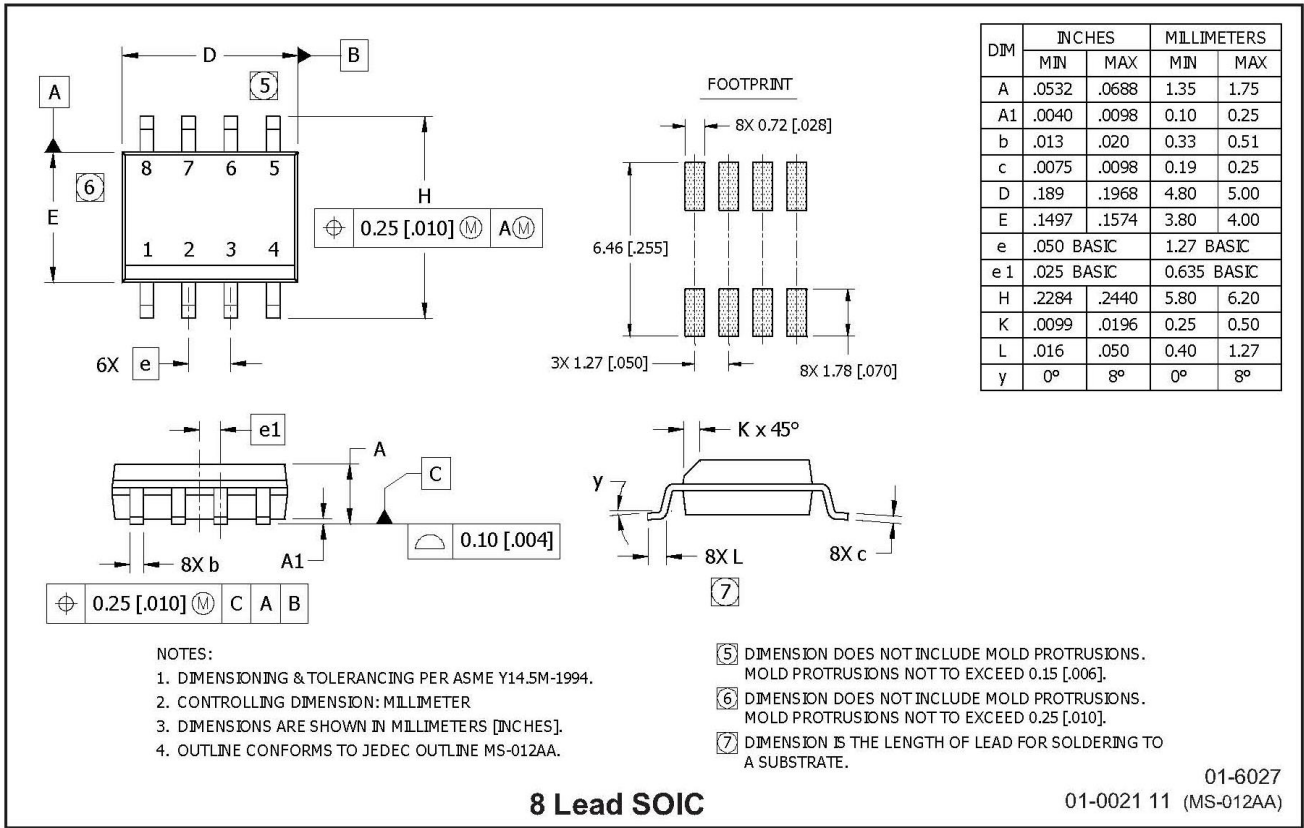
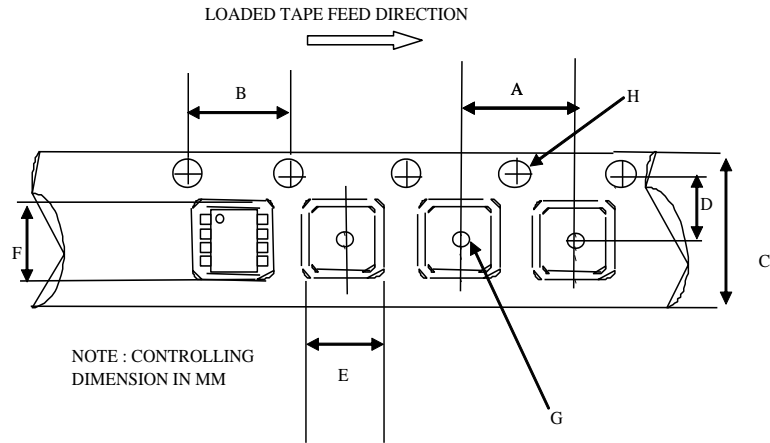


Figure 3. Delay Matching Waveform Definitions

Package Details

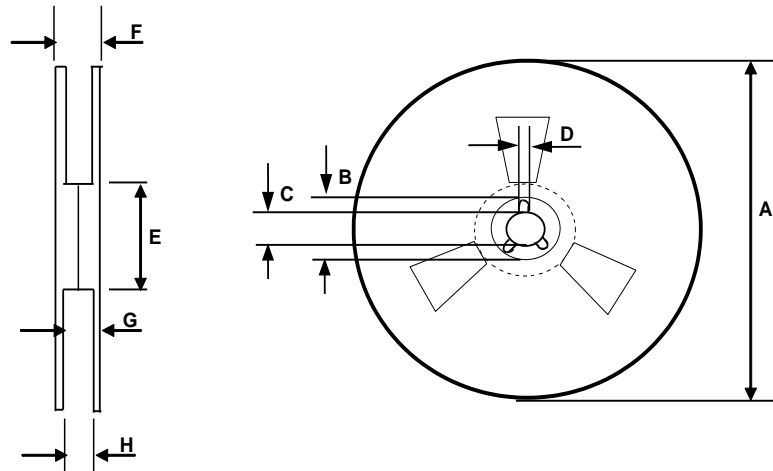


Tape and Reel Details



CARRIER TAPE DIMENSION FOR 8SOICN

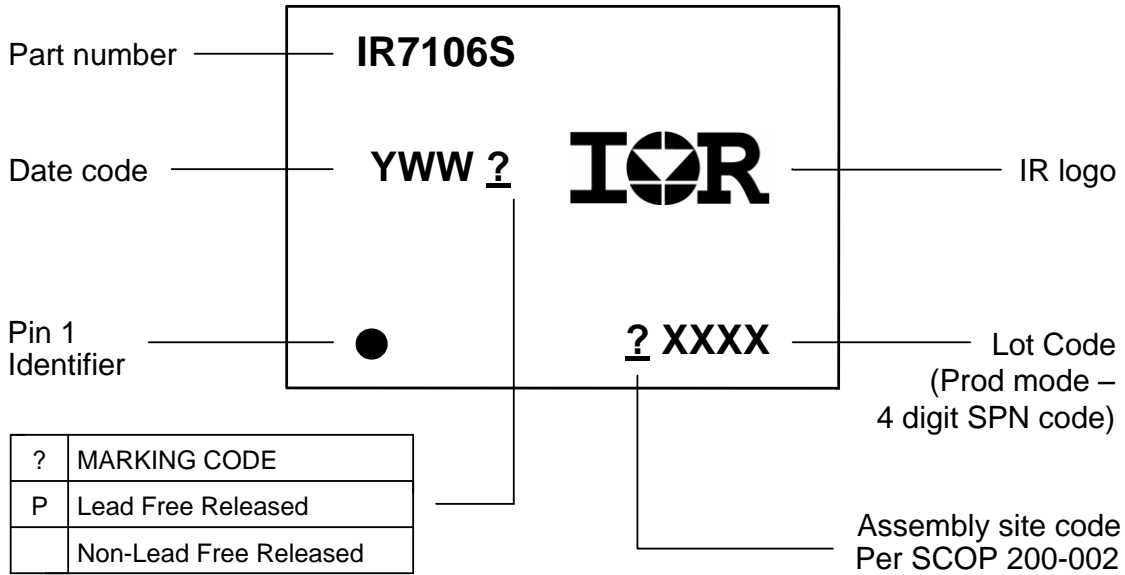
Code	Metric		Imperial	
	Min	Max	Min	Max
A	7.90	8.10	0.311	0.318
B	3.90	4.10	0.153	0.161
C	11.70	12.30	0.46	0.484
D	5.45	5.55	0.214	0.218
E	6.30	6.50	0.248	0.255
F	5.10	5.30	0.200	0.208
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062



REEL DIMENSIONS FOR 8SOICN

Code	Metric		Imperial	
	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	18.40	n/a	0.724
G	14.50	17.10	0.570	0.673
H	12.40	14.40	0.488	0.566

Part Marking Information



Qualification Information[†]

Qualification Level		Industrial ^{††}	
		Comments: This family of ICs has passed JEDEC's Industrial qualification. IR's Consumer qualification level is granted by extension of the higher Industrial level.	
Moisture Sensitivity Level		8 Lead SOIC	MSL2 ^{†††} , 260°C (per IPC/JEDEC J-STD-020)
ESD	Human Body Model	Class 1C (per JEDEC standard JEDEC JS-001-2012)	
	Machine Model	Class A (per EIA/JEDEC standard EIA/JESD22-A115)	
IC Latch-Up Test		Class I, Level A (per JESD78)	
RoHS Compliant		Yes	

- † Qualification standards can be found at International Rectifier's web site <http://www.irf.com/>
- †† Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information.
- ††† Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information.