Enpirion® Power Datasheet
ES1022SI Adjustable Quad Sequencer

Device Is Discontinued And No Longer Available

The ES1022SI IC provides four delay adjustable sequenced outputs while monitoring an input voltage all with a minimum of external components.

High performance DSP, FPGA, µP and various sub-systems require input power sequencing for proper functionality at initial power up and the ES1022SI provides this function while monitoring the distributed voltage for over and undervoltage compliance.

This IC operates over the +3.3V to +24V nominal voltage range. It has a user adjustable time from UV and OV voltage compliance to sequencing start via an external capacitor when in auto start mode and adjustable time delay to subsequent EN output signal via external resistors.

Additionally, the ES1022SI provides I/O for sequencing on and off operation (SEQ_EN) and for voltage window compliance reporting (FAULT) over the +3.3V to +24V nominal voltage range.

Easily daisy chained for more than 4 sequenced signals.

Altogether, the ES1022SI provides these adjustable features with a minimum of external BOM. See Figure 1 for typical implementation.

Features

- Adjustable Delay to Subsequent EN Signal
- Adjustable Delay to Sequence Auto Start
- Adjustable Distributed Voltage Monitoring
- Under and Overvoltage Adjustable Delay to Auto Start Sequence
- I/O Options: EN and SEQ_EN
- Voltage Compliance Fault Output
- Pb-Free Plus Anneal Available (RoHS Compliant)

Applications

- Power Supply Sequencing
- System Timing Function

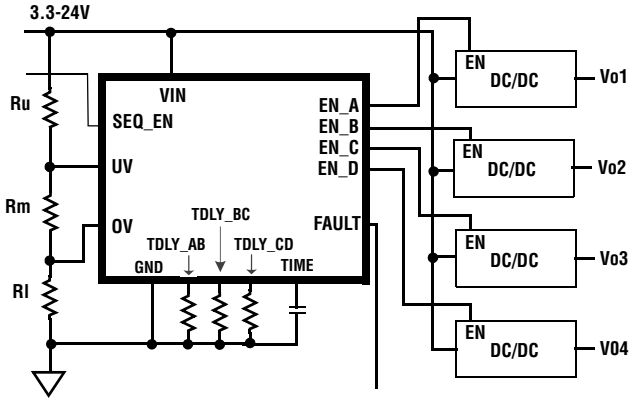


FIGURE 1. ES1022SI IMPLEMENTATION

101 Innovation Drive
San Jose, CA 95134
www.altera.com

Ordering Information

PART NUMBER (Note 1)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ES1022SI*	ES1022SI	-40 to +85	14 Ld SOIC	M14.15
EVB-ES1022SI	Evaluation Platform			

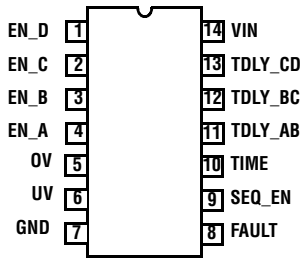
*Add "-T" suffix for tape and reel. Please refer to Packing and Marking Information: www.altera.com/support/reliability/packing/rel-packing-and-marking.html

NOTES:

1. Altera Enpirion Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Altera Enpirion Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pinout

ES1022SI
(14 LD SOIC)
TOP VIEW



Pin Descriptions

Pin Number	PIN NAME	FUNCTION DESCRIPTION
1	EN_D	EN output D. Active high open drain sequenced output. Sequenced on after EN_C and first output to sequence off. Pulls low with V_{IN} < 1V.
2	EN_C	EN output C. Active high open drain sequenced output. Sequenced on after EN_B and sequenced off after EN_D. Pulls low with V_{IN} < 1V.
3	EN_B	EN output B. Active high open drain sequenced output. Sequenced on after EN_A and sequenced off after EN_C. Pulls low with V_{IN} < 1V.
4	EN_A	EN output A. Active high open drain sequenced output. Sequenced on after CTIME period and sequenced off after EN_B. Pulls low with V_{IN} < 1V.
5	OV	The voltage on this pin must be under its 1.22V Vth or the four EN outputs will be immediately pulled down.
6	UV	The voltage on this pin must be over its 1.22V Vth or the four EN outputs will be immediately pulled down.
7	GND	IC ground.
8	FAULT	The V_{IN} voltage when not within the desired UV to OV window will cause FAULT to be released to be pulled high to a voltage equal to or less than V_{IN} via an external resistor.
9	SEQ_EN	This pin provides a sequence on signal input with a high input. Internally pulled high to ~2.4V.
10	TIME	This pin provides a 2.6µA current output so that an adjustable V_{IN} valid to sequencing on and off start delay period is created with a capacitor to ground.
11	TDLY_AB	A resistor connected from this pin to ground determines the time delay from EN_A being active to EN _B being active on turn-on and also going inactive on turn-off via the SEQ_EN input.
12	TDLY_BC	A resistor connected from this pin to ground determines the time delay from EN_B being active to EN _C being active on turn-on and also going inactive on turn-off via the SEQ_EN input.
13	TDLY_CD	A resistor connected from this pin to ground determines the time delay from EN_C being active to EN _D being active on turn-on and also going inactive on turn-off via the SEQ_EN input.
14	V_{IN}	IC Bias Pin Nominally 3.3V to 24V This pin requires a 1µF decoupling capacitor close to IC pin.

Absolute Maximum Ratings

V_{IN}, EN, FAULT . . . . . .27V, to -0.3V
TIME, TDLY_AB, TDLY_BC, TDLY_CD, UV, OV .+6V, to -0.3V
SEQ_EN. . . . . V_{IN}+0.3V, to -0.3V
EN Output Current 10mA

Operating Conditions

Temperature Range . . . . . .-40°C to +85°C
Supply Voltage Range (Nominal) . . . . . 3.3V to 24V

Thermal Information

Thermal Resistance (Typical, Note 2) . . . . . θ_{JA} (°C/W)
14 Ld SOIC 110
Maximum Junction Temperature (Plastic Package) +125°C
Maximum Storage Temperature Range . . . . . .-65°C to +150°C
Maximum Lead Temperature (Soldering 10s). . . . . +300°C
(SOIC Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:
2. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.

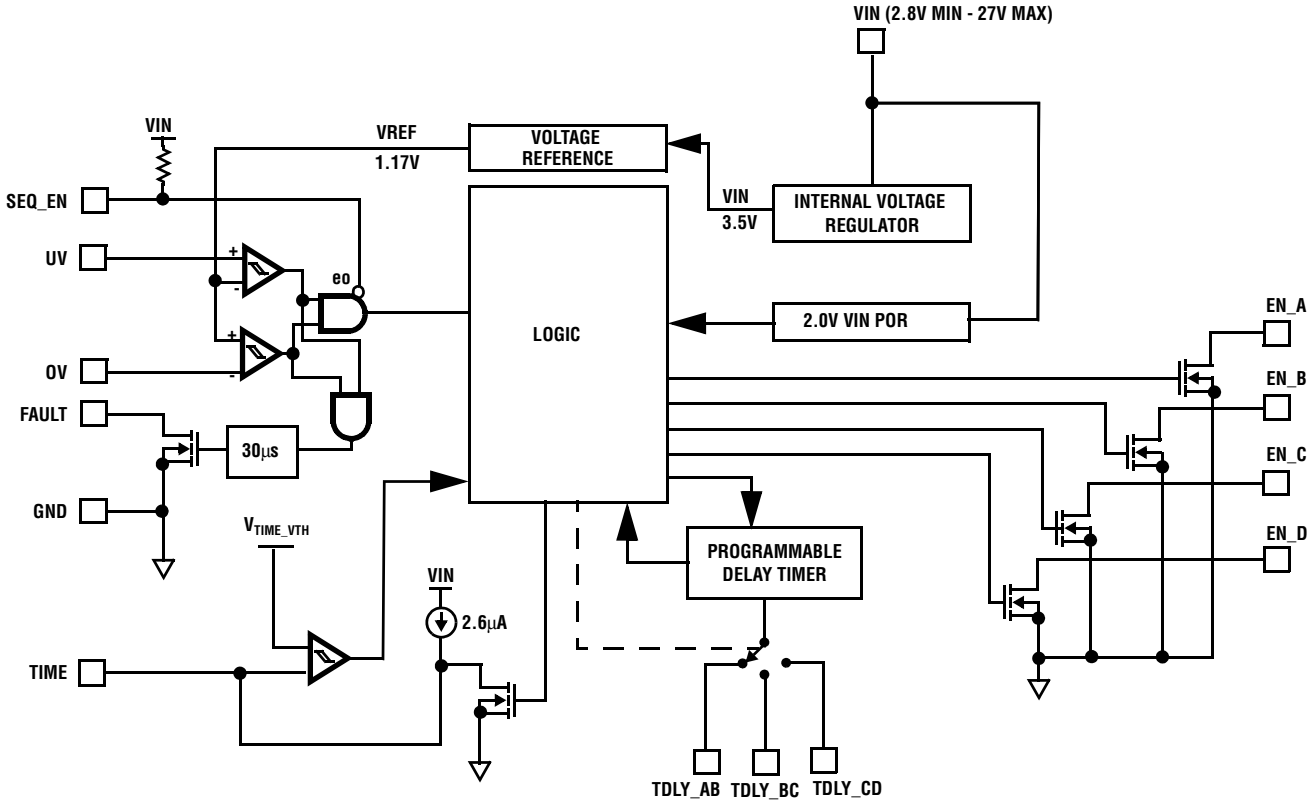
Electrical Specifications Nominal V_{IN} = 3.3V to +24V, T_A = T_J = -40°C to+85°C, Unless Otherwise Specified.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
UV AND OV INPUTS						
UV/OV Rising Threshold	V_{UVRvth}		1.16	1.21	1.28	V
UV/OV Falling Threshold	V_{UVFvth}		1.06	1.10	1.18	V
UV/OV Hysteresis	V_{UVhys}	V_{UVRvth} - V_{UVFvth}	-	104	-	mV
UV/OV Input Current	I_{UV}		-	10	-	nA
TIME, EN OUTPUTS						
TIME Pin Charging Current	I_{TIME}		-	2.6	-	µA
TIME Pin Threshold	V_{TIME_VTH}		1.9	2.0	2.25	V
Time from V_{IN} Valid to EN_A	$t_{VINSEQpd}$	SEQ_EN = high, C_{TIME} = open	-	30	-	µs
	$t_{VINSEQpd\_10}$	SEQ_EN = high, C_{TIME} = 10nF	-	7.7	-	ms
	$t_{VINSEQpd500}$	SEQ_EN = high, C_{TIME} = 500nF	-	435	-	ms
Time from V_{IN} Invalid to Shutdown	$t_{shutdown}$	UV or OV to simultaneous shutdown	-	-	1	µs
EN Output Resistance	R_{EN}	I_{EN} = 1mA	-	100	-	Ω
EN Output Low	Vol	I_{EN} = 1mA	-	0.1	-	V
EN Pull-down Current	I_{pulld}	EN = 1V	10	15	-	mA
Delay to Subsequent EN Turn-on/off	t_{del_120}	R_{TX} = 120kΩ	155	195	240	ms
	t_{del_3}	R_{TX} = 3kΩ	3.5	4.7	6	ms
	t_{del_0}	R_{TX} = 0Ω	-	0.5	-	ms
SEQUENCE EN AND FAULT I/O						
V_{IN} Valid to FAULT Low	t_{FLTL}		15	30	50	µs
V_{IN} Invalid to FAULT High	t_{FLTH}		-	0.5	-	µs
FAULT Pull-down Current		FAULT = 1V	10	15	-	mA
SEQ_EN Pull-up Voltage	V_{SEQ}	SEQ_EN open	-	2.4	-	V
SEQ_EN Low Threshold Voltage	Vil_{SEQ_EN}		-	-	0.3	V
SEQ_EN High Threshold Voltage	Vih_{SEQ_EN}		1.2	-	-	V
Delay to EN_A Deasserted	$t_{SEQ\_EN\_ENA}$	SEQ_EN low to EN_A low	-	0.2	1	µs

Electrical Specifications Nominal V_{IN} = 3.3V to +24V, T_A = T_J = -40°C to+85°C, Unless Otherwise Specified. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
BIAS						
IC Supply Current	$I_{VIN\_3.3V}$	V_{IN} = 3.3V	-	191	-	µA
	I_{VIN_12V}	V_{IN} = 12V	-	246	400	µA
	I_{VIN_24V}	V_{IN} = 24V	-	286	-	µA
V_{IN} Power On Reset	V_{IN_POR}	V_{IN} low to high	-	2.3	2.8	V

Functional Block Diagram



Functional Description

ES1022SI provides four delay adjustable sequenced outputs while monitoring a single distributed voltage in the nominal range of 3.3V to 24V for both under and overvoltage. Only when the voltage is in compliance will the ES1022SI initiate the pre-programmed A-B-C-D sequence of the EN outputs. Although this IC has a bias range of 3.3V to 24V it can monitor any voltage >1.22V via the external divider if a suitable bias voltage is otherwise provided.

During initial bias voltage (V_{IN}) application the ES1022SI EN outputs are held low once V_{IN} = 1V. Once V_{IN} > the V bias power on reset threshold (POR) of 2.8V, V_{IN} is constantly monitored for compliance via the input voltage resistor divider and the voltages on the UV and OV pins and reported by the FAULT output. Internally, voltage regulators generate 3.5V and 1.17V ±5% voltage rails for internal usage once V_{IN} > POR. Once UV > 1.22V and with the SEQ_EN pin high or open, the auto sequence of the four EN outputs begins as the TIME pin charges its external capacitor with a 2.6µA current source. The voltage on TIME is compared to the internal reference (V_{TIME_VTH}) comparator input and when greater than V_{TIME_VTH} the EN_A is released to go high via an external pull-up resistor or a pull-up in a DC/DC convertor EN input, for example. The time delay generated by the external capacitor is to assure continued voltage compliance within the programmed limits, as during this time any OV or UV condition will halt the start-up process. TIME cap is discharged once V_{TIME_VTH} is met.

Once EN_A is active (released high on the ES1022SI) a counter is started and using the resistor on TDLY_AB as a timing component a delay is generated before EN_B is activated. At this time, the counter is restarted using the resistor on TDLY_BC as its timing component for a separate timed delay until EN_C is activated. This process is repeated for the resistor on TDLY_CD to complete the A-B-C-D sequencing order of the EN outputs. At any time during sequencing if an OV or UV event is registered, all four EN outputs will immediately return to their low reset state. C_{TIME} is immediately discharged after initial ramp up thus waiting for subsequent voltage compliance to restart. Once sequencing is complete, any subsequently registered UV or OV event will trigger an immediate and simultaneous reset of all EN outputs.

On the ES1022SI, enabling of on or off sequencing can also be signaled via the SEQ_EN input pin once voltage compliance is met. Initially, the SEQ_EN pin should be held low and released when sequence start is desired. SEQ_EN is internally pulled high and sequencing is enabled unless it is pulled low. The on sequence of the EN outputs is as previously described. The off sequence is D off, then C off, then B off and finally A off. Once SEQ_EN is signaled low, the TIME cap is charged to 2V once again. Once this Vth is reached, EN_D transitions to its reset state and CTIM is discharged. A delay and subsequent sequence off is then determined by TDLY_CD resistor to EN_C. Likewise, a delay to EN_B and then EN_A turn-off is determined by TDLY_BC and TDLY_AB resistor values respectively.

The FAULT signal is always valid at operational voltages and can be used as justification for SEQ_EN release or even controlled with an RC timer for sequence on.

Programming the Under and Overvoltage Limits

When choosing resistors for the divider remember to keep the current through the string bounded by power loss at the top end and noise immunity at the bottom end. For most applications, total divider resistance in the 10kΩ to1000kΩ range is advisable with high precision resistors being used to reduce monitoring error. Although for the ES1022SI, two dividers of two resistors each can be employed to separately monitor the OV and UV levels for the V_{IN} voltage. We will discuss using a single three resistor string for monitoring the V_{IN} voltage, referencing Figure 1. In the three resistor divider string with Ru (upper), Rm (middle) and Rl (lower), the ratios of each in combination to the other two is balanced to achieve the desired UV and OV trip levels. Although this IC has a bias range of 3.3V to 24V, it can monitor any voltage >1.22V.

The ratio of the desired overvoltage trip point to the internal reference is equal to the ratio of the two upper resistors to the lowest (gnd connected) resistor.

The ratio of the desired undervoltage trip point to the internal reference voltage is equal to the ratio of the uppermost (voltage connected) resistor to the lower two resistors.

These assumptions are true for both rising (turn-on) or falling (shutdown) voltages.

The following is a practical example worked out. For detailed equations on how to perform this operation for a given supply requirement please see the next section.

1. Determine if turn-on or shutdown limits are preferred. In this example, we will determine the resistor values based on the shutdown limits.
2. Establish lower and upper trip level: 12V ±10% or 13.2V (OV) and 10.8V (UV)
3. Establish total resistor string value: 100kΩ, Ir = divider current
4. (Rm+Rl) x Ir = 1.1V @ UV and Rl x Ir = 1.2V @ OV
5. Rm+Rl = 1.1V/Ir @ UV = Rm+Rl = 1.1V/(10.8V/100kΩ) = 10.370kΩ
6. Rl = 1.2V/Ir @ OV = Rl = 1.2V/(13.2V/100kΩ) = 9.242kΩ
7. Rm = 10.370kΩ - 9.242kΩ = 1.128kΩ
8. Ru = 100kΩ - 10.370kΩ = 89.630kΩ
9. Choose standard value resistors that most closely approximate these ideal values. Choosing a different total divider resistance value may yield a more ideal ratio with available resistor's values.

In our example, with the closest standard values of Ru = 90.9kΩ, Rm = 1.13kΩ and Rl = 9.31kΩ, the nominal UV falling and OV rising will be at 10.9V and 13.3V respectively.

Programming the EN Output Delays

The delay timing between the four sequenced EN outputs are programmed with four external passive components. The delay from SEQ_EN being valid to EN_A is determined by the value of the capacitor on the TIME pin to GND. The external TIME pin capacitor is charged with a 2.6µA current source. Once the voltage on TIME is charged up to the internal

reference voltage, (V_{TIME_VTH}) the EN_A output is released out of its reset state. The capacitor value for a desired delay (±10%) to EN_A once V_{IN} and SEQ_EN where applicable has been satisfied is determined by:

$C_{TIME} = t_{VINSEQpd}/770k\Omega$

Once EN_A reaches V_{TIME_VTH}, the TIME pin is pulled low in preparation for a sequenced off signal via SEQ_EN. At this time, the sequencing of the subsequent outputs is started. EN_B is released out of reset after a programmable time, then EN_C, then EN_D, all with their own programmed delay times.

The subsequent delay times are programmed with a single external resistor for each EN output providing maximum flexibility to the designer through the choice of the resistor value connected from TDLY_AB, TDLY_BC and TDLY_CD pins to GND. The resistor values determine the charge and discharge rate of an internal capacitor comprising an RC time constant for an oscillator whose output is fed into a counter generating the timing delay to EN output sequencing.

The R_{TX} value for a given delay time is defined as:

$R_{TX} = t_{del}/1667nF$

An Advanced Tutorial on Setting UV and OV Levels

This section discusses in additional detail the nuances of setting the UV and OV levels, providing more insight into the ES1022SI than the earlier text.

The following equation set can alternatively be used to work out ideal values for a 3 resistor divider string of Ru, Rm and Rl. These equations assume that V_{REF} is the center point between V_{UVRvth} and V_{UVFvth} (i.e. $(V_{UVRvth} + V_{UVFvth})/2 = 1.17V$), Iload is the load current in the resistor string (i.e. $V_{IN}/(Ru + Rm + Rl)$), V_{IN} is the nominal input voltage and Vtol is the acceptable voltage tolerance, such that the UV and OV thresholds are centered at V_{IN} ± Vtol. The actual acceptable voltage window will also be affected by the hysteresis at the UV and OV pins. This hysteresis is amplified by the resistor string such that the hysteresis at the top of the string is:

$Vhys = V_{UVhys} \times V_{OUT}/V_{REF}$

This means that the V_{IN} ± Vtol thresholds will exhibit hysteresis resulting in thresholds of V_{IN} + Vtol ± Vhys/2 and V_{IN} - Vtol ± Vhys/2.

There is a window between the V_{IN} rising UV threshold and the V_{IN} falling OV threshold where the input level is guaranteed not to be detected as a fault. This window exists between the limits V_{IN} ± (Vtol - Vhys/2). There is an extension of this window in each direction up to V_{IN} ± (Vtol + Vhys/2), where the voltage may or may not be detected as a fault, depending on the direction from which it is approached. These two equations may be used to determine the required value of Vtol for a given system. For example, if V_{IN} is 12V, Vhys = (0.1 x 12)/1.17 = 1.03V. If V_{IN} must remain within 12V ± 1.5V, Vtol = 1.5 - 1.03/2 = 0.99V. This will give a window of 12 ±0.48V where the system is guaranteed not to be in fault and a limit of 12 ±1.5V beyond which the system is guaranteed to be in fault.

It is wise to check both these voltages, for if the latter is made to tight, the former will cease to exist. This point comes when Vtol < Vhys/2 and results from the fact that the acceptable window for the OV pin no longer aligns with the acceptable window for the UV pin. In this case, the application will have to be changed such that UV and OV are provided separate resistor strings. In this case, the UV and OV thresholds can be individually controlled by adjusting the relevant divider.

The previous example will give voltage thresholds of:

with V_{IN} rising
UVr = V_{IN} - Vtol + Vhys/2 = 11.5V and
OVr = V_{IN} + Vtol + Vhys/2 = 13.5V

with V_{IN} falling
Ovf = V_{IN} + Vtol - Vhys/2 = 12.5V and
UVf = V_{IN} - Vtol - Vhys/2 = 10.5V.

So with a single three resistor string, the resistor values can be calculated as:

Rl = (V_{REF}/Iload) (1 - Vtol/V_{IN})
Rm = 2(V_{REF} x Vtol)/(V_{IN} x Iload)
Ru = 1/Iload x (V_{IN} - V_{REF} (1+Vtol/V_{IN}))

For the above example, with Vtol = 0.99V, assuming a 100µA Iload at V_{IN} = 12V:

Rl = 10.7kΩ
Rm = 1.9kΩ
Ru = 107.3kΩ

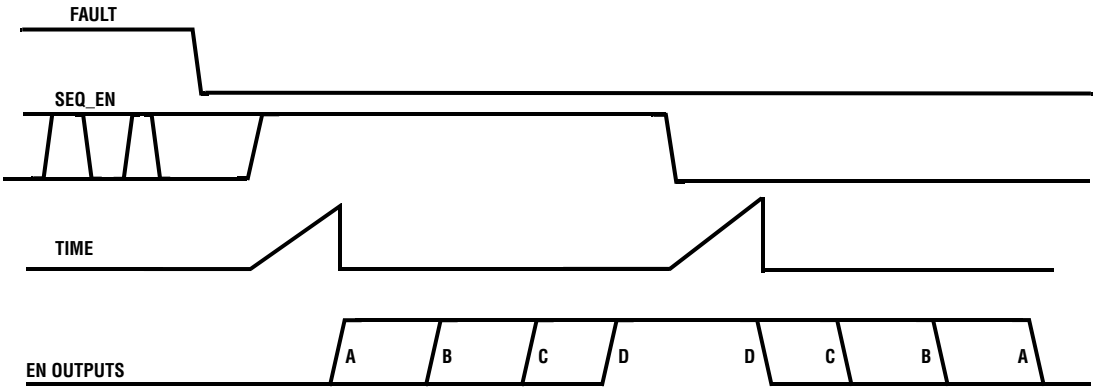


FIGURE 2. ES1022SI OPERATIONAL DIAGRAM

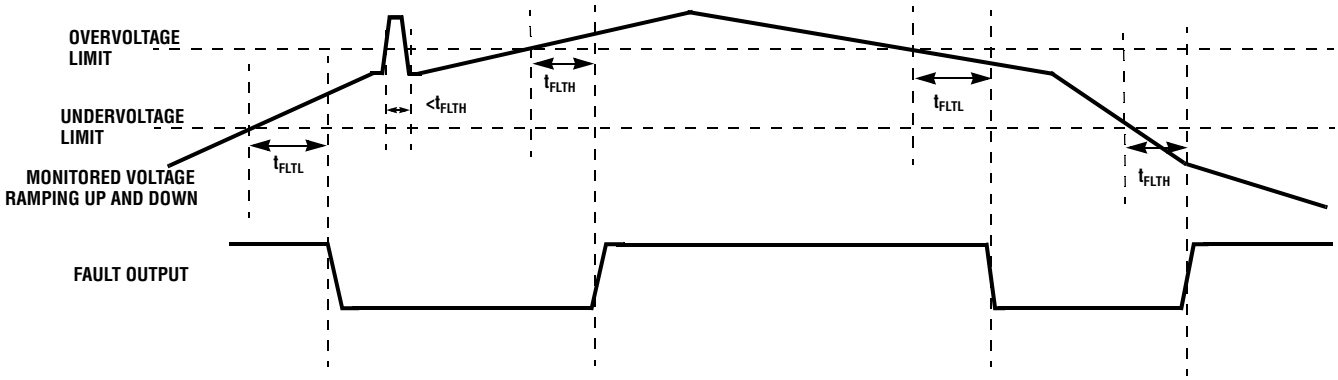


FIGURE 3. ES1022SI FAULT OPERATIONAL DIAGRAM

Typical Performance Curves

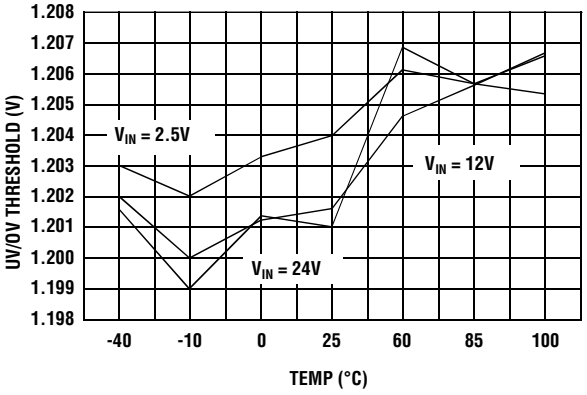


FIGURE 4. UV/OV RISING THRESHOLD

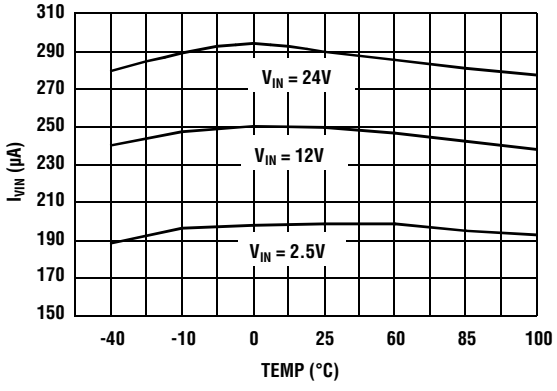


FIGURE 5. V_{IN} CURRENT

Applications Usage

Using the EVB-ES1022SI Platform

The EVB-ES1022SI platform is the primary evaluation board for this family of sequencers. See Figure 15 for photograph and schematic. The evaluation board is shipped with an ES1022SI mounted in the left position and with the other device variants loose packed. In the following discussion, test points names are **bold** on initial occurrence for identification.

The $\mathbf{V_{IN}}$ test point is the chip bias and can be biased from 3.3V to 24V. The **VHI** test point is for the EN and **FAULT** pull-up voltage which are limited to a maximum of 24V independent of V_{IN}. The UV/OV resistor divider is set so that a nominal 12V on the **VMONITOR** test point is compliant and with a rising OV set at 13.2V and a falling UV set at 10.7V. These three test points (V_{IN},VHI and VMONITOR) are brought out separately for maximum flexibility in evaluation.

VMONITOR ramping up and down through the UV and OV levels will result in the FAULT output signaling the out of bound conditions by being released to pull high to the VHI voltage as shown in Figures 6 and 7.

Once the voltage monitoring FAULT is resolved and where applicable, the **SEQ_EN** is satisfied, sequencing of the EN_X outputs begins. When sequence enabled the **EN_A**, **EN_B**, **EN_C** and lastly **EN_D** are asserted in that order and when SEQ_EN is disabled the order is reversed. See Figures 8 and 9 demonstrating the sequenced enabling and disabling of the EN outputs. The timing between EN outputs is set by the resistor values on the TDLY_AB, TDLY_BC, TDLY_CD pins as shown. Figure 10 illustrates the timing from either SEQ_EN and/or VMONITOR being valid to EN_A being asserted with a 10nF TIME capacitor. Figure 11 shows that EN_X outputs are pulled low even before V_{IN} = 1V. This is critical to ensure that a false EN is not signaled. Figure 12 shows the time from SEQ_EN transition with the voltage ramping across the TIME capacitor to TIME Vth being met. This results in the immediate pull down of the TIME pin and simultaneous EN_A enabling.

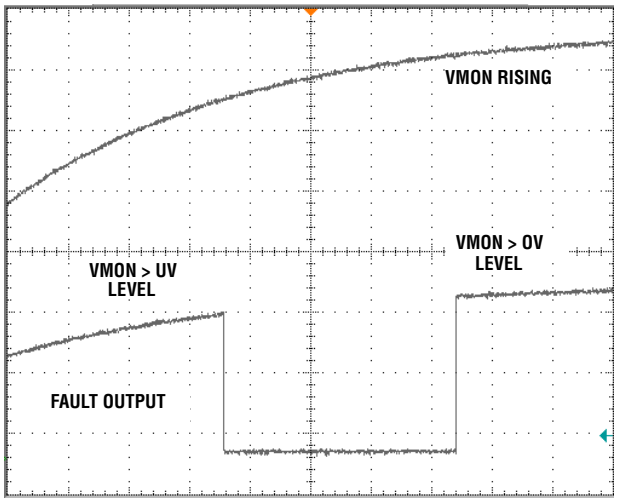


FIGURE 6. VMONITOR RISING TO FAULT

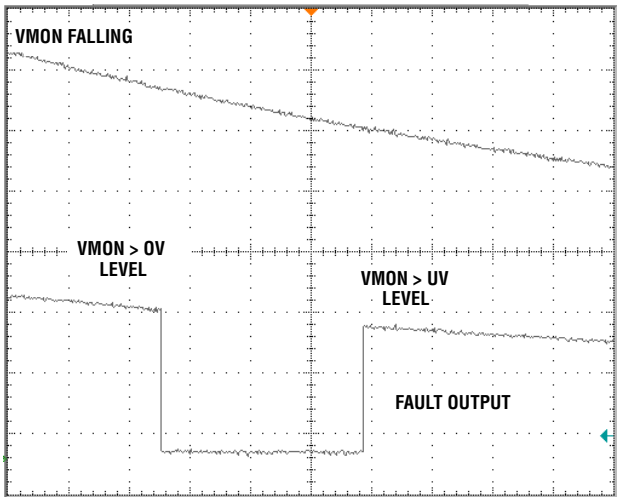


FIGURE 7. VMONITOR FALLING TO FAULT

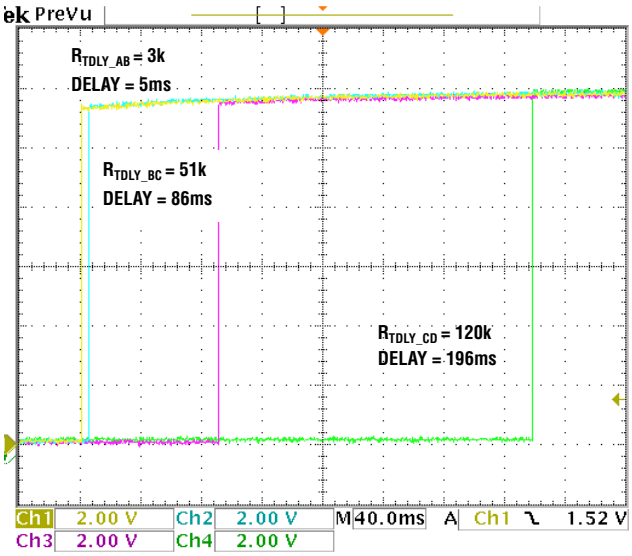


FIGURE 8. EN_X TO EN_X ENABLING

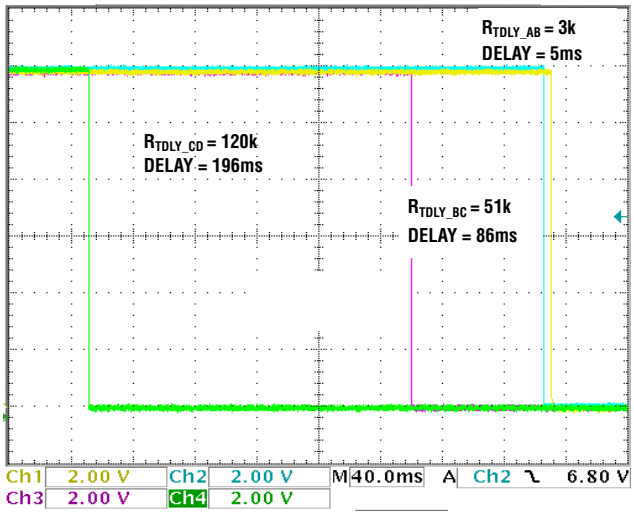


FIGURE 9. EN_X TO EN_X DISABLING

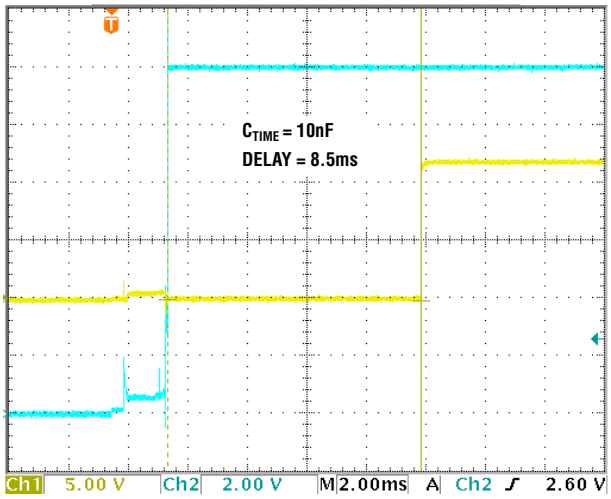


FIGURE 10. V_{IN}/SEQ_EN VALID TO EN_A

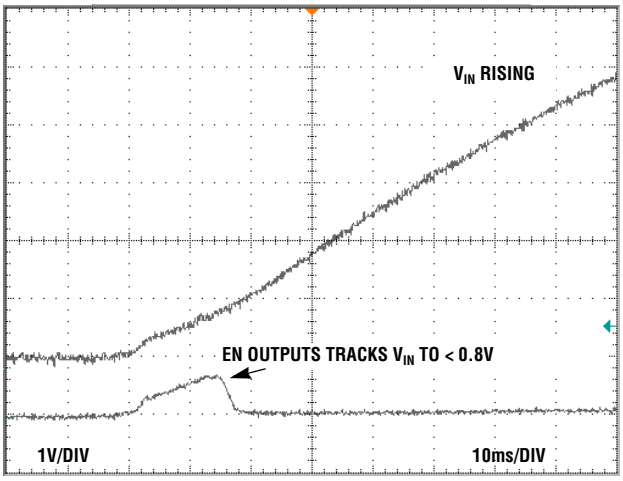


FIGURE 11. EN AS V_{IN} RISES

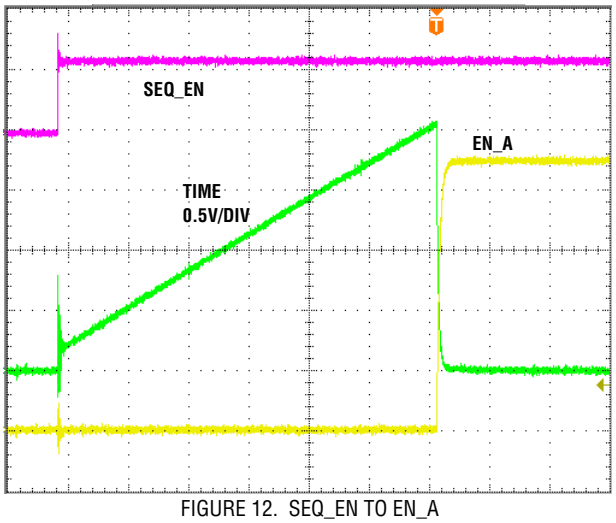


FIGURE 12. SEQ_EN TO EN_A

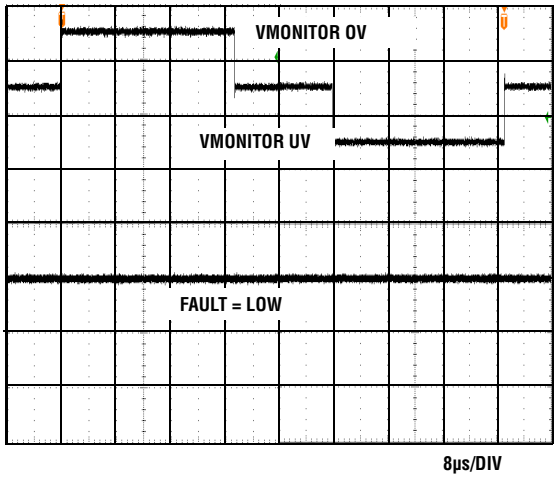


FIGURE 13. OV AND UV TRANSIENT IMMUNITY

Application Recommendations

Best practices V_{IN} decoupling is required, a 1µF capacitor is recommended.

Coupling from the EN_X pins to the sensitive UV and OV pins can cause false OV/UV events to be detected. This is relevant due to the EN_A and OV pins being adjacent. This coupling can be reduced by adding a ground trace between UV and the EN/FAULT signals, as shown in Figure 14. The PCB traces on OV and UV should be kept as small as practical and the EN_X and FAULT traces should ideally not be routed under/over the OV/UV traces on different PCB layers unless there is a ground or power plane in between. Other methods that can be used to eliminate this issue are by reducing the value of the resistors in the network connected to UV and OV (R2, R3, R5 in Figure 15) or by adding small decoupling capacitors to OV and UV (C2 and C7 in Figure 15). Both these methods act to reduce the AC impedance at the nodes, although the latter method acts to filter the signals which will also cause an increase in the time that a UV/OV fault takes to be detected.

When the ES1022SI is implemented on a hot swappable card that is plugged into an always powered passive back plane an RC filter is required on the V_{IN} pin to prevent a high dv/dt transient. With the already existing 1µF decoupling capacitor the addition of a small series R (>50Ω) to provide a time constant >50µs is all that is necessary.

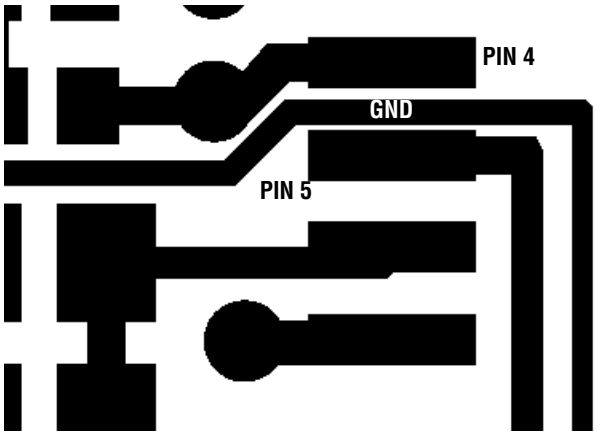
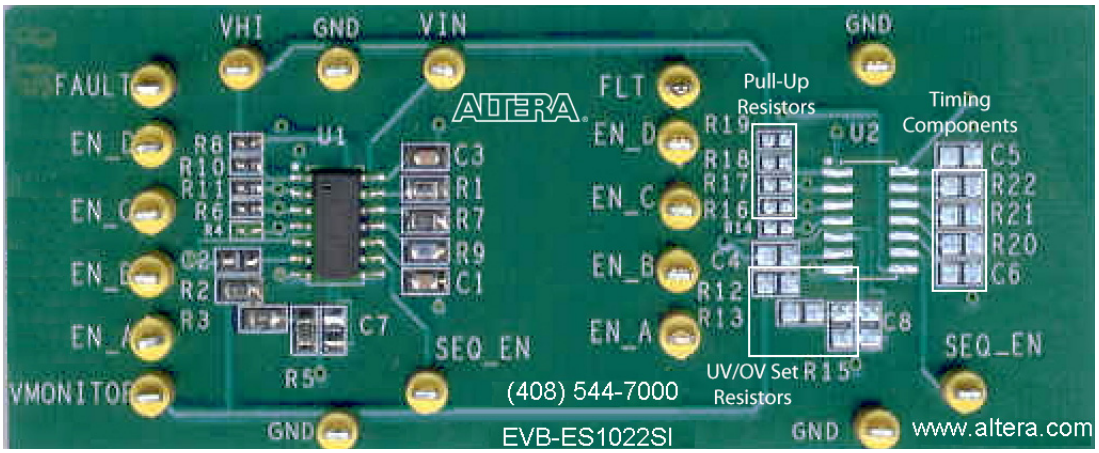


FIGURE 14. LAYOUT DETAIL OF GND BETWEEN PINS 4 AND 5



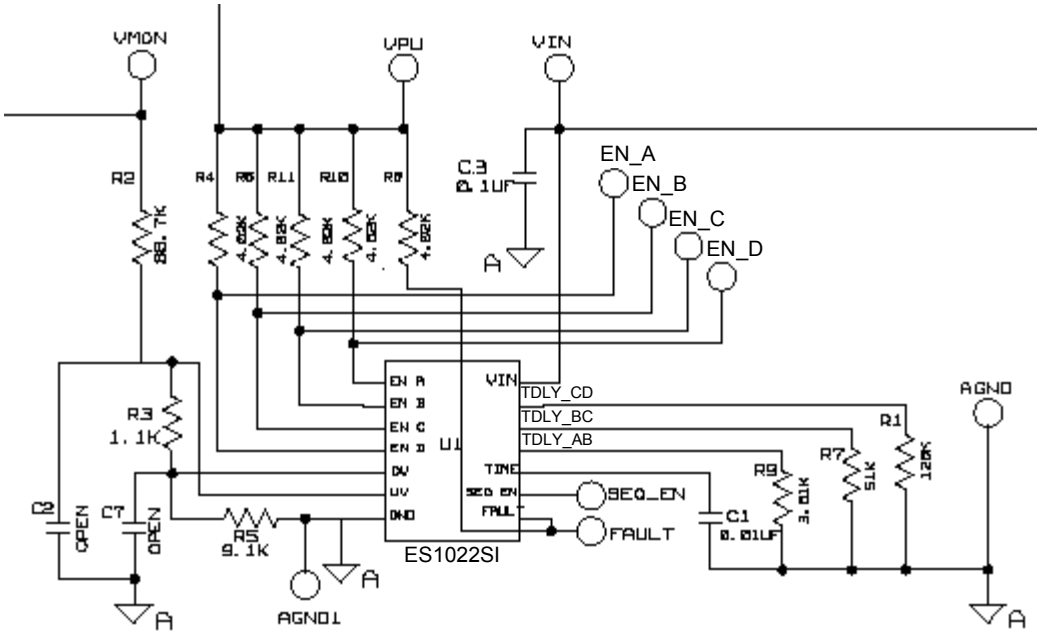


FIGURE 15. EVB-ES1022SI PHOTOGRAPH AND SCHEMATIC OF LEFT CHANNEL

TABLE 1. EVB-ES1022SI LEFT CHANNEL COMPONENT LISTING

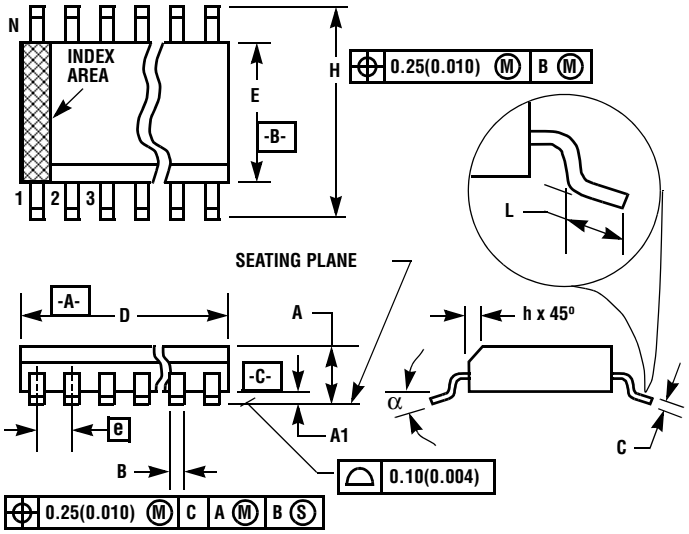
COMPONENT DESIGNATOR	COMPONENT FUNCTION	COMPONENT DESCRIPTION
U1	ES1022SI, Quad Under/Overvoltage Sequencer	Altera Enpirion, ES1022SI, Quad Under/Overvoltage Sequencer
R3	UV Resistor for Divider String	1.1kΩ1%, 0603
R2	VMONITOR Resistor for Divider String	88.7kΩ1%, 0603
R5	OV Resistor for Divider String	9.1kΩ1%, 0603
C1	C_{TIME} Sets Delay from Sequence Start to First EN	0.01µF, 0603
R1	R_{TDLY_CD} Sets Delay from Third to Fourth EN	120kΩ1%, 0603
R9	R_{TDLY_AB} Sets Delay from First to Second EN	3.01kΩ1%, 0603
R7	R_{TDLY_BC} Sets Delay from Second to Third EN	51kΩ1%, 0603
R4, R6, R8, R10, R11	EN_X and FAULT Pull-up Resistors	4kΩ10%, 0402
C3	Decoupling Capacitor	1µF, 0603

Revision History

The table lists the revision history for this document.

DATE	REVISION	CHANGE
May, 2014	A	Initial release.
August 2020	B	Device Discontinued

Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M14.15 (JEDEC MS-012-AB ISSUE C)

14 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.3367	0.3444	8.55	8.75	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	14		14		7
a	0°	8°	0°	8°	-

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