TDINV3500P100: 3.5 kW Inverter Evaluation Board

Introduction

The TDINV3500P100 3.5kW inverter kit provides an easy way to evaluate the performance advantages of GaN power FETs in various inverter applications, such as solar and uninterruptible power supplies (UPS). The kit provides the main features of a single-phase inverter in a proven, functional configuration, operating at or above 100kHz. At the core of the inverter are four TP90H180PS 180mΩ GaN FETs configured as a full bridge. These are tightly coupled to gate-drive circuits on a board which also includes flexible microcontroller options and convenient communication connection to a PC. The switch-mode power signals are filtered to provide a pure sinusoidal output. For more information and the complete design files, please visit https://www.transphormusa.com/en/evaluation-kit/tdinv3500P100-kit/.

The TDINV3500P100-**KIT is for evaluation purposes only.**

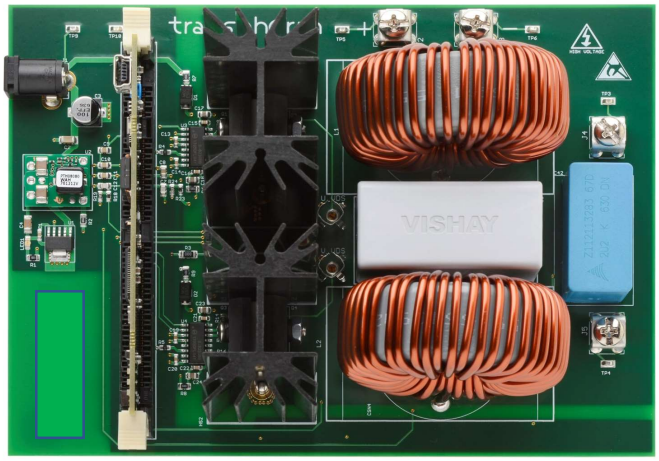


Figure 1. TDINV3500P100 inverter evaluation board

Warning

This evaluation board is intended to demonstrate GaN FET technology and is for demonstration purposes only and no guarantees are made for standards compliance.

There are areas of this evaluation board that have exposed access to hazardous high voltage levels. Exercise caution to avoid contact with those voltages. Also note that the evaluation board may retain high voltage temporarily after input power has been removed. Exercise caution when handling.

When testing converters on an evaluation board, ensure adequate cooling. Apply cooling air with a fan blowing across the converter or across a heatsink attached to the converter. Monitor the converter temperature to ensure it does not exceed the maximum rated per the datasheet specification.

The control portion of the circuit is designed around the popular C2000™ family of microcontrollers from Texas Instruments (TI). The source code is available along with related support information directly from TI. In addition to this general resource, Transphorm provides original firmware which comes loaded in flash on the microcontroller. The source code, configured as a complete project, is available at https://www.transphormusa.com/en/evaluation-kit/tdinv3500P100-kit/. This project is a convenient starting point for further developments. The microcontroller itself resides on a small, removable control card, supplied by TI, so that different C2000 devices may be used if desired. The schematic for the TDINV3500P100 circuit board is provided at the end of this user guide document, as well in the design files.

The TDINV3500P100-KIT includes:

- TDINV3500P100 single-phase inverter assembly
- Texas Instruments F28035 control card
- 12V power supply with U.S. adaptor

Complete design files, firmware files and support documentation can be found online at https://www.transphormusa.com/en/evaluation-kit/tdinv3500p100-kit/.

TDINV3500P100 input/output specifications

- High-voltage input: **750V_{DC} max**
- Auxiliary supply (J1): **12V_{CC}**
- Input Voltage: **0V_{DC} - 750V_{DC}**
- Output Voltage: **V_{DC} / √2V_{RMS} at 50/60Hz [1], up to 3500W**
- PWM frequency: **50kHz - 150kHz [2]**
- Power dissipation in the GaN FET is limited by the maximum junction temperature. Refer to the TP90H180PS datasheet

[1] The output frequency may be changed in the software; as delivered it is 60Hz

[2] The switching frequency may be changed in the software; as delivered it is 100kHz

Circuit description

Refer to Figure 2 for a block diagram of the inverter circuit. A detailed schematic is available in the design files.

The TDINV3500P100 inverter is a simple full-bridge inverter. Two GaN half-bridges are driven with pulse-width modulated (PWM) command signals to create the sinusoidal varying output. The output filter largely removes the switching frequency, leaving the 50/60Hz fundamental sinusoid. The high-frequency (100kHz+) PWM signals are generated by the TI microcontroller and connected directly to high speed, high voltage gate drivers. A connection for external communication to the microcontroller is provided by an isolated USB interface. Except for the high-voltage supply for the power stage, all required voltages for the control circuitry are derived from one 12V input.

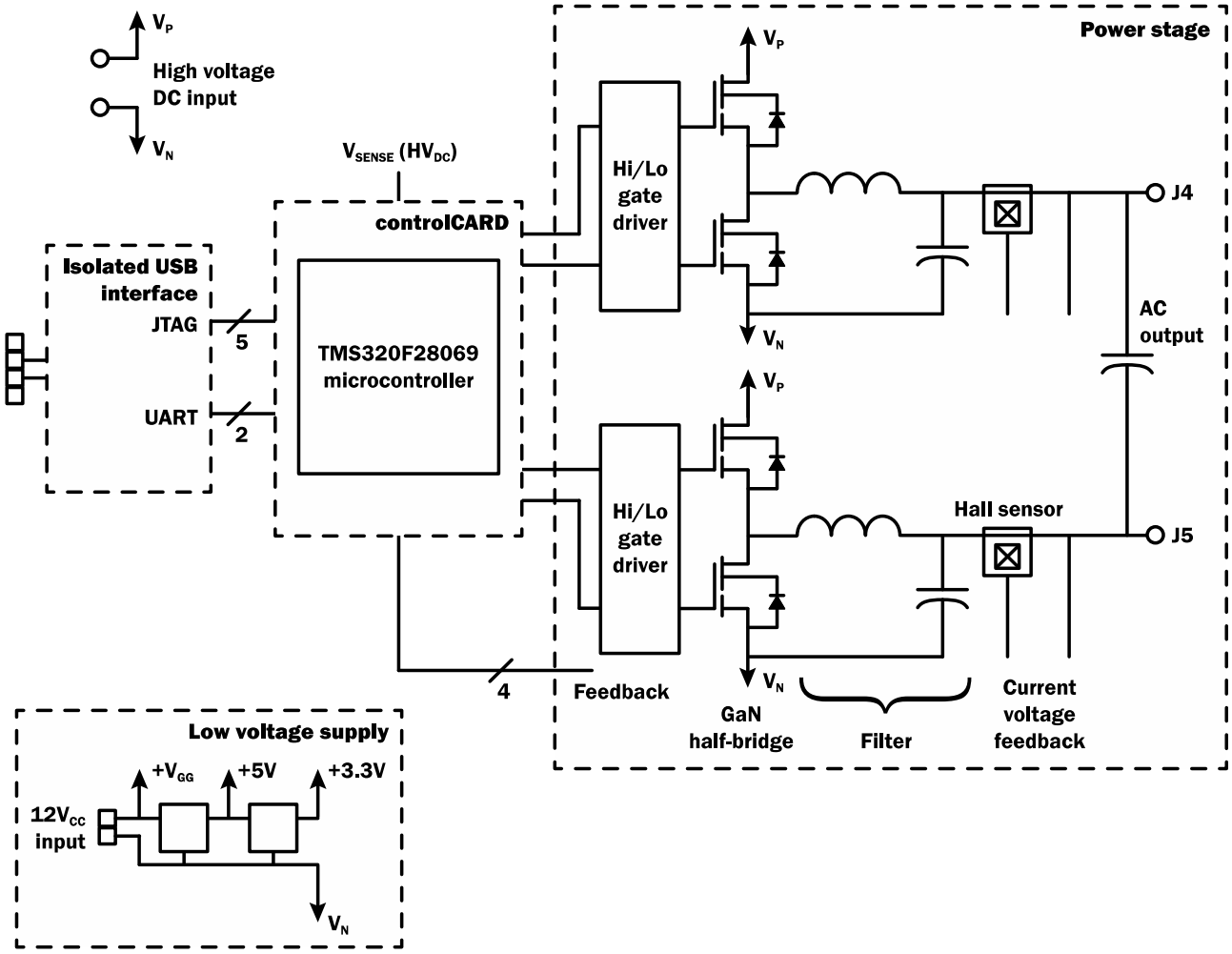


Figure 2. Circuit block diagram

The inverter takes advantage of diode-free operation, in which the freewheeling current is carried by the GaN FETs themselves due to their bi-directional capability, without the need of additional freewheeling diodes. For minimum conduction loss, the gates of the FETs are enhanced while they carry the freewheeling current. The high and low-side V_{GS} waveforms are therefore pairs of non-overlapping pulses, as illustrated in Figure 3 below.

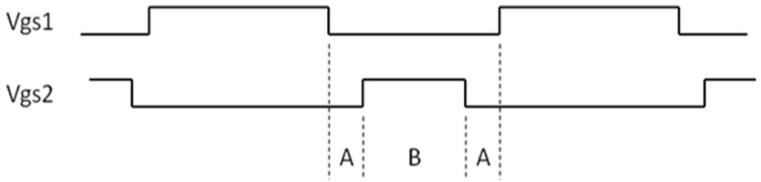


Figure 3. Non-overlapping gate-drive pulse; A is a dead time set in the firmware

Gate drivers

High-voltage integrated drivers supply the gate-drive signals for the high and low-side GaN FETs. These are 2500V isolation drivers (Silicon Labs Si823x family), specifically chosen for high-speed operation without automatic dead time insertion. The dead time between turn-off of one GaN FET in a half-bridge and turn-on of its mate is set in the firmware.

Dead time control

The required form of the gate-drive signals is shown in Figure 3. The times marked A are the dead times when neither transistor is driven on. The dead time must be greater than zero to avoid shoot-through currents. The Si8230 gate drive chip ensures a minimum dead time based on the value of resistor R24, connected to the AC input. The dead time in ns is equal to the resistance in kΩ x 10, so the default value of 12k corresponds to 120ns. This will add to any dead time already present in the input signals. The on-board pulse generator circuit; for example, creates dead times of about 100ns (see Figure 6). The resulting dead time at the gate pins of Q1 and Q2 is about 100ns. Either shorting or removing R4, R5 will reduce the dead time to 60ns.

Output filter

A simple filter on the output (L1, L2) attenuates the switching frequency, producing a clean sinusoidal waveform for output connections in terminals J4 and J5. The filter inductors and capacitors used on the demo board were chosen to provide the optional combination of benefits: low loss, good attenuation of the switching frequency, and small size. Consult the schematic and/or bill of materials to verify values; but in general, the cutoff frequency will be around 5kHz - 10kHz to accommodate 100Hz switching. The inductors have powder cores with relatively low permeability (60-90) and soft saturation characteristics. The inductors and/or capacitors can be changed to evaluate different filter designs.

Current sensing

Hall sensors U5 and U6 provide linear current feedback to the microcontroller. These signals are used to control output power flow, to protect against over current. Note that these are placed at an intermediate point of the output filter. Refer to the bill of materials on page 7 to confirm the sensor part numbers, but typical would be the Allegro ACS723-20A sensor, which has a ±40A range (100mV/A). These parts are pin-compatible with a ±5A and ±30A versions of ACS723, should lower ranges be desired. Note also that resistor dividers scale the 5V outputs for the 3V range of the A/D.

Communication

Communication between the microcontroller and a computer is accomplished with a mini USB cable to a JTAG microcontroller interface.

Control card

The microcontroller resides on a removable card, which inserts in a DIM100 socket on the inverter PCB. The socket can accept many of the C2000 series control cards from Texas Instruments. The TMDSCNCD28035ISO Piccolo control card supplied with the kit provides capability to experiment with a wide variety of modulation and control algorithms. It comes loaded with firmware to allow immediate, out-of-the-box, operation. Should the user wish to use an alternative microcontroller family, an appropriate control card can be designed to insert into the DIM100 socket.

Heatsink

The two TO-220 GaN FETs on each half-bridge are mounted on a common heatsink. The heatsink is adequate for 3500W operation with forced air flow. Even higher efficiency at high power may be achieved by minimizing the temperature rise. This may be accomplished with stronger airflow. Alternately the heatsinks could be replaced with larger and more effective ones.

Connections

Power for the AC output is derived from the high-voltage DC input. This will typically be a DC power supply with output voltage up to 750V_{DC}. A 22µF, low ESR film capacitor is provided as a bypass capacitor for the high voltage supply, along with several lower valued ceramic capacitors in parallel. This is not intended to provide significant energy storage. It is assumed that the power supply or preceding DC-DC stage contains adequate output capacitance.

The control, communication, and gate-drive circuits are all powered from a single 12V input (V_{CC}). The wall-plug adaptor provided generates the appropriate voltage (typically 12V) and power level.

Note that all signals on the board are referenced to the negative terminals of the high and low voltage supplies, which are tied together on the PCB. The heatsinks are also connected to the negative terminals of the supplies.

Powering on the board

- Refer to Figure 4. Insert the microcontroller card to the DIM100 socket before applying any power to the board.
- Before turning on the supply, connect the high-voltage power supply to the +/- inputs (J2 and J3). **DO NOT apply too much force to the J2 and J3 connectors, as excessive force may bend and/or crack the PCB.**
- If a load is to be used, connect the load to the output terminals (J4 and J5). **DO NOT apply too much force to the J4 and J5 connectors, as excessive force may bend and/or crack the PCB.**
- Insert the V_{CC} (12V) plug to jack J1. LED1 should illuminate, indicating power is applied to the 5V and 3.3V regulators. Depending on the specific control card used, one or more LEDs on the control card will also illuminate, indicating power is applied. A flashing LED indicates the firmware is executing.
- To use the pre-loaded firmware, no computer connection is required. If a computer connection is required for code modification, connect the USB cable from the computer to the USB connector on the microcontroller.
- Turn on the high-voltage power. The high-voltage supply may be raised gradually.

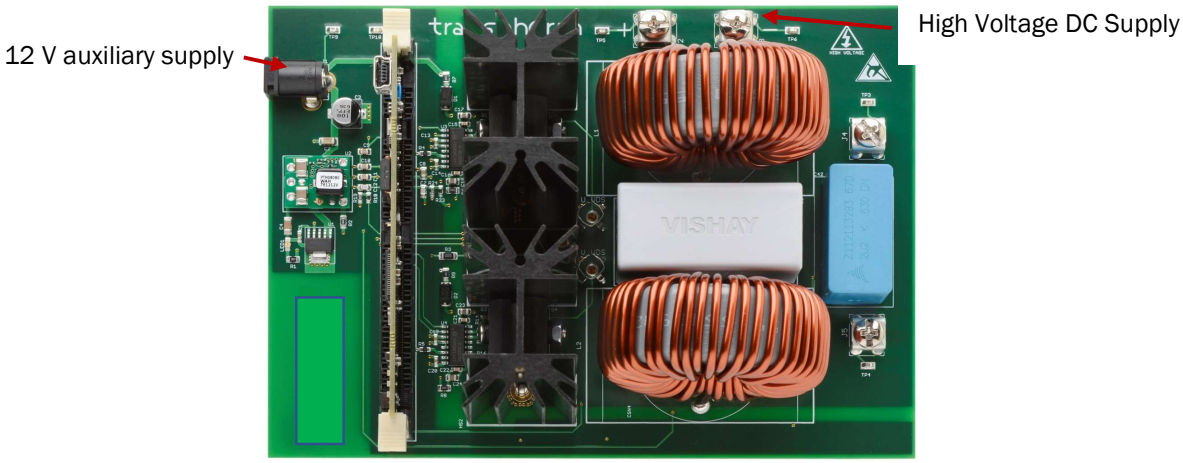


Figure 4. Connections

Powering off the board

1. Switch off high-voltage DC supply
2. Power off 12V aux supply

Test overview

Figure 5 shows typical waveforms. The negative terminal of the high-voltage supply is a convenient reference for the oscilloscope measurements, provided there are not multiple connections to earth ground.

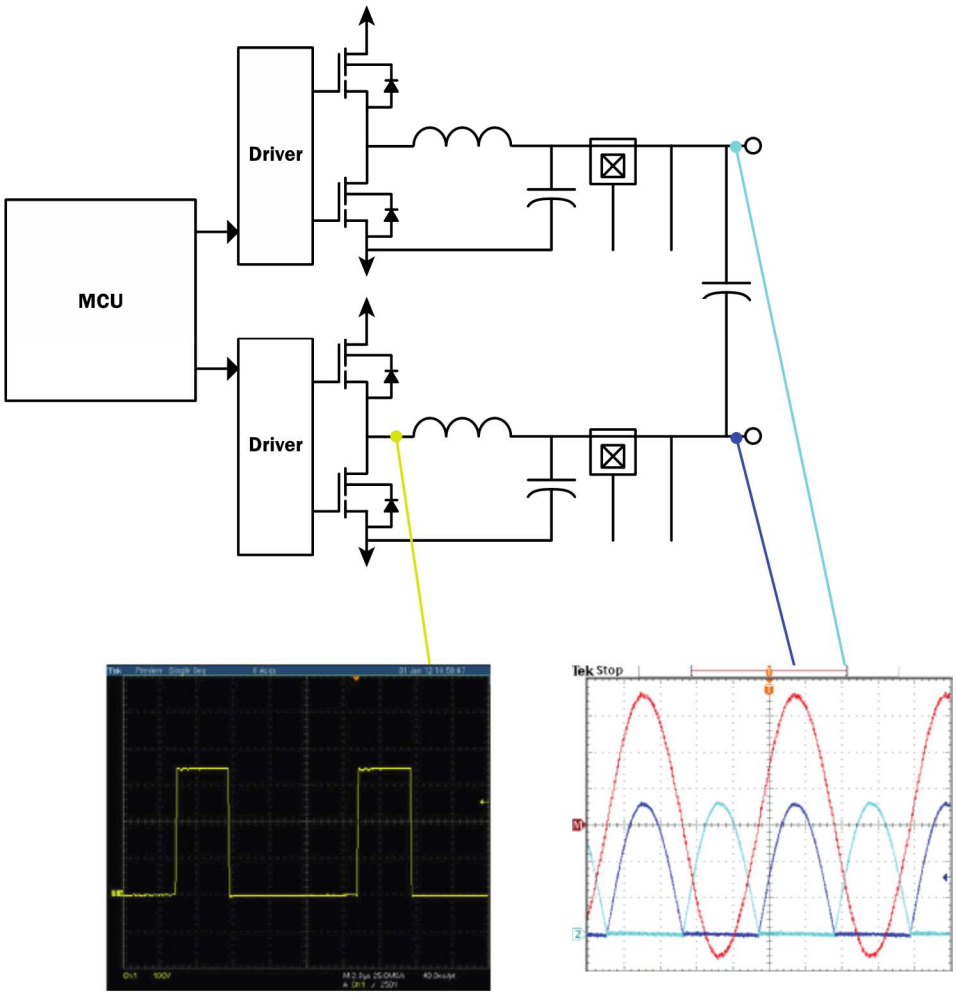


Figure 5. Typical waveforms

Typical efficiency results are shown in Figure 6. These data points correspond to efficiency measurements made in still air with 20 minutes' dwell at each power level. Input power from the 750V_{DC} source and output power to a resistive load were measured with a Yokogawa WT1800 power analyzer.

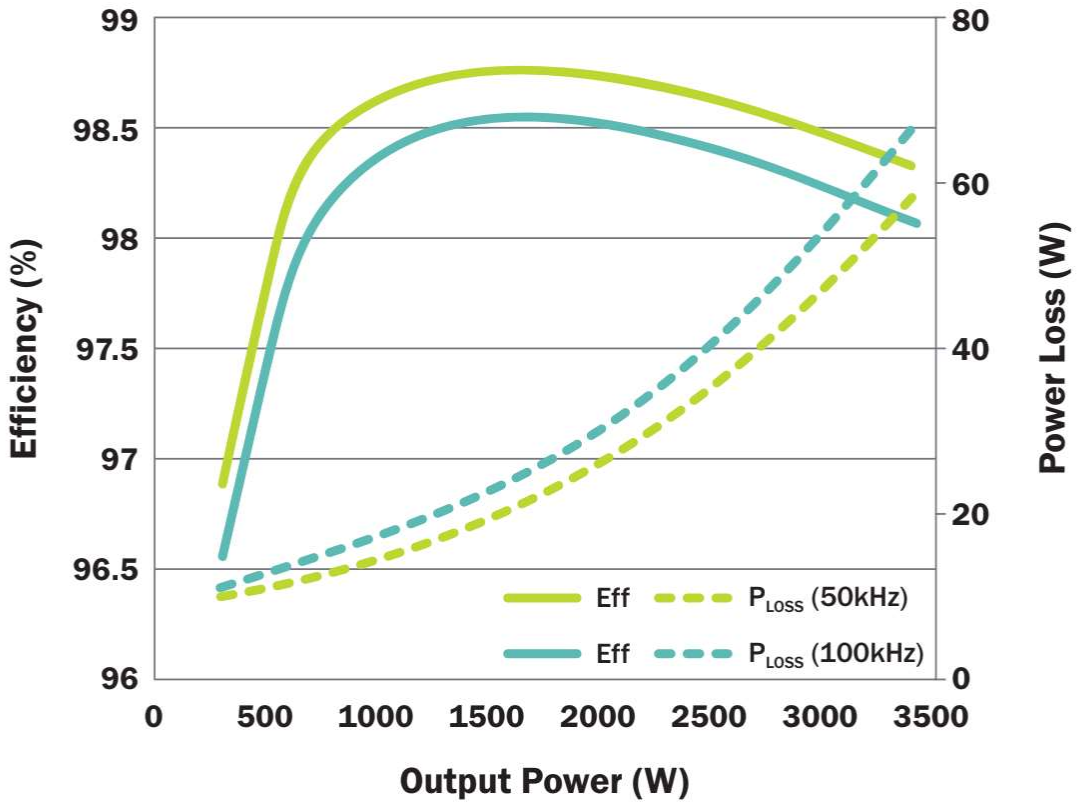


Figure 6. Typical efficiency: 730V_{DC} input, 500V_{AC} output

Design details

See Figures 7 and 8 for a detailed circuit schematic and Figure 9 for the PCB layers (also included in the design files). The parts list can be found in Table 1.

Table 1. TDINV3500P100 evaluation board bill of materials (BOM)

TDINV3500P100_0V2				
Qty	**Value**	**Device**	**Parts**	**Manf P/N**
2		529802B02500G_PINS	HS1, HS2	530002B02500G
4		KEYSTONE_7691	J2, J3, J4, J5	7691
1		LEDCHIP-LED0805	LED1	SML-211UTT86
1		PJ-002AH	J1	PJ-002AH
2		TEKTRONIX-PCB	U_VDS, V_VDS	131-4353-00

6		TESTPOINT-KEYSTONE5015	TP3, TP4, TP5, TP6, TP9, TP10	5015
11	.1u	C-USC0603	C1, C13, C14, C15, C16, C19, C20, C21, C22, C25, C27	06033C104JAT2A
4	.1u	C-USC0805	C8, C9, C10, C11	08053C104KAT2A
1	.1u DNI	C-USC2225K	C5	DNI
2	.1u	C-USC2225K	C43, C44	VJ2225Y104KXGAT
2	0	R-US_R0603	R54, R55	RCS06030000Z0EA
1	0	R-US_R1206	R3	ERJ-8GEY0R00V
8	1.6M	R-US_R1206	R33, R34, R35, R36, R37, R38, R39, R40	ERJ-8ENF1604V
1	1k	R-US_R0805	R1	ERJ-6GEYJ102V
2	1n	C-USC0805	C7, C12	CC0805KRX7R9BB102
2	1n DNI	C-USC0603	C26, C28	DNI
1	5uF	5uF	C42	C4AEOBU4500A11J
2	5.23k	R-US_R0603	R18, R23	ERJ-3EKF5231V
2	5.76k	R-US_R0603	R4, R5	ERJ-3EKF5761V
3	9.09k	R-US_R1206	R22, R27, R32	ERJ-8ENF9091V
4	10	R-US_R0603	R10, R12, R14, R16	RT0603DRE0710RL
4	10	R-US_R0805	R6, R7, R8, R9	ERJ-6GEYJ100V
4	10	R-US_R1206	R45, R46, R48, R49	ERJ-8ENF10R0V
2	10.2k	R-US_R0603	R19, R24	ERJ-3EKF1022V
4	10k	R-US_R0603	R11, R13, R15, R17	ERJ-3GEYJ103V
5	10k	R-US_R1206	R41, R42, R43, R44, R51	RC1206FR-0710KL
4	10n / 1200V	C-EUC1206	C34, C35, C38, C39	CS1206KKX7RCBB103
4	10u	C-EUC0805	C17, C18, C23, C24	CL21A106KAYNNNG
1	10u	C-USC1206	C4	CL31A106KAHNNNE
4	15 DNI	R-US_R1206	RSN1, RSN2, RSN3, RSN4	DNI
1	20uF	20uF	C6	MKP1848C62090JP4
4	22pF DNI	C-EUC1206	CSN1, CSN2, CSN3, CSN4	DNI
1	22u	C-USC1206	C2	CL31A226KAHNNNE

2	100nF	C-EUC1206	C31, C32	CL31F104MBCNNNC
1	100pF (10v)	C-USC0603	C33	885012006008
1	100u	PANASONICFPV	C3	EEE-FPE101XAP
4	120	FB0603	FB1, FB2, FB3, FB4	MMZ1608B121CTAH0
2	220pF	C-EUC1206	C29, C30	885012008014
1	348	R-US_R0805	R2	B32674D6225K
4	560k	R-US_R1206	R20, R21, R25, R26	RC1206FR-07560KL
4	680k	R-US_R1206	R28, R29, R30, R31	ERJ-P08J684V
2	ACS723	ACS723	U5, U6	ACS723LLCTR-20AB-T
1	DIM100_TICONTROLCARD	DIM100_TICONTROLCARD	CN1	5390213-1
2	DNI	R-US_R0603	R52, R53	DNI
2	ES1J	DIODE-DO-214AC	D1, D2	ES1J
1	OPA2350UA/2K5	OP_JC	U7	OPA2350UA/2K5
2	P11011_440UH	P11011_440UH	L1, L2	P11011
1	PTH08080WAH	PTH08080WAH	U2	PTH08080WAH
2	SI8230	SI8230	U3, U4	SI8230BB-D-IS
4	TP90H180PS	TP90H180PS	Q1, Q2, Q3, Q4	TP90H180PS
1	TPS79533	TPS79533	U1	TPS79533DCQR
2	Q1, Q3 insulator			SP2000-0.015-00-54
2	Q2, Q4 insulator			53-77-9G
2	Screw on TP90H180PS to heatsink	Screw on TP90H180PS to heatsink	Screw on TP90H180PS to heatsink	9902
2	Nut to mount TP90H180PS to heatsink	Nut to mount TP90H180PS to heatsink	Nut to mount TP90H180PS to heatsink	9600
4	Nylon washer shoulder in between screw/nut and TP90H180PS	Nylon washer shoulder in between screw/nut and TP90H180PS	Nylon washer shoulder in between screw/nut and TP90H180PS	3049
5	To place under PCB (5 locations: 4 each corner, 1 in the middle	To place under PCB (5 locations: 4 each corner, 1 in the middle	Bumper to be placed under PCB (5 locations: 4 each corner, 1 in the middle)	SJ-5003(BLACK)

1	12Vdc aux supply	12Vdc aux supply	CUI Inc	SMI6-12-K-P5
1	CONTROL CARD PICCOLO ISO F28035	CONTROL CARD PICCOLO ISO F28035	Texas Instruments	TMDSCNCD28035ISO

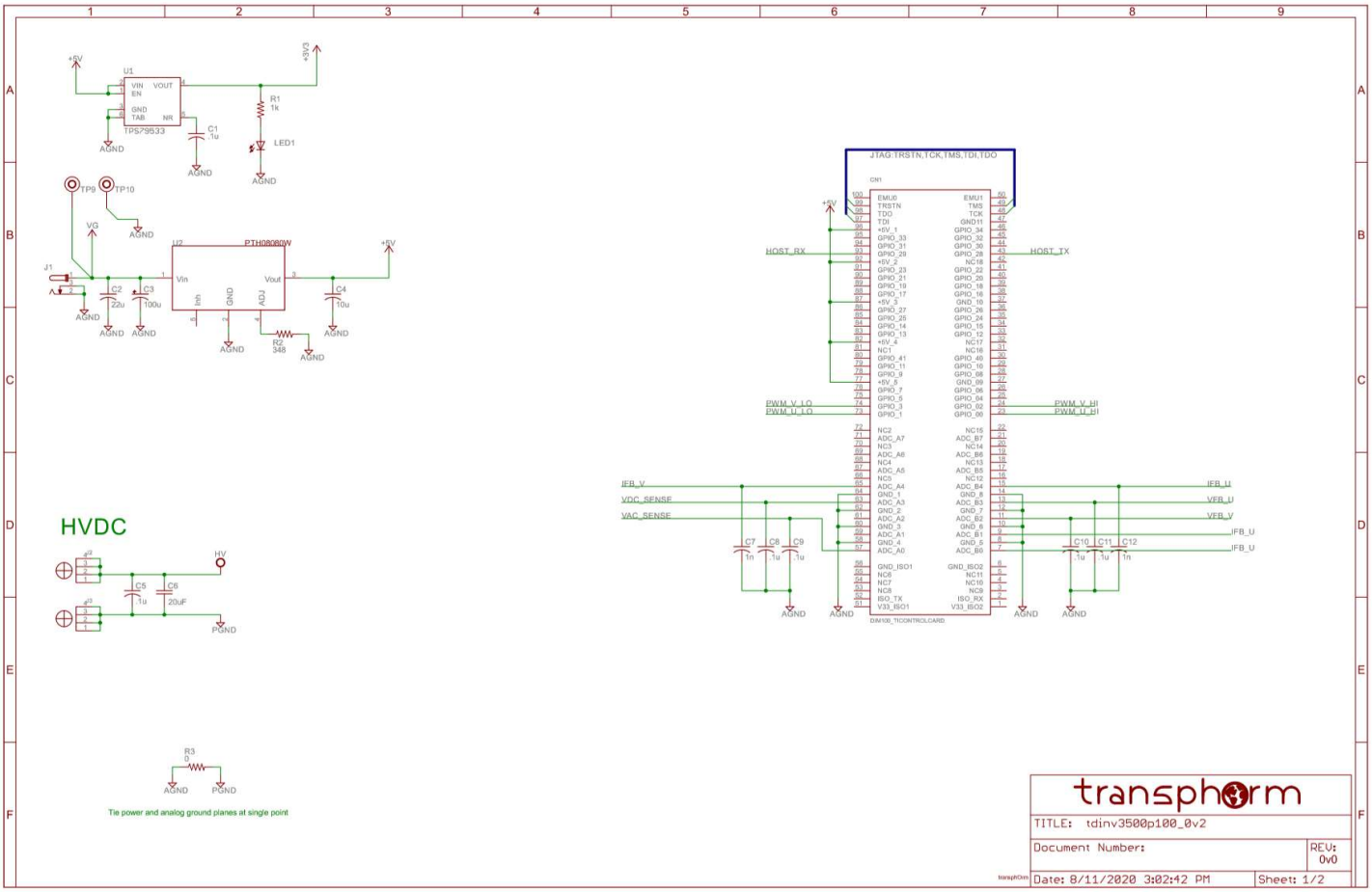


Figure 7. Detailed circuit schematic (1 of 2)

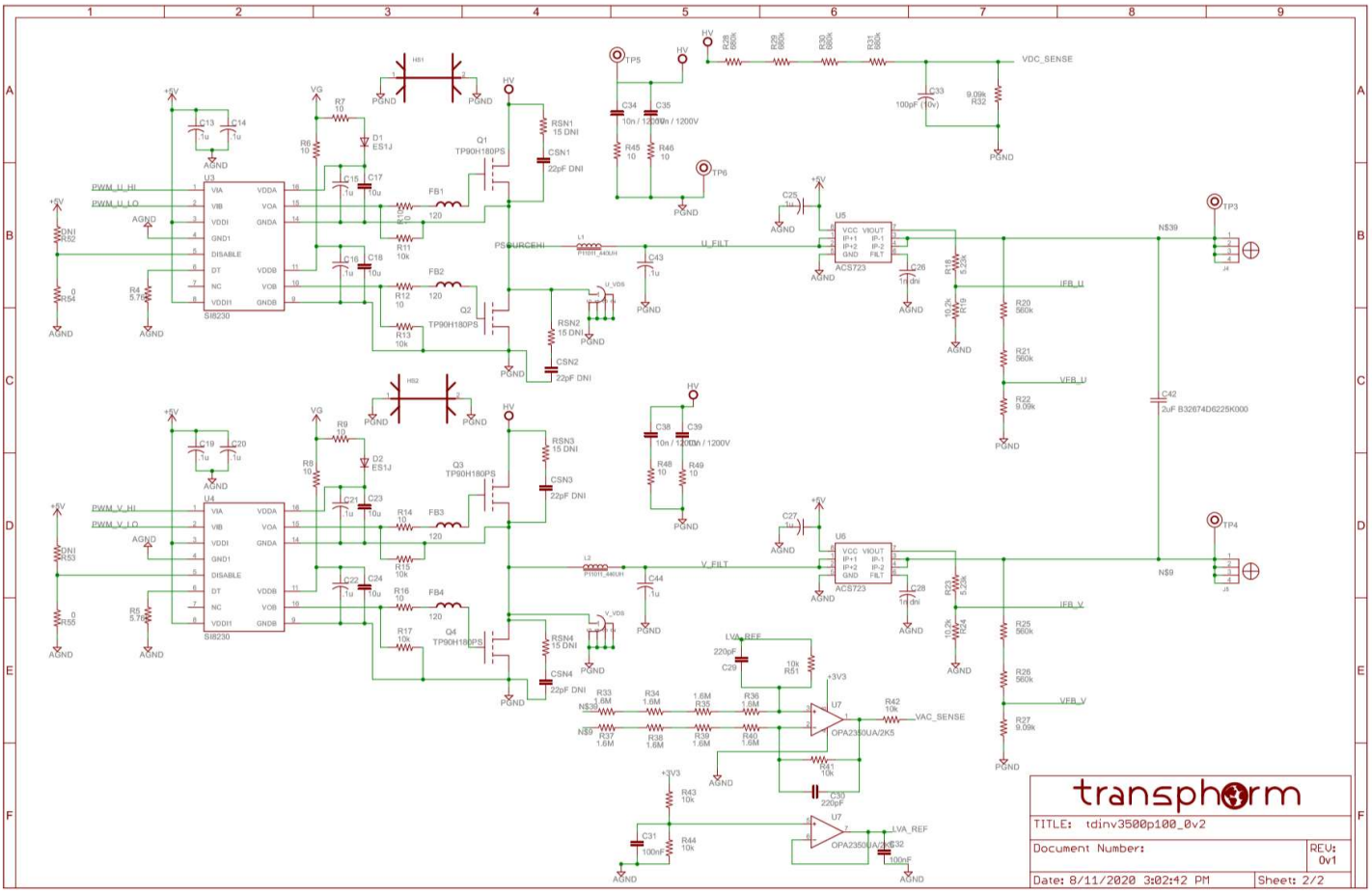
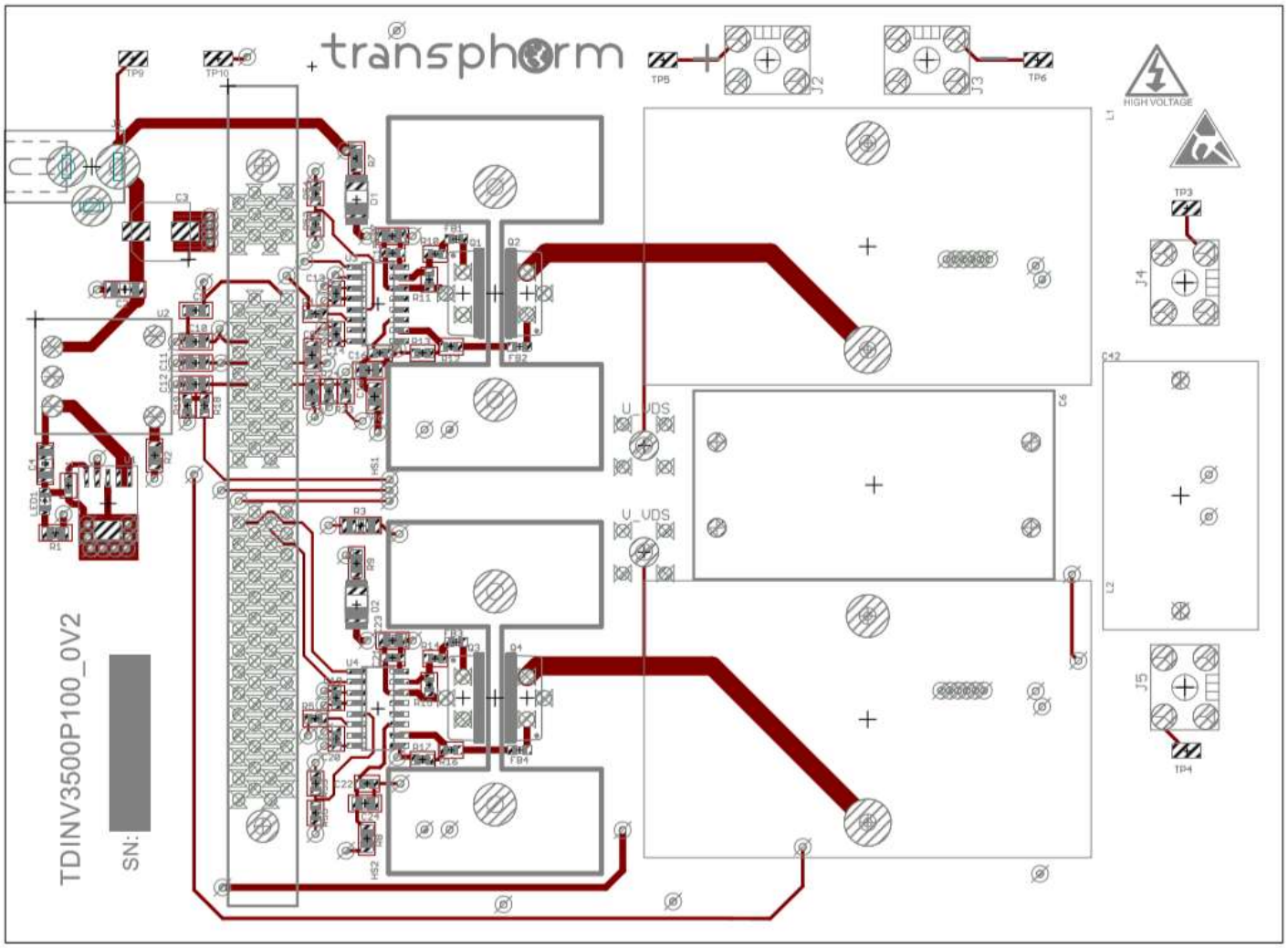
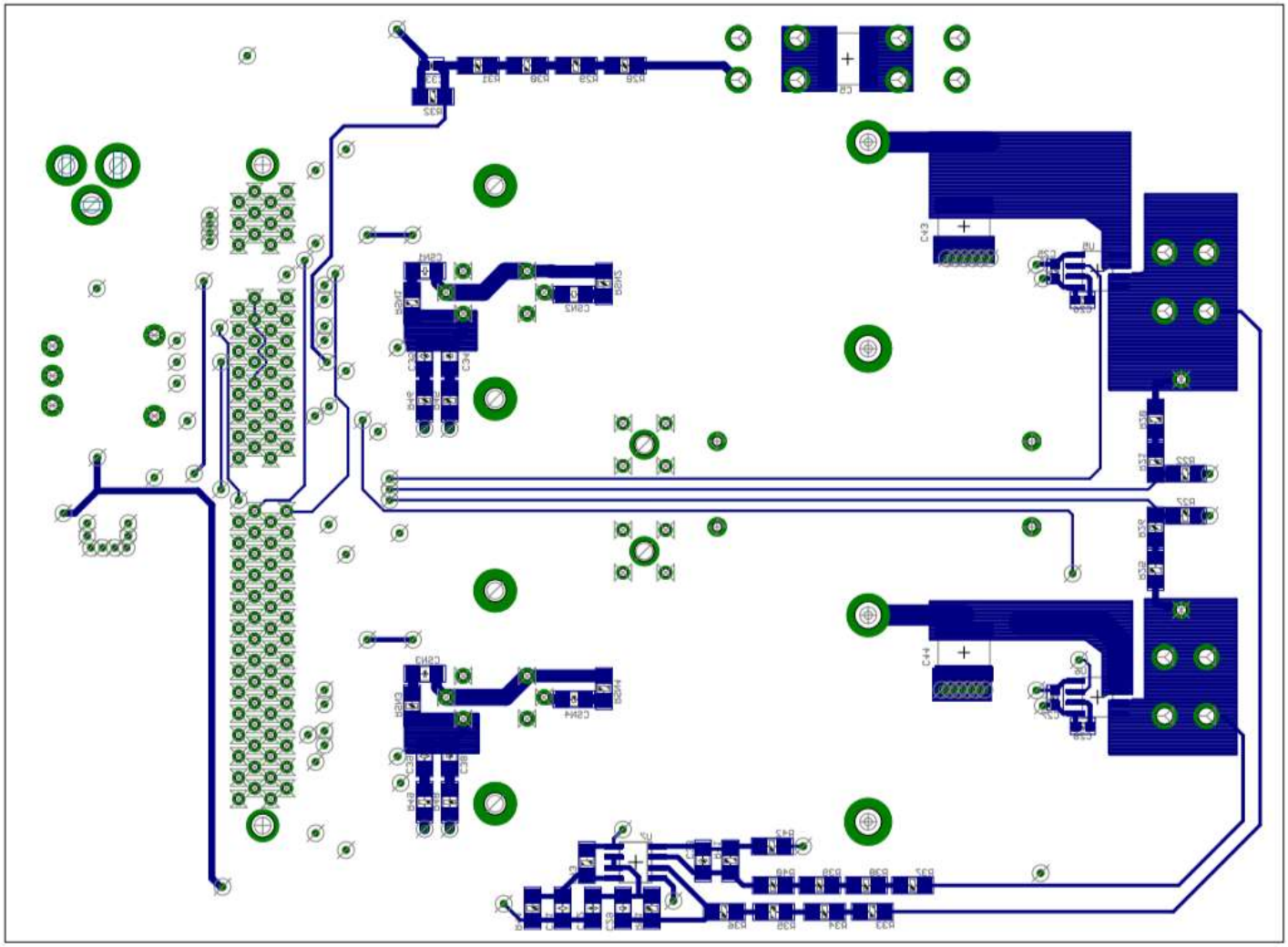


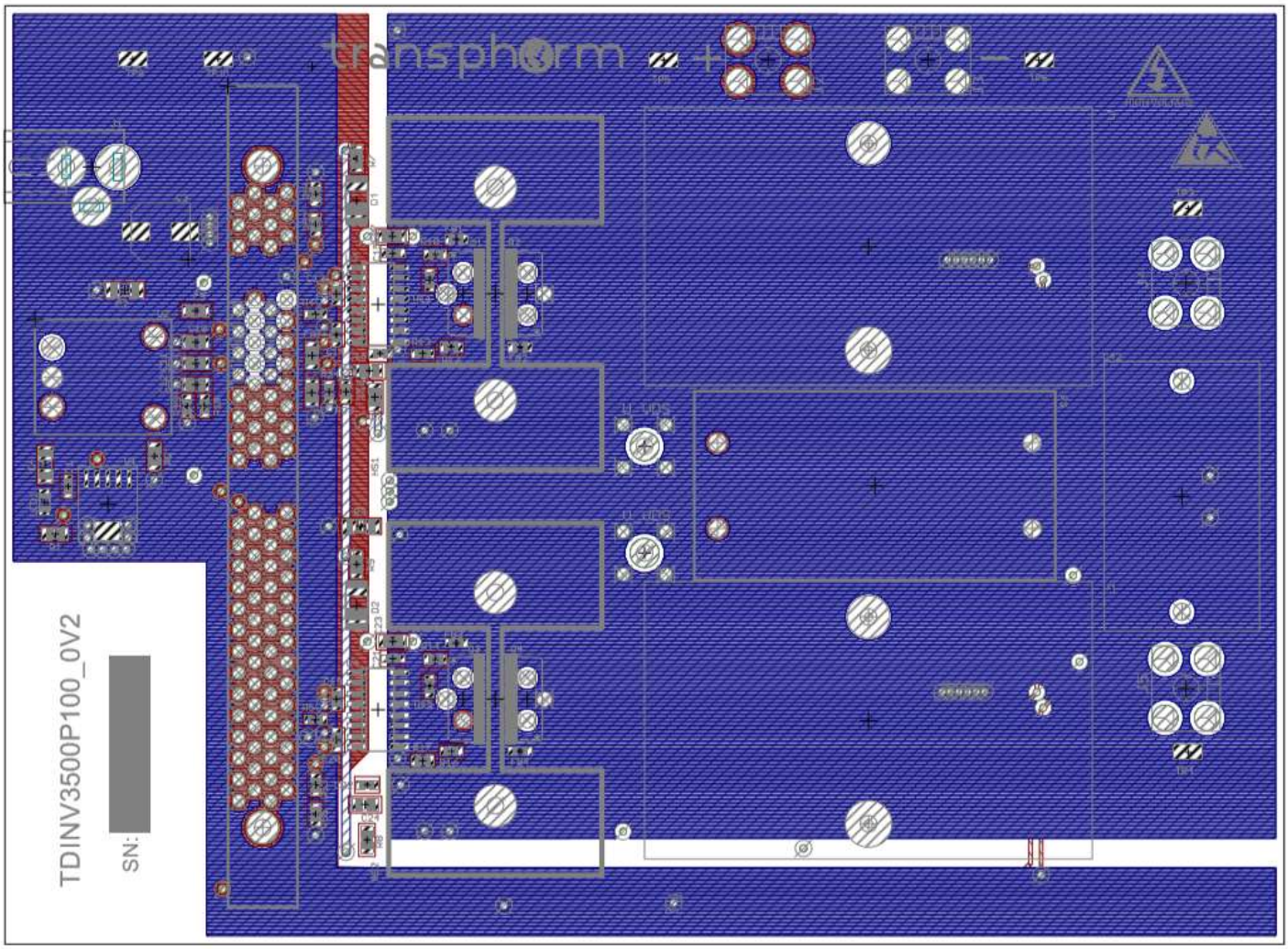
Figure 8. Detailed circuit schematic (2 of 2)



(a) PCB top layer



(b) PCB bottom layer



(c) PCB inner layer 2 (ground planes) and inner layer 3 (power plane)

Figure 9. PCB layers

Probing

There are two available Tektronix test points on the PCB used to monitor the low-side switching (node) capability of each half-bridge circuit during operation.

To minimize inductance during measurement, the tip and the ground of the probe should be directly attached to the sensing points to minimize the sensing loop. For safe, reliable, and accurate measurement, a scope probe tip may be directly soldered to the low-side FET drain and a short ground wire soldered to the low-side FET source. See Figure 10 for an alternative that does not require soldering the probe tip.

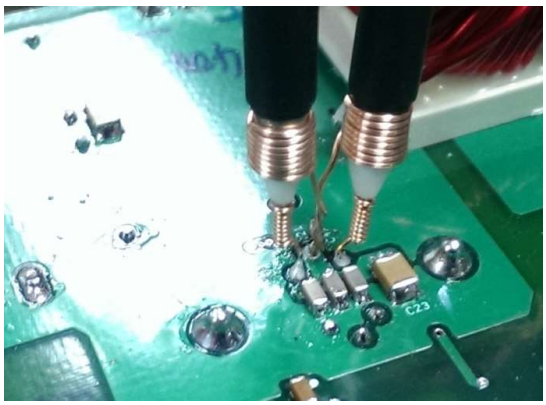


Figure 10. Low-inductance probing of fast, high-voltage signals

Protection features

Current limit

The TDINV3500P100 evaluation board supports user-defined current limit thresholds in both the positive- and negative-going directions. The current limits are peak and in amps.

```
// OCP setting:
#define OCP_LV_UP 1800
```