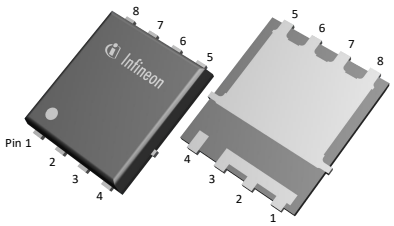
MOSFET

OptiMOS™ Power-Transistor, 60 V

PG-TDSON-8



Features

- Optimized for high performance SMPS, e.g. sync. rec.
- 100% avalanche tested
- Superior thermal resistance
- N-channel
- Qualified according to JEDEC[1] for target applications
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21
- Higher solder joint reliability due to enlarged source interconnection

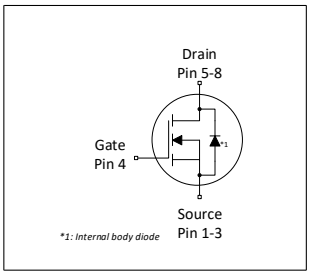


Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	60	V
$R_{DS(on),max}$	1.45	mΩ
I_D	240	A
Q_{OSS}	100	nC
Q_G(0V..10V)	89	nC

Type / Ordering Code	Package	Marking	Related Links
BSC014N06NS	PG-TDSON-8 FL	014N06NS	-

[1] J-STD20 and JESD22

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1 Maximum ratings

at T_j=25 °C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current[1]	I_D	- - -	- - -	240 152 30	A	V_{GS}=10 V, T_C=25 °C V_{GS}=10 V, T_C=100 °C V_{GS}=10 V, T_C=25°C, R_{thJA} =50K/W[2]
Pulsed drain current[3]	$I_{D,pulse}$	-	-	960	A	T_C=25 °C
Avalanche energy, single pulse[4]	E_{AS}	-	-	580	mJ	I_D=50 A, R_{GS}=25 Ω
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	- -	- -	156 2.5	W	T_C=25 °C T_A=25 °C, R_{thJA}=50 K/W[2]
Operating and storage temperature	T_j, T_{stg}	-55	-	150	°C	IEC climatic category; DIN IEC 68-1: 55/150/56

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, bottom	R_{thJC}	-	0.5	0.8	K/W	-
Thermal resistance, junction - case, top	R_{thJC}	-	-	20	K/W	-
Device on PCB, 6 cm² cooling area[2]	R_{thJA}	-	-	50	K/W	-

[1] Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature at 25°C. For higher case temperature please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.
[2] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.
[3] See Diagram 3 for more detailed information
[4] See Diagram 13 for more detailed information

3 Electrical characteristics

at T_j=25 °C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	60	-	-	V	V_{GS}=0 V, I_D=1 mA
Gate threshold voltage	$V_{GS(th)}$	2.1	2.8	3.3	V	V_{DS}=V_{GS}, I_D=120 µA
Zero gate voltage drain current	I_{DSS}	- -	0.5 10	1 100	µA	V_{DS}=60 V, V_{GS}=0 V, T_j=25 °C V_{DS}=60 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	10	100	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	- -	1.2 1.6	1.45 2.2	mΩ	V_{GS}=10 V, I_D=50 A V_{GS}=6 V, I_D=12.5 A
Gate resistance[1)]	R_G	-	2	3	Ω	-
Transconductance	g_{fs}	75	150	-	S	|V_{DS}|>2|I_D|$R_{DS(on)max}$, I_D=50 A

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	6500	8125	pF	V_{GS}=0 V, V_{DS}=30 V, f=1 MHz
Output capacitance[1)]	C_{oss}	-	1500	1875	pF	V_{GS}=0 V, V_{DS}=30 V, f=1 MHz
Reverse transfer capacitance[1)]	C_{rss}	-	59	118	pF	V_{GS}=0 V, V_{DS}=30 V, f=1 MHz
Turn-on delay time	$t_{d(on)}$	-	23	-	ns	V_{DD}=30 V, V_{GS}=10 V, I_D=30 A, $R_{G,ext}$,ext=2 Ω
Rise time	t_r	-	10	-	ns	V_{DD}=30 V, V_{GS}=10 V, I_D=30 A, $R_{G,ext}$,ext=2 Ω
Turn-off delay time	$t_{d(off)}$	-	43	-	ns	V_{DD}=30 V, V_{GS}=10 V, I_D=30 A, $R_{G,ext}$,ext=2 Ω
Fall time	t_f	-	11	-	ns	V_{DD}=30 V, V_{GS}=10 V, I_D=30 A, $R_{G,ext}$,ext=2 Ω

Table 6 Gate charge characteristics[2)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	28	-	nC	V_{DD}=30 V, I_D=50 A, V_{GS}=0 to 10 V
Gate charge at threshold	$Q_{g(th)}$	-	18	-	nC	V_{DD}=30 V, I_D=50 A, V_{GS}=0 to 10 V
Gate to drain charge[1)]	Q_{gd}	-	16	21	nC	V_{DD}=30 V, I_D=50 A, V_{GS}=0 to 10 V
Switching charge	Q_{sw}	-	26	-	nC	V_{DD}=30 V, I_D=50 A, V_{GS}=0 to 10 V
Gate charge total[1)]	Q_g	-	89	104	nC	V_{DD}=30 V, I_D=50 A, V_{GS}=0 to 10 V
Gate plateau voltage	$V_{plateau}$	-	4.3	-	V	V_{DD}=30 V, I_D=50 A, V_{GS}=0 to 10 V
Gate charge total, sync. FET	$Q_{g(sync)}$	-	78	-	nC	V_{DS}=0.1 V, V_{GS}=0 to 10 V
Output charge[1)]	Q_{oss}	-	100	125	nC	V_{DD}=30 V, V_{GS}=0 V

[1)] Defined by design. Not subject to production test.
[2)] See ″Gate charge waveforms″ for parameter definition

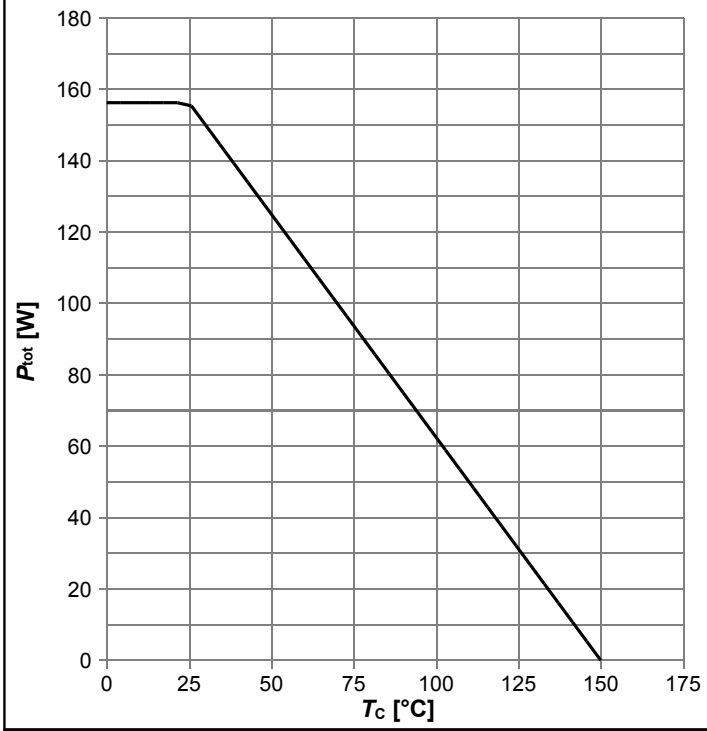
Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	156	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$	-	-	960	A	T_C=25 °C
Diode forward voltage	V_{SD}	-	0.8	1.2	V	V_{GS}=0 V, I_F=50 A, T_j=25 °C
Reverse recovery time[1)]	t_{rr}	-	52	83	ns	V_R=30 V, I_F=50 A, di_F/dt=100 A/µs
Reverse recovery charge	Q_{rr}	-	139	-	nC	V_R=30 V, I_F=50 A, di_F/dt=100 A/µs

[1)] Defined by design. Not subject to production test.

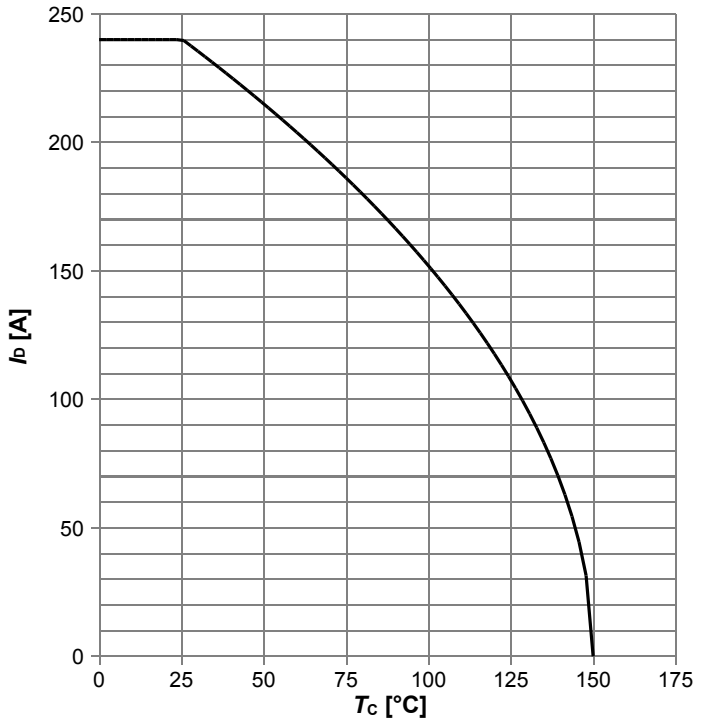
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



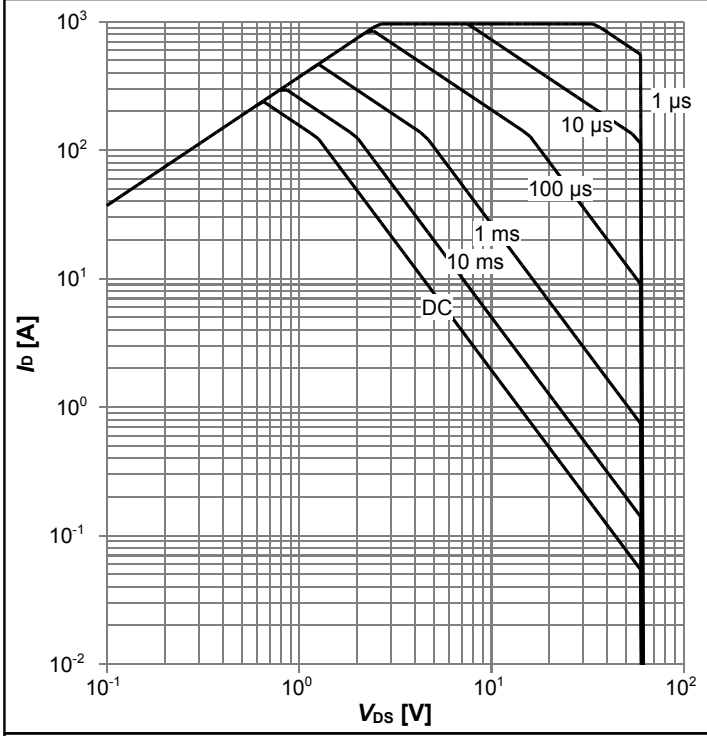
$P_{tot}=f(T_C)$

Diagram 2: Drain current



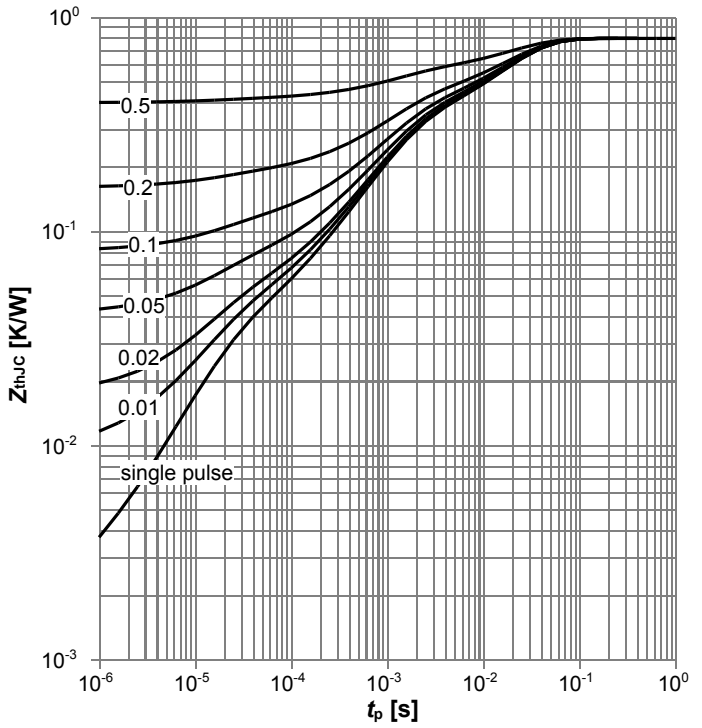
$I_D=f(T_C)$; $V_{GS}\geq 10$ V

Diagram 3: Safe operating area



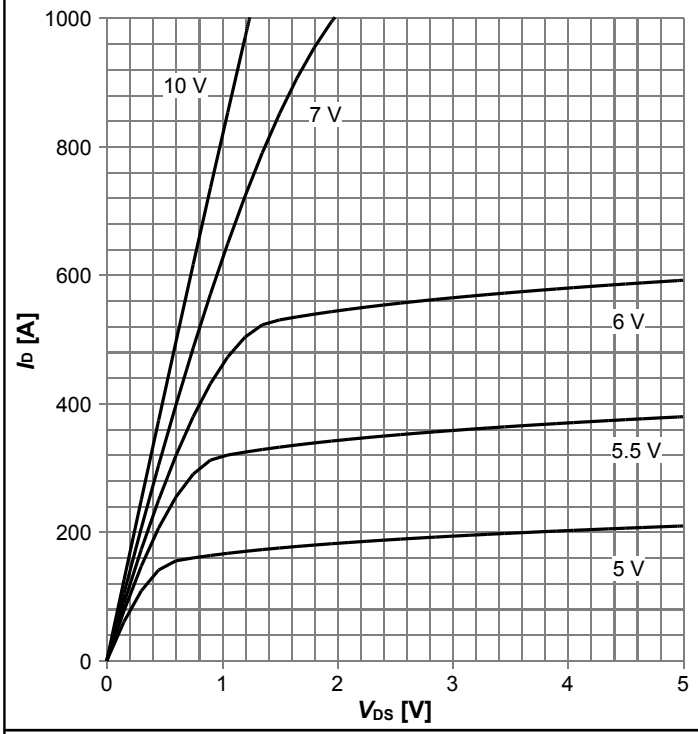
$I_D=f(V_{DS})$; T_C=25 °C; D=0; parameter: t_p

Diagram 4: Max. transient thermal impedance



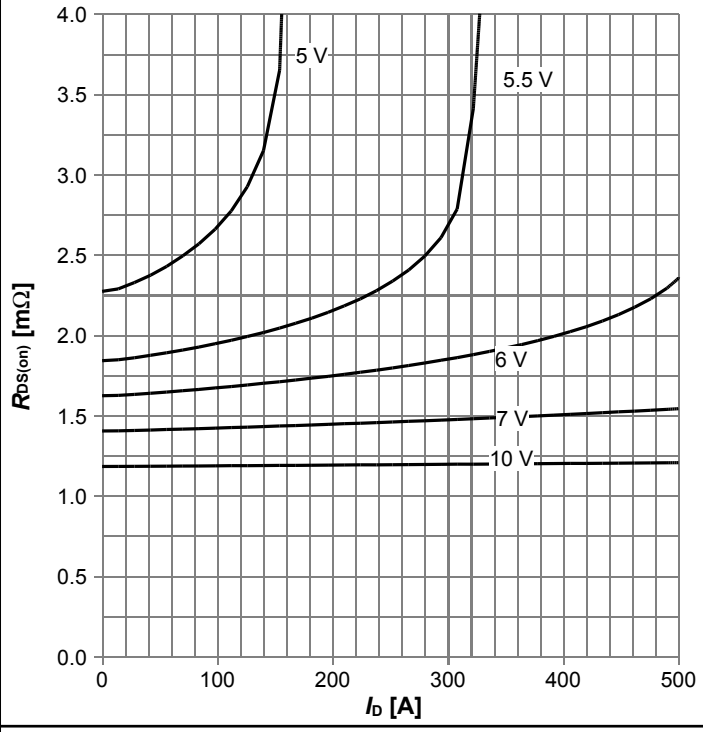
$Z_{thJC}=f(t_p)$; parameter: $D=t_p/T$

Diagram 5: Typ. output characteristics



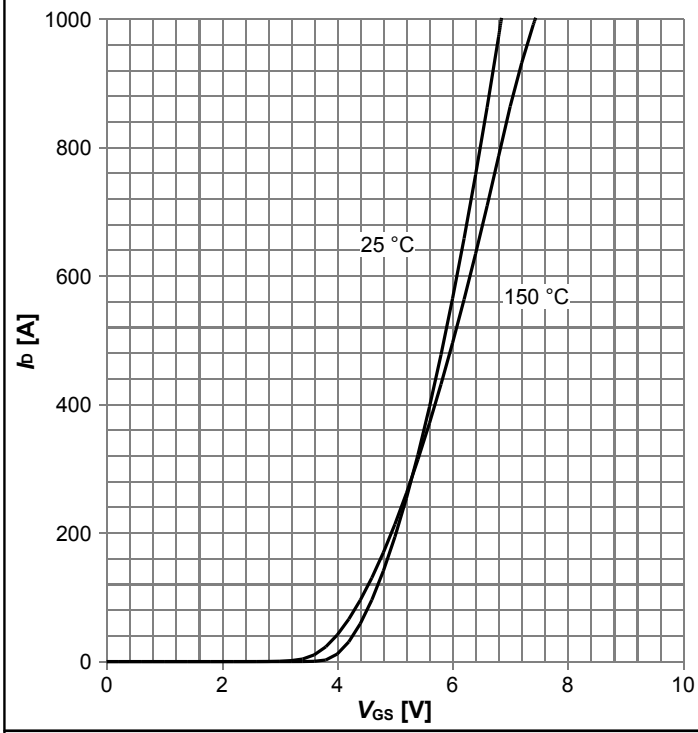
$I_D=f(V_{DS})$, $T_j=25$ °C; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



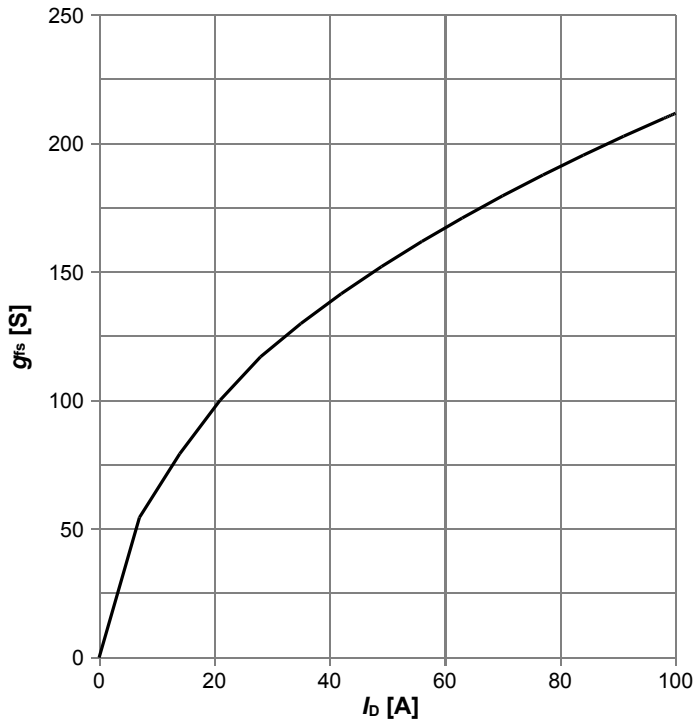
$R_{DS(on)}=f(I_D)$, $T_j=25$ °C; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



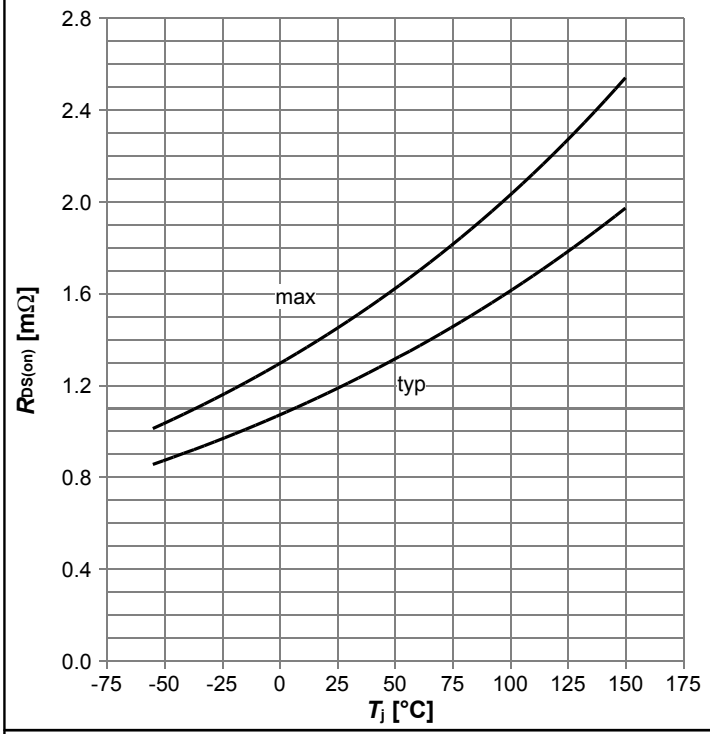
$I_D=f(V_{GS})$, $|V_{DS}|>2|I_D|R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. forward transconductance



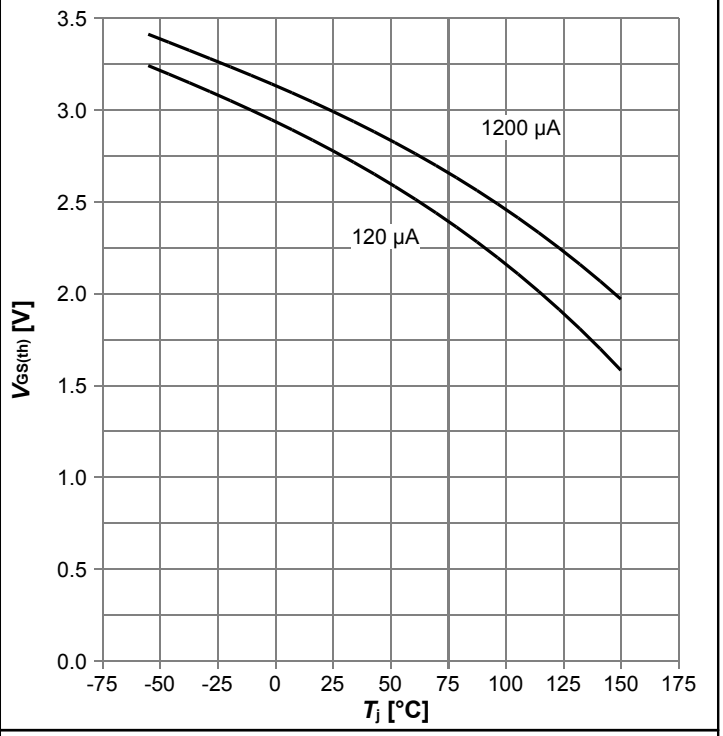
$g_{fs}=f(I_D)$; $T_j=25$ °C

Diagram 9: Drain-source on resistance



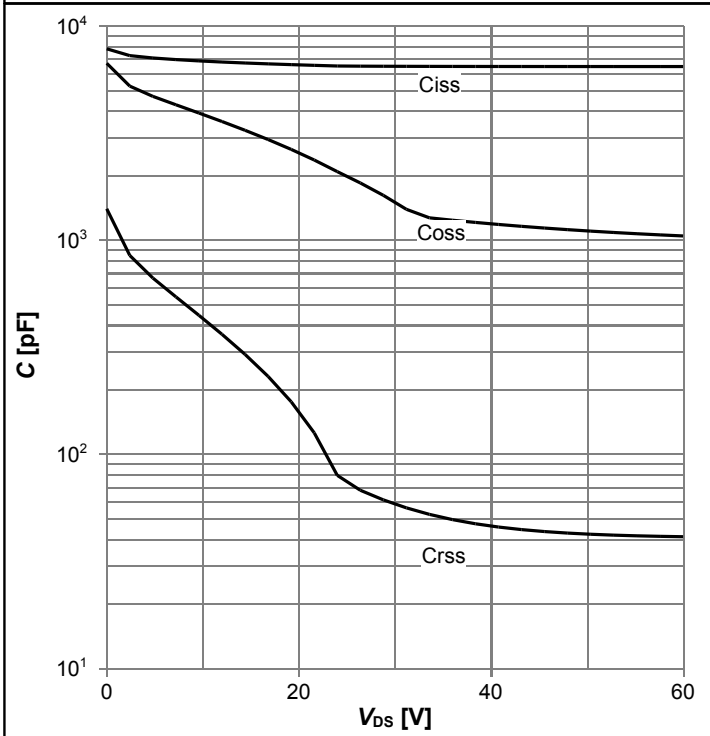
$R_{DS(on)}$=f(T_j), I_D=50 A, V_{GS}=10 V

Diagram 10: Typ. gate threshold voltage



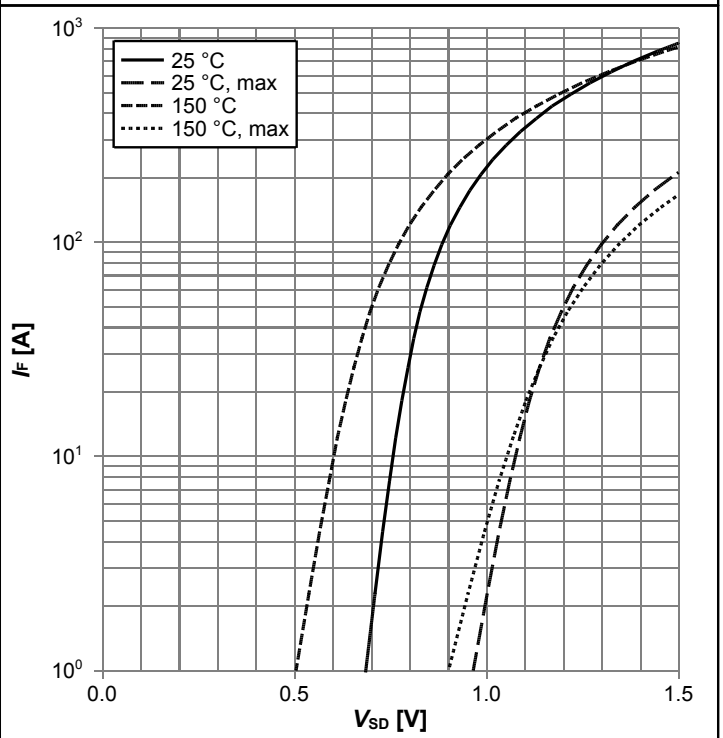
$V_{GS(th}$=f(T_j), V_{GS}=V_{DS}; parameter: I_D

Diagram 11: Typ. capacitances



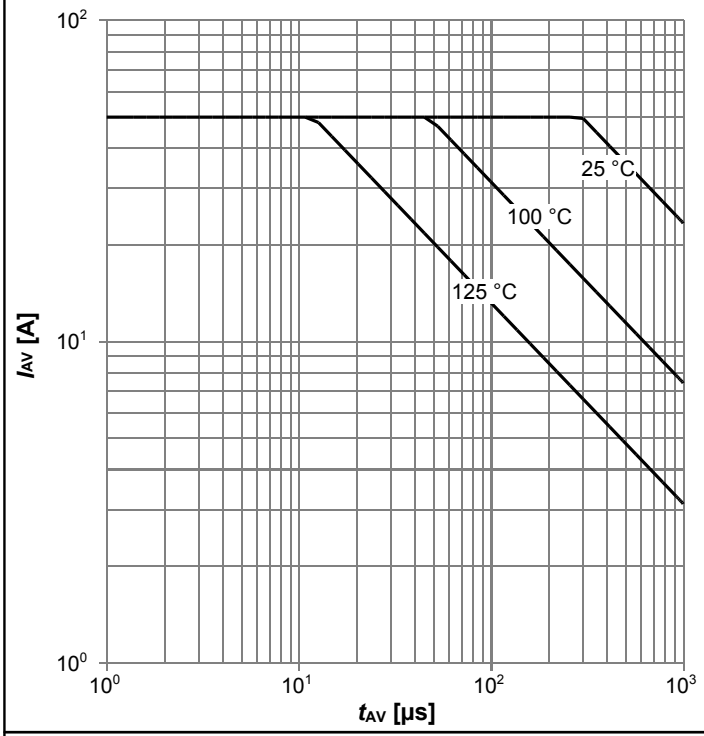
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz

Diagram 12: Forward characteristics of reverse diode



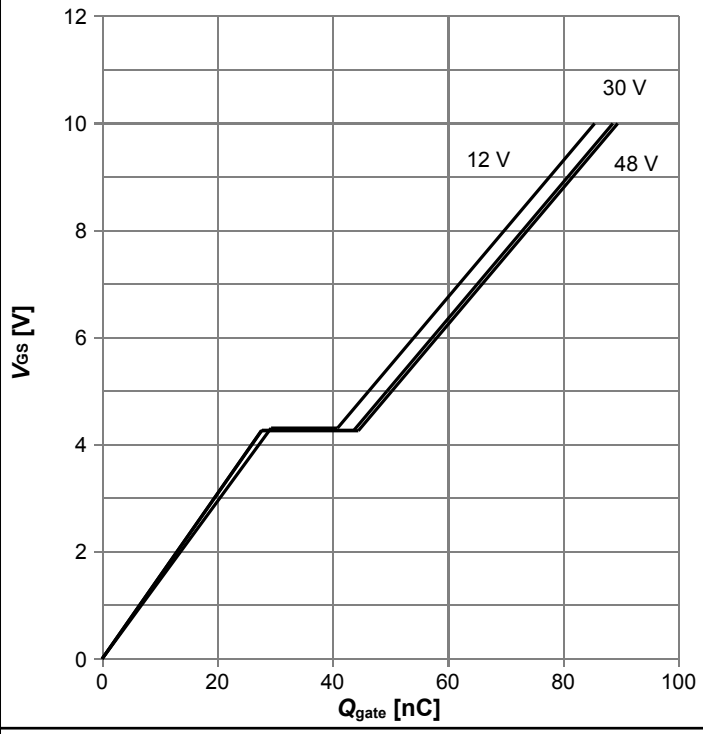
I_F=f(V_{SD}); parameter: T_j

Diagram 13: Avalanche characteristics



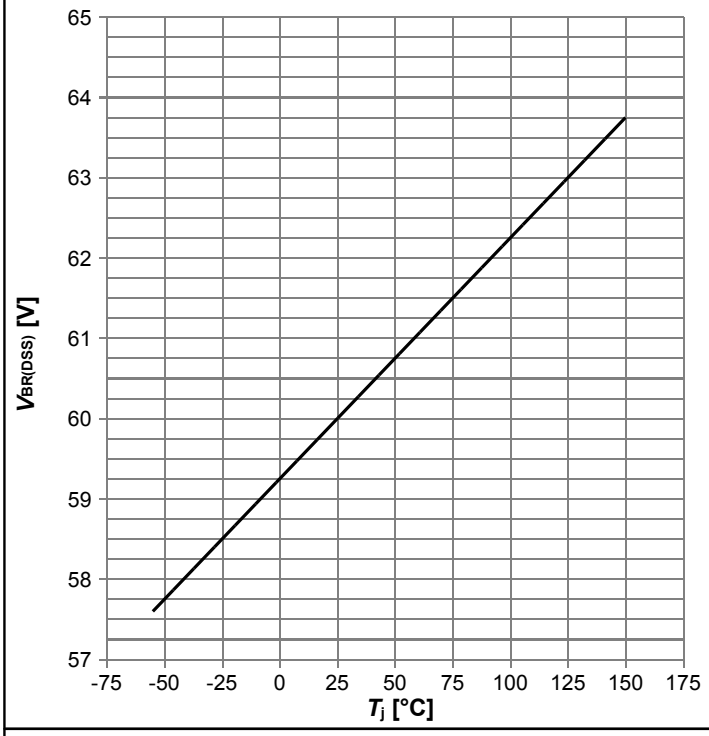
I_{AS}=f(t_{AV}); R_{GS}=25 Ω; parameter: $T_{j(start)}$

Diagram 14: Typ. gate charge



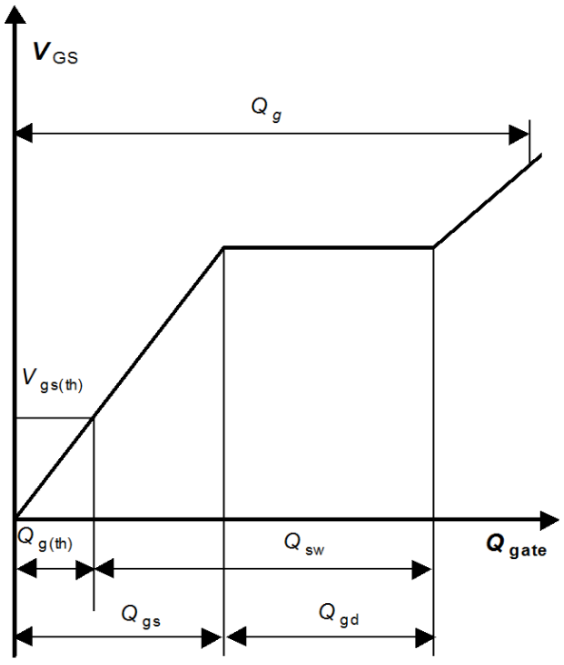
V_{GS}=f(Q_{gate}); I_D=50 A pulsed; parameter: V_{DD}

Diagram 15: Min. drain-source breakdown voltage

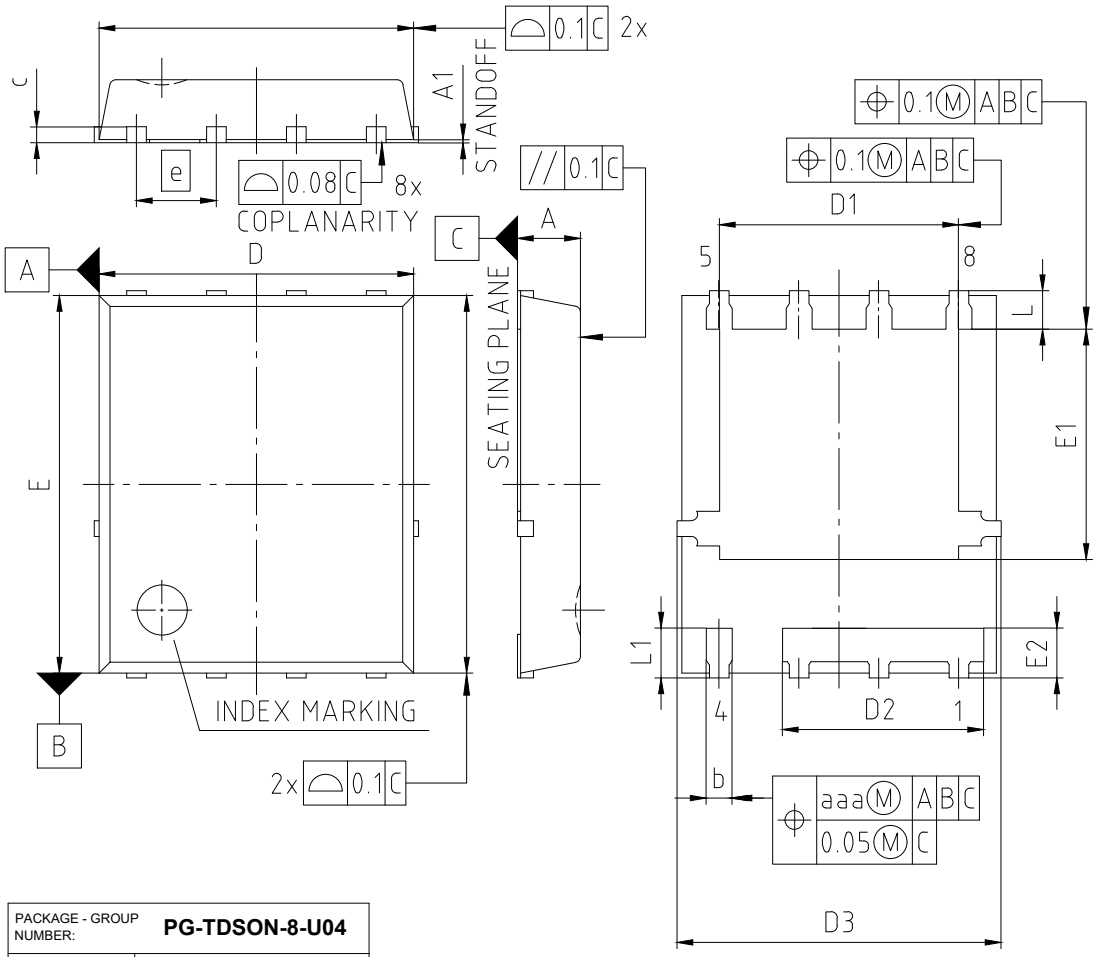


$V_{BR(DSS)}$=f(T_j); I_D=1 mA

Diagram Gate charge waveforms



5 Package Outlines



PACKAGE - GROUP NUMBER:	PG-TDSON-8-U04	
DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	0.90	1.20
A1	0	0.05
b	0.26	0.54
c	0.15	0.35
D	4.80	5.35
D1	3.70	4.40
D2	2.94	3.25
D3	5.05	5.38
E	5.70	6.10
E1	3.43	3.76
E2	0.69	0.89
e	1.27	
L	0.45	0.66
L1	0.69	0.90
aaa	0.10	0.25

1) EXCLUDING MOLD FLASH
2) REMOVAL ON MOLD GATE
   INTRUSION 0.1 MM
   PROTRUSION 0.1 MM
3) LEAD LENGTH UP TO ANTI FLASH LINE
4) ALL METAL SURFACES ARE PLATED,
   EXCEPT AREA OF CUT

Figure 1 Outline PG-TDSON-8 FL, dimensions in mm

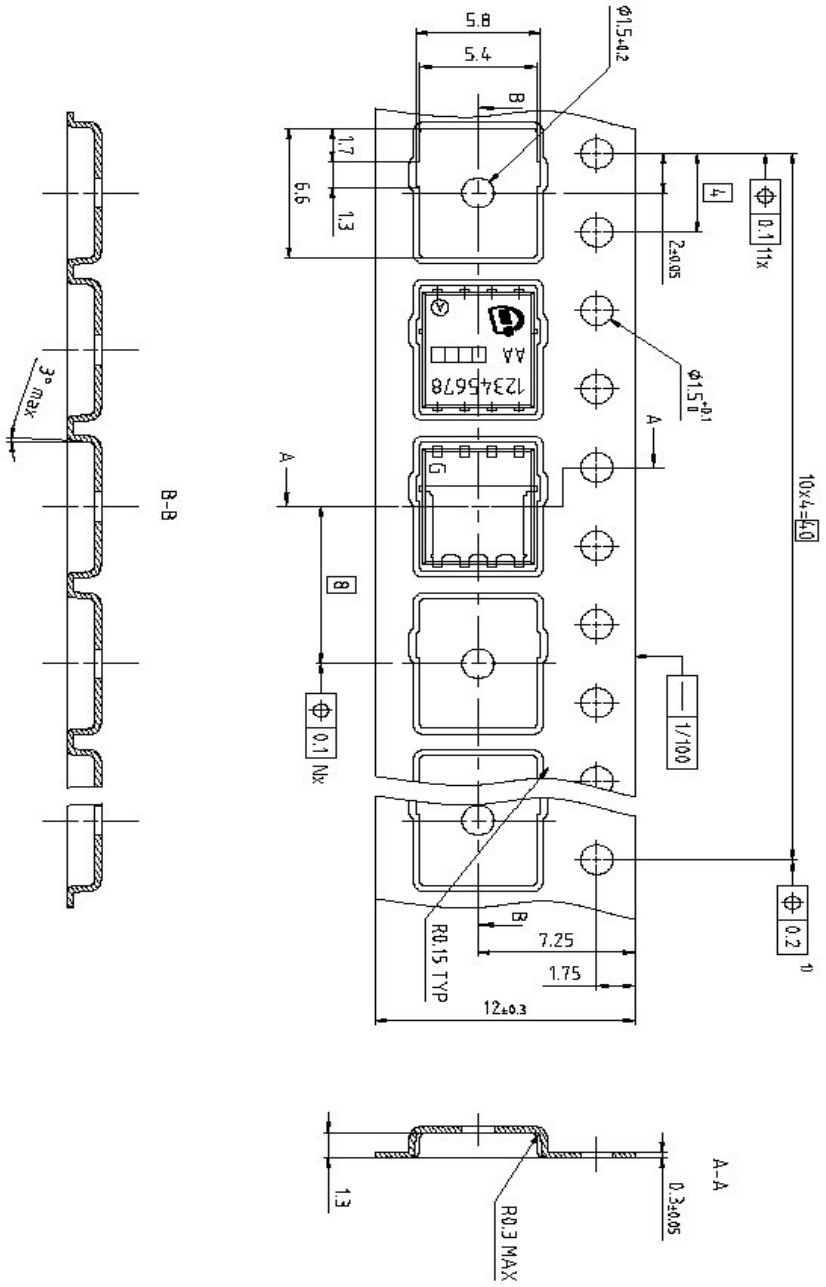


Figure 2 Outline Tape (TDSON-8 FL)

Revision History

BSC014N06NS

Revision: 2022-08-09, Rev. 2.5

Previous Revision		
Revision	Date	Subjects (major changes since last revision)
2.3	2014-10-16	Rev.2.3
2.4	2020-02-28	Update current rating
2.5	2022-08-09	Update outline drawing and footnotes

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