

The T9KC is a high voltage, high current disc pack SCR employing a high di/dt gate structure. This gate design allows the SCR to be reliably operated at high di/dt and dv/dt conditions in various phase control applications.

#### FEATURES:

- Low On-State Voltage
- High di/dt Capability
- High dv/dt Capability
- Hermetic Ceramic Package
- Excellent Surge and I<sup>2</sup>t Ratings

#### APPLICATIONS:

- DC Power Supplies
- Motor Controls
- AC Soft-Starters

#### ORDERING INFORMATION

Select the complete 12 digit Part Number using the table below.  
 EXAMPLE: T9KC650603DH is a 6500V-600A SCR with 200ma IGT and 12 inch gate and cathode potential leads.

PART	Voltage Rating $V_{DRM}-V_{RRM}$	Voltage Code	Current Rating $I_{TAVG}$	Current Code	Turn-Off $I_q$	Gate $I_{GT}$	Leads
<b>T9KC</b>	6500	<b>65</b>	600	<b>06</b>	<b>0</b>	<b>3</b>	<b>DH</b>
	6200	<b>62</b>					
	6000	<b>60</b>			600us (typ.)	200ma (max)	12"

Revised: 5/28/2010

**Absolute Maximum Ratings**

Characteristic	Symbol	Rating	Units
Repetitive Peak Voltage	$V_{DRM}-V_{RRM}$	6500	Volts
Average On-State Current, $T_C= 73\text{ }^\circ\text{C}$	$I_{T(Avg.)}$	600	A
RMS On-State Current, $T_C= 73\text{ }^\circ\text{C}$	$I_{T(RMS)}$	942	A
Average On-State Current, $T_C= 56\text{ }^\circ\text{C}$	$I_{T(Avg.)}$	700	A
RMS On-State Current, $T_C= 56\text{ }^\circ\text{C}$	$I_{T(RMS)}$	1100	A
Peak One Cycle Surge Current, 60Hz, $V_R=0V$	$I_{TSM}$	7,750	A
Peak One Cycle Surge Current, 50Hz, $V_R=0V$	$I_{TSM}$	7,307	A
Fuse Coordination $I^2t$ , 60Hz	$I^2t$	2.50E+05	A <sup>2</sup> s
Fuse Coordination $I^2t$ , 50Hz	$I^2t$	2.67E+05	A <sup>2</sup> s
Critical Rate-of-Rise of On-State Current	$di/dt$ -- Rep.	150	A/us
$.67 \cdot V_{DRM}$ $I_{TM} = 600A$	$di/dt$ -- Non-Rep.	300	A/us
Gate Drive: 20V 10Ω Tr=0.5us			
Peak Gate Power, 100us	$P_{GM}$	16	Watts
Average Gate Power	$P_{G(avg)}$	5	Watts
Operating Temperature	$T_j$	-40 to+125	°C
Storage Temperature	$T_{Stg.}$	-50 to+150	°C
Approximate Weight		1	lb
		0.45	Kg
Mounting Force		5500-6000	lbs
		24.5 - 26.7	Knewtons

Information presented is correct to the knowledge and capabilities of the manufacturer. This information is subject to change without notice. The manufacturer makes no claim as to suitability for use, reliability, capability or future availability of this product.

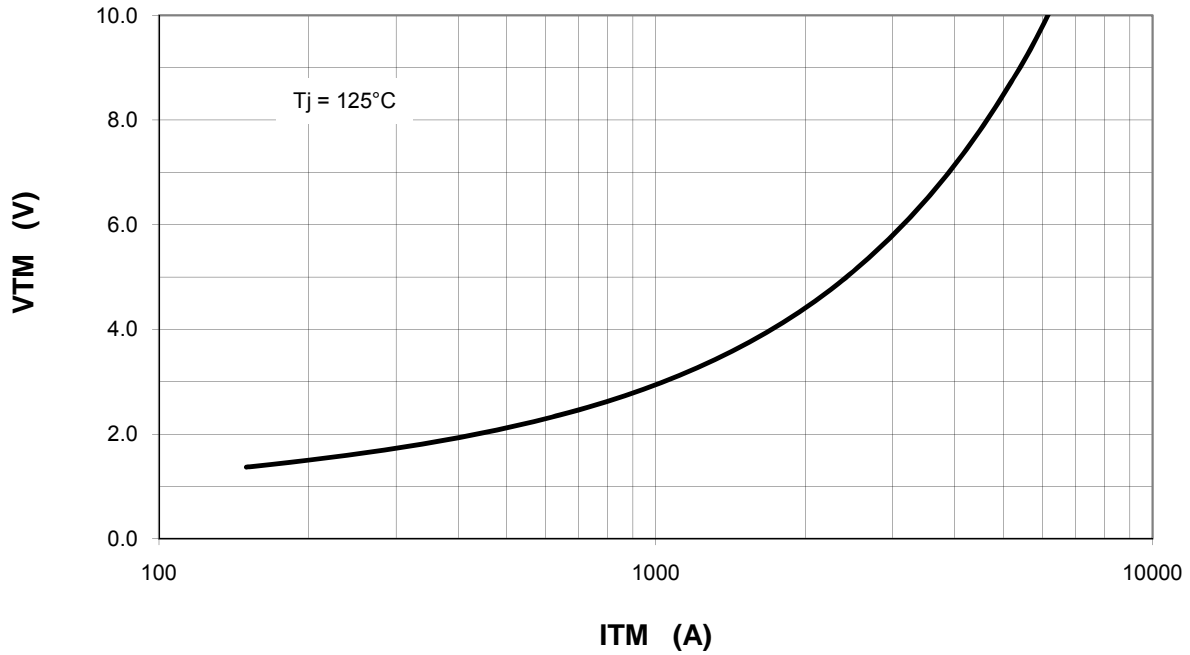
**Electrical Characteristics, T<sub>j</sub>=25°C unless otherwise specified**

Characteristic	Symbol	Test Conditions	Rating			Units
			min	typ	max	
Repetitive Peak Forward Leakage Current	I <sub>DRM</sub>	T <sub>j</sub> =125°C, V <sub>DRM</sub> =Rated		110	180	ma
Repetitive Peak Reverse Leakage Current	I <sub>RPM</sub>	T <sub>j</sub> =125°C, V <sub>RPM</sub> =Rated		70	180	ma
Repetitive Peak Leakage Current Distribution	I <sub>DRM</sub> -I <sub>RPM</sub>	T <sub>j</sub> =125°C, Voltage=Rated	5% 70	50% 95	95% 165	ma
Peak On-State Voltage	V <sub>TM</sub>	T <sub>j</sub> =125°C, I <sub>TM</sub> =1500A			3.70	V
V <sub>TM</sub> Model, Low Level	V <sub>0</sub>	T <sub>j</sub> =125°C			1.32	V
V <sub>TM</sub> = V <sub>0</sub> + r•I <sub>TM</sub>	r	15% I <sub>TM</sub> - π•I <sub>TM</sub>			1.58E-03	Ω
V <sub>TM</sub> Model, High Level	V <sub>0</sub>	T <sub>j</sub> =125°C			1.73	V
V <sub>TM</sub> = V <sub>0</sub> + r•I <sub>TM</sub>	r	π•I <sub>TM</sub> - I <sub>TSM</sub>			1.32E-03	Ω
V <sub>TM</sub> Model, 4-Term	A	T <sub>j</sub> =125°C			0.140	
V <sub>TM</sub> = A + B•Ln(I <sub>TM</sub> ) +	B	15%I <sub>TM</sub> - I <sub>TSM</sub>			0.185	
C•(I <sub>TM</sub> ) + D•(I <sub>TM</sub> ) <sup>½</sup>	C				0.00121	
	D				0.0100	
Turn-On Delay Time	t <sub>d</sub>	V <sub>D</sub> = 0.5•V <sub>DRM</sub> Gate Drive: 40V - 20Ω		2.0		us
Turn-Off Time	t <sub>q</sub>	T <sub>j</sub> =125°C dv/dt = 20V/us to 67% V <sub>DRM</sub>		600		us
Reverse Recovery Current	I <sub>R(Rec)</sub>	T <sub>j</sub> =125°C 1000A -10A/us VR= 50V		160		A
Reverse Recovery Charge	Q <sub>RR</sub>			2200		uCoul
Reverse Recovery Current Distribution	I <sub>R(Rec)</sub>	T <sub>j</sub> =125°C 1000A -10A/us VR = 50V	5% 100	50% 112	95% 125	A
dv/dt <sub>(Crit)</sub>	dv/dt	T <sub>j</sub> =125°C Exp. Waveform V <sub>D</sub> =67% Rated	1000	>2000		V/us
Gate Trigger Current	I <sub>GT</sub>	T <sub>j</sub> =25°C V <sub>D</sub> = 12V	30	100	200	ma
Gate Trigger Voltage	V <sub>GT</sub>		0.8	1.5	3.0	V
Peak Reverse Gate Voltage	V <sub>GRM</sub>				5	V

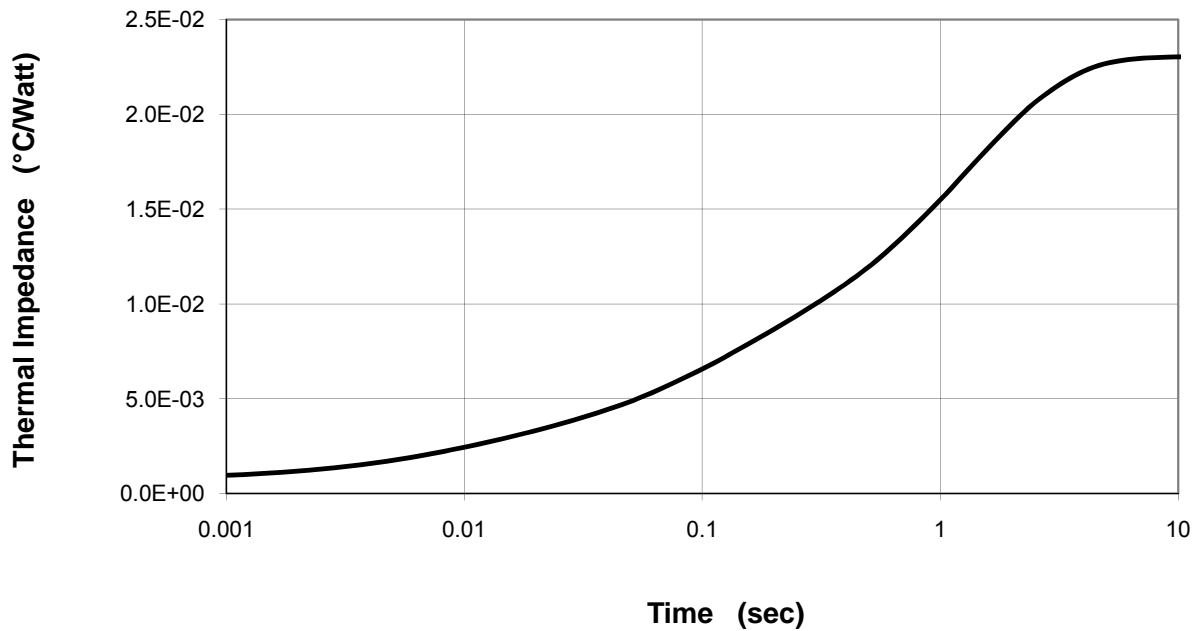
**Thermal Characteristics**

Characteristic	Symbol	Test Conditions	Rating				
			max			Units	
Thermal Resistance							
Junction to Case	Rθ <sub>jc</sub>	Double side cooled			0.023	°C/Watt	
Case to Sink	Rθ <sub>cs</sub>	Double side cooled			0.006	°C/Watt	
Thermal Impedance Model	Zθ <sub>jc</sub>	Double side cooled					
Zθ <sub>jc</sub> (t) = Σ(A(N)•(1-exp(-t/Tau(N))))		where:	N =	1	2	3	4
			A(N) =	7.26E-04	1.58E-03	4.55E-03	1.62E-02
			Tau(N) =	4.49E-05	8.21E-03	8.84E-02	1.31E+00

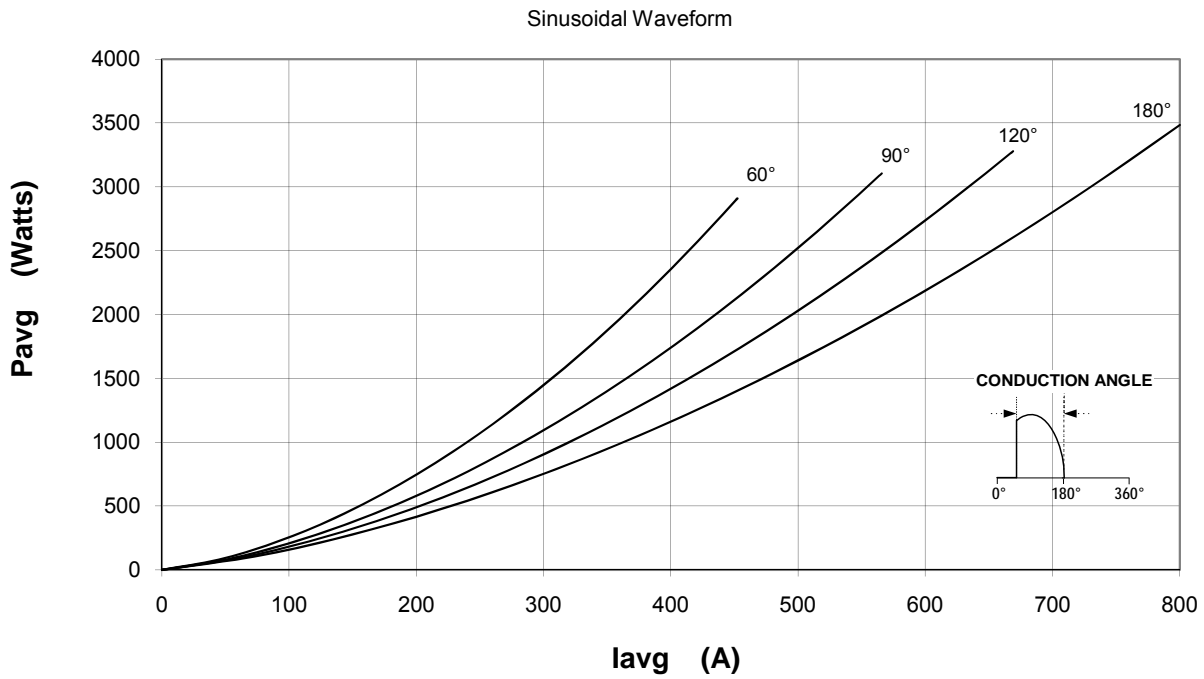
### Maximum On-State Voltage Drop



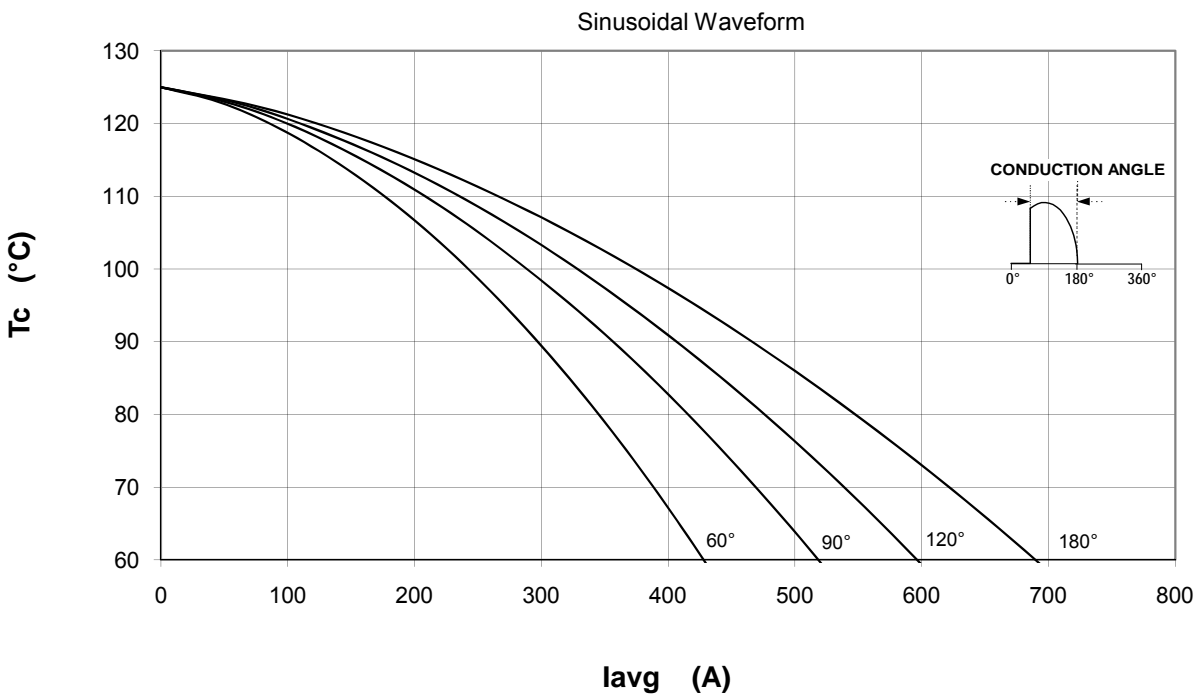
### MAXIMUM TRANSIENT THERMAL IMPEDANCE



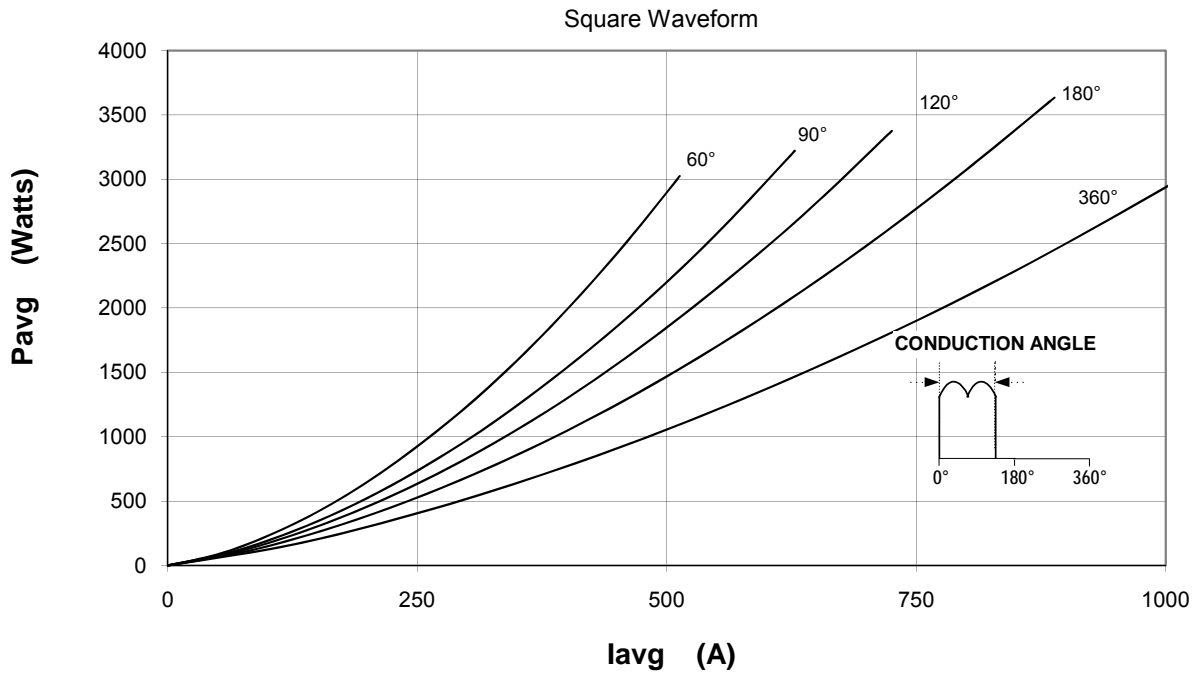
### Maximum On-State Power Dissipation



### Maximum Allowable Case Temperature



**Maximum On-State Power Dissipation**



**Maximum Allowable Case Temperature**

